The Chinese University of Hong Kong
Department of Computer Science and Engineering
CENG2010 Digital Logic Design Laboratory

Lab 4: Finite State Machine

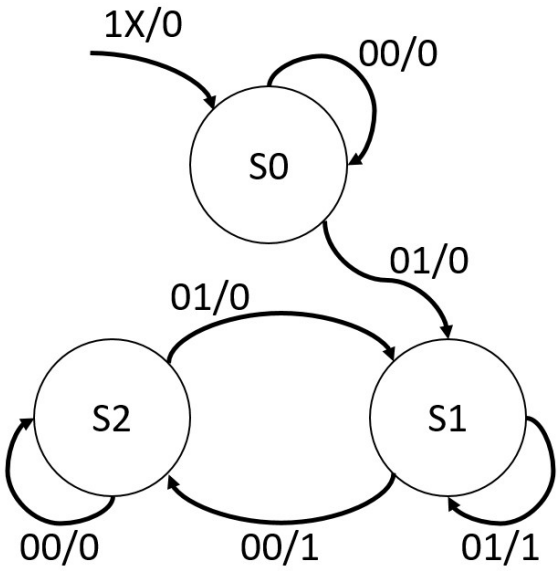
Submission Instructions:

- You are required to submit **BOTH <u>demo videos</u>** and **<u>VHDL codes</u>** to Blackboard.
- Create each VHDL project with a project name based on the lab and question number, e.g. "**ceng2010_lab1_q2**".
- Zip all the project folders to ONE single zip/rar file named with your student ID number, e.g. "**1155123456.zip**".
- Upload the zip/rar file to Blackboard before the deadline stated in Blackboard
- Marks will be deducted for late submission, deduct 10 marks per day

For each question below, you are required to record a short mp4 video to demonstrate the answers. In the video, the following elements are required:

A. Next to your FPGA board, show your full name and SID on a paper [5 marks]
B. Voice descriptions in English/Cantonese/Mandarin on what you are doing [5 marks]
C. Demonstrate works by presenting all possible input combinations step-by-step clearly [30 marks]

1. Implement the following Mealy Finite State Machine using VHDL. In the transitions below, for instance, 01/0 denoted that input RESET=0, input INPUT=1, and output=0. [60 marks]



a. Use switch sw0 as system INPUT
b. Use btnC button as the CLOCK signal to synchronize the whole machine by its rising edges. Since we are not using the real CLOCK signal on the board, please avoid naming this CLOCK as "CLK" or "CLOCK" in the VHDL codes.
c. Use btnD button to RESET the machine to S0 when pressed.
d. Use led0 to show the system output
e. Turn led5, led6, or led7 on when the system at State S0, S1, or S2 respectively
f. Name the processes similar to the examples in the lecture notes, i.e. SYNC_PROC, OUTPUT_DECODE, and NEXT_STATE_DECODE

THE END