

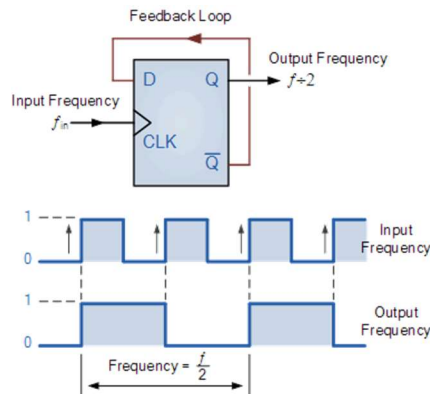
Lab 5: Hierarchical Design & Test Bench

Submission Instructions:

- You are required to submit **BOTH demo videos** and **VHDL codes** to Blackboard.
- Create each VHDL project with a project name based on the lab and question number, e.g. “ceng2010_lab1_q2”.
- Zip all the project folders to ONE single zip/rar file named with your student ID number, e.g. “1155123456.zip”.
- Upload the zip/rar file to Blackboard before the deadline stated in Blackboard
- Marks will be deducted for late submission, deduct 10 marks per day

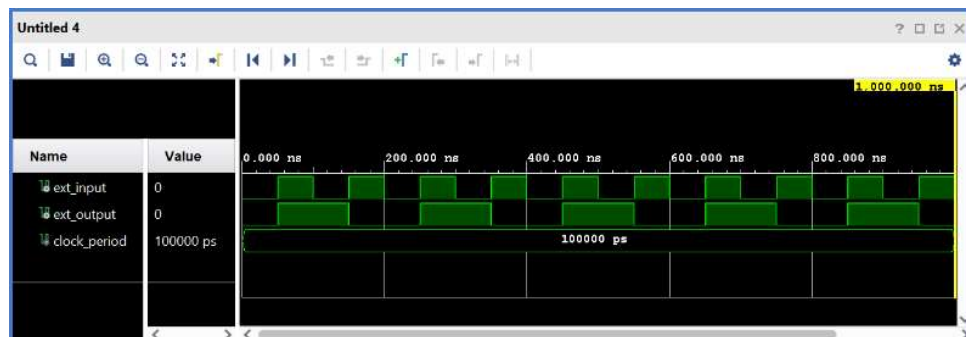
For each question below, you are required to record a short mp4 video to demonstrate the answers. In the video, the following elements are required:

- A. Next to your FPGA board, show your full name and SID on a paper [5 marks]
 - B. Voice descriptions in English/Cantonese/Mandarin on what you are doing [5 marks]
 - C. Demonstrate works by presenting all possible input combinations step-by-step clearly [30 marks]
1. Use VHDL to build a positive-edge-triggered D flip-flop with switch sw0 as input D, button btnC as CLK input, LED led0 as output Q, and LED led1 as output Q'. [30 marks]
 2. To build the divide-by-2 counter as shown below, reuse the D flip-flop module in question 1 by using the hierarchical design method. In this part, **hardware implementation** and **demo video** are **NOT** required, build a testbench to observe the waveforms of the input and output, and **capture the entire screen** of Vivado with the simulation waveforms for submission. [30 marks]



Hints

- a. Some antivirus software may stop the simulation process of Vivado, so disabling the antivirus software is preferable.
- b. Since the Q' feed back to the input D, it cannot be initialized in the testbench. It should be initialized in the VHDL of the divide-by-2 counter.
- c. For setting up the testbench, please refer to the example in Lec00b VHDL First Example Using Vivado and Basys3. The output will be something like shown below:



THE END