Report

Opcodes are given below.

```
Loadi = "00001000"
mov   = "00000000"
add   = "00000001"
sub   = "00001001"
and   = "00000010"
or    = "00000011"
j     = "00000100"
beq   = "00000101"
mult  = "00100110"
sll   = "01000110"
srl   = "01100110"
sra   = "10000110"
ror   = "10100110"
bne   = "11000110"
```

following opcodes are not used.

```
load    = "00011000"
store   = "00011001"
```

As the 3 bit ALUOP is not enough for all the given functions, first 3 bits of each opcodes are used as 3 bit EXTRA and that helps to implement all the functions.
So from each opcodes last 3 bits of the opcode is used as ALUOP and the first 3 bits of the opcode is used as EXTRA.

For logical shift left,logical shift right,arithmatic shift right and rotate right functions, a latency of 2 time units are added.And also for default cases result zero will be generated with a latency of 1 time unit.

For bne fuction, a new control signal is used as "bneIndicator" and that indicates whether a bne instruction is available to execute.In addition same data path which is used for j and beq instructions, is used for bne function as well.