Theo Hatzis, MSc

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USt-IdNr: DE259921718 ▫ Language: English▫ available Summer 2022

Engineer with experience in mobile platform design verification, post-silicon component verification, silicon validation, and schematic design capture work seeks new projects in hardware design and test; or in post-silicon semiconductor verification testing and validation

- Experience includes electronics design and development of medical devices and diagnostics equipment, scientific instruments, highways informatics subsystems, wireless-handheld terminals; Hardware verification on 3G/4G modems; Validation of DCDC converters and PMICs; and IBJT and SiC gate drivers

- My interests include test-related work on sensor-based systems, sensor-conditioning and interfaces, and component verification of power devices (DCDC/PMICs, MOSFETs, IBJT, SiC, GaN and gate drivers), ADC and RF blocks, Power and Battery. Automated testing with MATLAB, Python, Teststand, and LabVIEW. Test-data analysis and visualization with libraries, including Pandas, Numpy, Matplotlib, and Plotly

- Industry sectors worked in my career include semiconductor testing, electronics design for 3G/4G hardware, medical devices, medical diagnostics, industrial materials analysis (oils, fats, chocolate and cements), photovoltaics and traffic data and highways informatics subsystems

Experience Areas

Semiconductors
- Component verification of IBJT and SiC high-voltage gate drivers
- Validation of DCDC, Buck-Boost, Charge Pumps, PMIC Chipsets, and Modems PMU
- Correlations between Simulation and ATE and Bench
- Datasheets and PRQ Verification
- Automation of test cases with MATLAB, Python/PyVISA/Pandas, Teststand, LabVIEW, C#/VISA, Test-Frameworks, and APIs
- FMEDA
- ADC measurements
- Issues and investigations
- Competitive analysis and side-by-side work

Hardware Design and Verification
- Architecture and Concept design and design captures
- Component technology selection
- Design of 8/16/32 embedded microprocessor applications, analogue, digital, ADCs, DACs and interfaces
- JTAG, Lauterbach Power Trace32, I2C Analyser, Logic Analyser, Clocks Jitter, SIM test, USB test
- Multiphase, master-slave DCDC FPGA core supply design for Stratix III FPGA and Power routing
- Schematic design capture with Mentor Graphics (Expedition), Protel SE (or Altium) and OrCAD
- Simulation with LTSPICE and Simetrix

Equipment, Tools and Software
- Python libraries, Pandas, Numpy, Plotly, MATPLOTLIB, YAML, PyVISA and Ninja2
- Visual Studio, VSC, PyCharm, Teststand, LabVIEW, GIT, Matlab, C# and Teststand
- Mentor Graphics (Expedition), Protel SE (or Altium) and OrCAD
- Bench (with VISA mainly) includes Keithley 2400, 2450 2460, 2000/2001, Agilent B2912, 335600, 34465A, N6705A, 90408A, 91600X, Tektronix 3022, Lecroy HDO8108A, Tektronix 4000/5000, Rohde Schwarz FSW8 and CMW500; Lauterbach Power-Trace and the JTAG debugger

- Spotfire for Windows
- JAMA, Jira with Kanban
- MSOffice automation (C#/.NET), WinForms, PyQT
- LTSPICE and Simetrix SPICE

Training

Courses in RF Circuit and System Design, TestStand, LabVIEW, EMI, ESD, Spectrum Analyzer, Allegro/Cadence, TIBCO Spotfire. Schools MSc (distinction), BSc(Hons) and HNC(BTEC). Roads Signing and Guarding and Highways Safety courses

Projects

Component Verification Engineer, Infineon Technologies AG, PS ATV, Oct 2021 – June 2022 [Hays]
- Component verification on high-voltage IBJT/SiC gate drivers; Test reports, verification reviews

Test and Verification Engineer for Radar Applications, Infineon Technologies AG, Oct 2020 – Mar 2021 [Hays]
- Software development, 60GHz Radar Sensors SDK and GUI tests

Validation Expert, Texas Instruments GmbH, July 2018 – June 2020 [Hays]
- Device characterization and Bench validation of DCDC converters

Application Engineer, Dialog Semiconductor GmbH, October 2017 – April 2018 [Hays]
- Mixed-signal PMIC Chipset DCDC Buck evaluation and documentation

Validation Engineer, TI Deutschland GmbH, August 2014 – September 2017 [Hays]
- Device Characterization and Bench validation of DCDC Buck, Buck-boost and Charge pump devices

Senior Baseband Designer (Digital), Intel Mobile Communications GmbH, February 2011 – January 2014 [ERL]
- Intel XMM series XGOLD 2-4G modem reference designs verification

Senior Baseband Designer (Digital), Infineon Comneon GmbH, August 2010 – February 2011 [ERL]
- Infineon XMM series XGOLD 2-4G modem reference designs verification

Hardware Consultant, ST Ericsson AT (Ericsson GmbH), Jan 2006 – Dec 2009 [Harvey Nash]
- Concept design and implementation of power and distribution on early access FPGA-based boards intended for 3G+ and 4G protocol stack development, and power design for an LTE demonstration phone

Baseband Engineer, Texas Instruments A/S, Oct 2004 – Dec 2005 [WAC]
- 3G Mobile platforms designs verification. Validation test documentation.