Theo Hatzis, MSc

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USt-IdNr: DE259921718 ▫ Language: English▫ available from July 2022 or maybe later

Engineer with experience in mobile platform design verification, post-silicon component verification, silicon validation, and schematic design capture work seeks new projects in hardware design and test; or in post-silicon semiconductor verification testing and validation

- Experience includes electronics design and development of medical devices and diagnostics equipment, scientific instruments, highways informatics subsystems, wireless-handheld terminals; Hardware verification on 3G/4G modems; Validation of DCDC converters and PMICs; high-voltage IBJT and SiC gate driver verifications

- My interests include test-related work on sensors-based systems, sensor-conditioning and interfaces, and component verification of power devices (DCDC/PMICs, MOSFETs, IBJT, SiC, GaN and gate drivers), also with ADC and RF blocks. Automation test in MATLAB, Python, Teststand and LabVIEW. Visualisation and analysis of test data in pandas, numpy, matplotlib, and plotly. Automation test for automotive drives, power inverters and batteries stack. SPICE analogue design simulation. Also, work on Gas sensors, Magnetic sensors, and Radar devices would be great to do at an applications or verification test level

Experience Areas

Semiconductors
- Component verification of IBJT and SiC high-voltage gate drivers
- Evaluation of PMIC Chipsets Bucks and Validation of DCDC, BuckBoost, and Charge Pump devices
- FMEDA pins faults; Fault states
- Correlations with Simulation and ATE with Bench
- Resolving the Measurements against PRQs and Datasheet
- Test automation bench scripts in MATLAB, Python, C#, Teststand, LabVIEW
- Test frameworks and APIs as a user. Drivers and classes for advanced measurements
- Test automation scripting in MATLAB, Python, Teststand and with .NET/Python Adapters
- Issues and investigations work
- Verification on 3G and 4G-LTE Modems, mainly analog baseband topics (TI, Ericsson, Infineon and Intel), includes SIM, USB, RTC, Clocks Jitter, Power-domain decouplings on DDR2, and some transceiver and PA with two CMW500's related to DC power and Sensitivity
- Test-bench bare-metal microprocessor setup in timing-critical validation runs
- Standard DCDC converter measurements, e.g. protections, startups, shutdowns, ripple, load-transients, line-transients, inductor currents, glitches, and much much more
- Test reports, component verification meetings and reviews
- Competitive analysis and other side-by-side work
- Spread-spectrum modes, Noise emissions measurements with FSW8
- Quiescent current measurements

Hardware Design and Design Verification
- Architecture and Concept design. Design capture
- Component technology selection
- Circuit Design and PCB Layout Reviews
- Design of 8/16/32 embedded microprocessor applications, analogue, digital, ADCs, DACs and interfaces
- Design of FPGA and embedded micro boards
- Gained product acceptance and conformance testing in designs, EMV, EMC, CE, Sars, FCC, UL, Network, Safety and Environmental performance on industrial IT equipment. Often supported test-house usually on day one at their locale

- ADC measurements, gains, offset, INL, DNL, resolution and sample rates
- RF measurements, particularly on antenna matching and performance and EMC
- I2C, SPI, 1-Wire, UARTs, ADC INL and Testmode interfaces. Some C coding
- Boards designs verification functional tests, including PSU testing
- Multiphase, master-slave DCDC FPGA core supply on Stratix III FPGAs
- JTAG, Lauterbach Power Trace32, I2C Analyser, Logic Analyser, Clocks Jitter, SIM test, USB test
- Design of RS-485 Opto/galvanically isolated, line-bias, DTE V.29, DCE V26b interfaces, on existing highways infrastructure longitudinal 5km copper and PCM tranches
- Design documentation and Verification test documentation
- Prototype and Module testing
- Clock jitter, Eye diagrams and histogramming measurements
- High-Speed slewing GaN MOSFET active loads-design concepts and simulation

Equipment, Tools and Software
- Spotfire
- Python libraries, Pandas, Numpy, Plotly, MATPLOTLIB, YAML and PyVISA, Ninja2 and more
- Visual Studio, VSC, PyCharm, Teststand, LabVIEW, GIT, Matlab, C# and Teststand
- Mentor Graphics (Expedition), Protel SE (now Altium) and OrCAD
- Simulation with LTSPICE and Simetrix
- Equipment: Keithley 2400, 2450 2460, 2000/2001, Agilent B2912, 335600, 34465A, N6705A, 90408A, 91600X, Tektronix 3022 Lecroy HDO8108A, Tektronix 4000/5000, Rohde Schwarz FSW8 and CMW500; Lauterbach Power-Trace and JTAG debugger
- JAMA, Jira issues, Kanban and Webex

Training

Courses in RF Circuit and System Design, TestStand, LabVIEW, EMI, ESD, Spectrum Analyzer, Allegro/Cadence, TIBCO Spotfire. Schools MSc (distinction), BSc(Hons) and HNC(BTEC). Roads Signing and Guarding and Highways Safety courses

Projects

Component Verification Engineer, Infineon Technologies AG, PS ATV, Oct 2021 – June 2022 [Hays]
- Component verification on high-voltage IBJT/SiC gate drivers; Test reports, verification reviews

Test and Verification Engineer for Radar Applications, Infineon Technologies AG, Oct 2020 – Mar 2021 [Hays]
- Software development, 60GHz Radar Sensors SDK and GUI tests

Validation Expert, Texas Instruments GmbH, July 2018 – June 2020 [Hays]
- Device characterization and Bench validation of DCDC converters

Application Engineer, Dialog Semiconductor GmbH, October 2017 – April 2018 [Hays]
- Mixed-signal PMIC Chipset DCDC Buck evaluation and documentation

Validation Engineer, TI Deutschland GmbH, August 2014 – September 2017 [Hays]
- Device Characterization and Bench validation of DCDC Buck, Buck-boost and Charge pump devices

Senior Baseband Designer (Digital), Intel Mobile Communications GmbH, February 2011 – January 2014 [ERL]
- Intel XMM series XGOLD 2-4G modem reference designs verification

Senior Baseband Designer (Digital), Infineon Comneon GmbH, August 2010 – February 2011 [ERL]
- Infineon XMM series XGOLD 2-4G modem reference designs verification

Hardware Consultant, ST Ericsson AT (Ericsson GmbH), Jan 2006 – Dec 2009 [Harvey Nash]
- Concept design and implementation of power and distribution on early access FPGA-based boards intended for 3G+ and 4G protocol stack development, and power design for an LTE demonstration phone

Baseband Engineer, Texas Instruments A/S, Oct 2004 – Dec 2005 [WAC]
- 3G Mobile platforms designs verification. Validation test documentation.