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The FASER W-Si High Precision Preshower

Technical Proposal

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ABSTRACT: The FASER detector is designed to search for light weakly interacting new particles decaying into charged final states at the LHC. While the first physics data will be taken at the start of Run 3 of the LHC program, an upgrade is already foreseen to enhance the sensitivity to long-lived particles decaying into photons. A high-precision preshower detector will be constructed within the next two years allowing to distinguish the predicted axion-like particles signature of two very closely spaced highly energetic photons. Profiting from recent developments in monolithic pixel silicon detectors, the FASER Collaboration plans to build instrumented silicon pixel detector planes with a granularity of $100\text{ }\mu\text{m}$ interleaved with tungsten absorber planes. The addition of the new pre-shower detector will expand the physics search capability of FASER.

Contents

1	Introduction	3
2	Physics motivations	5
60	2.1 Physics case	5
	2.2 Expected performance	5
3	Detector environment	11
65	3.1 Radiation level and particle flux	11
	3.2 Ambient temperature and humidity	11
	3.3 Existing services in TI12	11
4	Monolithic detector readout chip	13
	4.1 Previous developments and prototyping	13
	4.2 FASER monolithic detector ASIC	15
70	5 Detector plane	20
	5.1 Module	20
	5.2 Plane layout	21
	5.3 Thermal management	23
6	Preshower layout	26
75	7 Backend readout chain and TDAQ	30
	7.1 Expected Data Rates	30
	7.2 Active Patch Panel (APP)	30
	7.3 Preshower Readout Board (PRB)	31
	7.4 Readout scheme	31
80	8 Detector integration	33
	8.1 Mechanics and cooling	33
	8.2 Service and powering	33
	8.3 Slow control and interlock	35
	8.4 Network	37
85	9 Software reconstruction and calibrations	38
	9.1 Detector simulation	38
	9.2 Photon reconstruction	38
	9.3 Detector calibrations	39
10	Project organisation, resources, costs and schedule	41

1 Introduction

The Forward Search Experiment (FASER)[1][2][3] at the LHC will permit searches for light and weakly interacting particles during Run 3 and beyond. While the main background will arise from the flux of neutrinos and muons reaching the FASER detector, long-lived particles (LLPs) would travel and decay with specific signatures within the detector active volume.

The proposed tungsten-silicon high-precision preshower will significantly extend the FASER sensitivity to LLPs decaying into photons, such as axion-like particles (ALPs) or CP-odd scalars. This new detector will allow to distinguish, for example, the predicted ALP signature of two very closely spaced photons with energy between 100 GeV and a few TeV from the irreducible background, constituted essentially by high-energy electrons produced by ν_e DIS interactions in the material in front of the calorimeter.

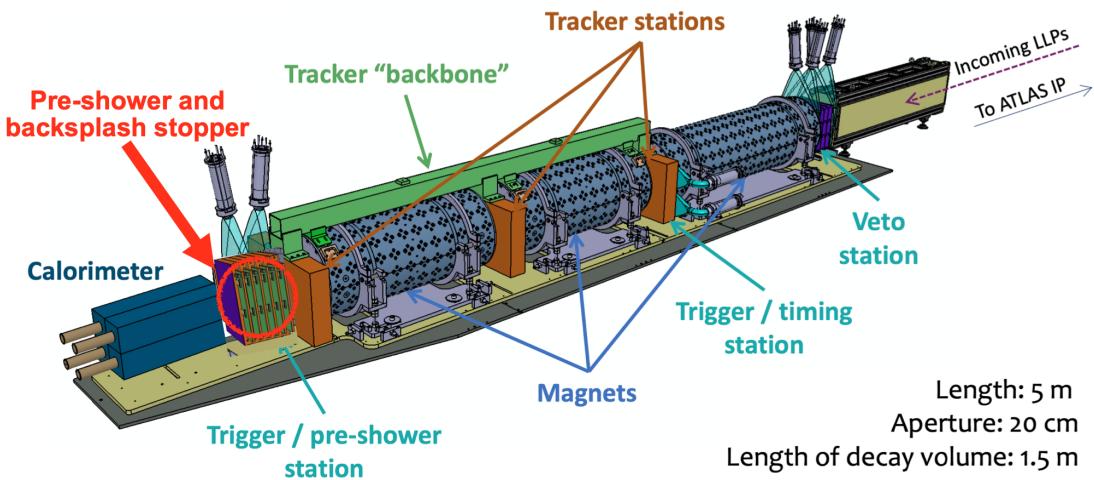


Figure 1: Layout of the FASER detector, showing the proposed high-precision tungsten-silicon preshower.

The high-resolution preshower will be installed in front of the calorimeter and partially replace the present FASER preshower, which contains 2 radiation lengths (X_0) of tungsten absorber (see Figure 1). In the proposed layout, six layers of 1 X_0 tungsten absorber alternated with planes of monolithic silicon pixel detectors will allow the longitudinal granularity needed for high-efficiency two-photon detection while maximising the rejection of backgrounds.

This detector upgrade uses as an opportunity the development of monolithic silicon pixel detector technology to instrument FASER with a very high granularity silicon preshower, avoiding the high cost and the production complexity typical of hybrid pixel detectors. The ASIC will feature hexagonal pixels with a pitch of 100 μm . A dedicated front-end has been designed with a very large dynamic range in the charge measurement, to be able to cope with the huge charges (up to 100 fC) deposited in single pixels at the core of the electromagnetic showers initiated in the tungsten planes by photons of the highest expected energies.

The preshower installation is scheduled at the end of 2023, to be able to take data in 2024 when

- ¹¹⁵ the LHC is expected to deliver an integrated luminosity of 90 fb^{-1} ¹. The detector will be available for data taking during the High Luminosity LHC (HL-LHC) period, when 3 ab^{-1} will be delivered. In order to minimize costs and schedule, it will use, where possible, existing or minimally modified components and infrastructure as used by the current FASER detector.

¹A 1 year extension to LHC Run 3 has been recently approved, which would allow the upgraded FASER detector either to collect an additional 90 fb^{-1} in 2025 or to consider spreading the installation towards 2024 if significant delay would be met

2 Physics motivations

120 2.1 Physics case

The LHC and the HL-LHC programs offer a unique opportunity to search for dark matter at the high-intensity frontier, with an approach that has not been exploited so far. FASER was the first experiment purposely designed to investigate the production at the LHC of low-mass LLPs decaying into two leptons, thus extending the LHC physics program. The discovery potential of FASER can
125 be extended further by enabling the precise measurement of LLPs having photons in the final state: the introduction of a new preshower detector made of interleaved layers of tungsten and silicon pixel sensors will make FASER the first and unique LHC experiment sensitive to low-mass LLPs with photons in the final state. It will also extend the FASER detection capability to all possible final states, maximizing the sensitivity to new physics of the experiment.

130 There are many models that predict LLPs decaying into photons:

1. The benchmark model that we chose to drive the design of the high-resolution preshower detector is that of ALPs, a broad class of pseudoscalar particles decaying into photons [4][5][6].
2. Any model involving LLPs that can decay into final states involving neutral pions, which then decay into two photons, like in $V \rightarrow \gamma\pi^0 \rightarrow 3\gamma$. A prominent example is a light dark scalar boson [4], which decays into two neutral pions. Another example is a sterile neutrino N decaying via $N \rightarrow \nu\pi^0$ [7].
135
3. Any model and extension of the previous cases in which the LLP decays into two charged pions and a neutral pion. An example is the $U(1)_B$ or $U(1)_{B-3L_{tau}}$ gauge boson considered in [8], which decays in $V \rightarrow \pi^+\pi^-\pi^0$. Another example would be an ALP with coupling to gluons, which would decay for example into $a \rightarrow \pi^+\pi^-\gamma$ or $\pi^+\pi^-\pi^0$ as considered in [9]. In these cases the information from the preshower and the one from the tracker would complement each other to reconstruct the event.
140

In addition to the above models, the new detector could enable the detection of a dark-sector
145 consisting of dark matter X_1 and another state X_2 with mass splitting $m_{X_2} - m_{X_1} < 1$ MeV, such that only decays $X_2 \rightarrow X_1 + \gamma$ are allowed.

In all the cases described, the photons would be highly energetic ($O(100\text{GeV} - 5\text{TeV})$) and very collimated. In the present FASER preshower and calorimeter, they would be indistinguishable from any high energy neutral background particle. The high-granularity preshower proposed here
150 will enable these measurements in FASER. It will increase the sensitivity of the present FASER detector, allowing a search that is complementary to the other LHC experiments.

2.2 Expected performance

To characterise the performance of the preshower detector, we consider a model of an ALP which couples to the field strength tensor of the $SU(2)_L$ gauge group via $\mathcal{L} \sim g_{aWW} a W\tilde{W}$, as discussed in [10]. After electroweak symmetry breaking, it acquires couplings to all the electroweak gauge
155 bosons, for example W -bosons and photons. The coupling to W -bosons allows for an abundant

production at the LHC, via loop induced decays such as $b \rightarrow sa$. Due to the high mass of the other weak gauge bosons, it exclusively decays into photons, making it an ideal benchmark scenario for this study. We produce a full simulation of the ALP production, propagation and decay to photons, probing several scenarios of ALP mass m_a and coupling to electroweak bosons g_{aWW} .

The study, based on events generated with the FORESEE numerical package [11], focused on the (m_a, g_{aWW}) parameter space ($0.10 \text{ GeV} < m_a < 0.48 \text{ GeV}$ and $8.2 \times 10^{-6} \text{ GeV}^{-1} < g_{aWW} < 4.3 \times 10^{-4} \text{ GeV}^{-1}$) not yet excluded by experiments. Figure 2 shows the photon energy distribution for three points in the (m_a, g_{aWW}) parameter space, which highlights the importance of a detector sensitive to a large range of photon energies from about 100 GeV to several TeV.

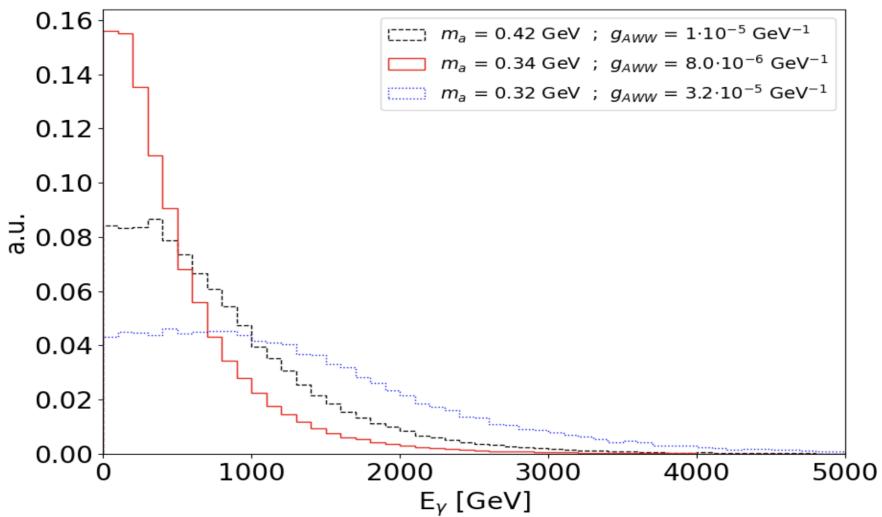


Figure 2: Simulation result. Photon energy spectra for three of the considered ALP physics cases. The three distributions are normalised to unit area.

To account for the different kinematics of distinct (m_a, g_{aWW}) parameter-space points, we have parameterized the efficiencies for two-photon reconstruction as a function of the energies of the two photons and their spatial separation. We built a Geant4 [12] simulation of the FASER preshower detector, whose performance has been assessed by simulating photon pairs at the various energies and separations of the ALP decays. To cover all relevant scenarios photon-pairs were generated via the Geant4 "particle gun" for all combinations of the discrete photon-energy values $E_\gamma = [250, 350, 450, 750, 1000, 1500, 2000, 3500] \text{ GeV}$ and spatial separations $\delta_{\gamma\gamma} = [0.2, 0.3, 0.5, 1.0, 2.0] \text{ mm}$. Several detector configurations were studied, which include 4, 5, or 6 silicon planes, 4 to 6 X_0 of tungsten radiators positioned in different configurations as well as pixels of 50 and 100 μm pitch. Figure 3 shows the charge deposited in $100 \times 100 \mu\text{m}^2$ pixels in the sixth silicon layer by two photons of energy 750 GeV and 1.5 TeV respectively, generated at 200 μm distance from each other. The two photons are clearly distinguishable, and are each characterised by a pixel in which a very large energy is deposited, surrounded by a large number of firing pixels over a region of several mm^2 . Thus the simulations support the need for a detector that integrates small pixel size, very large dynamic range and the capability to read thousands of pixels in a single event.

One of the reasons to sample the shower at different stages of the development comes from a

small fraction of low-energy electrons depositing a large energy in a single pixel. Those electrons are generated in the shower, most of them from local backsplash coming from the silicon itself near the sensor active area. Since these very large energy deposits are local to a specific silicon plane, this background can be eliminated verifying that adjacent planes do not show similar large deposits in the same position. This necessity to confirm a large energy deposit at different stages of a shower is one of the reasons that motivates several silicon planes. Another possible source of background is the Deep Inelastic Scattering (DIS) of neutrinos in the preshower itself, which would be indistinguishable from the photon signal without tracking the propagation of the shower core.

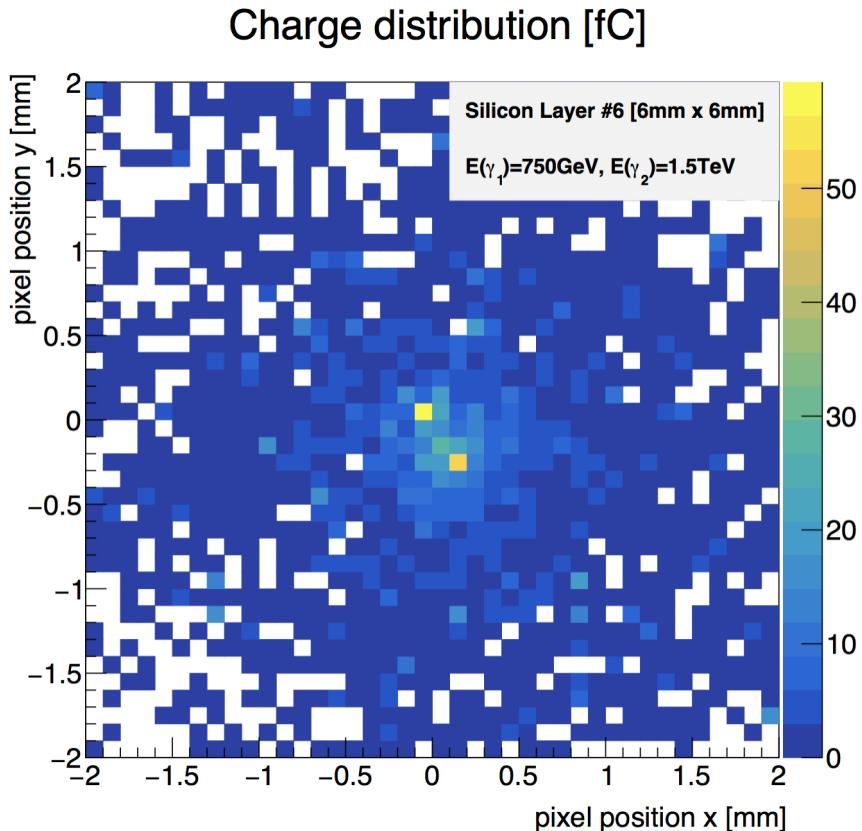


Figure 3: Simulation result. Charge deposition across the pixels of the 6th silicon layer by two photons of energies of 750 GeV and 1 TeV and a separation of 0.2 mm. Only a small area of 4×4 mm² around the photon positions is shown.

A simple photon-reconstruction algorithm was developed to reconstruct the positions and the layers of conversion of the two photons using the charge deposition in each pixel across the different preshower silicon planes. This study showed that among the different detector configurations considered, the one with six layers of $1 X_0$ of tungsten each followed by a plane of silicon pixel detectors with 100 μm pitch provided the needed performance over the photon energy range studied. As shown in Figure 4 we found that even the simple algorithm that we developed provides an efficiency of resolving photon pairs of 65-75% for a separation $\delta_{\gamma\gamma} = 0.2$ mm, which rises to 85-90% for $\delta_{\gamma\gamma} = 0.3$ mm or larger, where the variation in the quoted efficiencies is due to the

variation of the energies of the photon pairs. The same algorithm was also used to study how often two photons are reconstructed when only one photon is generated. This study gives a fake rate of about 2% for $E_\gamma = 1$ TeV, raising to about 4% for the highest relevant photon energies.

To evaluate the preshower performance with a more evolved reconstruction, we have developed a di-photon event tagging algorithm that uses a convolutional neural network, which treats the event reconstruction as an imaging problem [13][14]. The preliminary results are very promising: as shown by the blue curve in Figure 4 the machine-learning-based approach achieves 95% efficiency and < 0.5% fake rate, outperforming the more conventional event-reconstruction algorithm.

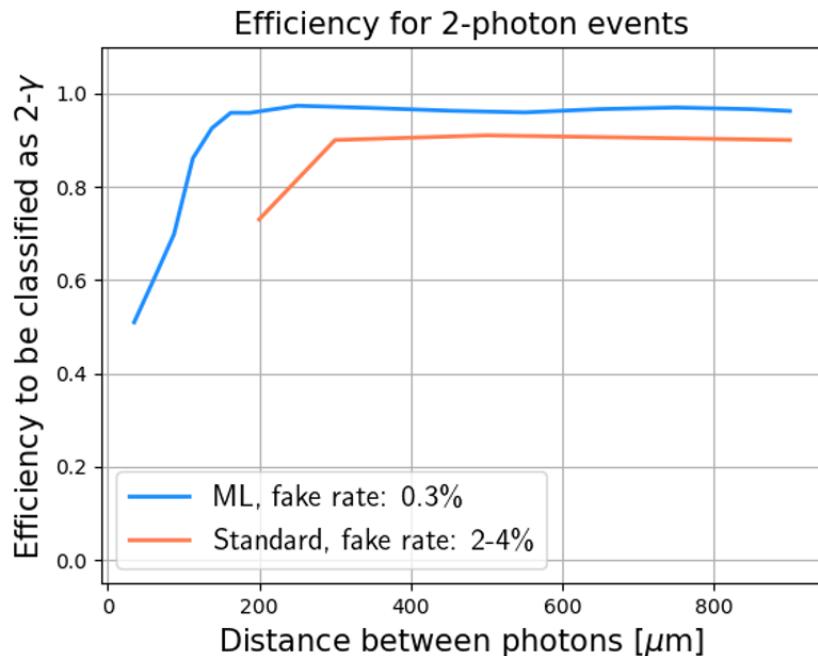


Figure 4: Di-photon event tagging efficiency expected for the upgraded preshower. The orange line shows the results obtained with the purposely-developed conventional algorithm. The blue line shows the results obtained with a Machine-Learning-based approach. Photons of 1 TeV energy are considered in this study.

We highlight that a pixel pitch of 100 μm and the longitudinal granularity provided by six silicon layers allows simultaneous reconstruction of the shower positions of two close by photons within a large energy range (from 100 GeV to several TeV) and provides a minimum redundancy for an effective operation during data taking. The marginal gain provided by the 50 μm pixel pitch was not large enough to justify the increase of complexity, power consumption and dead space of the resulting ASIC.

The results obtained with the simple reconstruction algorithm were used to assess the discovery potential for ALPs with the proposed preshower. The di-photon reconstruction efficiencies as a function of the photon energies and separation were used together with the ALP predicted cross-section for the various (m_a, g_{aWW}) points in the ALP parameter space considered. The results are shown in Figure 5, where the curves for FASER correspond to the observation of at least 3 signal events with 100% background rejection, and are calculated for an integrated luminosity of 90 fb^{-1} .

(the luminosity expected to be delivered by the LHC in 2024) and 3 ab^{-1} (the expected luminosity from the HL-LHC). The results are shown for two cases: i) an ideal detector with 100% identification efficiency for photon-pairs across the whole energy and separation range (red and blue lines); ii) the realistic scenario in which the efficiencies of the preshower detector from the reconstruction algorithm described above are applied, with different scenarios of minimal separation between the photons (black curves). Figure 5 shows clearly that the preshower detector we propose will allow FASER to significantly extend the sensitivity reach of past experiments already with the 90 fb^{-1} to be delivered by the LHC in 2024.

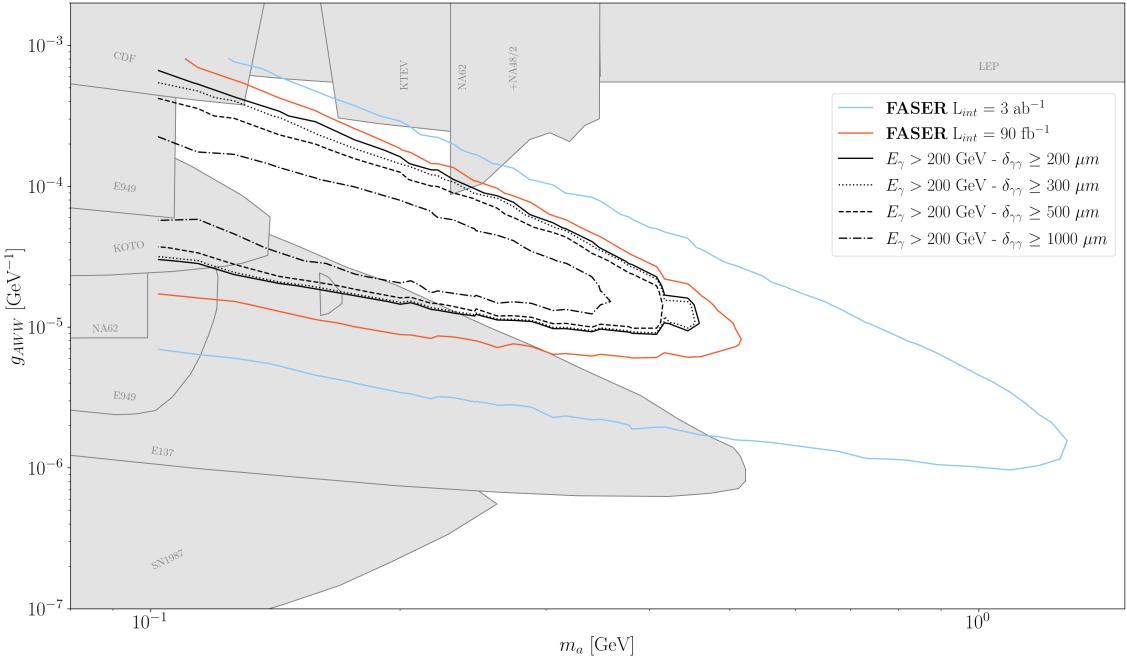


Figure 5: Sensitivity reach of the FASER W-Si preshower in the ALP parameter space. The blue and red lines show the reach for an ideal detector with 100% photon-pair reconstruction efficiency for the Run-3 (90 fb^{-1}) and HL-LHC (3 ab^{-1}) expected integrated luminosities for 14 TeV collision energy. The black lines show the sensitivity reach for 90 fb^{-1} of data including simulated efficiencies for photon-pairs with $E_\gamma > 200 \text{ GeV}$ and various values of $\delta_{\gamma\gamma}$. The grey-shaded regions represents the parameter space currently excluded by experiment [10][6].

The sensitivity reach is calculated for the acceptance of the proposed new FASER preshower. The preshower will cover an area of $175 \times 134 \text{ mm}^2$, which corresponds approximately to 74% of the total FASER acceptance (a 10 cm-radius circle determined by the magnet aperture).

As well as allowing a robust $\text{ALP} \rightarrow \gamma\gamma$ search, the updated detector could also improve the search for dark-photons ($A' \rightarrow e^+e^-$) or similar final states. Here the upgraded preshower allows more measurements of charged particles at the back of the detector, compared to the existing back tracking station, and with better position resolution. This could allow to separate very closely spaced tracks, which can not be separated with the current detector, and may allow to increase the length of the decay volume, to include the second magnet, increasing the acceptance by 70%. It will also make the detector more robust to possible inefficiencies in the back tracking station

(for example if one or more modules is lost). However, the addition of the new preshower, which includes 6 radiation lengths of material in front of the calorimeter, compared to the 2 radiation lengths in the current preshower, will degrade the calorimeter energy resolution. This degradation can be mitigated by correcting the calorimeter energy, taking into account the preshower data - but
240 such a correction will not be possible outside of the region where the preshower is instrumented. It should be noted that a minor degradation of the energy resolution of the calorimeter is not expected to effect the physics of FASER.

3 Detector environment

In this section we describe the expected detector environment for the FASER preshower upgrade,
245 including the radiation level, high energy particle flux, ambient temperature and humidity, as well as the existing services installed for FASER, which will be used for the preshower upgrade.

3.1 Radiation level and particle flux

In preparation for FASER in 2018, FLUKA [15] simulations and in situ measurements were made
250 in order to understand the flux of high energy particles and the radiation level in TI12. These studies are documented in detail in the FASER Technical Proposal [1].

The FLUKA simulation estimate of the radiation level in TI12 corresponds to a dose of less than $5 \cdot 10^{-3}$ Gy per year and a 1 MeV neutron equivalent fluence of less than $5 \cdot 10^7$ per year.
255 These estimates were validated by measurements taken with a CERN BatMon radiation monitoring device installed in TI18 (the symmetric tunnel to TI12 on the other side of ATLAS) during 2018 running. It is therefore expected that radiation will not be a problem for the preshower detector or the associated electronics.

The FLUKA simulations also showed that a flux of 0.5 Hz cm^{-2} of high energy muons will traverse the area of the FASER location, for a luminosity of $2 \cdot 10^{34} \text{ cm}^{-2} \text{s}^{-1}$ (the expected peak luminosity in LHC Run 3). For the HL-LHC this rate will increase with the luminosity to 1.25 Hz cm^{-2} at $5 \cdot 10^{34} \text{ cm}^{-2} \text{s}^{-1}$. Measurements with an emulsion detector show good agreement with this estimate, and additional measurements with a TimePix beam-loss monitoring system show that the rate of charged particles is correlated with the ATLAS luminosity as expected from the FLUKA simulations.

3.2 Ambient temperature and humidity

265 In 2018, before the installation of FASER the temperature in TI12 has been measured to be very stable at 19°C . After the installation of electronics related to FASER the temperature is higher but below 22°C . The humidity of the air in TI12 has been measured to vary considerably. In order to avoid problems from condensation, the cooled FASER tracker stations are flushed with filtered dry air provided by CERN EN-CV, and a similar approach will be used for the preshower upgrade.

270 3.3 Existing services in TI12

For FASER a new 16A/400V 3-phase electrical power circuit/breaker was installed into TI12. This can provide a total power of 11 kW, of which FASER is using 5 kW, leaving more than 5 kW which is expected to be sufficient power for the preshower. The power is separated into six circuits of which one can be used for the preshower with a small reconfiguration of the breaker to increase the limit for that circuit to 2kW. The circuit for the cooling unit will also be used for the cooling of the preshower. In addition to this power there is also a small (10A \times 220V) UPS power circuit installed into TI12 for FASER, which is used for powering the DCS hardware electronics, and the DCS network switch. A small amount of UPS power could be used for the detector-monitoring and safety systems needed for the preshower system.

275 FASER uses seven optical fibers for communication from TI12 to the servers in the surface building SR1 in point-1 (2 pairs for DAQ and 1 pair for DCS, and 1 fiber for the clock and LHC

signals). The current setup has a total DAQ bandwidth of 10Gb/s. In total 24 fibers were blown from TI12, so the bandwidth needs could be significantly increased without laying new fibers, if the existing unused ones are connected. Such an increase in bandwidth is not expected to be needed.

285 For FASER operations with an event size of 25kB and a trigger rate of order 500 Hz we expect to use a bandwidth of 100Mb/s. At HL-LHC luminosity this could increase to 400Mb/s, not including the preshower or other upgrades.

Space in TI12 for additional electronics is rather limited. The two electronics racks installed for FASER are full, and there is no space to easily install a third rack without restricting access. It
290 is currently planned that the preshower readout electronics will be situated on the detector (as is the case for the FASER tracker), and these will be connected directly into the current DAQ network switch. Therefore the only additional space required will be for the power supplies of the preshower system. As is discussed in more detail in section 8.2, these have been chosen such that the full system (including both HV and LV) can be housed in 1 MPOD crate. There is room for this crate
295 to be installed in a mini-rack behind the current electronics racks in TI12.

4 Monolithic detector readout chip

4.1 Previous developments and prototyping

The design of the monolithic detector ASIC that will be used for the upgrade of the FASER preshower is based on an R&D that has been ongoing at the University of Geneva since 2015

³⁰⁰ [16][17][18][19].

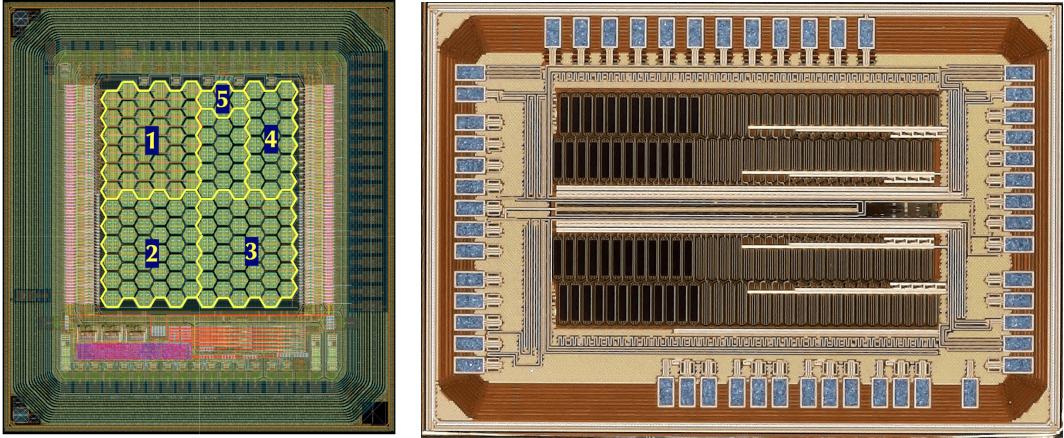


Figure 6: Left: prototype chip with hexagonal pixels of the final size of the FASER WSi preshower. The ASIC contains four matrices with different electronics implementation as well as the analog channels (indicated by "5") which were tested with sources and at a testbeam. Right: the prototype chip produced to validate several possible front-end configurations expressly produced for the FASER preshower. These two prototypes were manufactured in the same SG13G2 130nm IHP process that will be used for the final FASER ASIC.

Figure 6 left shows a small prototype with pixels of the final size that was used to measure the efficiency and the time resolution. The results obtained at a testbeam line at CERN in summer 2021 are shown in Figure 7 [20]. A degradation of the time resolution is observed at lower amplifier bias current, due to the worsening of the pre-amp Equivalent Noise Charge (ENC) and signal rise time. Despite this, the results show that the time resolution measured at the lowest pre-amp bias current of $7 \mu\text{A}$ is more than sufficient for the preshower, where the requirement is to be able to assign the event to the correct bunch crossing of the LHC. This value of the amplifier current was selected to match the power consumption that can be handled by the water-based cooling system available from the FASER tracking detector: for the final chip we can foresee a power consumption of 150 mW/cm^2 , which corresponds to a current budget of $12.5 \mu\text{A}$ per pixel. The efficiency of the same prototype ASIC was also measured at the beam line. Figure 8 shows that already at a sensor bias voltage of 120 V the efficiency is larger than 99.5% at the highest power consumption. The small drop observed for Minimum Ionizing Particles (MIPs) at lower current is due to the limited depletion region depth of the prototypes under test ($24 \mu\text{m}$). This effect, which has no impact on the detector performance in reconstructing the EM shower core, will not be present in the FASER preshower detector, which will have a depletion region depth of $50 \mu\text{m}$.

A second prototype specifically designed (Figure 6 right) to validate possible configurations of the front-end electronics in pixel was produced in fall 2020 and tested in spring 2021 [21]. The

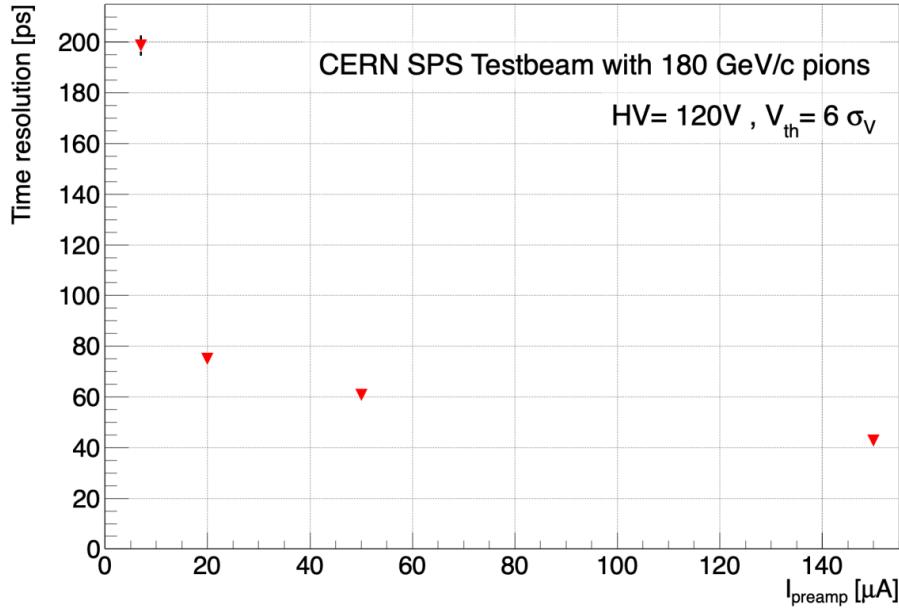


Figure 7: Time resolution vs. bias current in the pre-amplifier as measured with the prototype of Figure 6 left for a sensor bias of 120 V. The measurement was obtained by a coincidence between two identical detectors in a testbeam at CERN.

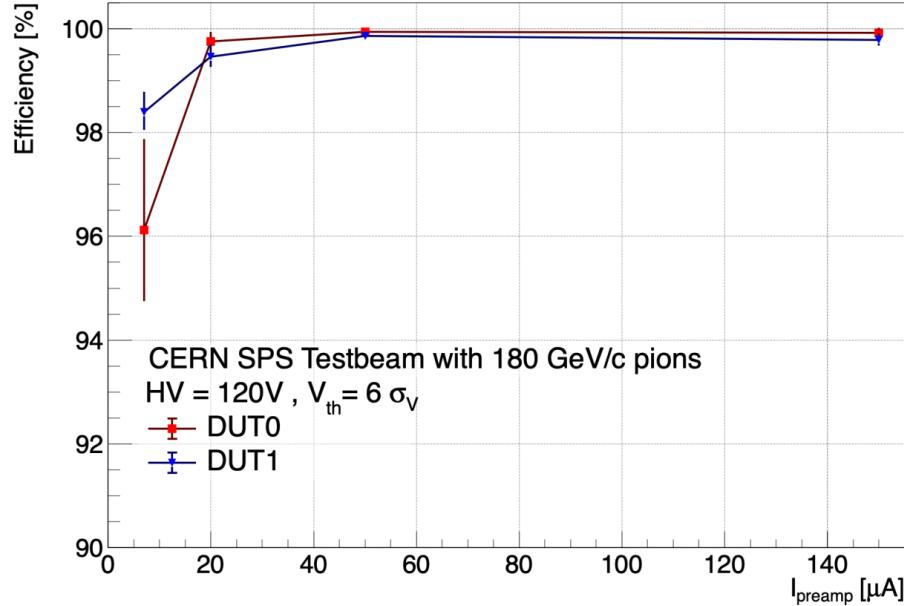


Figure 8: Efficiency to detect MIPs vs. amplifier current as measured in a testbeam at CERN with two prototype detectors (DUT0 and DUT1) like the ones described in Figure 6 left.

result showed that both a large pixel configuration with all the front-end electronics contained in a
320 pixel and a reduced configuration with only an amplification and driver stage in each pixel can be used and are compatible with the power and sensitivity requirements of FASER.

4.2 FASER monolithic detector ASIC

The silicon pixel detector proposed for the upgrade of the FASER preshower is a monolithic silicon pixel sensor in 130nm SiGe BiCMOS. The technology used for the ASIC is SG13G2 from IHP Microelectronics². The chip will be able to discriminate particle showers generated by two photons with energies ranging from 100 GeV to 3 TeV, with a separation between the primary particles above 200 μm .

Geant4 simulations of the detector (Section 2.2) show that the ASIC should be able to measure independently the charge in each pixel and time tag the events at a pixel level with sufficient time resolution to provide bunch crossing identification. The use of SiGe Heterojunction Bipolar Transistors (HBT) for the signal amplification, which delivers the best noise performance with a fast signal integration, guarantees a time resolution of 300 ps, more than sufficient for the new preshower. The possible use of this excellent time resolution to improve the event reconstruction will be investigated when developing the offline reconstruction software. Depending if it is in the core or in the periphery of a photon shower, the expected charge per pixel ranges from 1 fC to 100 fC in the case of the most energetic photons. Since the scope of the preshower is to separate the cores of two adjacent electromagnetic (EM) showers, the ASIC charge-measurement capability must have a large dynamic range. As a consequence, we have opted for a design in which the charge measurement in pixel can be done with 4 bit resolution using a logarithmic compression of the dynamic range.

The sensor ASIC will feature a matrix of N-on-P hexagonal pixels of 65 μm sides, each pixel containing the front-end electronics and analog memories to store the charge information. The sensor will be produced on special wafers with a 50 μm thick, high-resistivity boron doped epitaxial layer on top of a highly doped P-substrate. It will reach the target depletion depth at the nominal bias voltage of 120 V, with the possibility to be operated at maximum 200 V. The ASIC will be composed of 13 "super-columns", each "super-column" composed of 16 pixel columns, each with 128 pixels and all share a common digital logic. Each super-column is composed of 8 identical 16 by 16 matrices one above the other, referred to as "super-pixels". The total matrix size is 208 \times 128 pixels, with a chip size of $2.2 \times 1.5 \text{ cm}^2$. Figure 9 shows a portion of the ASIC layout, highlighting a super-pixel. The preshower will be composed by 432 ASICs, for a total of 11.5 Mpixels. The division in super-columns and further more in super-pixels allows sharing the local digital electronics among a large number of pixels: this solution will generate a local dead area of only 5.9% inside the pixel matrix. The ASIC will have also a digital periphery and guard ring which accounts for 720 μm of dead area on the readout side and 260 μm of dead area on the other three sides. This dead area is compensated by overlapping of the ASICs on the detector module (Section 5.1).

The chip features a slow-control interface implementing a Serial Peripheral Interface (SPI) protocol, that allows to configure the chip and its many internal Digital-To-Analog Converters (DACs), so that the working point of all the analog structures can be tuned to optimize their operation. The detection threshold can be set arbitrarily, and multiple zones of the chip can be set to a different threshold to compensate for process gradients.

²<https://www.ihp-microelectronics.com/>

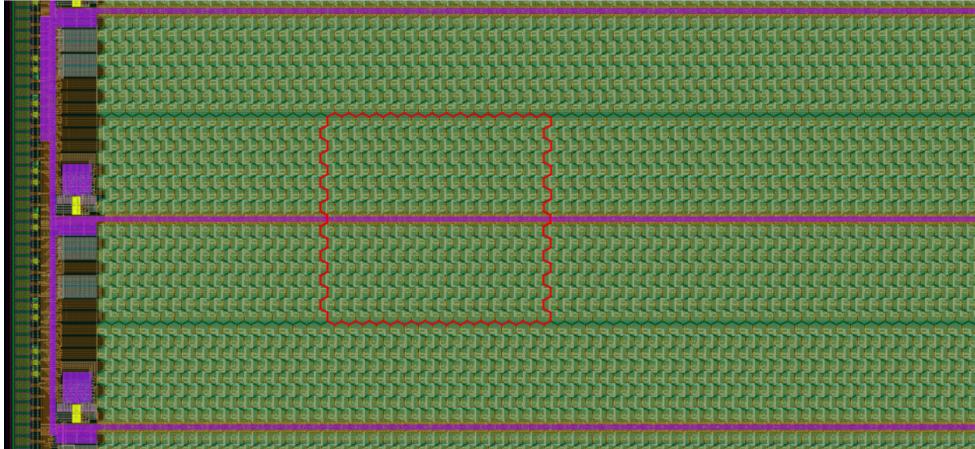


Figure 9: Detail of the layout of the FASER pre-production ASIC showing a portion of the pixel matrix and on the left the digital periphery. A super-pixel is contoured in red.

When a particle hits the sensor, the charge information is stored in analog memories inside the pixels, while three fast-OR signals per super-pixel are sent to the digital periphery to generate a trigger. The time of arrival of fast-OR signals are digitized at the base of the column using a multi-channel Time-to-Digital Converter (TDC). After receiving the trigger, the digital periphery will start the readout of the chip, one column at a time, starting from the leftmost and continuing right. During the column readout, the charge stored into the analog memories is digitized at super-pixel level. Corresponding pixels from different super-pixels are digitized at the same time using a 256-to-1 analog multiplexer and a 4-bit flash ADC. This structure is repeated for each super-pixel. The charge information is then transferred down towards the periphery and the readout will move to the following pixels, switching the multiplexer to its next connection until all the pixels are read. This solution allows limiting the amount of area dedicated to the digital memories to just a 5-bit register per super-pixel. Figure 10 shows the working principle of the super-pixel. This architecture would generate a very large amount of data if every pixels needed to be read out. For this reason the data is compressed on-the-fly by the readout logic, sending a much shorter data stream if only a few pixels are hit. The exact amount of data being sent out depends on the occupancy and the exact positions of the hits, but in a typical case (less than 10 pixels firing for a muon signal) the data stream can be compressed to less than 4 kb, including charge and timing information for all the pixels hit and all the necessary data for an event-by-event measurement of the TDC time base³. The data is read out using a single LVDS line reading at 200 Mb/s, making a typical readout 20 μ s long.

The front-end electronics will be based on SiGe HBTs, using a design validated in the prototyping phase leading to this proposal. The front-end consists of a preamplifier and a low-impedance driver, both integrated in the pixel active area, and a charge measurement circuit. The output of the driver is compared with a fixed threshold and a local metal-to-metal capacitor implemented on

³The pixel occupancy for signal events increases with the development of the EM shower, with the highest occupancy expected in the last preshower plane. The nominal discrimination threshold will be set at 1 fC, with the possibility to adjust its value between 0.5 and 4 fC to have a uniform occupancy on the preshower detector planes.

top of the pixel is charged with a constant current for a time proportional to the input charge. The voltage at one terminal of the capacitor is then sampled and converted on-the-fly to a 4-bit digital value by a flash ADC during readout.

Each pixel can be masked after the discrimination stage, with a mask bit that can be programmed via the SPI. This mask bit also controls the propagation of an analog test pulse with a programmable amplitude, that can be used to characterize and calibrate the pixel matrix.

The nominal power consumption by design is $150 \text{ mW} \cdot \text{cm}^{-2}$, mostly due to the absorption from the front-end electronics.

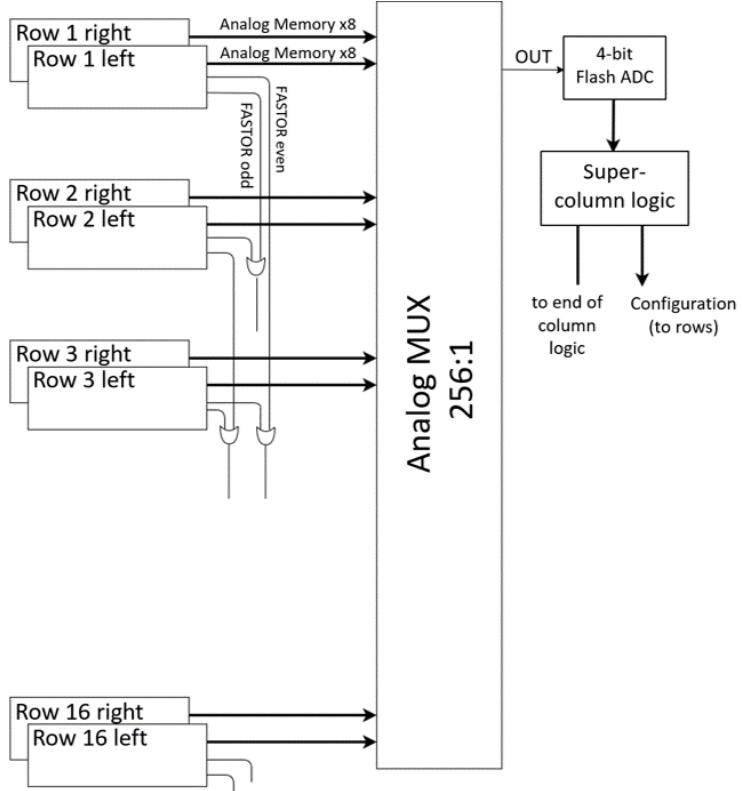


Figure 10: Conceptual diagram of a super-pixel.

The main specifications of the ASIC area reported in Table 1.

Table 1: Main parameters of the ASIC.

	Nominal
Area [mm²]	15.445×22.154
Thickness [μm]	150
Bias voltage [V]	120
Number of pixels	128×208
Hexagonal pixel side [μm]	65
Power consumption [mW · cm⁻²]	150

395 Three test versions (pre-production) of the ASIC with 4 and 3 columns were submitted in June 2021 (Figure 11). Figure 12 shows a diagram of the pre-production chip architecture. The three-column versions of the chip have alternative designs of the front-end and charge measurement technique. The final ASIC submission is foreseen for June 2022.

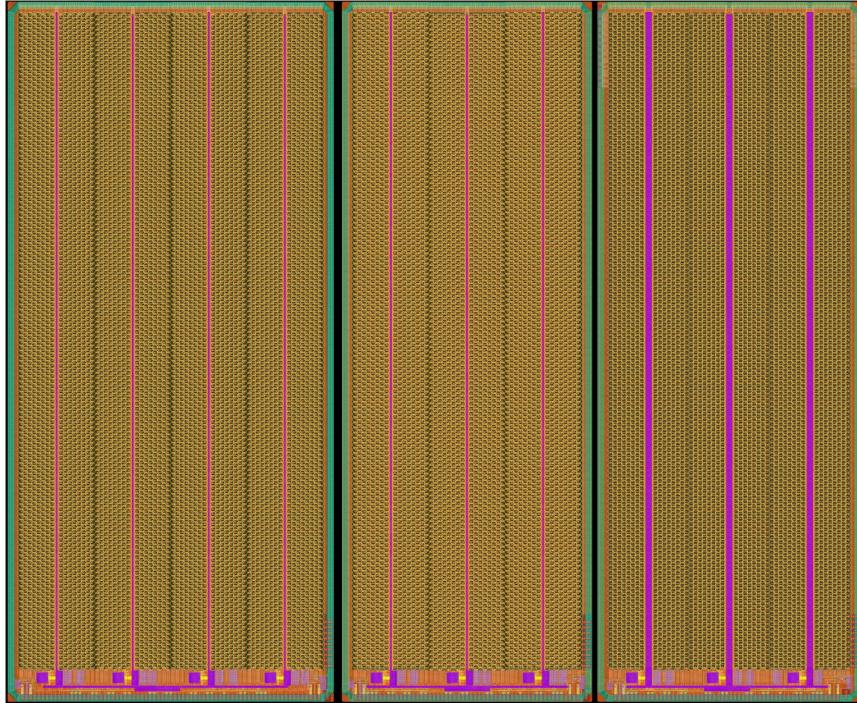


Figure 11: Fabrication reticle of the FASER pre-production ASIC. Three matrices with full-length super-columns have been submitted for production. The main matrix, on the left, has 4 super-columns with the full functionality of the final chip. The other two matrices, each with three super-columns, contain variations of the front-end electronics and charge measurement circuit.

400 The leading institute for the design of the ASIC is the University of Geneva. CERN and KIT participate also to the design and verification of the monolithic chip with experienced ASIC designers.

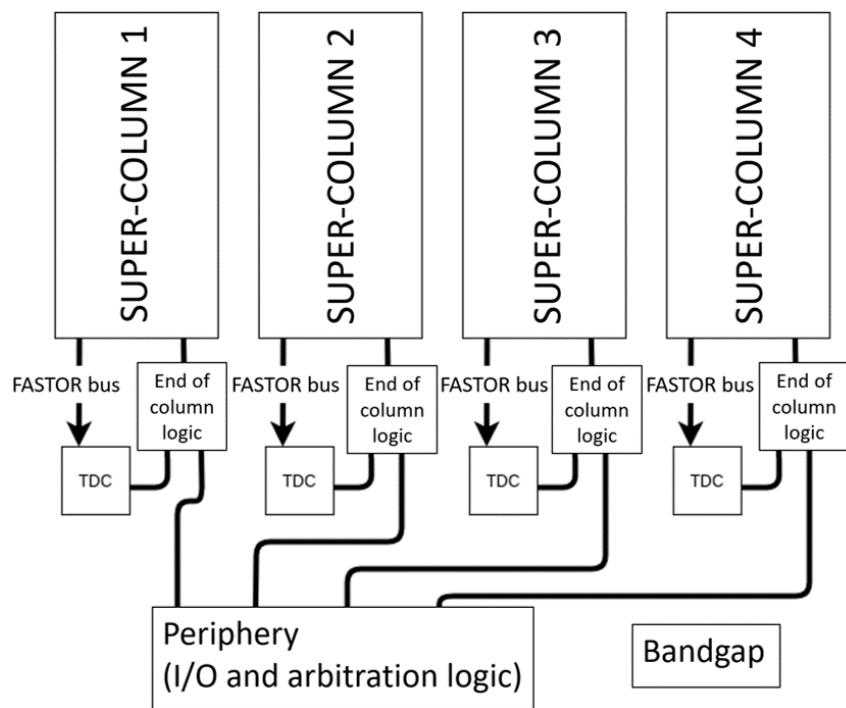


Figure 12: Conceptual diagram of the FASER pre-production monolithic detector ASIC.

5 Detector plane

5.1 Module

The readout module will consist of an assembly of six ASICs mounted in an array of two by three.
405 Given the expected dimensions of an ASIC the module size will be $31 \times 67 \text{ mm}^2$. The gap between the ASICs will be minimal, leading to an inactive area of the order of the guard-ring width ($\lesssim 300 \mu\text{m}$).

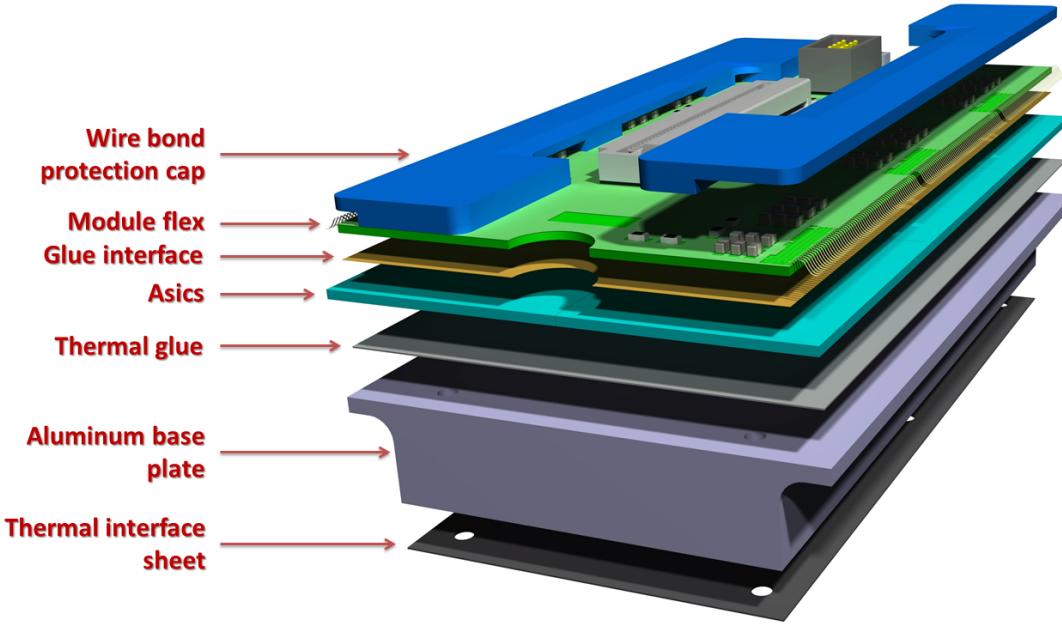


Figure 13: Exploded CAD view of a module assembly. A module is composed by six ASICs glued to an aluminum base-plate. The module flex with the electrical interconnection and the SMD components is glued on the top of the ASICs. The bottom layer is the thermal interface sheet that will be added when integrating a module to the cooling plate. The size is $\sim 31 \times 67 \text{ mm}^2$.

Each module will be supported by a base-plate with thermo-mechanical and electrical insulation features (See Figure 13). The base-plate will be made of aluminum with a high thermal conductivity.
410 The base-plate will be machined with six threaded holes plus a reference mounting hole and slot. It will then receive an electrolytic passivation treatment called hard anodising for surface insulation and protection of the sensor edge against electrical breakdown. This procedure was already used to produce the first thermo-mechanical prototype (Figure 14).

The electrical interface to the six ASICs for the I/O and powering will be made through a flexible printed circuit board (PCB). Each ASIC has ~ 100 wire bonding pads to be interconnected to the flex PCB. The module flex will be interconnected to an external patch panel with zero-insertion force connector for the digital signal, clock and command and with a separate pigtail for the module powering.
415

The module will drive four types of power lines, three LV supply and one HV for the six ASICs.
420 While the sensors will have low current consumption (below $100 \mu\text{A}$), the analog, the digital and the driver supply lines will consume $\sim 1 \text{ A}$ each. The system is designed to handle a module power



Figure 14: Picture of the prototype of the module aluminum base block to be used for the assembly support.

consumption of 4 W (30% more than the expected value by chip design), with the heat dissipation flowing through the module base-plate and being evacuated through the cooling plate (see sections 5.2 and 5.3).

⁴²⁵ **5.2 Plane layout**

The design will consist of equipping one plane with 2 rows and 6 columns with a total of 12 modules. The modules will be mounted on one side of a cooling plate and with an overlap of about 2 mm between adjacent modules in order to minimize the dead area of the chip periphery as represented on the CAD view (see figure 15). This will impose to have two module types mechanically distinct ⁴³⁰ but electrically identical. The only difference is the module base-plate geometry for which the lower module will have a height of 4 mm instead of 8 mm for the higher one and a special machining groove allowing the overlap. In addition, in the wire bond region at the chip periphery a mechanical protection cap (See Figure 13) will allow to have the service pigtails laid on top without any damage risk for the electrical integrity of the module. The mechanical gap between two module rows will ⁴³⁵ be $\sim 200 \mu\text{m}$ allowing some clearance for the integration of the neighboring modules.

The assembly precision requirements of the ASICs on a module and of the modules on the plane are not very stringent. Even if an accuracy 50 microns could be achieved for chip localisation on the plane, the metrology survey results of the modules and of the plane will not be a criteria for the production QC acceptance. The ASICs will have fiducial marks at two corners that will be used for ⁴⁴⁰ the metrology of each module after assembly. Once all the modules will be integrated on a plane the metrology of the module relative to the localisation points of the cooling plate will be done thanks to a combination of measurements between mechanical touch probes and optical measurements. The survey data will be used for the geometrical description for the software reconstruction which will be fine tuned with track alignment data.

⁴⁴⁵ The approximate dimensions and mass for a plane are listed in table 2. The dimension of the tungsten absorber plane will be $20 \times 20 \text{ cm}^2$ which is fully covering the opening of the FASER magnet diameter. The active area of the plane, which accounts for the overlap of the modules on the ASIC readout side, is $13.4 \times 17.5 \text{ cm}^2$. The mass of the modules corresponds to 2.3% of the total mass (3.6 kg) which is dominated by the tungsten absorber plate and of the aluminum support.

⁴⁵⁰ The cooling channel follows the longer direction of the module as can be seen in figure 16. The cooling plates will be made in aluminum alloy (AlSi10Mg) using a direct metal laser sintering

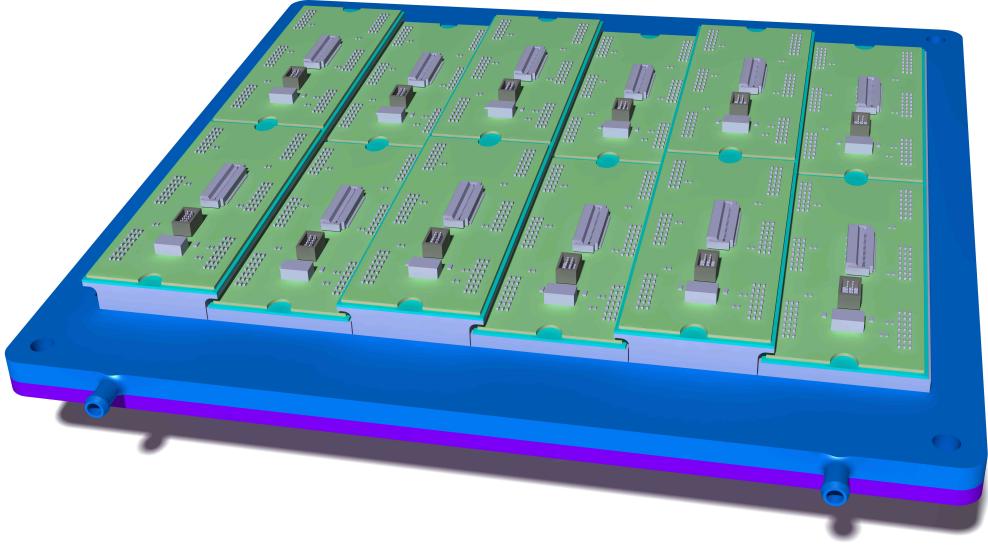


Figure 15: Preshower plane layout with 12 modules mounted on a cooling plate with an overlap along the longer side of the modules. The cooling plate size is $\sim 20 \times 20 \text{ cm}^2$ and 5 mm thick.

Table 2: List of parts in an instrumented plane with dimensions and mass. The module consists of all the parts described on Figure 13 except the base plate and the thermal interface sheet.

Item	Number	Section [cm ²]	Thickness [mm]	Weight [g]
Module	12	6.7×3.1	4	84
Lower mount base plate	6	6.7×3.1	4	120
Upper mount base plate	6	6.7×3.1	8	216
Aluminum cooling plate	1	20×20	5	500
Tungsten absorber plane	1	20×20	3.5	2700

(DMLS) method⁴ allowing to have the design features easily implemented and especially for the cooling channel and external interfaces. It has the advantage, after a heat post-treatment, of having an excellent isotropic thermal conductivity of $\sim 180 \text{ W/mK}$ and similar mechanical properties as
455 with a standard aluminum material. The plan is to machine the plates after being built allowing to achieve the necessary precision for the reference mounting holes and for the surface roughness. Each module will be mounted with 6 screws and fixed against the cooling plate with a thermal interface material called soft PGS (Pyrolytic Graphite Sheet) from Panasonic. This material has the advantage of being a dry contact with a much better conductivity than any thermal paste or grease
460 existing on the market provided that a relatively uniform and high compression force can be applied (above 50 N/cm²). The module integration allows a very modular mounting and dismounting assembly, which facilitates the reworking of a plane in case of necessity.

⁴The process of compacting and forming a solid mass of material by heat but without reaching the point of liquefaction.

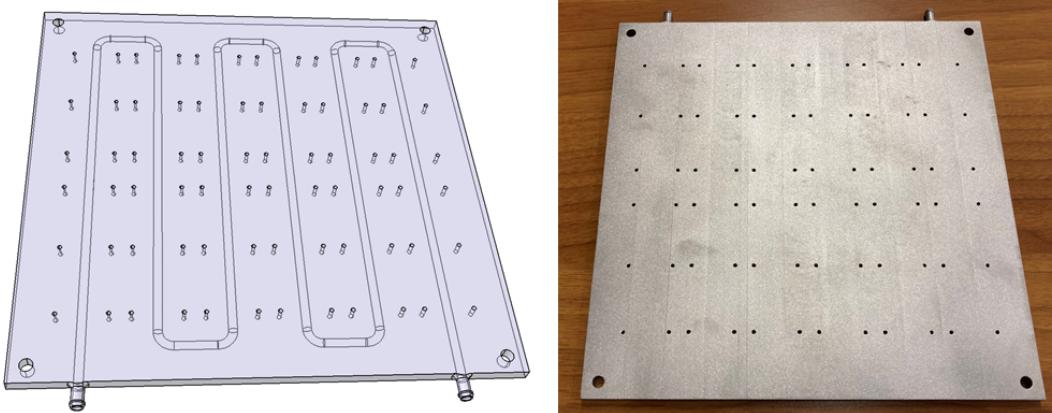


Figure 16: Left: 3D model of the cooling plane with cooling channels visible. Right: the first prototype of cooling plane, produced for the thermo-mechanical mock-up.

5.3 Thermal management

The system is designed to operate at room temperature. The non-negligible power density in a module will require a relatively good thermal path to the cooling channel to be able to maintain the temperature below $\sim 30^\circ\text{C}$ during operation. The fluid that will be used for the cooling channel will be water at a temperature of 15°C as for the FASER tracker stations.

In order to get experience with the module construction while assessing the thermal performance, it was decided to build a thermo-mechanical mock-up (Figure 17 left) with the layout close to the design described previously except that the modules are mounted on the two sides with a single type module base-plate of 4 mm thick. The module base plates were equipped with polyimide film with resistive metal traces embedded (thermo-foil from MINCO⁵) to simulate the heatload. In addition a thermal sensor, NTC (negative temperature coefficient), was glued on each module block. The measurement conditions were the following:

- Cooling fluid set point was controlled at 15°C and tested with flow rates from 0.7 to 2 L/min
- Ambient temperature of 21°C
- An injected power in the 12 modules mounted on the cooling plate of 48 W.

Figure 18 shows a set of measurements recording the temperature of 4 modules along the cooling line as well as the inlet and outlet water temperature. The measured excess temperature between the inlet and the exhaust of the cooling fluid for a flow rate of 2 L/min was 0.3°C which is indicating a heat transfer coefficient (HTC) of $\sim 15500 \text{ W/m}^2\text{K}$. Lower flow rate measurements were made and the HTC decreases almost linearly. An interesting observation is that even if the flow rate is decreased by a factor of 3 the module temperature is increasing by not more than 1°C . An interesting test condition was to simulate a cooling failure while all the modules are still powered. In this case, there is quite some time (~ 3 min) to take an interlock action and prevent the modules to exceed 30°C

⁵<https://www.minco.com/>

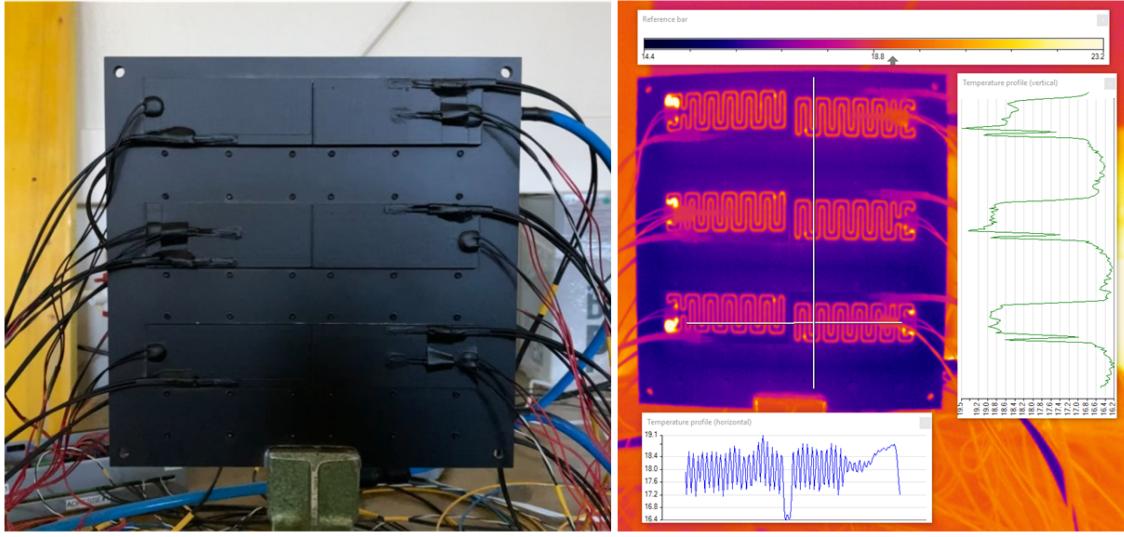


Figure 17: Left: thermo-mechanical prototype mock-up with six modules mounted on each side of the cooling plate. Right: IR image with 4 W injected power per module, showing a temperature increase of less than 3 °C.

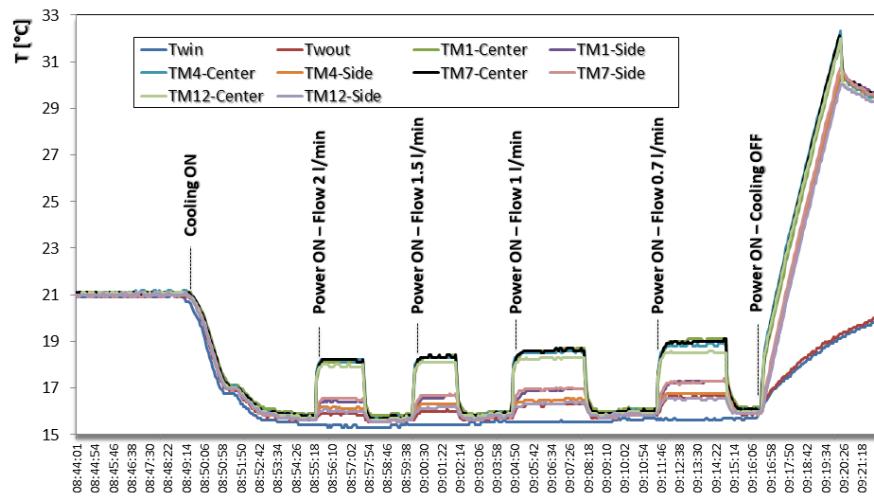


Figure 18: Results from a thermal mock-up test showing the temperature-variation measurement recorded with 10 NTCs. TM1, TM4, TM7, TM12 are the module temperatures as a function of the cooling line, while Twin and Twout are the inlet and outlet water temperatures.

Additionally thermal infrared (IR) images (see Figure 17) were taken with painted black surface in order to avoid a reflectivity and an emissivity variation of the observed objects. The IR images are showing very similar results to the NTC temperature measurements.

The results are re-assuring and could allow to configure the cooling distribution flow with some level of flexibility during the future installation. A recent FASER reconfiguration was made by reducing slightly the cooling flow in the tracker station loops without any visible impact in term of cooling performance while "faking" the preshower cooling loop in TI12. Such reduction allows a flow rate for the Preshower upgrade of 1.7 l/min. Based on this, the system will allow putting all the 6 preshower planes cooling flow in series with an expected temperature increase between the 1st and the last plane of a maximum of 4°C. Such an increase should have a negligible impact on the noise and pixel response uniformity.

%

6 Preshower layout

500 The preshower station will be located at the downstream part of FASER. One of the geometrical requirements is to fit the preshower detector within the available space between the last tracker plane and the calorimeter, for which the longitudinal gap is 280 mm (see figure 19), while keeping at least 1 scintillating detector in this region for triggering.

505 The physics of FASER requires the detector is situated on the ATLAS collision-axis line-of-sight (LoS), and this requirement plays an important role in the overall detector design. The beam crossing-angle in IP1 can move the actual LoS in TI12 by around 7.5cm from the nominal position. In Run 3 the crossing angle is expected to move the LoS vertically down or up (with the direction changing during Run 3, but only during a year end technical stop). On the longer term the crossing angle will change to horizontal, which will push the LoS towards the TI12 tunnel wall. The main 510 FASER detector has been designed to be able to (mostly) follow changes in the crossing angle as much as possible. The supports for the magnets, which also support the tracker, can be raised and lowered to (mostly) follow vertical changes in the crossing-angle. The full detector is installed on an upper baseplate which can be pushed sideways by several cm to follow as much as possible a horizontal change in the crossing angle.

515 The mechanical frame of the current scintillator station will be removed to clear the interfaces for the new preshower station, while the upper frame holding the calorimeter will stay in place. The supporting stand or frame for the preshower will use the existing aluminium profiles and the upper base-plate. The estimated predefined envelope including at least one trigger scintillating detector and the side electrical patch panels should fit within a volume of $280 \times 720 \times 460 \text{ mm}^3$ and takes into 520 account the clearance for integration of $\sim 10 \text{ mm}$ on both sides along the beam axis. The expected weight per plane is $\sim 3.6 \text{ kg}$ (see table 2) to which we should add $\sim 1.6 \text{ kg}$ for the mechanical support frame which will support each plane and the active patch panel in the preshower cradle (see Section 7 for active patch panel). The total weight is estimated to be between 35 and 40 kg including all the electrical services.

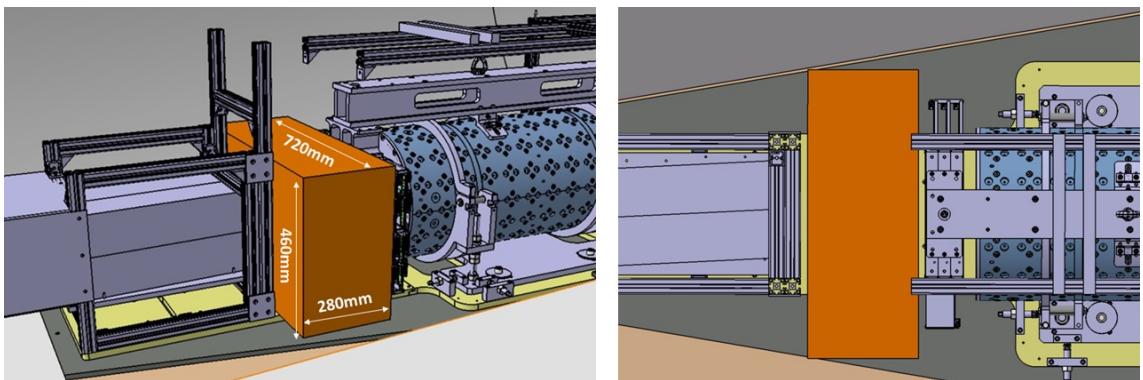


Figure 19: Left: Envelope of the preshower detector between the calorimeter and the last station of the tracker. Right: Top view of the preshower volume (orange) showing the last tracker station on the right hand-side.

525 Figure 20 shows the present situation in TI12 in the region of the FASER preshower scintillator station. Part of the cables from the Tracker station and from the calorimeter will be re-routed to

allow for the removal of some aluminum profiles (holding the scintillator station). The maximum envelope has been defined to accommodate the size of the bottom baseplate in aluminum along the transverse axis. The vertical axis is only driven by the LoS, defined at 253mm nominally above
530 the baseplate, so that the FASER Preshower has to be centered with respect to this LoS. Some further clearances are needed when moving FASER to accommodate with the ATLAS crossing angle modification (maximum lowering by -18 mm while the maximum upward movement is 66 mm up from the nominal LoS, and 60 mm maximum towards the trench wall). The mechanical design and service integration should take this constraint into account, meaning that the detector
535 will be able to move accordingly without interfering with neighboring parts. The latter constraint led to a decision to have the electrical services placed only on one side (away from the tunnel wall) for which the available space is larger and accessibility is much better. This will make the integration and cabling of the active patch panels much easier.



Figure 20: Left: Overview of the FASER detector as of today, with the calorimeter on the left side and the current preshower detector highlighted in green . Right: Side view of the current preshower detector with at the right hand side the last tracking station with the service cables connected.

The preshower layout and concept allows for modularity between the absorber plane made of
540 Tungsten and the instrumented plane with the readout modules. The design is to have 6 successive layers, each made of an absorber plane of one radiation length, followed by a readout module plane.

Figures 21 show projective and perspective views of the stackup of the proposed FASER preshower station with a superposition of the magnet opening.

Figure 22 shows a CAD view of the integrated preshower with plastic scintillators in front and
545 on the rear side. The latter two counters will allow to feed additional inputs to the trigger logic board (TLB) which will provide online the relevant trigger decision to the preshower backend readout (see section 7.4). The space along the beam axis between the different parts is relatively large and it is used for integration clearance but may allow to have some contingency (~ 40 mm) when making the detailed integration drawings. The data cables will make the interconnection between the active patch panels on the left hand side (looking from the front of FASER) and the GPIO cards located
550

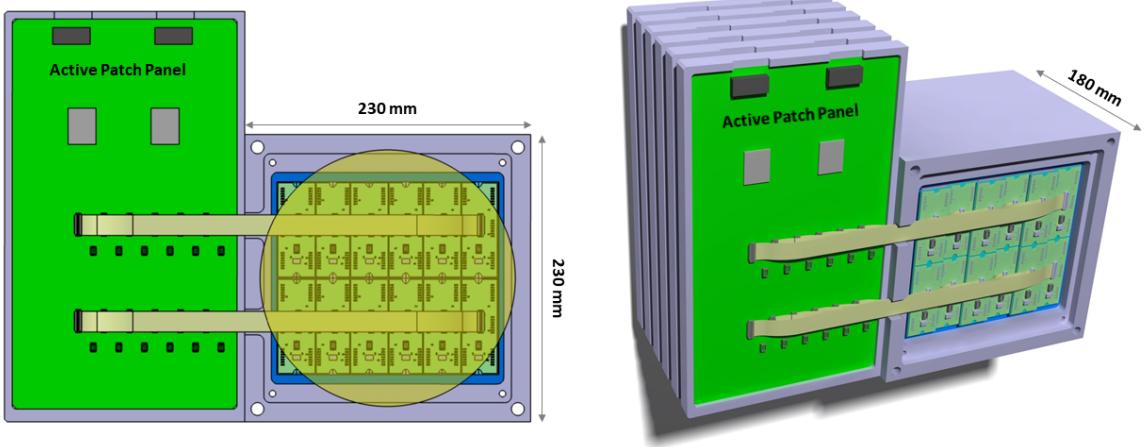


Figure 21: Left: Front projected CAD view of the preshower detector overlaid with the yellow shade of the magnet aperture. Right: Perspective view of the 6 preshower planes and with the configuration of one active patch panel per layer on one side.

in the crate on top of the preshower detector (see Figure 22).

The detector integration will be implemented in such a way that the access to some reference points will be possible to perform a survey with the laser system to be done by the CERN BE-GS group. The preshower station will have a system to tune its position with respect to the Tracker stations within a few hundred microns of precision. A crane put in place for the main FASER detector installation and situated directly above the FASER detector, can be used to ease the installation of the Preshower station.

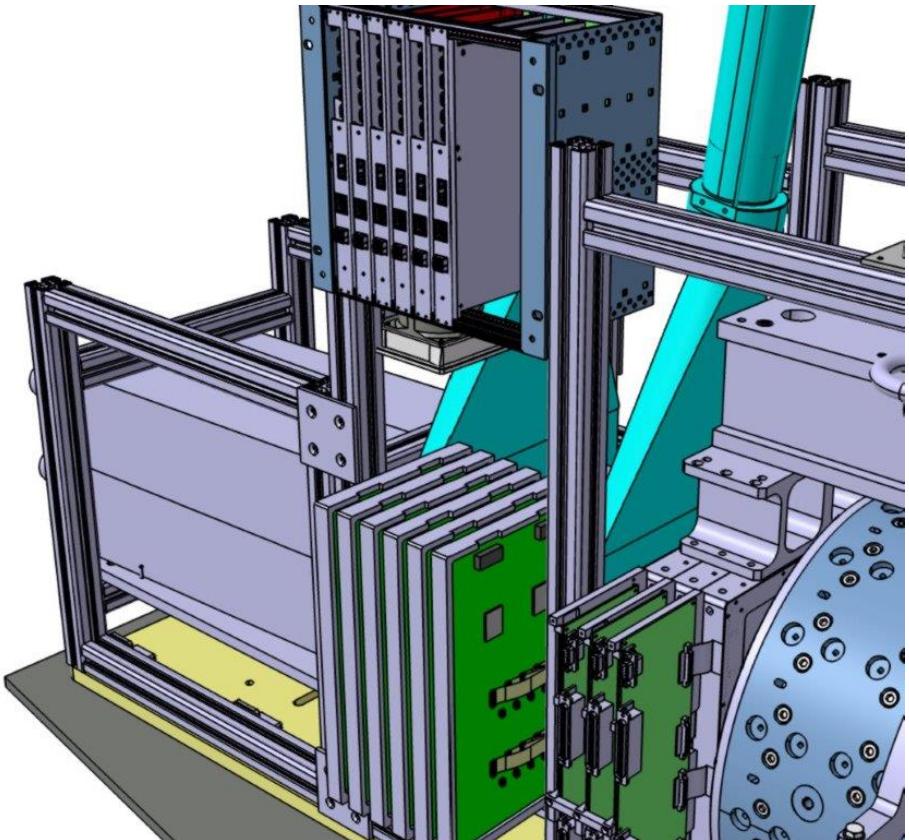


Figure 22: CAD view of the preshower Upgrade located right after the last tracker station. On each side plastic scintillators with light guide are represented allowing to give input to the trigger decision. On top are located the preshower readout boards with the GPIO.

7 Backend readout chain and TDAQ

The preshower readout chain will be composed of 2 levels of concentration boards. The 1st level of data concentration are the Active Patch Panels (APP), located close to the plane (2 per plane). The 560 2nd level used for the readout and the slow control are the three Preshower Readout Boards (PRBs), located at a few meters from the APP. A PRB will serve two planes of the preshower. This modular architecture is based on the module layout, the plane layout and the expected data rates.

7.1 Expected Data Rates

565 The average data rate for the new FASER preshower depends on the measurement of the (mostly muon) background events, while the largest signals are expected for photon-induced EM showers. With a deposited charge of 0.5 fC for a MIP and a nominal operating threshold of 1 fC, Geant4 simulations of the preshower show that the typical pixel multiplicity for muons on the monolithic detector ASIC is ~ 1 (setting a threshold slightly above the MIP charge largely suppresses high-
570 multiplicity events coming from muon-bremsstrahlung). The data pruning implemented on chip limits the event size for an event with a single pixel (or few pixels) firing to 3 kb, which corresponds to a time to send the data from the chip to the APP of 15 μ s at 200 Mbps single data rate. At the estimated muon background rate of 0.5 Hz/cm², the average data rate per plane (for an ASIC size of 1.5 \times 2.5 cm² and a plane of 12 \times 6 = 72 chips) is $3 \text{ kb} \times 1.5 \times 2.5 \times 0.5 \times 72 = 405 \text{ kbps}$, rounded to
575 450 kbps. The system is conservatively designed to sustain an increase in muon background rate of a factor ten, allowing a smooth operation at the High-Luminosity LHC running even at an ultimate instantaneous luminosity of $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$.

580 The largest events in terms of occupancy are observed on the last detector plane for showers generated by a $\mathcal{O}(1)$ TeV photon; these events are rare, but since these are the signal events, it is extremely important to be able to read them out with a high efficiency. With a discrimination threshold of 1 fC such an event can produce a maximum occupancy of 1700 pixels. If those pixels are distributed in adjacent columns, the expected event size is 17 kbit, which leads to a maximum readout time of 85 μ s for the largest event, a factor of 5.7 higher than the muon background. This value is within the specifications of the ASIC and the FASER readout.

585 If necessary, it is possible to significantly reduce the pixel occupancy on the last plane up to a factor 10 by increasing the discrimination threshold from 1 to 4 fC.

7.2 Active Patch Panel (APP)

590 The APP is a fully custom board to be designed. Each plane will be instrumented with two APPs, placed on the same side to avoid clashing with the tunnel wall (the two APPs may be logically distinct but placed on the same board, as shown in Figure 21). One APP is connected to six modules through the module flex pigtails. An embedded FPGA will merge the modules' data into a single stream to be sent to the 2nd level (PRB) through a several meters long (3 - 4 m) SAMTEC ECUE Firefly cable like those used on the existing FASER experiment between the tracker station patch panels and the Tracker Readout Boards (TRBs) [22].

595 A feasibility study of the APP functionality has been carried out to confirm the possibility of deserializing and pushing into 40 FIFOs a stream of 40 \times 200 Mbps data with an intel Cyclone 5 FPGA (Device 5CEBA7F23C8, maximum frequency of 225 MHz, 3270 ALMs, 5925 registers

and 720 kb of memory used after synthesis, *i.e.* 5.8% of ALMs and 9.3% of total memory). Thus, having 6 modules \times 6 chips = 36 data streams per APP for the experiment will easily fit into the chosen FPGA target.

The APP board will read the 36 FIFOs, concatenate, serialize and send the data to the PRB through the Firefly cable with a 1×100 Mbps link, which is sufficient to handle the 225 kbps half-plane average data throughput while maintaining an ample safety factor for HL-LHC operation (4.5 ms duration within two seconds of 0.5 Hz/cm^2 muon background rate, or maximum 25.7 ms for the largest signal event). A zero suppression mechanism will be also implemented to reduce the data throughput and data stored at the DAQ output. Finally, the APP also handles the slow control communication for the modules configuration and calibration from commands coming from the PRB through the same firefly cable.

The initial architecture is based upon two APP boards per plane but the two boards (ie one full plane) can be merged into a single hardware board if cost reduction and/or better mechanical integration are identified. In any case the location of the two boards or of a single one will be at one side of an instrumented plane (See Figure 21). This leads to either a configuration of 12 half-plane (1 FPGA per board) or 6 full-plane (2 FPGAs per board) APP boards for the preshower.

7.3 Preshower Readout Board (PRB)

The PRB is based on the same principle as the existing FASER TRB *i.e.* using the existing General Purpose Input and Output (GPIO) board from the University of Geneva [22] and a small custom adapter board to be designed for the APP interconnection with the Firefly cable. The PRB will be located in a minicrate above the preshower detector (see Figure 22). The PRB will first deserialize the data from two planes (4 APP boards or 4×100 Mbps data streams), then concatenate them into a single data stream and finally push it to the DAQ system through the GPIO 1 Gbps Ethernet link. Reading two planes leads to 4×225 kbps data read in parallel within 4.5 ms and pushed into 1×800 Mbps output data stream, *i.e.* 2.25 ms duration within two seconds of 0.5 Hz/cm^2 muon background rate, or punctually 12.8 ms for the largest event, assuming 80 % of the 1 Gbps Ethernet link usable bandwidth.

The PRB also handles the modules slow control communication from commands coming from the DAQ system through the same firefly cable connected to the APP.

The initial architecture is based on one PRB for four APPs leading to three PRBs in total for the experiment. Based on the previous calculations, the total bandwidth required on Ethernet corresponds to six planes of 450 kbps = 2.7 Mbps for the muon background, or punctually 15.4 Mbps for the largest but rare signal events.

7.4 Readout scheme

The FASER TDAQ system is described in [22]. The scintillators and calorimeter modules provide trigger signals to the Trigger Logic Board (TLB) via a digitizer board. The different trigger signals are combined to provide a trigger accept decision (L1A). The TLB then distributes the L1A with fixed latency to the different sub-detectors triggering the data readout, and the various data fragments are then combined into full FASER events by Event Building processes. In addition to the L1A, the TLB also transmits a 40.08 MHz clock (synchronous to the LHC clock) and a Bunch Counter Reset (BCR) signal generated on every LHC orbit signal.

In the case of the preshower, whenever a pixel records a signal above threshold its charge is
640 stored in the in-pixel analog memory, and an internal signal generated on the digital periphery after
a programmable delay triggers the readout of the entire chip. The readout delay will be set so that
the L1A sent from the TLB to the PRB / APP will arrive before the start of data transmission from
the chips. Upon reception of a L1A, the chip data is buffered and then serialized on the APP. A
645 BUSY signal is asserted to the TLB until the APP is ready for receiving new L1As. The data is
transferred to the PRB and then to the GPIO that will create an event fragment and transmit it to the
DAQ over Ethernet. The proposed system will naturally fit into the existing FASER DAQ scheme
with minimal modifications needed for the DAQ software, with only a new PRB receiver software
module needed.

8 Detector integration

650 8.1 Mechanics and cooling

The preshower detector as described in section 6 will consist of a single assembly of the 6 layers including the absorber and the sealed planes as well as the APPs on one side. Each of the readout planes will dissipate approximately 50 W which will require a water cooling flow to allow to maintain the required temperature. Each plane will have one inlet and one exhaust which will be connected to the main cooling system already used by the FASER tracker stations which was built by CERN EN-CV division. The cooling system is based on a commercial air-exchanger with a controlled temperature of the circulating fluid. Two chillers are running in parallel for redundancy while each of them has a cooling capacity of more than 2.2 kW for the fluid set at 15°C and with an ambient temperature at 25°C. The tracker stations are dissipating about 550 W meaning that the cooling capacity even after installing the preshower detector will be more than a factor of 2 above that needed. Another parameter that is essential to take into consideration is the cooling flow that is limited to 12 L/min which is now currently used by the tracker stations. Adding the new preshower detector will require reducing the flow rate in the tracking station. The original setting of the flow was defined not according to cooling performance and the heat transfer coefficient (HTC) in the fluid but was instead maximized for the distribution. According to past experience the HTC should not be severely impacted if the flow will decrease from 3 to 2 L/min per tracking station. A test was performed with the IFT tracking station when it was under commissioning in EHN1 surface building at CERN and it showed that when reducing the cooling flow rate from 3 to 2 L/min the impact on the module temperature when normally powering and operating the modules is minimal and of the order of an increase of 0.4°C. Finally and as discussed earlier, since there is no stringent requirement on the chip temperature or even on the temperature dispersion across the modules, it is conceivable to limit the consumption to 1 to 2 L/min for the entire preshower detector by having a serial flow in each consecutive module plane. Thanks to the recent flow reduction applied to the tracker stations while mimicking the future preshower consumption of 1.7 l/min and based upon the results of the measurements shown in Section 5, we are confident that the cooling system will operate optimally with enough flow capacity.

In order to maintain the environment of the detector volume above the dew point, a dry air flush will be manifolded and connected to each of the module plane. The dry and compressed air is one of the services that is already available in TI12 and used for the tracker station in order to maintain the relative humidity as low as possible.

680 8.2 Service and powering

The expected power requirements per preshower module is listed in Table 3. With 72 modules in the final system and four different power lines per module, it is not feasible to provide separate power connections for each individual channel from a small commercial power supply system. Instead power channels will be merged on the Power Supply (PS) side and then split on the patch panel using DC/DC converters and low-dropout regulators (LDO) to supply the nominal voltages while using a significantly higher supply voltage to reduce the voltage drop in the 15 m low-power cables (see below). At the same time, the granularity needs to be sufficiently fine to robustly handle failures and keep currents manageable. The baseline scheme is illustrated in Figure 23. Each half-plane

690 has four 12 V input lines and a single 200 V HV input line. The HV is used by all six modules on a half-plane⁶, while pairs of modules get their three required low voltages from a single LV line through a DC/DC converter and six LDOs. A 400 mV drop-out voltage is assumed as well as 85% efficiency in the DC/DC converter. The fourth LV line is used to power electronics on the patch panel.

695 The proposed powering granularity is well-matched with the Wiener MPOD system [23] currently used in FASER. An MPOD LV module provides two 4-channel outputs, thus six modules are required, while two 8-channel ISEG HV modules can supply the required bias voltage. This can be hosted in a single 10-slot MPOD crate. The full system requirement including spares are listed in Table 4. No dedicated spare is foreseen for the MPOD crate as it is the same crate as
700 used by the FASER tracker/scintillator system and thus can share the same spare crate. The LV and HV modules cannot be shared as different voltages/polarities are used than for the FASER tracker system. Using the MPOD system for powering will make integration into the existing Detector Control System (DCS) rather simple as it will function largely in the same way as for the tracker. Both the MPOD LV modules and the ISEG HV modules support interlock signals to be provided
705 by the Preshower Interlock and Monitoring (PIM, described in the next section).

In addition to the preshower modules, the GPIO-based readout system and the PIM will need to be supplied with 24 V. As these do not have strong requirements on monitoring or voltage, simple 220 V to 24 V power supplies in a custom case will likely be used rather than adding a dedicated MPOD LV module. The proposed solution is the same as is done in the current FASER detector to
710 power the TIMs and tracker patch panels. The PIM power supply will be powered by UPS-backed power in order ensure continuous monitoring also in the case of a power cut.

Table 3: Expected module power requirements

Type	Nominal voltage [V]	Maximum current [A]
Analog	1.2	1.0
Digital	1.2	1.0
Driver	0.9	1.0
Bias	200	10×10^{-6}

Table 4: Proposed power supply system

Type	Number needed (spares)
Wiener MPOD LV/HV crate	1 (0)
Wiener MPV8016I	6 (1)
ISEG EHS8405	2 (1)

As described in Section 3, the preferred location of the power supply system is at the top of the TI12 tunnel next to the existing power supplies and readout in order to minimize the radiation exposure. Unfortunately the two existing racks cannot accommodate an extra MPOD crate. Instead

⁶To ease testing and handling of broken modules, the splitting of the HV might be done off the patch-panel, which would also allow increasing the granularity in the future if needed.

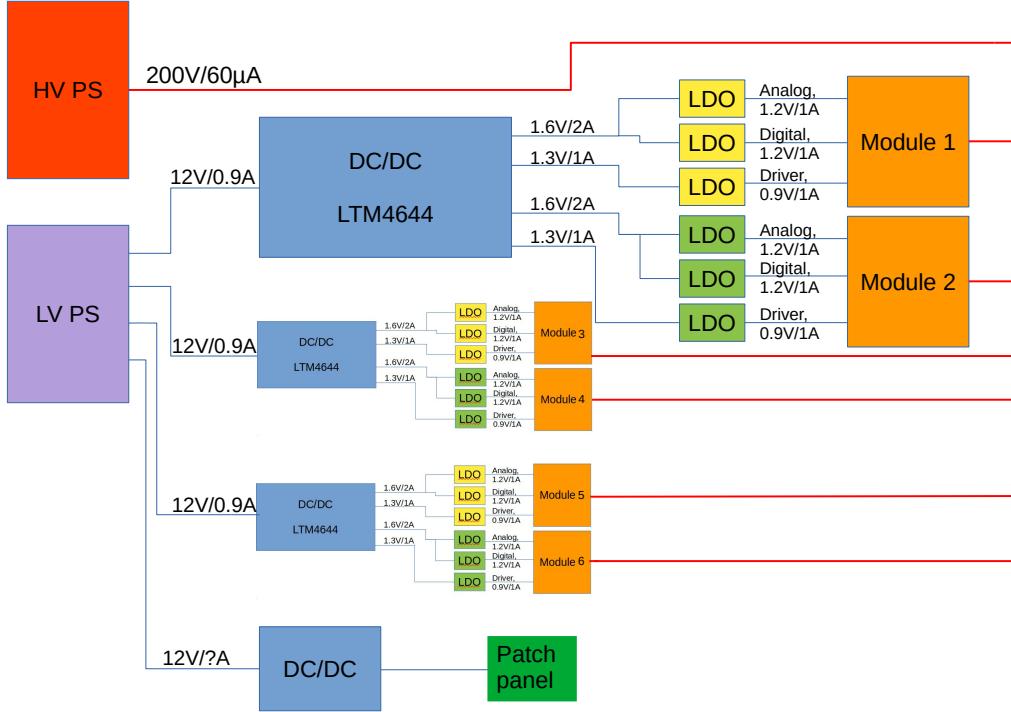


Figure 23: Proposed powering scheme for one half-plane.

the preferred solution is to install a small rack in front of the existing rack or a custom support of the side of the rack, see Figure 24. With a total power consumption of about 600 W including overhead in the MPOD system, the powering can easily be accommodated by the existing 230V distribution system. An existing FASER network-controlled PDU (Power Distribution Unit) can be used to provide remote power-cycling capability. The power is delivered from the MPOD crate to the preshower patch panels by twelve 15m long LV cables and twelve HV cables of the same type as used for the FASER tracker and scintillator, respectively, which were manufactured in the EP-DT cable shop to fulfill CERN’s firesafety rules. The cables (including spares) will be installed in the existing cable tray. With a current of about 1 A per LV channel, a 1 V voltage drop is expected.

8.3 Slow control and interlock

The aim of the safety system of the FASER preshower is to protect the modules from damage under all circumstances. The preshower follows the standard approach of a multi-level protections system consisting of high-level software-based monitoring (DCS) and a low-level hardware-based interlock system. The software system is capable of triggering automatic actions that can turn off individual detector components in a controlled way while the hardware interlock system turns off power supplies immediately and acts therefore as the last level of safety.

The PIM module is the core of the interlock system of the FASER Preshower, and is based on the existing FASER Tracker Interlock Module (TIM). Two PIM boards will be installed in the tunnel. The PIM module is designed to provide a hardware interlock on one side based upon module

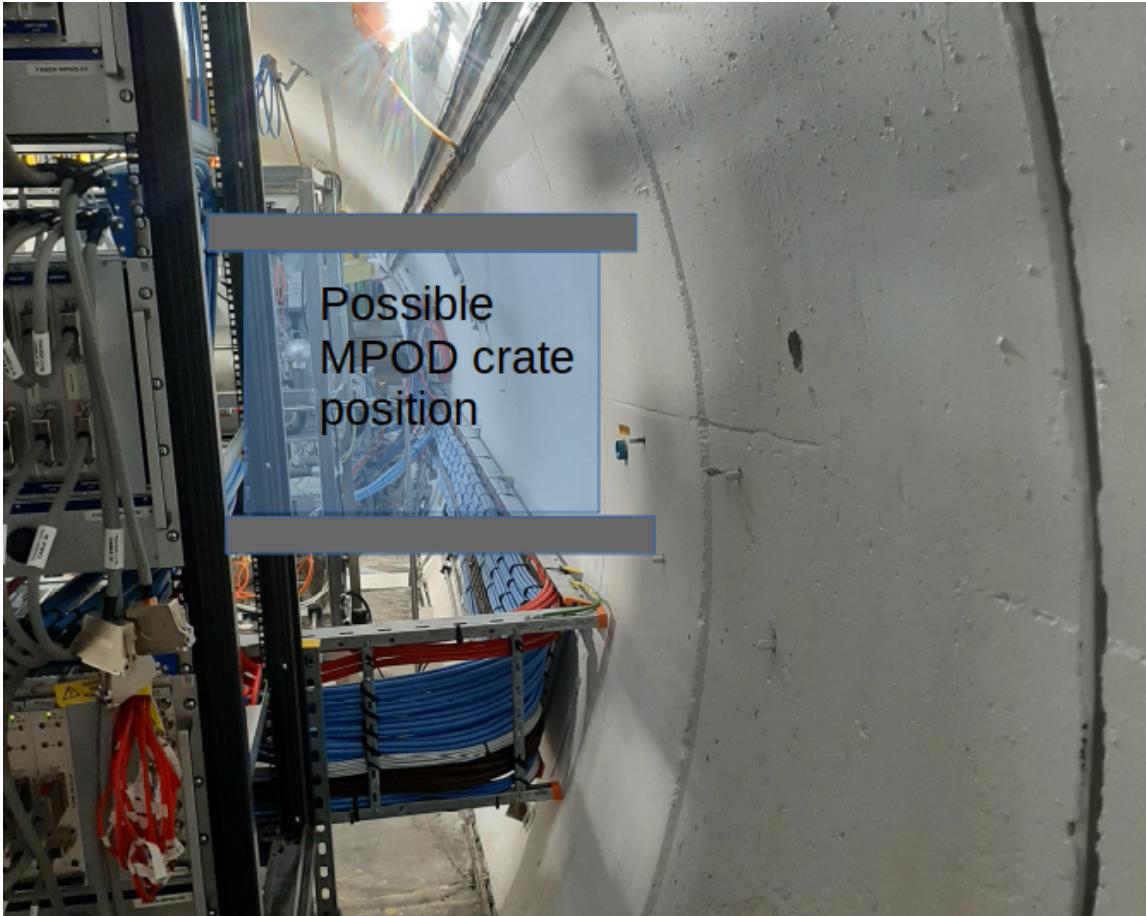


Figure 24: Possible location of preshower MPOD crate.

temperature to interlock all the supply lines and on the other side a new feature (with respect to
 735 what was implemented for the tracking stations) will be implemented to interlock a corresponding
 HV supply line in the case of a LV channel would be down. The PIM will also monitor the LV
 module supply lines, the temperature and humidity information from the Preshower and send all the
 information to the DCS for further processing. The main inputs of the PIM module are the NTC
 sensors and the LV supply monitoring . There are 36 NTCs for the modules and 6 NTCs for the
 740 frame as the input of one PIM board.

Each preshower layer is equipped with 12 modules, with 1 NTC-10k thermistor attached to a
 module. This makes 12 NTC thermistors per layer and 36 NTCs in total for 3 layers (managed by
 one PIM board). In order to measure the temperature at the inlet and outlet of the cooling loop
 per layer, two additional NTC-10k thermistors per layer are attached directly on the frame (6 NTCs
 745 in total for 3 layers / 1 PIM). Furthermore, each layer may have one or two HIH-4000 humidity
 sensors. Temperature and humidity information collected by all these sensors will be read out by
 the Micro-computer on the PIM and then sent to DCS for further processing.

The hardware interlock uses the NTCs on the modules as input. The hardware interlock is an
 extra protection, which should not be triggered in the ideal case. In the case of high temperature, the

- 750 comparator-based interlock circuit turns off both the HV and the LV power supplies simultaneously for a layer. For each preshower layer, 2 (out of 12) NTCs are chosen as the input to a hardware interlock circuit. There are three circuits in one PIM board controlling the three layers separately, so the power supply can be turned on and off layer by layer while for the HV there are 2×6 HV interlock outputs that are sent to two HV cards (each card has 8 channels while 2 will be unused).
- 755 For the LV interlock 2×3 outputs are sent to 6 APPs through DB25 connectors. The interlock signal outputs are also sent to the Micro-computer on the PIM at the same time, so that the status can be checked from the server-side.

8.4 Network

Both the DAQ and DCS readout can easily be accommodated in the existing FASER network infrastructure. The DAQ will require three additional 1 Gb/s Ethernet connections and the DCS 760 three additional 1 Gb/s Ethernet connections (two PIMs and one MPOD crate). This number of additional network ports is available in the existing 24-port DAQ and DCS switches, both of which have less than 16 ports currently occupied. At an expected DAQ data rate of 2.7 Mb/s at peak luminosity there is no bandwidth limitation in the 10 Gb/s uplink and the existing DAQ/DCS servers 765 should be able to accommodate the additional readout/monitoring processes. During calibrations bandwidth usage will be much higher than during physics data taking and the 1 Gb/s connections from the PRB to the main switch could potentially limit the time needed for calibration, whereas the existing 10 Gb/s uplink should not be.

9 Software reconstruction and calibrations

770 9.1 Detector simulation

Currently, the simulation is based on a simplified but reliable detector description realized in Geant4, and the di-photon signals are generated through the “particle gun” functionality in Geant4, as described in Section 2.2. With this setup, the simulation time is approximately 1 second per event, when focusing on pairs of photons with energy of 1 TeV each. The simulation time quoted 775 here is only indicative, as it depends strongly on the characteristics of the simulated event, and it has a large margin of improvement. While the preshower simulation is currently a standalone software, it will soon be integrated in the full FASER simulation. In parallel, as an integration to the preshower simulation and to support the photon reconstruction development, a detailed description of the detector is being implemented in the Allpix² simulation framework [24]. The 780 new tool will integrate the generation of the signal inside the silicon pixel detector and the electronic contribution to the measurement of the charge in pixel, comprising readout resolution, saturation and pixel-to-pixel mismatch. The calibration curves are being implemented from realistic Monte Carlo simulations using the same software adopted for the design of the detector ASIC (Cadence Virtuoso [25]).

785 9.2 Photon reconstruction

Reconstructing photons in the 100 GeV to few TeV energy range, while disentangling signatures from di-photon events at a few hundreds μm separation, poses a significant challenge. In order to characterize the performance of the proposed detector design, a first photon reconstruction algorithm 790 has been developed, which might be the base for the more advanced offline reconstruction software to be integrated into the official FASER software framework. The EM shower produced by photons converting in the preshower provides a clear signature. Its reconstruction exploits the main features of the deposited charge distribution across the Silicon pixels of the different planes: the presence 795 of a sharp peak corresponding to the center of the EM shower, usually contained in a 1-2 $100 \mu\text{m}$ pitch pixel, with tails which ranges on average from a few percent to 15-20% of the peak. The reconstruction algorithm follows a two-step approach: first, all local maxima in the pixel charge 800 distribution are found, with a minimum charge threshold a function of the preshower layer. The local maximal positions are then matched across layers, to reconstruct the direction of the incoming photons. This simple approach provides a first estimate of the photon position, and allows to quote the discrimination power for di-photon events compared to single-photon background. The reconstruction algorithm is tested with the simulated detector output and, as mentioned in Section 2 805 the efficiency of resolving di-photon events ranges from 65% to 90%, with fake rates between 2% and 4%, depending on the photons energy and separation. The time required for the photon reconstruction is currently similar to the time required for the detector simulation, so the complete chain requires a few seconds for each event. This time has the possibility of being substantially improved with software optimizations.

Finally, the preshower reconstruction will be integrated with the one from the calorimeter to measure the photon energy. A study based on Geant4 simulation and testbeam data will be carried out to assess the combined performance of the preshower and calorimeter.

9.3 Detector calibrations

810 Due to the rarity of the expected signal events, a periodic calibration of the preshower is required to guarantee the functionality and performance of the system. During the preshower-calibration run (performed at the same time as the calibration of the tracking stations) the detector will not be able to take data, therefore a dedicated design effort was put in to minimizing the calibration time. The proposed solution is to perform a complete scan on the calibration parameters (threshold and injected charge) and do the analysis of the calibration data offline. This solution allows avoiding possible bottlenecks generated by any software operation during calibration. Moreover, using a dedicated command sequences with a "rolling mask" procedure, it will be possible to further reduce the calibration time by minimizing the number of configuration commands to be sent to the ASICs.

815 The calibration procedure is divided in three phases:

- 820 1. Threshold scan.
2. Noise occupancy.
3. Charge calibration.

Threshold scan

825 The first step of the calibration procedure is the threshold scan. It is used to set the thresholds at the average input equivalent charge of 1 fC. Since there are only 8 global thresholds on the chip and no pixel-to-pixel calibration, a spread in threshold of 20% is accepted among different pixels. The scan will be done for 128 threshold values, producing 50 charge injections per step. The pixels are pulsed in groups of 16, 4 pixels per row; to avoid re-configuring the entire matrix at each change of the pixel group, a rolling mask will be used (Figure 25).

830 **Noise occupancy**

The noise occupancy measurement is used to verify that the detector is noise free at the selected threshold. It requires setting the global thresholds identified with the previous calibration step and starting a readout for a duration long enough to estimate an appropriate upper limit for the noise rate. Considering a coincidence readout window of 100 ns, to target a noise occupancy per chip 835 below 10^{-7} (events), the noise hit rate per chip should be less than one hit per second.

Charge calibration

The charge calibration is used to generate the calibration data for all the pixels with different charge injections. The calibration follows the same method used for the threshold scan. The ASIC is set at the reference threshold and then it is pulsed with 16 different charge values.

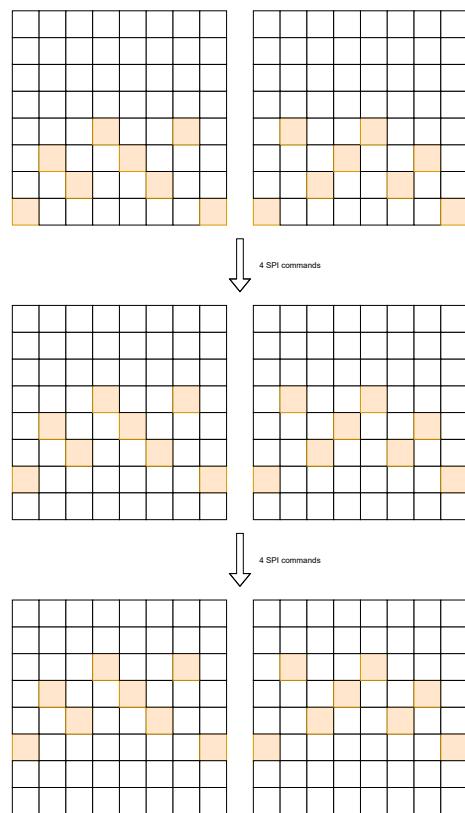


Figure 25: Unmasked pixel distribution for rolling mask and examples of rolling mask shift.

840 10 Project organisation, resources, costs and schedule

For the design and construction phase, the FASER high resolution preshower upgrade project has been organized in the following work packages:

- 845
1. Monolithic detector readout chip
 2. Module and on-detector services
 3. Mechanics and integration
 4. Readout system
 5. Detector control and interlock systems
 6. Off-detector services and power supply system
 7. Commissioning

850 Each work package has a coordinator and sufficient expert manpower for its execution. The financial and manpower resources available for the development and construction of the FASER high resolution preshower upgrade are summarized in Table 5, which also contains the breakdown of the contributions by the participating Institutes. In terms of services, power supplies, DCS and mechanics, the upgraded preshower system is very similar to the existing tracker system. Five
855 FASER institutes that already contributed to the FASER tracker construction are participating in the preshower upgrade. This assures existing FASER expertise on these items and maximises the confidence on a successful execution of the preshower project. The main effort of the collaboration will thus be on the remaining items, which are the ASIC, the module and the patch panel, each requiring design, prototyping and qualification. For these items the project relies on the expertise
860 of the University of Geneva and KIT groups in the production of SiGe BiCMOS monolithic pixel ASICs and on that of the Japanese groups on the production of the ATLAS pixel modules.

Table 5: List of Institutes participating in the preshower upgrade and their contributions.

Institute	Contribution			Project items	
	Financial [kCHF]	Manpower [FTE/year]			
		Scientist/ Engineer	Doctoral student		
CERN		0.8	1	ASIC design, services and PS, commissioning	
University of Geneva	924	5.1	4	ASIC design, modules, on-detector services, mechanics and integration, readout, simulations, commissioning	
Japan (KEK, Kyushu University)	55	0.5		Module, on-detector services, PS, DCS, commissioning	
Karlsruhe Institute of Technology			0.3	ASIC design	
Mainz University	42	0.9		Mechanics and integration	
Tsinghua University	30	1.5	1	Monitoring and interlock, PS, commissioning	
Total	1'051	8.8	6.3		

865 A detailed breakdown of the project cost is reported in Table 7. The most expensive item is the production of the pre-production (V1) and production (V2) ASICs (655 kCHF). The total cost of 905 kCHF includes the thermo-mechanical demonstrator, the prototypes based on the pre-production ASIC, spares and consumables. For the main cost driver (the ASIC production) the cost is well

known. For many other smaller items the cost estimate is based on those used to purchase similar items for FASER in the last 1-2 years. The difference of 146 kCHF between the available funding of Table 5 and the estimated costs of Table 7 provides large enough funding contingency.

The overall project schedule is summarized in the chart of Figure 26. The schedule is mainly
870 driven by the following milestones:

- June 2021: Submission of the pre-production ASIC
- June 2022: Submission of the final ASIC
- June 2022: Project status and schedule update
- December 2022: In-depth internal review
- 875 • June 2023: Project status and schedule update
- December 2023: Installation of the high-precision preshower

The pre-production ASIC was submitted for production in June 2021 according to schedule and will be used to build the first prototype module with almost the final size in Q2 2022. Due to a problem in the delivery of the epitaxial wafers to the foundry, the foundry had to delay the
880 delivery of the pre-production ASIC to March 2022. As a consequence, the schedule was recently re-baselined. To take into account the reduced time available for the testing and qualification of the pre-production ASIC before the submission of the production ASIC (second milestone), the Geneva team has anticipated to Q4 2021 the preparation of the test boards and readout system for the V1 ASIC as well as the design of the production ASIC. In September 2022 a testbeam period
885 is scheduled at CERN SPS north experimental area for the validation of the detector and readout design. The test will be carried out using V1 modules and it will include the calorimeter (using a spare calorimeter module). The testbeam data will be used to optimize the reconstruction algorithms and to evaluate the combined performance of the preshower and calorimeter in measuring the photon energy. In Q3 2023 the preshower detector will be integrated on surface and commissioned in the
890 FASER lab in EHN1 at CERN. Based on the experience with the installation of the FASER detector, we expect that the installation and the metrology survey in the detector experimental area TI12 will take less than a week. If needed more time (up to about three weeks) should be available for this.

A contingency of three months is foreseen after the surface commissioning period. In case of unexpected delays that would go beyond this contingency, the modular structure of the preshower
895 will allow for a partial installation of the detector during the technical stop of December 2023, while the remaining planes will be installed in a later access, with a possibility during the technical stop of December 2024 if LHC Run3 is extended.

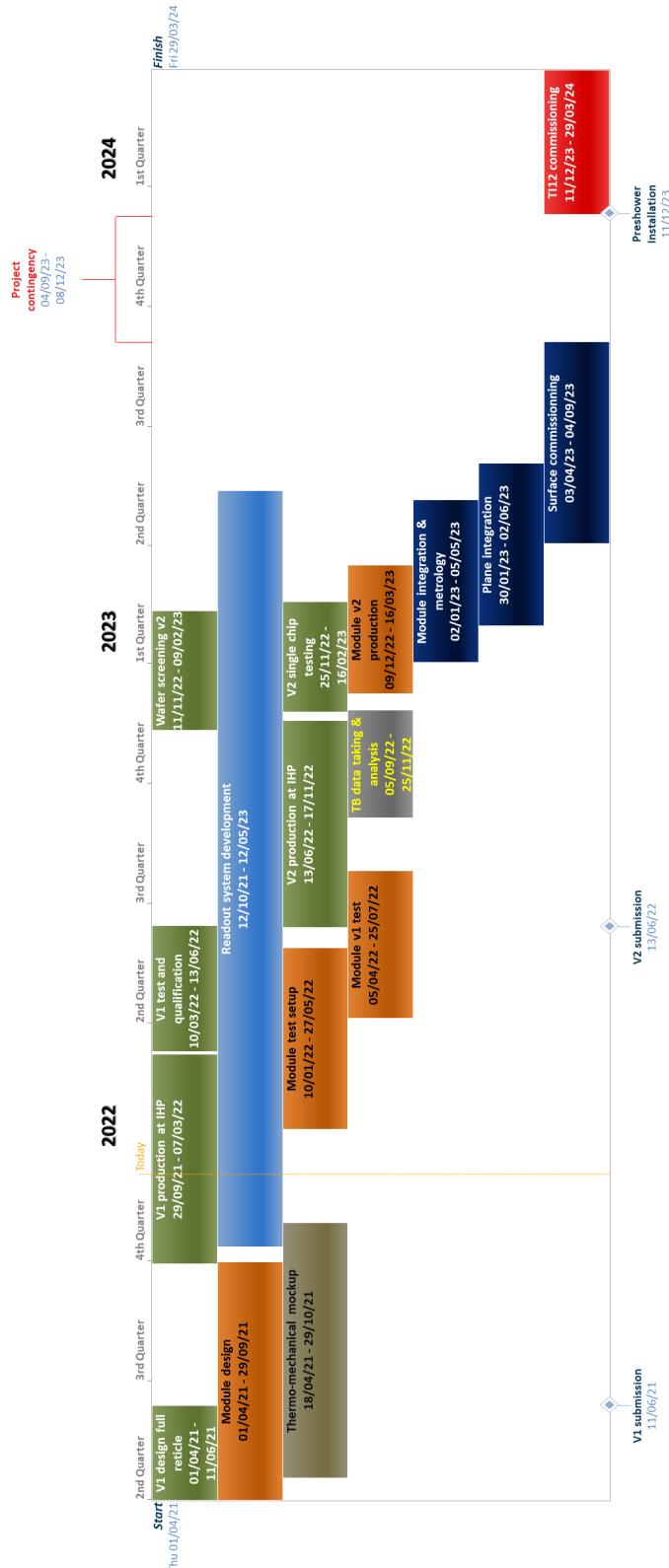


Figure 26: Schedule of the FASER Preshower construction and installation

Table 6: Breakdown of the cost of the preshower project including spares

Category	Item	Thermo-mechanical demonstrator			V1 ASIC module prototype			Production		
		Units	Price/unit [CHF]	Total [CHF]	Unit	Price/unit [CHF]	Total [CHF]	Unit	Price/unit [CHF]	Total [CHF]
ASICs	V1 submission				1	267,000	267,000	1	267,000	267,000
	Final submission							14	6,500	91,000
	Additional wafers				6	1,000	6,000	20	1,000	20,000
	Laser wafer dicing				20	100	2,000	20	100	2,000
	Single chip test board									4,000
Electronics	Active Patch panel	1	700	700	15	700	10,500	15	700	11,200
	Readout board	2	550	1,100	8	550	4,400	8	550	5,500
	Readout board adapter	2	400	800	8	400	3,200	8	400	4,000
	Pigtails	20	300	6,000	80	200	16,000	80	200	22,000
	Module flex	20	100	2,000	500	10,000	50,000	450	36,000	48,000
Mechanics	Base plates	20	150	3,000	20	150	3,000	80	150	12,000
	Cooling plates	1	2,000	2,000	2	2,000	4,000	7	2,000	14,000
	Tungsten plates							6	1,500	9,000
	Aluminum frames							6	2,000	12,000
	Support frame							1	2,000	2,000
Power supplies and cables	HV (8-channel)	1	5,000	5,000	2	5,000	10,000	2	5,000	15,000
	LV (8-channel)	1	3,000	3,000	6	3,000	18,000	6	3,000	21,000
	PS crate (MPOD)							1	7,500	7,500
	Rack							1	2,000	2,000
	LV cables	2	200	400	14	200	2,800	14	200	3,200
DCS & interlock	HV cables	2	200	400	14	200	2,800	14	200	3,200
	Firefly data cables	6	70	420	36	70	2,520	36	70	2,520
	PIM board	1	2,000	2,000	2	2,000	4,000	2	2,000	4,000
	Test equipment									6,000
	Lab power supply	1	5,000	5,000					5,000	
Consumables	Adapter boards	1	3,000	3,000					3,000	
	Glue, wire bonding, thermal interfaces, storage boxes	1	2,000	2,000	1	4,000	4,000	1	24,000	24,000
	Total	4,250	9,000	110	295,170	323,820	423	328,520	572,720	905,540

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A Appendix 1 - Table of project risks

Table 7: Table of risks with probability, impact and possible mitigation actions

WP	Risk description	Probability	Impact Type	Impact	Mitigations
1	Qualification of chip v1 longer than scheduled and delay in the design of the final chip	< 20%	Schedule	up to 3 months	Being sure that all the test equipment are ready and that sufficient personal is allocated for such test. In addition to that, three complete version of the final chip will be designed before even starting the tests of v1, each version corresponding to one of the configurations implemented in the v1 submission. The outcome of the tests will determine which configuration will be updated and submitted as v2.
	Final chip fabrication delay	< 20%	Schedule	up to 3 months	Relationship with IHP is very good and should help trying to mitigate whatever is possible on the production side.
2	Final chip not working as specified	< 5%	Schedule, cost	9 months + 267 kCHF extra cost	The likelihood is low since the v1 is supposed to catch-up features and issues. Minor new features should be added to the final chip design.
	Unexpected delay for the production the module flex	< 10%	Schedule	1 month	The prototype flex will be produced with the same technology than the final flex and the company should be the same unless issues are identified
3	Unexpecterd delay delivery of the SMD component	< 20%	Schedule	up to 6 months	The ordering of components for the module flex and for the APP will be made as soon as possible and if either the design robust and signed off or/and validated with the evaluation prototypes.
	In-house machining or metrology system is out of order for module production.	< 10%	Schedule	1- 2 months	The way out would be to out-source the work which will impact and plus in the schedule there is some slack in between the successsing tasks that could also mitigate.
4	Tungsten procurement plane and machining delay longer than expected	< 10%	Schedule	2 months	It is possible to order ahead of schedule the Tungsten material as soon as the integration design is final and signed off.
	In-house specialized man-power unavailability to complete metrology or integration	< 20%	Schedule	< 2 months	If metrology is required and the programmed is made in advance by the expert it is possible to find a replacement. Alternative is to outsource the task which may lead to more impact.
	Delay in production of the APP PCB	< 10%	Schedule	< 2 months	Unavailability of PCB is not entirely excluded.
	Unexpecterd delay delivery of the SMD components and of the FPGAs	90 % of parts < 20% 10% of parts < 60%	Schedule	4 - 6 months	The schedule already take into account some unusual delay for the component delivery. However further unexpected delay may be mitigated by ordering them much earlier that needed and when the design is under way.
	Validation and commissioning of the APP	<30 %	Schedule	< 3 months	FPGAs for the APP will be ordered soon. Features or bug in the programmation of the FPGA may lead to unexpected delay. The specification will be reviewed and the team of people to work on the testing will have to be strengthen with an optimal communication with the electronic engineer.