Translinear Circuits

4.1 Objectives

In this lab, you will learn about *translinear* circuits. In 1975, Barrie Gilbert coined the word *translinear* to describe a class of circuits, which he had invented in the late 1960s, whose large-signal behavior hinges on the extraordinarily precise exponential current-voltage characteristic of the bipolar transistor and the intimate thermal contact and close matching of monolithically integrated devices. The word *translinear* derives from a contraction of the phrase "*trans*conductance is *linear* in the (collector) current," which is a direct consequence of an exponential current-voltage relationship. Translinear circuits are capable of performing a wide range of useful nonlinear signal-processing functions, such as multiplication, division, squaring, square-rooting, vector magniute, and vector nomalization.

4.2 Prelab

The following prelab questions have been constructed to help you prepare to do the lab efficiently. Please complete these questions *before* you come to lab. While you may discuss the prelab questions with your lab partner or with other students in the class, each student in a lab group should complete the prelab assignment individually, so that you each understand the circuit(s) that you will be testing and what you will be doing in the lab.

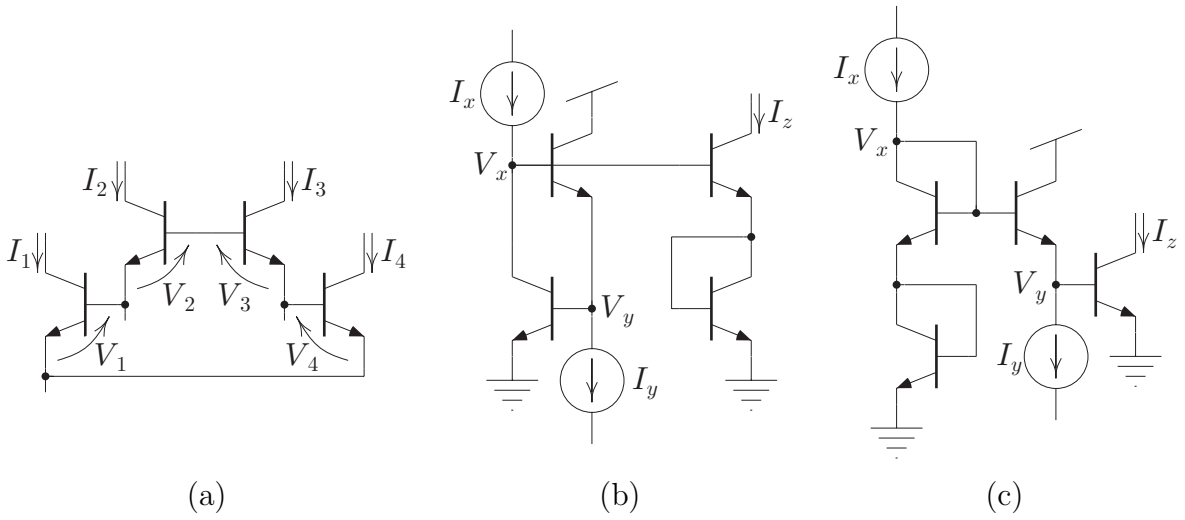
1. **Second-Order Translinear Loop**. Consider the circuit shown in Fig. 4.1a comprising four *npn* bipolar transistors whose base-emitter junctions form a closed loop. In answering this question, you should assume that all four transistors are matched (i.e., they have the same values of I_s and β) and are operating at the same temperature (i.e., the value of U_T is the same for each). You should also assume that the devices are all operating in the forward-active mode and that the Early effect is negligible.

   (a) What relationship holds between the ith base-emitter voltage, V_i, and the ith collector current, I_i?

   (b) What relationship holds among the four base-emitter voltages?

   (c) What relationship holds among the four collector currents?

2. **Translinear Circuit 1**. Consider the circuit shown in Fig. 4.1b, which incorporates the abstract loop of bipolar transistors from Fig. 4.1a, biased in such a way that it accepts two input currents, I_x and I_y, and generates an output current, I_z. In answering this question, you should again assume that the transistors are matched and operating at the same temperature. You should assume that the Early effect is negligible, that all



(a) (b) (c)

Figure 4.1: Translinear circuits comprising (a) a closed loop of four matched *npn* bipolar transistors. Parts (b) and (c) show the abstract translinear loop of part (a) properly biased so they accept two input currents, I_x and I_y, and produce and output current, I_z. Note that all currents must be positive in the directions indicated and that the transistors are assumed to remain in their forward-active regions.

base currents are negligibly small (i.e., β is infinite), and that the output voltage is held high enough that the output transistor is guaranteed to operate in the forward-active mode.

(a) Assuming that the input currents are both positive in the directions indicated, will all of the transistors operate in their forward-active modes? Explain your reasoning.

(b) What is the relationship between the output current, I_z, and the input currents, I_x and I_y?

(c) What approximate values will the input voltages, V_x and V_y, take on for typical values of the input currents? For each input voltage, which input current(s) does it depend on?

3. **Translinear Circuit 2**. Now, consider the circuit shown in Fig. 4.1c, which also incorporates the abstract loop of bipolar transistors from Fig. 4.1a, biased in such a way that it accepts two input currents, I_x and I_y, and generates an output current, I_z. You should answer this question under the same assumptions as you did the previous one.

(a) Assuming that the input currents are both positive in the directions indicated, will all of the transistors operate in their forward-active modes? Explain your reasoning.

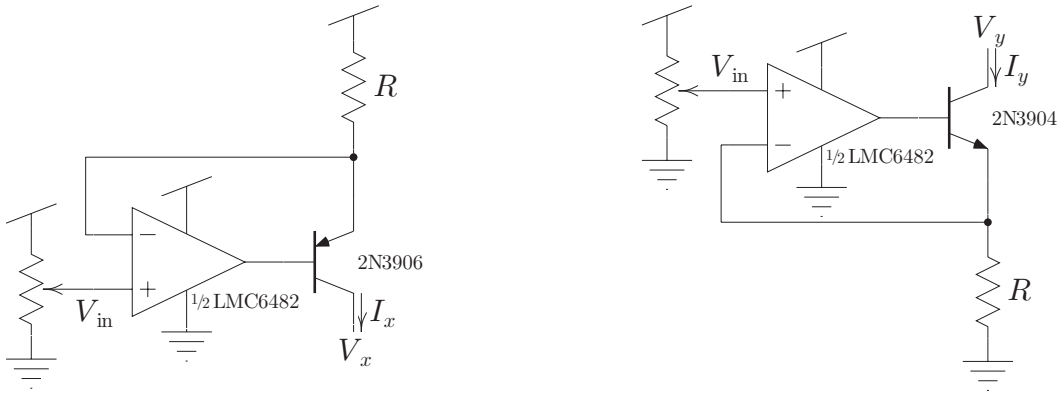


Figure 4.2: Adjustable current (a) source and (b) sink comprising a trim pot, an operational amplifier, a resistor, and a bipolar transistor.

(b) What is the relationship between the output current, I_z, and the input currents, I_x and I_y?

(c) What approximate values will the input voltages, V_x and V_y, take on for typical values of the input currents? For each input voltage, which input current(s) does it depend on?

4. **Current Source/Sink**. Next, consider the circuits shown in Fig. 4.2, each of which comprises a trim pot, an operational amplifier, a resistor, and a bipolar transistor. The circuit of Fig. 4.2a is a current *source* (i.e., it produces a positive current flowing from the positive power supply rail, V_{dd}), while the circuit of Fig. 4.2b is a current *sink* (i.e., it produces a negative current flowing to ground).

(a) For each circuit, what determines the output current?

(b) For each circuit, what constraints exist on the output voltage in order to ensure that the circuit acts as a current source?

4.3 Experiments

You will be doing three experiments in this lab. In the first experiment, you will be examine the current-voltage characteristics of four *npn* bipolar transistors to see how closely their characteristics match one another. In the second and third experiments, you will examine the current transfer characteristics of two simple translinear circuits made from four matched *npn* bipolar transistors.

For this lab, you will be using *npn* bipolar transistors from an MAT14 quad transistor array whose pinout is shown in Fig. 4.3a. Please note that all four of the transistors are in a common substrate, which is tied both to pin 4 and pin 11 of the package. The datasheet

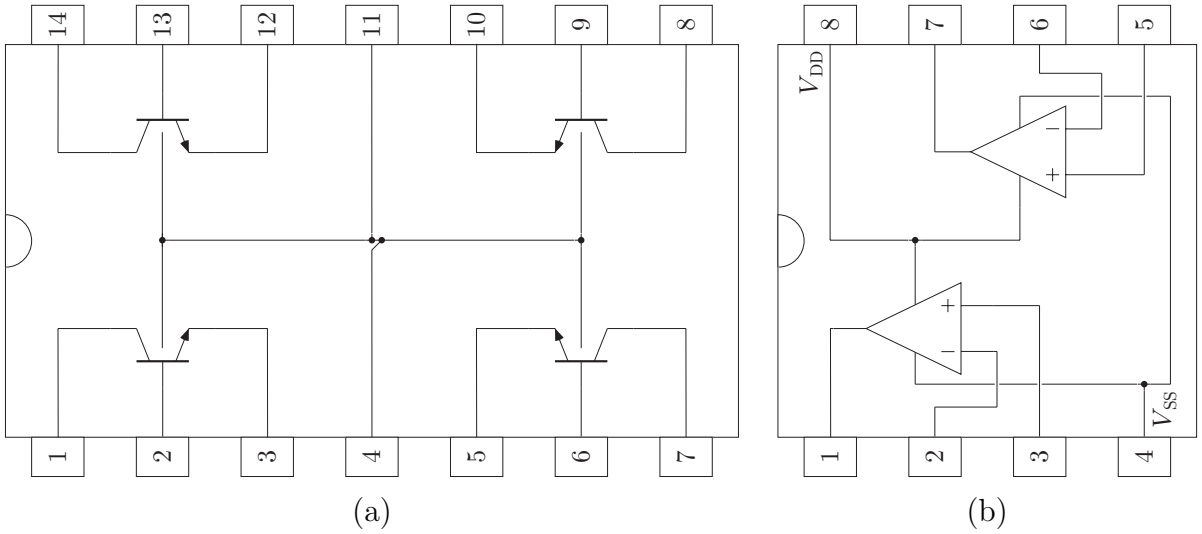


Figure 4.3: Pinouts of (a) the MAT14 quad *npn* bipolar transistor array and (b) the LMC6482 dual rail-to-rail CMOS operational amplifier.

recommends that both of these pins be tied to the negative supply rail (i.e., ground) to minimize the coupling between devices. For the second and third experiments, you will also need a second current source input, which you will be constructing as shown in Fig. 4.2 from an LMC6482 dual CMOS rail-to-rail operational amplifier, whose pinout is provided in Fig. 4.3c. Please note that the LMC6482 is a CMOS part and is sensitive to ESD, so please handle them carefully.

In your lab report, you should include graphs of all theoretical and experimental curves. In general, you should plot the measurements in a point style so the individual points are distinguishable. Any theoretical fits to the data should be plotted on the same graph as the experimental data in a line style.

4.3.1 Experiment 1: Bipolar Transistor Matching

Obtain an MAT14 quad *npn* bipolar transistor array. For each of the four transistors, measure the base current and the emitter current as you sweep the base voltage with the collector tied to the +5 V power supply. From the measured emitter and base currents, compute the collector current. For each transistor, extract a value for the collector saturation current, I_s, and forward current gain, β from appropriate theoretical fits. In your report, include a table showing these extracted parameters. For your report, make a single semilog plot showing all four collector currents and all four base currents as a function of the base voltage. Also, include a plot showing the percentage difference between each transistor's collector current and the mean value of all four collector currents as a function of base voltage. Finally, include a single semilog plot showing β as a function of base current for all four transistors. How well do the transistors match each other? Do you notice any systematic matching trends?

4.3.2 Experiment 2: Translinear Circuit 1

Construct the circuit of Fig. 4.1b from the four *npn* bipolar transistors on your MAT14. You should tie the output voltage to the +5 V power supply rail and measure the output current at the emitter of the bottom transistor in the stack in the output branch of the circuit. You will also need to construct an adjustable current source and current sink, as shown in Fig. 4.2, to supply the second input required by the circuit. Measure the output current, I_z, as a function of the first input current, I_x, for at least three values of the second input current, I_y, spanning at least two decades. Your sweep values should span a large dynamic range (e.g., 10 nA to 10 mA) and should be equally spaced on a log scale. In your report, include a single log-log plot showing I_z as a function of I_x for all three values of I_y along with appropriate theoretical fits.

Next, measure I_z as a function of I_y for at least three values of I_x spanning at least two decades. In your report, include a single log-log plot showing I_z as a function of I_y for all three values of I_x along with appropriate theoretical fits. Does the circuit behave as you expect from your prelab analysis?

4.3.3 Experiment 3: Translinear Circuit 2

Construct the circuit of Fig. 4.1c from the four *npn* bipolar transistors on your MAT14. Repeat everything that you did in the second experiment on this circuit. Does this circuit behave as you expect from your prelab analysis?

4.4 Postlab

Consider the translinear circuit shown in Fig. 4.4, which has been augmented with operational amplifiers and resistors to perform voltage-to-current conversion at the inputs and current-to-voltage conversion at the output. In order to function properly, all of the bipolar transistors in the circuit should operate in the forward-active mode. In answering the first question, you should assume that all of the transistors are matched and operate at the same temperature. You should also assume that the Early effect is negligible. Finally, you should assume that the operational amplifiers are ideal and are operating from a dual power supply, so that their inputs and outputs can go both above and below ground.

1. (a) For this circuit, are there any restrictions on the input voltages, V_x and V_y, to ensure proper circuit operation? If so, what are they and what happens if the input voltages go outside of this range. If not, explain why not.

   (b) What relationship holds between each input voltage and its respective input current? What relationship holds between the output current, I_z, and the output voltage, V_z?

   (c) What relationship holds among I_z, I_{z1}, and I_{z2}?

   (d) What relationship holds among I_z, I_{z1}, and I_x?

   (e) What relationship holds among I_z, I_{z2}, and I_y?

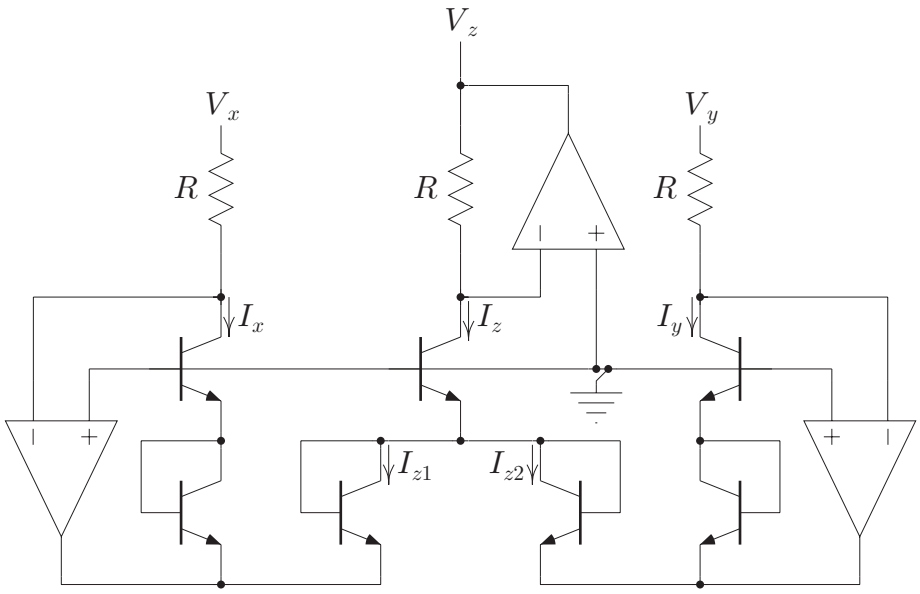


Figure 4.4: A translinear circuit with operational amplifiers and resistors to convert input voltages, V_x and V_y, into input currents, I_x and I_y, and output current, I_z, to output voltage, V_z. Note that the operational amplifiers shown in this circuit are run from a dual power supply, so that their inputs and outputs can go both above and below ground.

(f) Express the output current, I_z, as a function of the two input currents, I_x and I_y.

(g) Express the output voltage, V_z, as a function of the two input voltages, V_x and V_y.

2. Perform a DC simulation of the circuit shown in Fig. 4.4 using LTspice, sweeping V_x over an appropriate range for at least five values of V_y. Make sinlge a plot showing your simulation results along with the theoretical expression that you derived. Does the circuit behave as you expected?