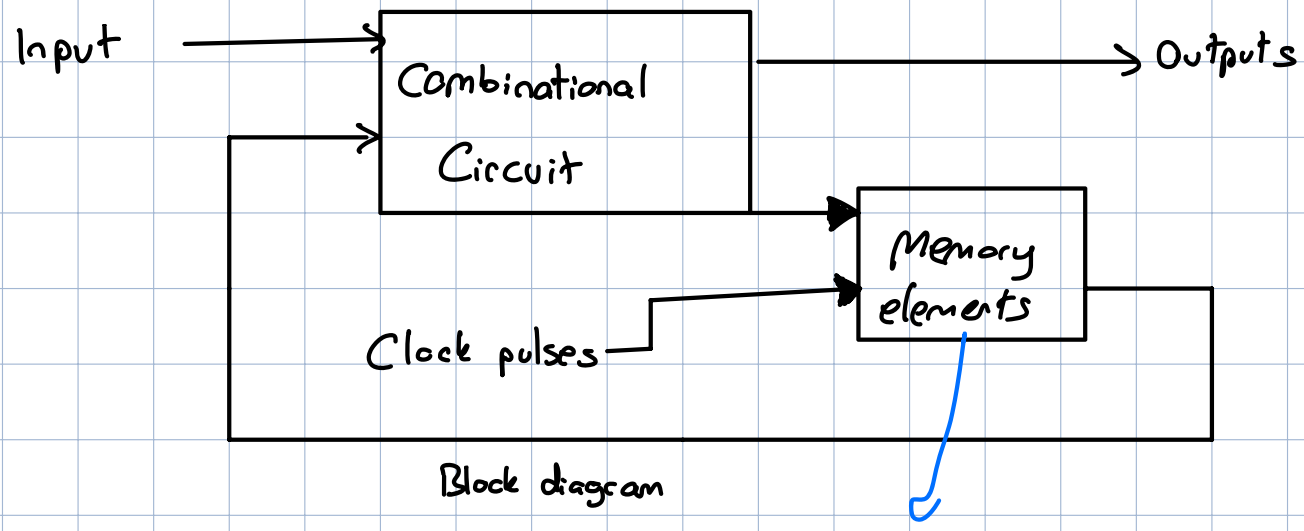
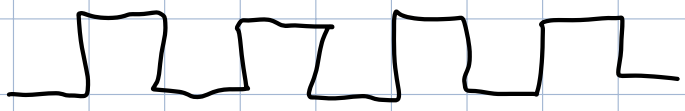


Block diagram

Binary resi saklar 1 yada 0
Saat vurusu ile calisir.
Flip-Flop = Hafiza
iki durumlu da denir.



Timing diagram of clock pulses

Latch (mandallar)
Flip-Flop (iki durumlular)

Latchler (mandallar) Level sensitive devrelerdir.

Saat vurusunun pozitif kisminda tetiklenicler.

a) Response to positive level

Flip-floplar Edge Sensetive

Positive edge

Bubble'siz Clk girisi

yada

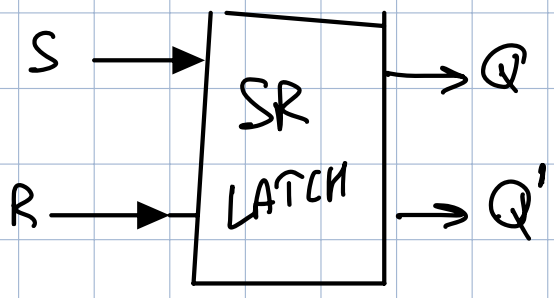
Bubbleli Clk girişi

Negative edge response

LATCHES

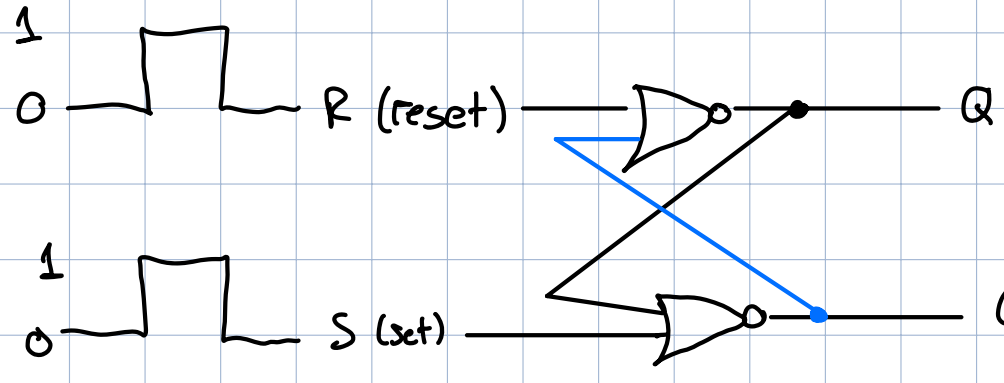
S - set

R - reset



Q ve Q' birbirinin tümleyeni olmalıdır.

NOR ile



Durum 1

S	R	Q	Q'
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
~~1~~	~~1~~	~~0~~	~~0~~

D2

D3

D4

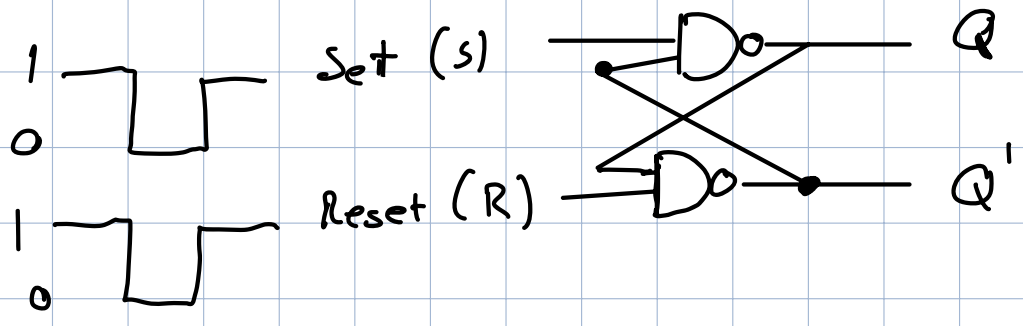
S = 1 olursa Q = 1

R = 0 " Q' = 1

Girişta (Q = 1 , Q' = 0) => Latch Set konumunda

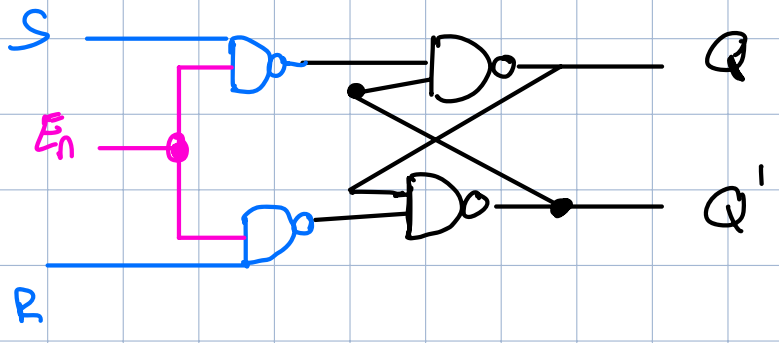
(Q = 0, Q' = 1) => Reset konumunda

NAND ile SR Latch



S	R	Q	Q'
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	~~1~~	~~1~~

Enable ucu eklemek sistemi yönetilebilir.



Set durumu : $E_n=1$, $S=1$, $R=0$

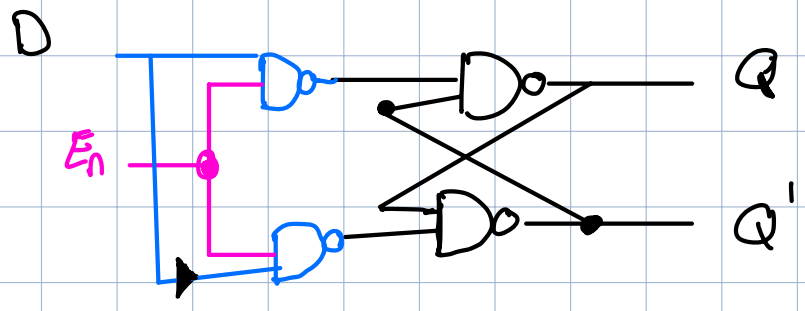
Reset durumu : $E_n=1$, $S=0$, $R=1$ ile

Set 1'den 0'a dönerse Latch durumu korur.

3 giriş 1 olursa belirsiz duruma girer

D-Latch durumu önlemek için üretilmiş.

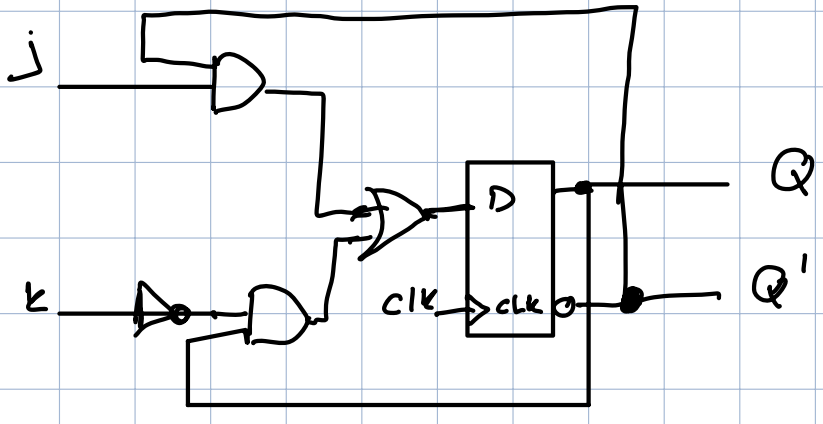
D-Latch

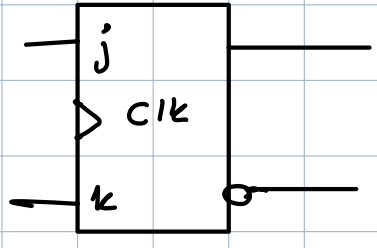


E=1 then D=Q

En	D	Next state of Q
0	x	No change
1	0	Q=0 reset state
1	1	Q=1; set value

JK Flip Flop





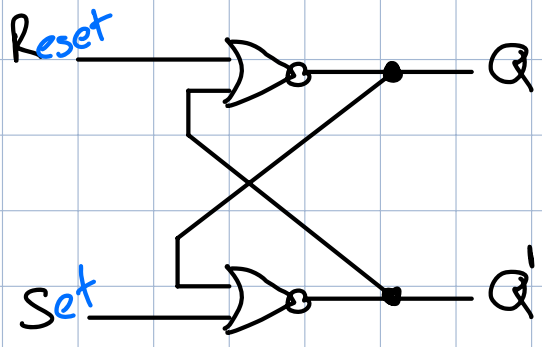
$D = JQ' + K'Q$

j	k	Q(t+1)
0	0	Q(t+1) No change
0	1	0 Reset
1	0	1 Set
1	1	Q'(t) complement

Uygar Video

SR Latch

NOR

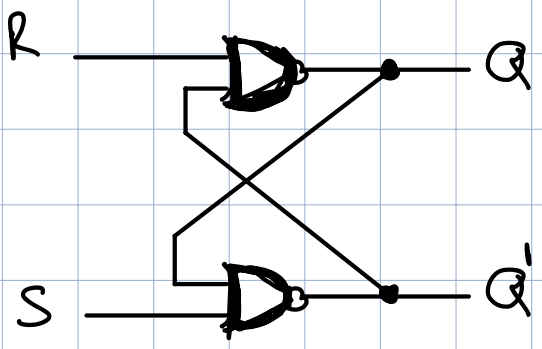


S	R	Q	Q'
0	0	Q	Q'
0	1	0	1
1	0	1	0
1	1	—	

Next state Table

SR	OUT
00	No change
01	Q = 0
10	Q = 1
11	invalid

NAND

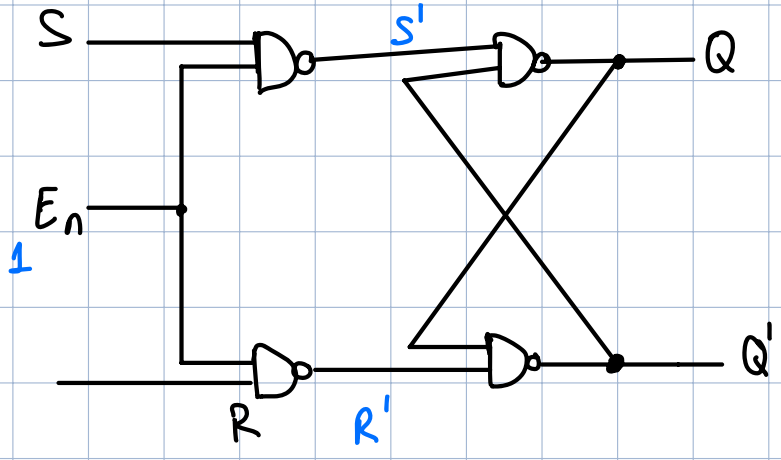


S	R	Q	Q'
1	1	1	1
1	0	1	0
0	1	0	1
0	0	—	

Next state table

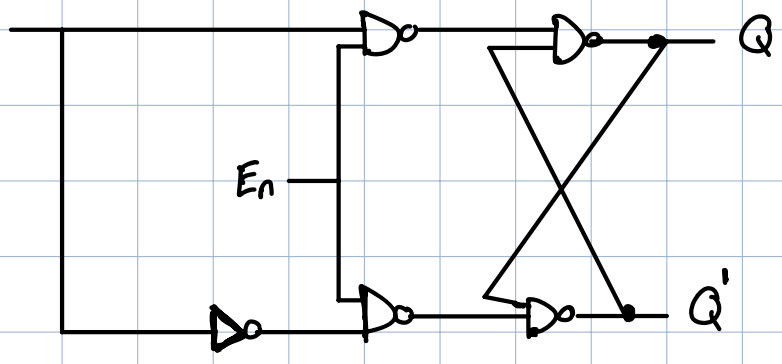
SR	OUT
11	No change
10	Q = 0
01	Q = 1
00	invalid

SR Latch with Enable

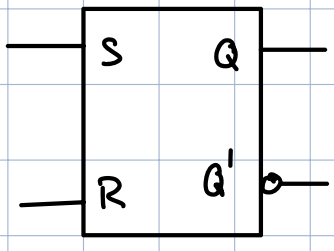


E_n	S	R	Next State of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0
1	1	0	Q = 1
1	1	1	invalid

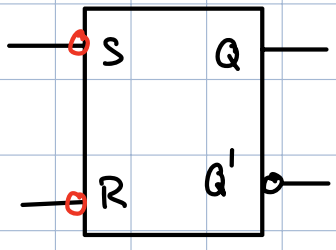
D Latch



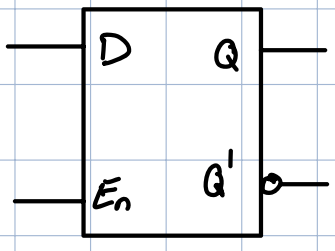
En	D	
0	X	No change
1	0	Q=0
1	1	Q=1



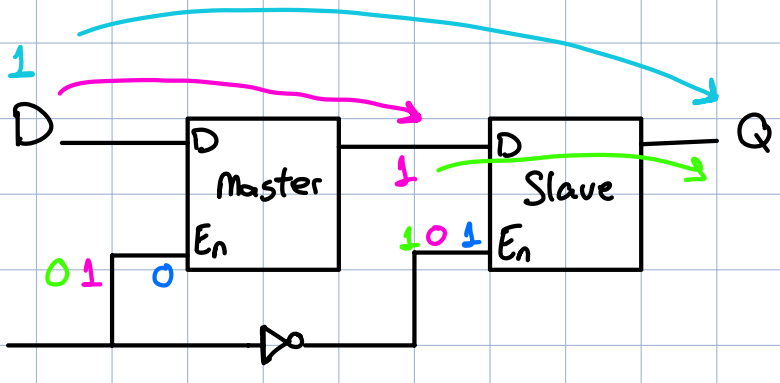
SR Latch
with NOR

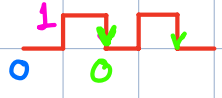


SR Latch
with NAND

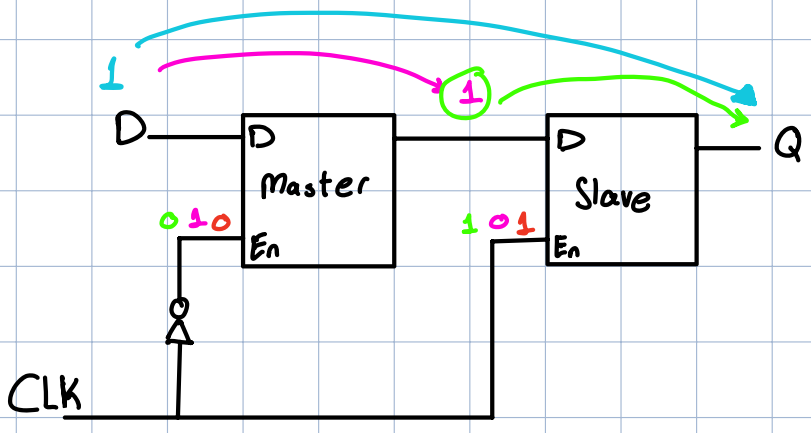


D Latch

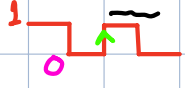




Bu devre CLK'nın negatif olduğu yerlerde giriş değerini çıkışa aktarıyor

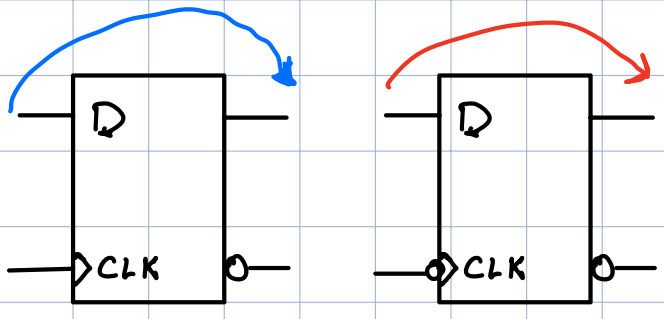


"POSEDGE CLK"



En son tekrar 0 olduğu için D'deki değişiklikler outputa aktarılmayacak. 2. defa ise 1 olduğundan aktarım yapacak

---

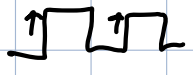


D-Flip Flop

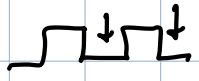
D	Q(t+1)	
0	0	Reset
1	1	Set

Positive edge D-FF

Negative edge D-FF

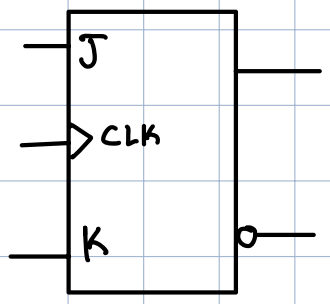


Pozitif kısımlarda çıkışa aktarır



Negatif kısımda aktarır

JK Flip-Flop

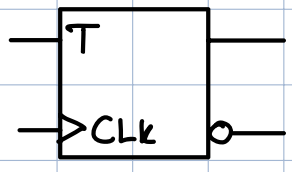


J	K	Q(t+1)
0	0	Q(t) No change
0	1	Q = 0 (Reset)
1	0	Q = 1 (Set)
1	1	Q'(t) (Complement)

$$Q(t+1) = J.Q'(t) + K'.Q(t)$$

$$Q(t+1) = JQ' + K'Q$$

T Flip-Flop



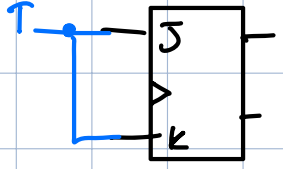
T	Q(t+1)
0	Q(t)
1	Q'(t)

$$Q(t+1) = T \oplus Q(t)$$

Örnek: a) JK-FF kullanarak T-FF yap
b) D-FF ile yap

?

a)

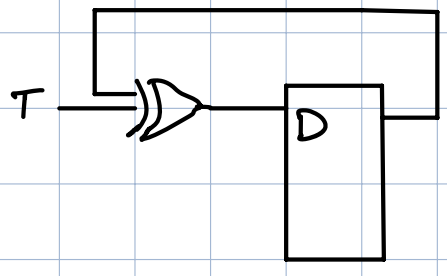


J	K	Q(t+1)
0	0	Q(t)
1	1	Q'(t)

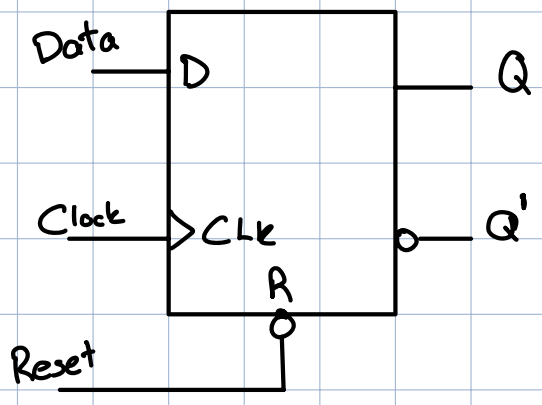
T	Q(t+1)
0	Q(t)
1	Q'(t)

b)

$$Q(t+1) = T \oplus Q(t)$$



D Flip-Flop with Asynchronous Reset



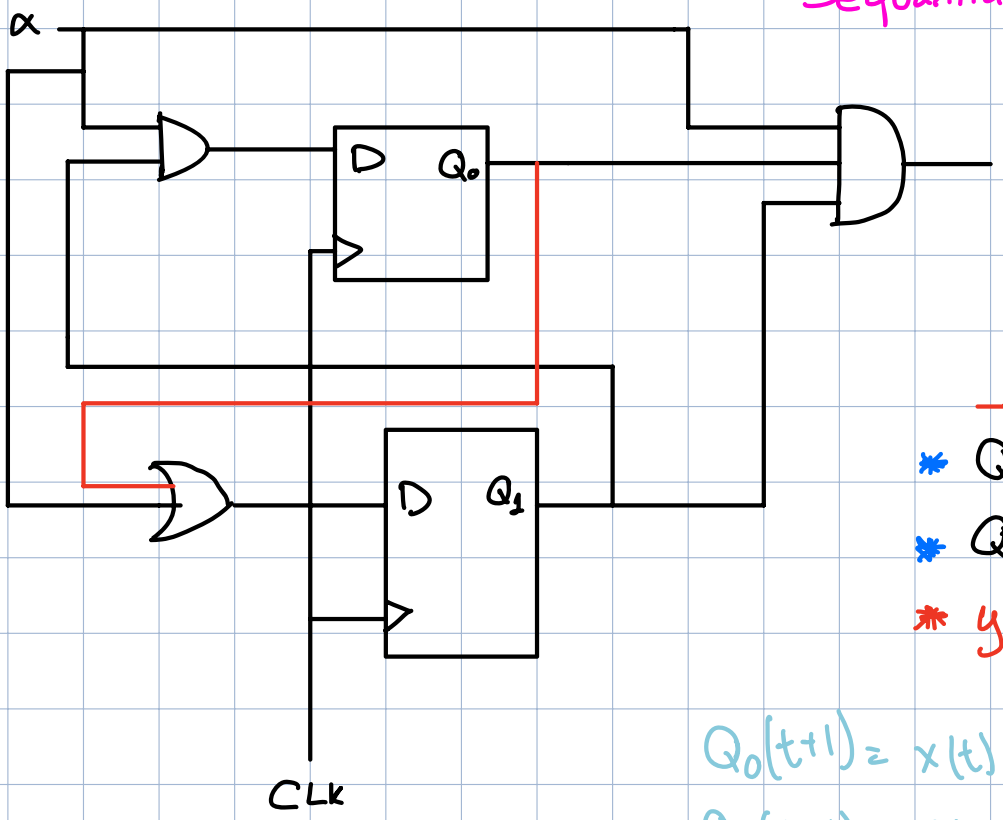
R	CLK	D	Q	Q'
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

$$y(t) = Q_0(t) \cdot Q_1(t) \cdot \alpha(t)$$

$$Q_0(t+1) = \alpha(t) \cdot Q_1(t)$$

$$Q_1(t+1) = Q_0(t) + \alpha(t)$$

Sequantial Devre



$y = x(t) \cdot Q_0(t) \cdot Q_1(t)$

State EQ's

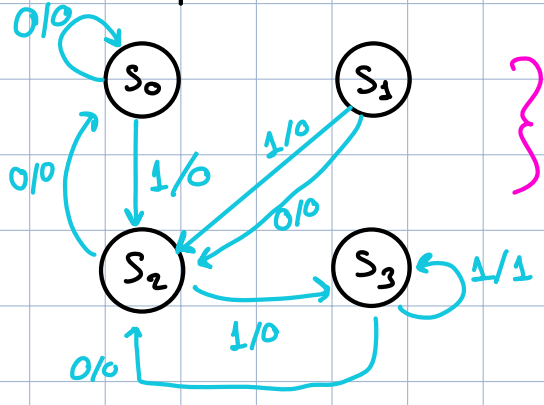
* $Q_0(t+1) = x(t) \cdot Q_1(t)$
* $Q_1(t+1) = x(t) + Q_0(t)$
* $y(t) = x(t) \cdot Q_0(t) \cdot Q_1(t)$

$Q_0(t+1) = x(t) \cdot Q_1(t)$

$Q_1(t+1) = x(t) + Q_0(t)$

State Table

	Present State		Next State						y	
			input → x=1			→ x=0			output	
	$Q_1(t)$	$Q_0(t)$		$Q_1(t+1)$	$Q_0(t+1)$		$Q_1(t+1)$	$Q_0(t+1)$	x=1	x=0
S_0	0	0	4	1	0	0	0	0	0	0
S_1	0	1	5	1	0	1	1	0	0	0
S_2	1	0	6	1	1	2	0	0	0	0
S_3	1	1	7	1	1	3	1	0	1	0

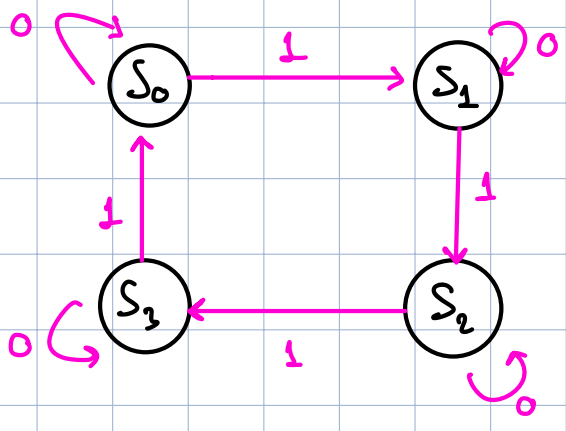


State diagram (durum)

x \ Q_1Q_0	00	01	11	10
0	0	1	1	0
1	1	1	1	1

örnek 2-bit sayaç oluştur. Enable ile

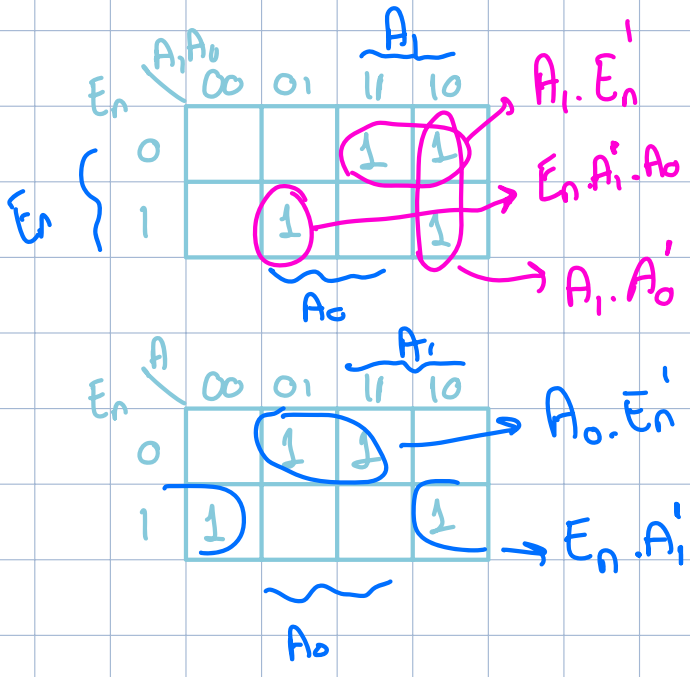
	EN	$A_1(t)$	$A_0(t)$	$A_1(t+1)$	$A_0(t+1)$	
öyle kalsın	0	0	0	0	0	0
	0	0	1	0	1	1
	0	1	0	1	0	2
	0	1	1	1	1	3
	1	0	0	0	1	4
	1	0	1	1	0	5
	1	1	0	1	1	6
	1	1	1	0	0	7



1 olduğu yerler

$A_1(t+1) = \Sigma(2,3,5,6)$

$A_0(t+1) = \Sigma(1,3,4,6)$



$$A_1(t+1) = A_1 \cdot E_n' + A_1' \cdot A_0 \cdot E_n + A_1 \cdot A_0'$$

$$A_0(t+1) = A_0 \cdot E_n' + E_n \cdot A_1'$$