Advanced Computer Achitecture

High Performance Processors and Systems

April 28, 2025

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Name
Last Name
ID Number

Question 1 (20%)	
Question 2 (20%)	
Problem 1 (30%)	
Problem 2 (30%)	
Total (100%)	

To pass the midterm, a minimum score of 20% is requested by each "section" (section 1: problems, section 2: questions). The overall score, to consider the midterm as passed to access the project, has to be greater or equal to 50%

Question 1 (write your answer on the paper)

Define the main characteristics of a VLIW architecture. Explain which is the basic idea behind Trace Scheduling for VLIW and why is it necessary to get good performance from a VLIW?

Question 2 (write your answer on the paper)

Using the "Early Evaluation of PC" applied to branch instructions, how many stalls are needed to execute the following assembly code. Effectively support your answer

```
lw $1, 0($5)
beq $1, $0, label
```

Circle the bullet of the right answer

- **Answer 1**: 1
- **Answer 2**: 2
- **Answer 3**: 0
- **Answer 4**: 3

Problem 1

Assume that the following code has been executed on a CPU with TOMASULO with the following configuration:

- 2 RS (RS1, RS2) with 2 MUL unit and 10 CC of latency
- 2 RS (RS3, RS4) 2 ADDD/SUBD unit and 1 CC of latency
- 1 RS (RS5) 1 LDU and 2 CC of latency

	Instruction	ISSUE	Start EXE	WB
I1	**LD F1, 0 (R2)**	1	2	4
I2	**MULTD F2, F1, F1**	2	5	15
I3	**ADDD F3, F1, F5**	5	5	6
I4	**MULTD F2, F3, F1**	4	7	17
I5	**SUBD F5, F1, F5**	3	6	7

A. List all the possible conflicts in the code.
B. Is the proposed table correct? If it is not correct, please, write the right one.

	Instruction	ISSUE	Start EXE	WB
I1	**LD F1, 0 (R2)**			
I2	**MULTD F2, F1, F1**			
I3	**ADDD F3, F1, F5**			
I4	**MULTD F2, F3, F1**			
I5	**SUBD F5, F1, F5**			

Problem 2 (write your answer on the paper)

Describe (the answer has to be effectively supported) a 1-BHT and a 2-BHT able to execute the following assembly code (R0 is set to 1, R1 is set to 0)

```
LOOP:   LD     F1   0     R0
        ADDD   F2   F1    F1
        ADDI   R1   R1    1000
LOOP2:  MULTD  F2   F2    F1
        SUBI   R1   R1    1
        BNEZ   R1   LOOP2
        SUBI   R0   R0    1
        BNEZ   R0   LOOP
```

The obtained result, in terms of miss predictions, is inline with theoretical characteristics of the two predictors? Please effectively support your answer.

THEORY 1

VLIW IS A STATIC SCHEDULING APPROACH THAT PACKS MULTIPLE OPERATIONS INTO ONE LONG INSTRUCTION WORD WITH PARALLELISM DETERMINED AT COMPILE TIME.

IF NOT ALL SLOTS ARE FILLED, IT INSERTS NOP WHICH LEADS TO POTENTIAL CODE BLOAT.

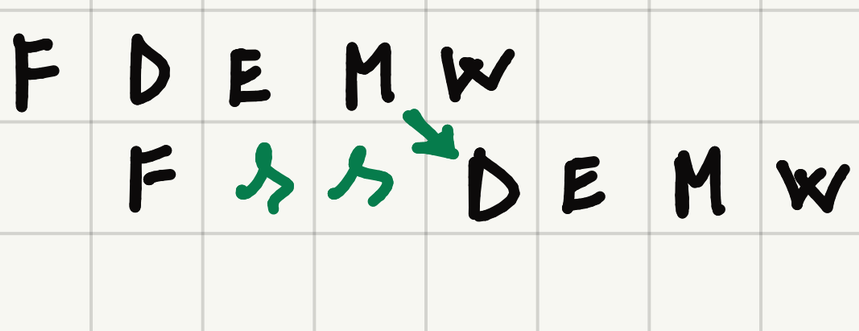
VLIW EXECUTES INSTRUCTIONS EXACTLY IN THE ORDER PROVIDED BY THE COMPILED BUNDLES. TRACE SCHEDULING IS A COMPILER OPTIMIZATION THAT RESTRUCTURES CODE ALONG THE MOST COMMON EXECUTION PATHS TO FILL VLIW SLOTS MAXIMIZING PARALLELISM AND REDUCING NOP. IT'S ESSENTIAL TO EXPOSE ILP BECAUSE VLIW HARDWARE IS SIMPLE AND RELIES ENTIRELY ON THE COMPILER TO

THEORY 2

EARLY EVALUATION OF PC MEANS THAT THE PROCESSOR TRIES TO COMPUTE THE BRANCH TARGET AS SOON AS POSSIBLE, GENERALLY AT THE END OF D.

RAW

```
lw $1, 0($5)
beq $1, $0, label
```



2 STALLS ARE NEEDED

EXERCISE 1

LD F1, 0 (R2)
MULTD F2, F1, F1
ADDD F3, F1, F5
MULTD F2, F3, F1
SUBD F5, F1, F5

RAW F1 I1-I2
RAW F1 I1-I3
RAW F1 I1-I4
RAW F1 I1-I5
RAW F3 I3-I4

WAW F2 I2-I4

WAR F5 I3-I5

	Instruction	ISSUE	Start EXE	WB
I1	LD F1, 0 (R2)	1	2	4
I2	MULTD F2, F1, F1	2	5 ✓	15
I3	ADDD F3, F1, F5	5	5	6
I4	MULTD F2, F3, F1	4	7	17
I5	SUBD F5, F1, F5	3	6	7

ISSUE AND START EXE OF SAME INSTRUCTION CANNOT OCCUR AT THE SAME TIME

	Instruction	ISSUE	Start EXE	WB
I1	LD F1, 0 (R2)	1	2	4
I2	MULTD F2, F1, F1	2	5	15
I3	ADDD F3, F1, F5	3	5	6
I4	MULTD F2, F3, F1	4	7	17
I5	SUBD F5, F1, F5	5	6	7

- 2 RS (RS1, RS2) with 2 MUL unit and 10 CC of latency
- 2 RS (RS3, RS4) 2 ADDD/SUBD unit and 1 CC of latency
- 1 RS (RS5) 1 LDU and 2 CC of latency

ESERCIZIO 2

```
LOOP:   LD      F1   0     R0
        ADDD    F2   F1    F1
        ADDI    R1   R1    1000
LOOP2:  MULTD   F2   F2    F1
        SUBI    R1   R1    1
        BNEZ    R1   LOOP2
        SUBI    R0   R0    1
        BNEZ    R0   LOOP
```

R0=1 R1=0

R1=1000

1000 ITERATIONS

0=0 ⇒ 0 ITERATIONS

1-BHT NO COLLISION

```
LOOP:   LD      F1   0     R0
        ADDD    F2   F1    F1
        ADDI    R1   R1    1000
LOOP2:  MULTD   F2   F2    F1
        SUBI    R1   R1    1
    T   BNEZ    R1   LOOP2
        SUBI    R0   R0    1
    T   BNEZ    R0   LOOP
```

T→NT

1 + 1

2-BHT NO COLLISION

```
LOOP:   LD      F1   0     R0
        ADDD    F2   F1    F1
        ADDI    R1   R1    1000
LOOP2:  MULTD   F2   F2    F1
        SUBI    R1   R1    1
   T1   BNEZ    R1   LOOP2
        SUBI    R0   R0    1
   T2   BNEZ    R0   LOOP
```

$T_1 \rightarrow T_W$

1 + 1

```
LOOP:   LD      F1   0     R0
        ADDD    F2   F1    F1
        ADDI    R1   R1    1000
LOOP2:  MULTD   F2   F2    F1
        SUBI    R1   R1    1
  NT1   BNEZ    R1   LOOP2
        SUBI    R0   R0    1
  NT2   BNEZ    R0   LOOP
```

$NT \rightarrow T$ $T_2 \rightarrow T_W$

2 + 1 + 0

RESULTS NOT IN LINE WITH THEORETICAL CHARACTERISTIC, AS W.C. 2BHT ISN'T BETTER THAN B.C. 1-BHT