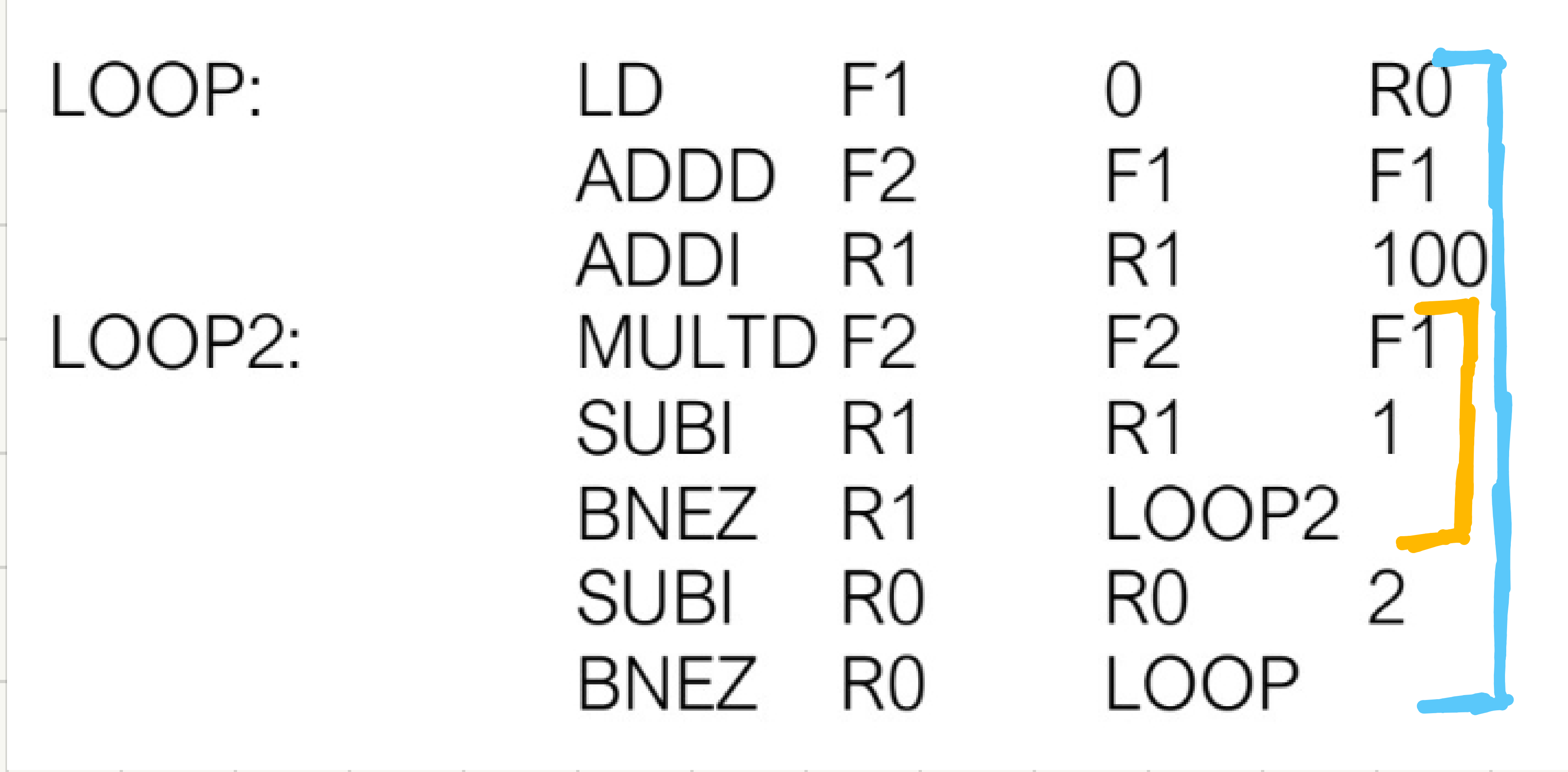
Dynamic Branch Predictor

- Describe (the answer has to be effectively supported) a 1-BHT and a 2-BHT able to execute the following assembly code (R0 is set to 2000, R1 is set to 0)

```
LOOP:       LD    F1   0      R0
            ADDD  F2   F1     F1
            ADDI  R1   R1     100
LOOP2:      MULTD F2   F2     F1
            SUBI  R1   R1     1
            BNEZ  R1   LOOP2
            SUBI  R0   R0     2
            BNEZ  R0   LOOP
```

- The obtained result, in terms of mispredictions, is inline with theoretical characteristics of the two predictors? Please effectively support your answer.

LET'S FIRST UNDERSTAND WHERE AND HOW A LOOP WORKS



```
LOOP:     LD     F1   0      R0
          ADDD   F2   F1     F1
          ADDI   R1   R1     100
LOOP2:    MULTD  F2   F2     F1
          SUBI   R1   R1     1
          BNEZ   R1   LOOP2
          SUBI   R0   R0     2
          BNEZ   R0   LOOP
```

R0=2000

R1=0

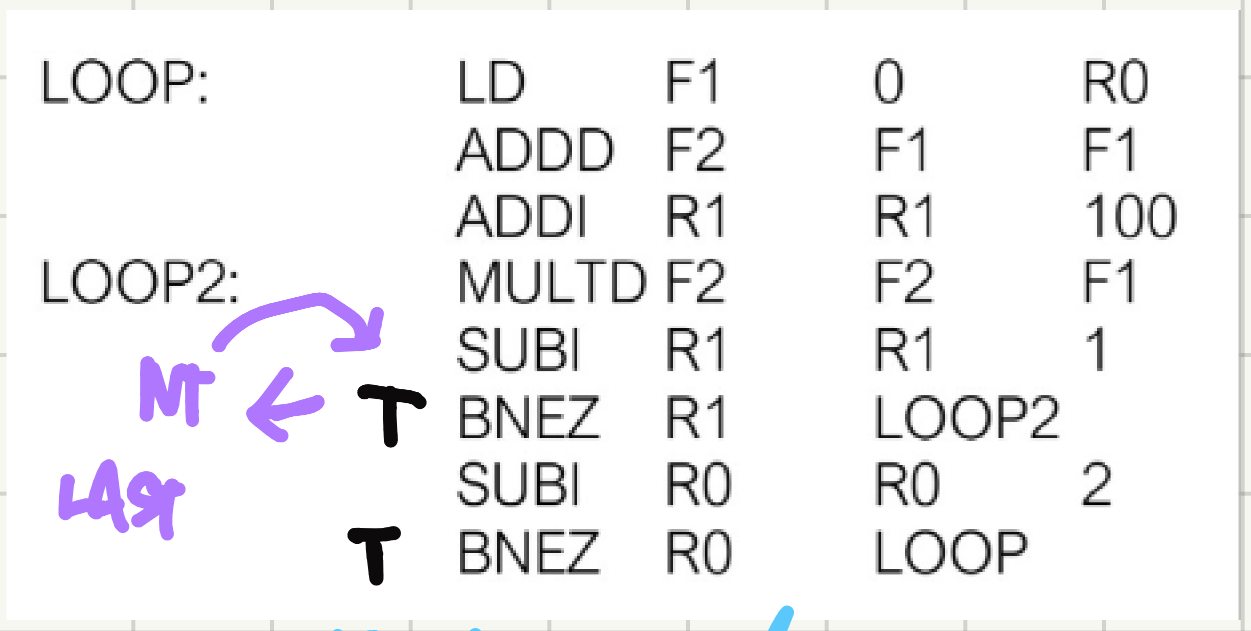
LOOP2 100 ITERATIONS · #LOOP   LOOP 1000 ITERATIONS

DYNAMICALLY COMPUTE THE NUMBER OF MISPREDICTIONS

1-bit BHT WITH NO COLLISION

LOOP T

LOOP2 T



```
LOOP:     LD     F1   0      R0
          ADDD   F2   F1     F1
          ADDI   R1   R1     100
LOOP2:    MULTD  F2   F2     F1
          SUBI   R1   R1     1
          BNEZ   R1   LOOP2
          SUBI   R0   R0     2
          BNEZ   R0   LOOP
```

NT ← T

LAST

T

LAST: NT = NT ✓

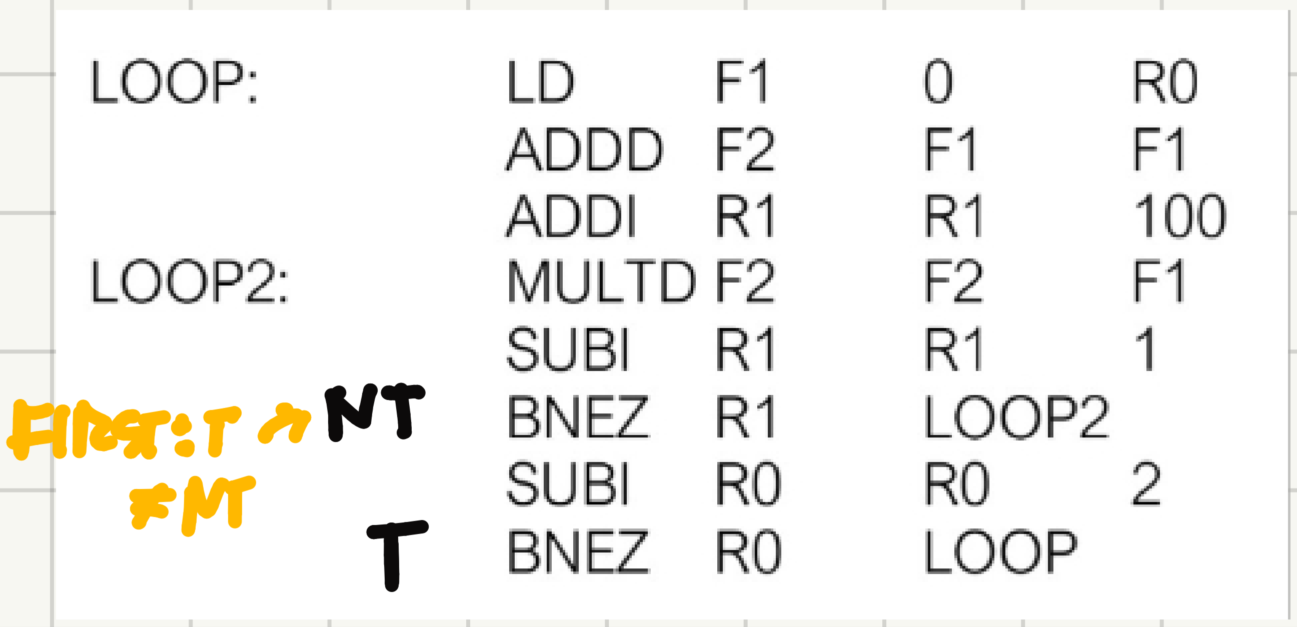
T→NT   T→NT

$1+(1+1)\cdot 999 + 1$

T→NT   NT→T

LOOP T

LOOP2 NT



```
LOOP:     LD     F1   0      R0
          ADDD   F2   F1     F1
          ADDI   R1   R1     100
LOOP2:    MULTD  F2   F2     F1
          SUBI   R1   R1     1
          BNEZ   R1   LOOP2
          SUBI   R0   R0     2
          BNEZ   R0   LOOP
```

FIRST: T → NT

≠ NT

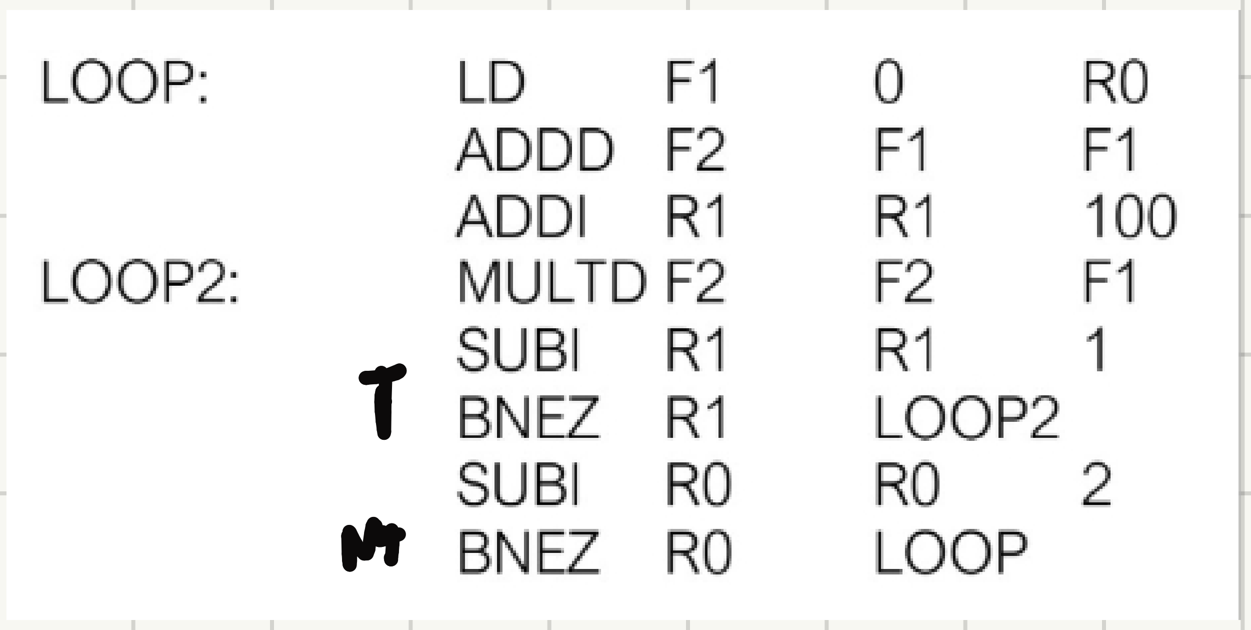
T

NT→T   T→NT

$(1+1)\cdot 1000 + 1$

LOOP NT

LOOP2 T



```
LOOP:     LD     F1   0      R0
          ADDD   F2   F1     F1
          ADDI   R1   R1     100
LOOP2:    MULTD  F2   F2     F1
          SUBI   R1   R1     1
          BNEZ   R1   LOOP2
          SUBI   R0   R0     2
          BNEZ   R0   LOOP
```

T

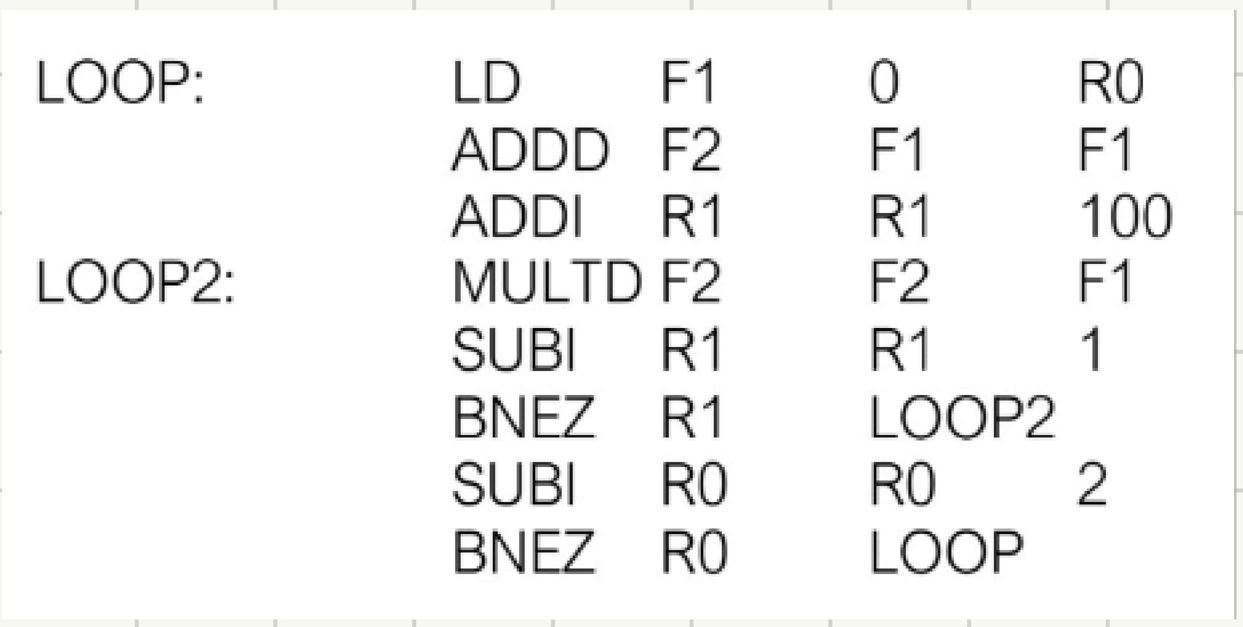
NT

NT→T   T→NT

$1+(1+1)\cdot 999 + 1 + 1$

LOOP NT

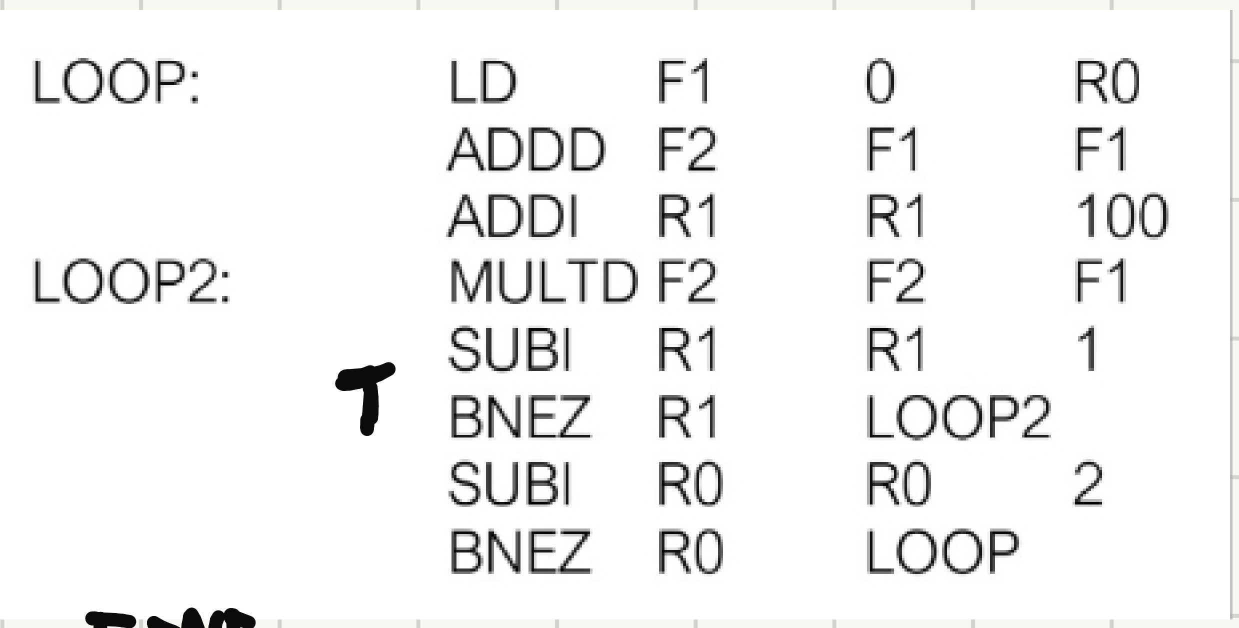
LOOP2 NT



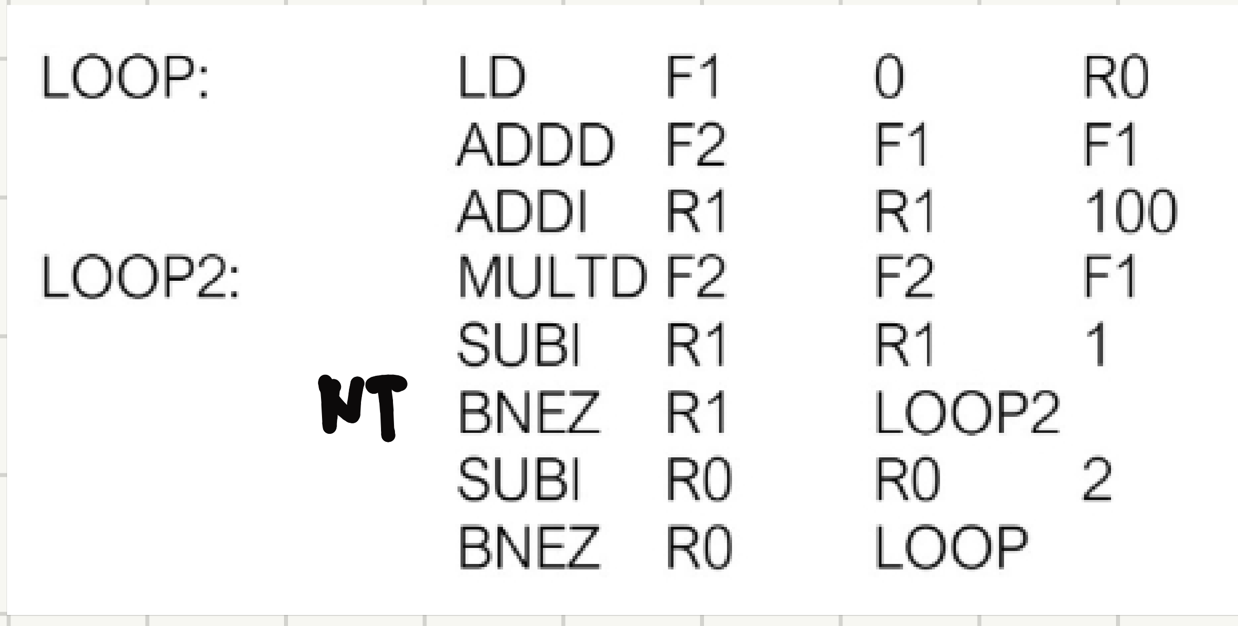
```
LOOP:     LD     F1   0      R0
          ADDD   F2   F1     F1
          ADDI   R1   R1     100
LOOP2:    MULTD  F2   F2     F1
          SUBI   R1   R1     1
          BNEZ   R1   LOOP2
          SUBI   R0   R0     2
          BNEZ   R0   LOOP
```

$(1+1)\cdot 1000 + 2$

1-bit BHT WITH COLLISION



```
LOOP:     LD    F1   0      R0
          ADDD  F2   F1     F1
          ADDI  R1   R1     100
LOOP2:    MULTD F2   F2     F1
          SUBI  R1   R1     1
        T BNEZ  R1   LOOP2
          SUBI  R0   R0     2
          BNEZ  R0   LOOP
```



```
LOOP:     LD    F1   0      R0
          ADDD  F2   F1     F1
          ADDI  R1   R1     100
LOOP2:    MULTD F2   F2     F1
          SUBI  R1   R1     1
       NT BNEZ  R1   LOOP2
          SUBI  R0   R0     2
          BNEZ  R0   LOOP
```

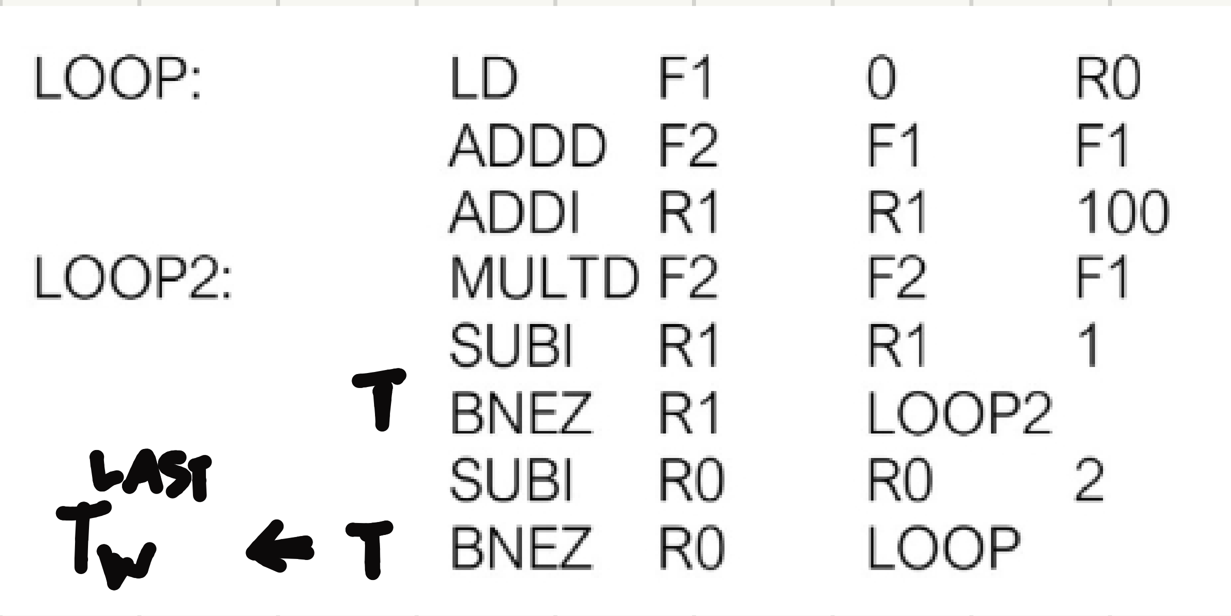
$(\overset{T\to NT}{1} + \overset{NT\to T}{1}) \cdot 999 + \overset{T\to NT}{1}$

$\overset{NT\to T}{1} + (1 + 1) \cdot 999 + 1$

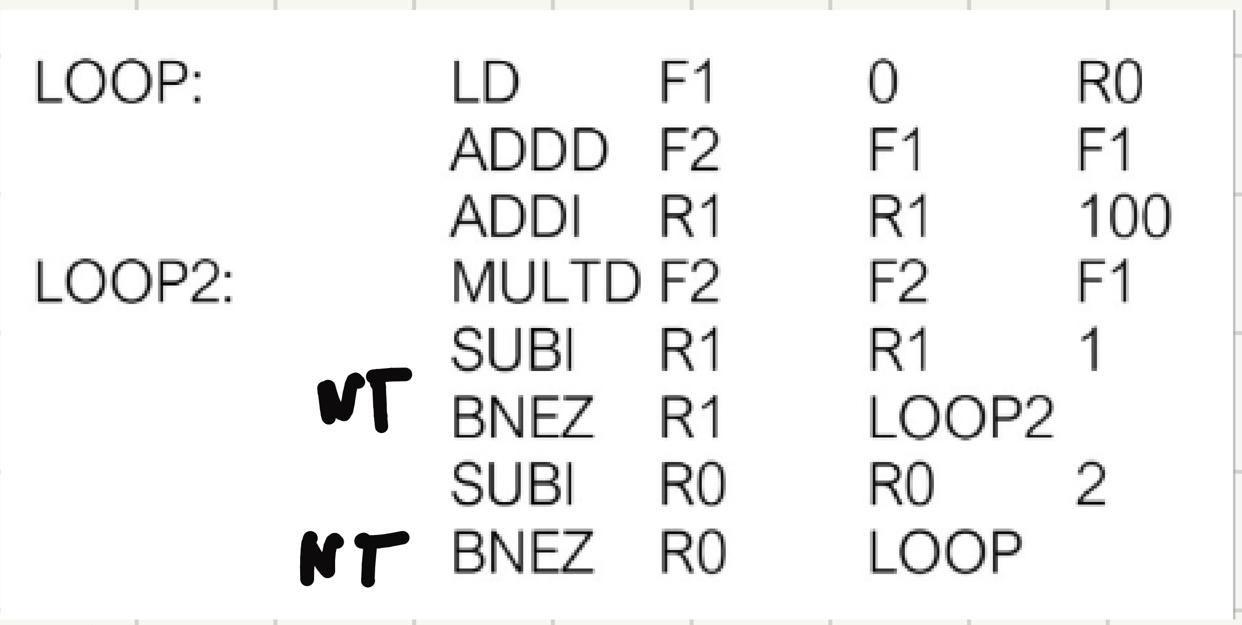
2-bit BHT WITH NO COLLISION

LOOP TT
LOOP2 TT

LOOP NT NT
LOOP2 NT NT



```
LOOP:     LD    F1   0      R0
          ADDD  F2   F1     F1
          ADDI  R1   R1     100
LOOP2:    MULTD F2   F2     F1
          SUBI  R1   R1     1
        T BNEZ  R1   LOOP2
   LAST   SUBI  R0   R0     2
   Tw ← T BNEZ  R0   LOOP
```

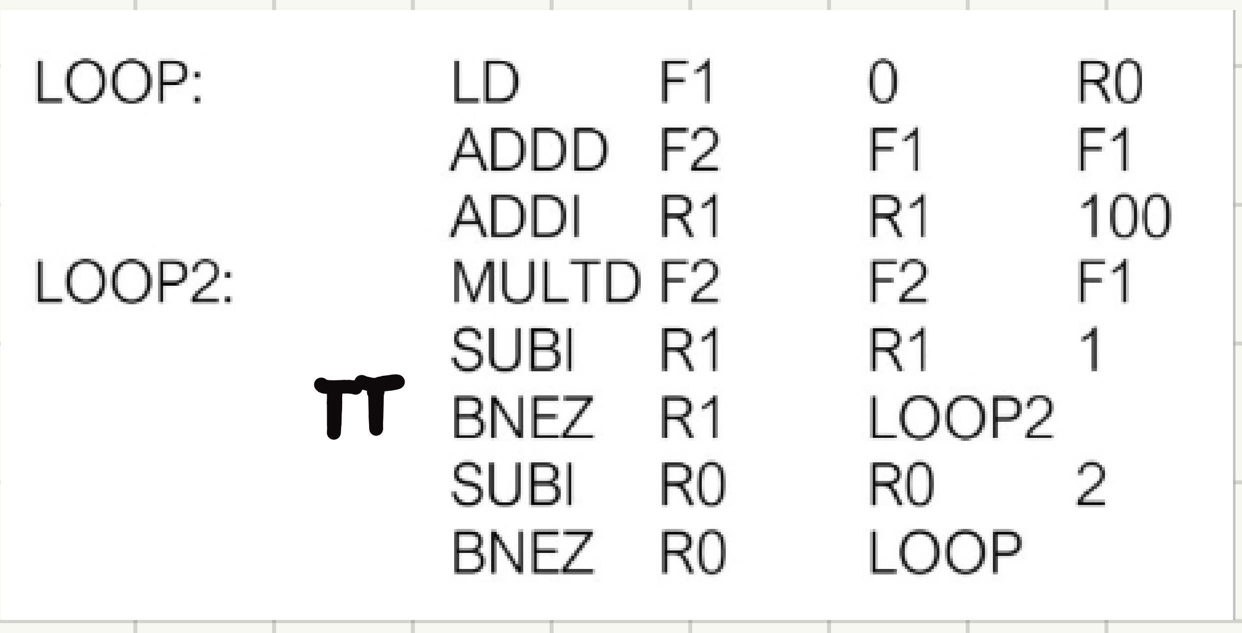


```
LOOP:     LD    F1   0      R0
          ADDD  F2   F1     F1
          ADDI  R1   R1     100
LOOP2:    MULTD F2   F2     F1
          SUBI  R1   R1     1
       NT BNEZ  R1   LOOP2
          SUBI  R0   R0     2
       NT BNEZ  R0   LOOP
```

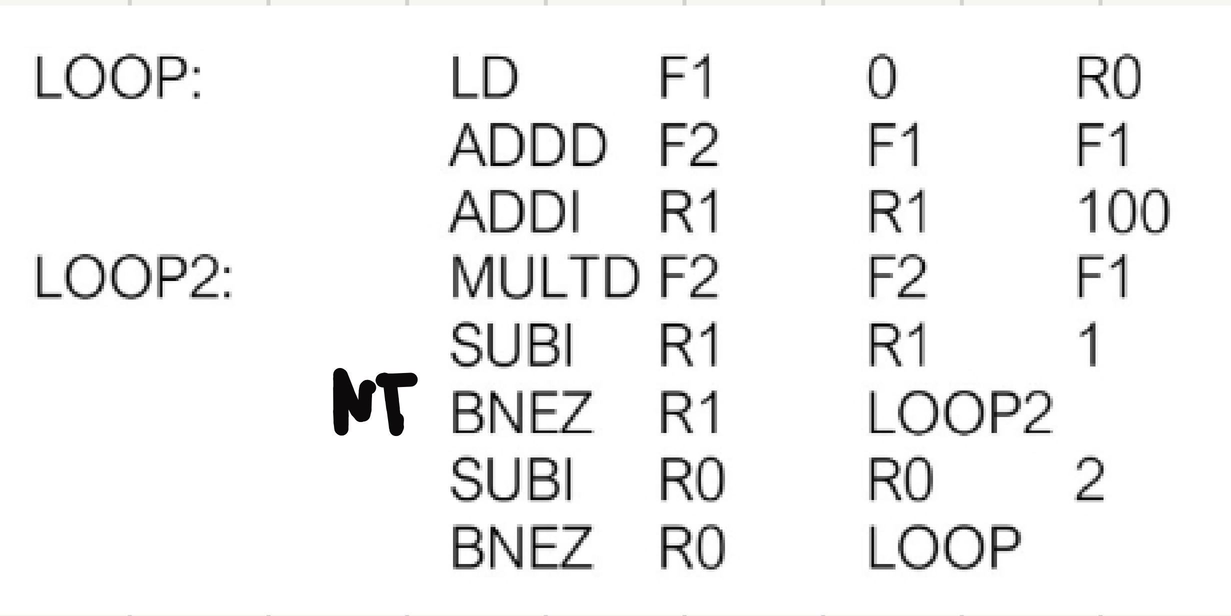
$\overset{T_s\to T_w}{1} \cdot 1000 + \overset{T_s\to T_w \text{ LAST}}{1}$

$(\overset{NT_s\to NT_w}{1} + \overset{NT_w\to T}{1} + \underset{T_s\to T_w}{1}) + (\overset{T_s\to T_w}{1} \cdot 999) + (\underset{NT_s\to NT_w}{1} + \overset{NT_w\to T}{1} + \underset{T_s\to T_w \text{ LAST}}{1})$

2-bit BHT WITH COLLISION



```
LOOP:     LD    F1   0      R0
          ADDD  F2   F1     F1
          ADDI  R1   R1     100
LOOP2:    MULTD F2   F2     F1
          SUBI  R1   R1     1
       TT BNEZ  R1   LOOP2
          SUBI  R0   R0     2
          BNEZ  R0   LOOP
```



```
LOOP:     LD    F1   0      R0
          ADDD  F2   F1     F1
          ADDI  R1   R1     100
LOOP2:    MULTD F2   F2     F1
          SUBI  R1   R1     1
       NT BNEZ  R1   LOOP2
          SUBI  R0   R0     2
          BNEZ  R0   LOOP
```

$\overset{T_s\to T_w}{1} \cdot 1000 + \overset{T_s\to T_w \text{ LAST}}{1}$

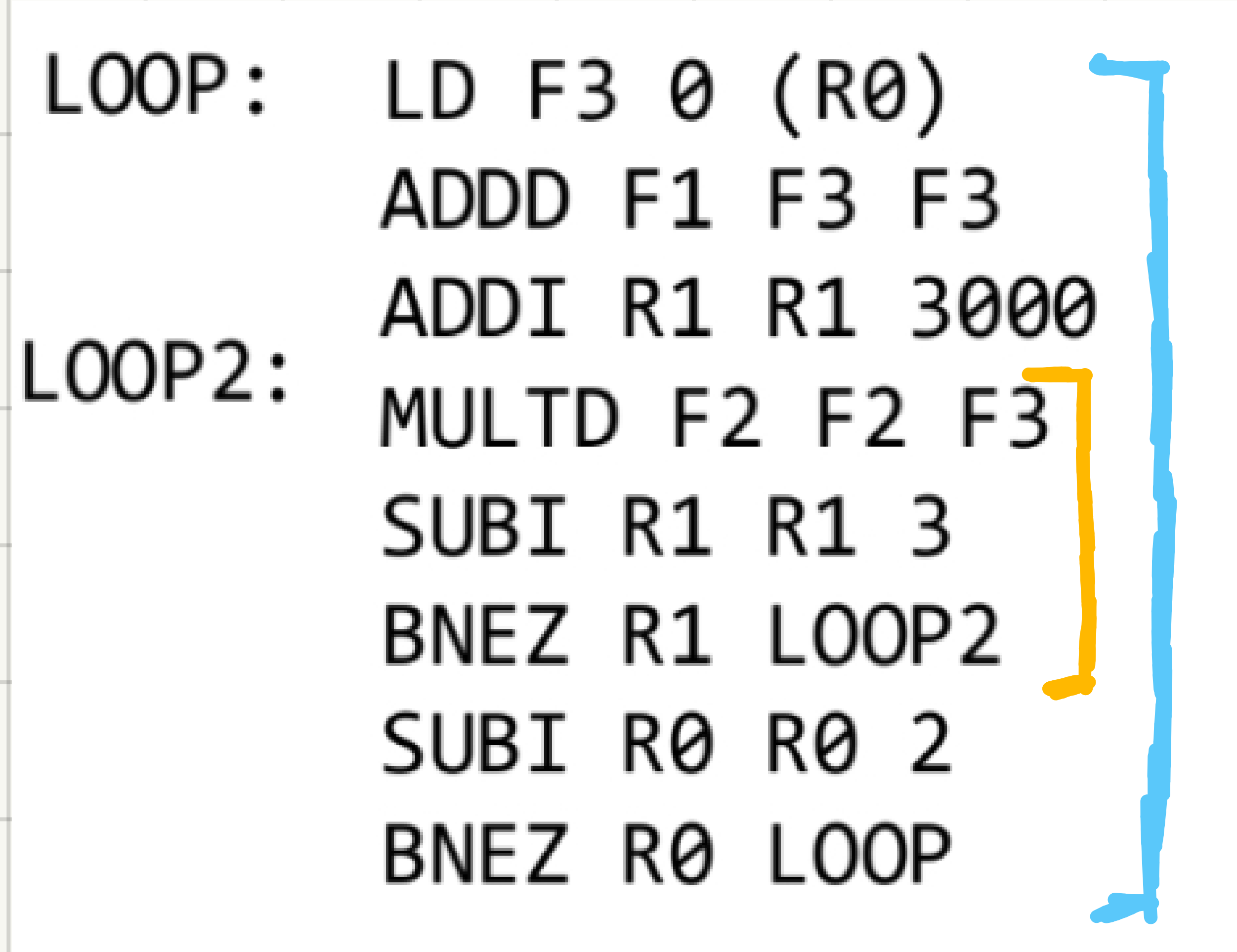
$\overbrace{1+1}^{NT\to T} + \overset{T_s\to T_w}{1} + 0 + \overbrace{1 \cdot 999}^{T_s\to T_w} + \overset{T_w\to NT \text{ (LAST)}}{1}$

Dynamic Branch Predictor

- Describe (the answer has to be effectively supported) a 1-BHT and a 2-BHT able to execute the following assembly code (R0 is set to 1, R1 is set to 300)

```
LOOP:   LD F3 0 (R0)
        ADDD F1 F3 F3
        ADDI R1 R1 3000
LOOP2:  MULTD F2 F2 F3
        SUBI R1 R1 3
        BNEZ R1 LOOP2
        SUBI R0 R0 2
        BNEZ R0 LOOP
```

- The obtained result, in terms of mispredictions, is inline with theoretical characteristics of the two predictors? Please effectively support your answer.



```
LOOP:   LD F3 0 (R0)
        ADDD F1 F3 F3
        ADDI R1 R1 3000
LOOP2:  MULTD F2 F2 F3
        SUBI R1 R1 3
        BNEZ R1 LOOP2
        SUBI R0 R0 2
        BNEZ R0 LOOP
```

$R_1=300$ $R_0=1$

$R_1=300+3000=3300$

$\frac{3300}{3}=1100$ ITERATIONS

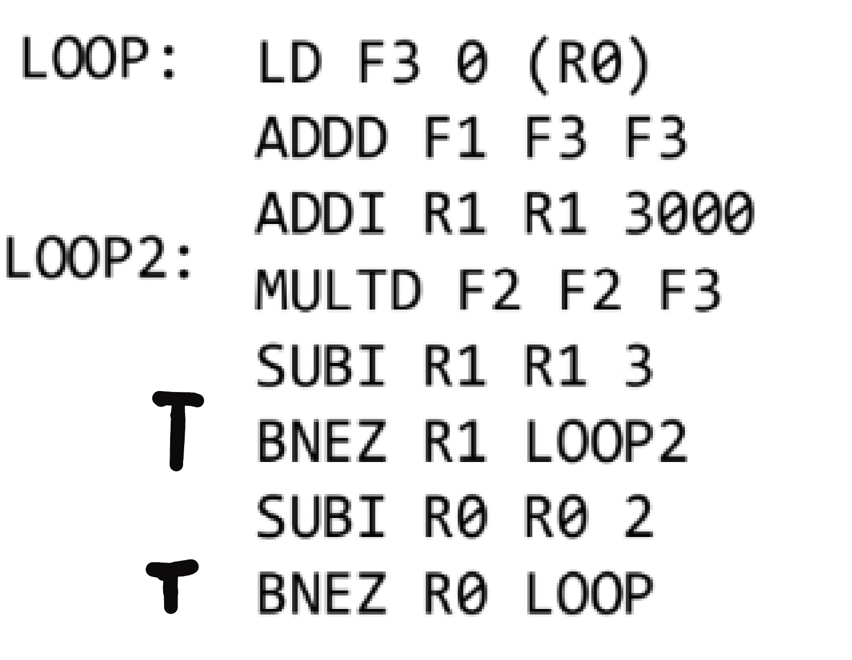
$1-2-2-2-\dots-2$ NEVER $=0$

→ ∞ ITERATIONS

AURE $R_1=3000$ → 1000

1-bit BHT WITH NO COLLISION

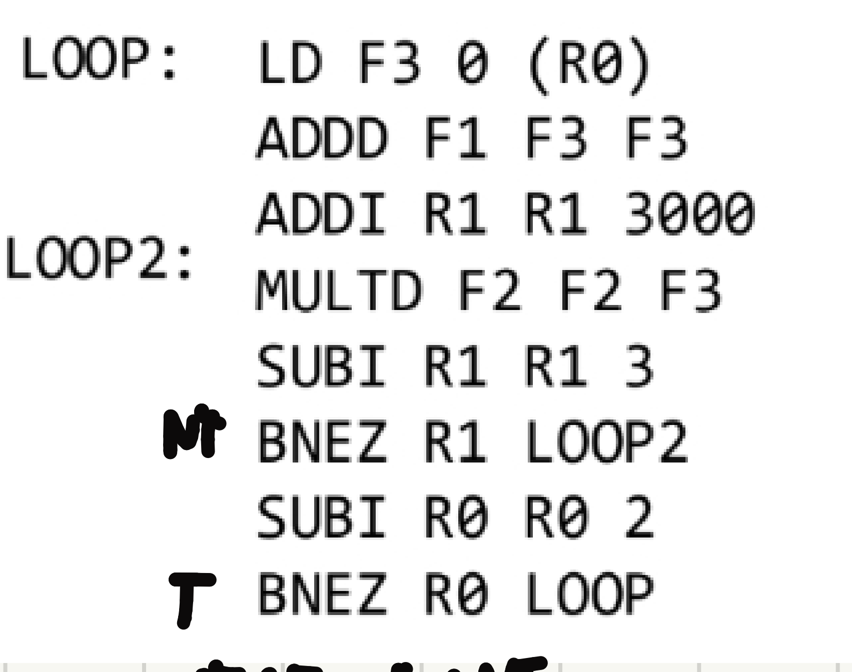
LOOP	T
LOOP2	T



```
LOOP:   LD F3 0 (R0)
        ADDD F1 F3 F3
        ADDI R1 R1 3000
LOOP2:  MULTD F2 F2 F3
        SUBI R1 R1 3
     T  BNEZ R1 LOOP2
        SUBI R0 R0 2
     T  BNEZ R0 LOOP
```

$$\overset{T\to NT}{1}+(\overset{NT\to T}{1}+\underset{T\to NT}{1})\cdot\overbrace{(\infty-1)}^{\infty}+0$$

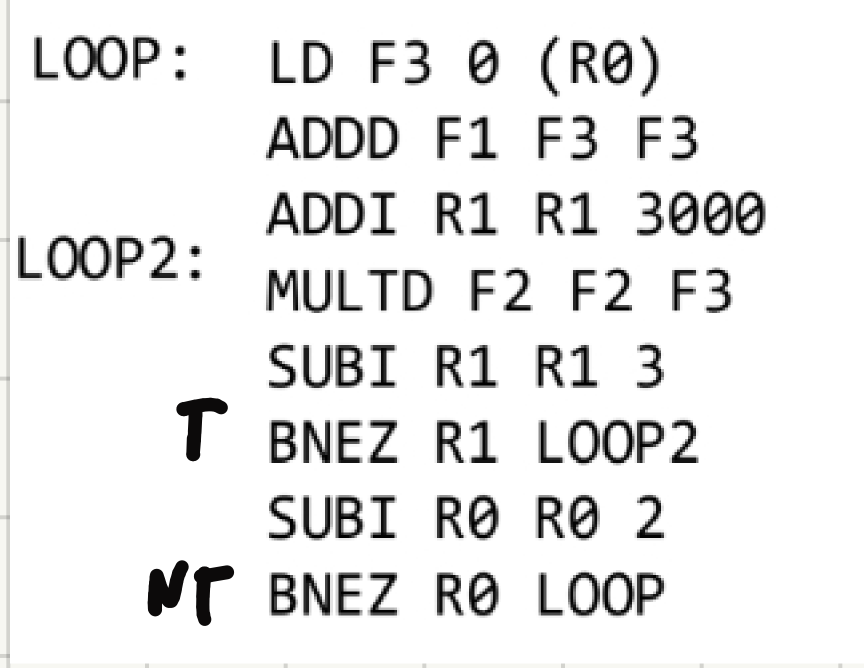
LOOP	T
LOOP2	NT



```
LOOP:   LD F3 0 (R0)
        ADDD F1 F3 F3
        ADDI R1 R1 3000
LOOP2:  MULTD F2 F2 F3
        SUBI R1 R1 3
    NT  BNEZ R1 LOOP2
        SUBI R0 R0 2
     T  BNEZ R0 LOOP
```

$$(\overset{NT\to T}{1}+\overset{T\to NT}{1})\cdot\infty+0$$

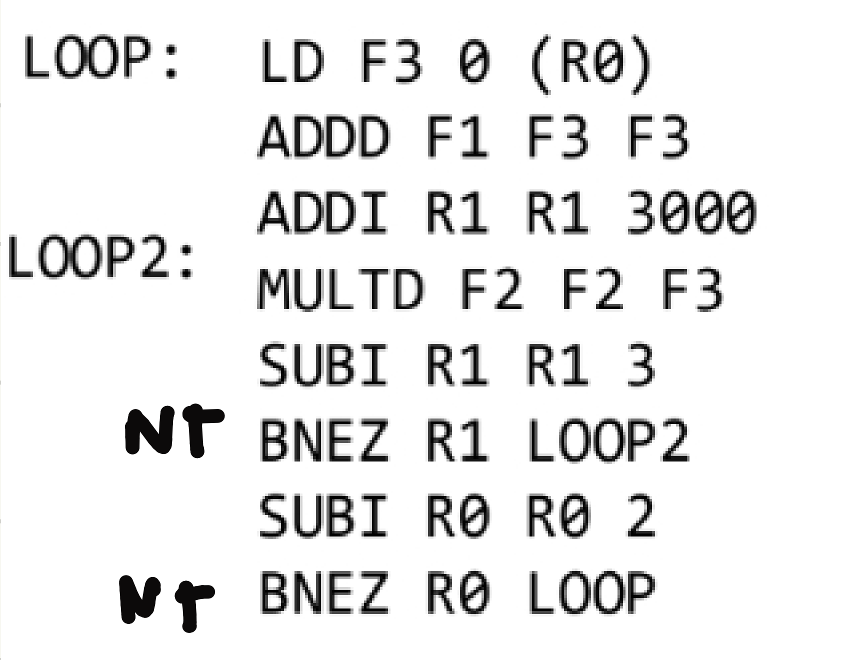
LOOP	NT
LOOP2	T



```
LOOP:   LD F3 0 (R0)
        ADDD F1 F3 F3
        ADDI R1 R1 3000
LOOP2:  MULTD F2 F2 F3
        SUBI R1 R1 3
     T  BNEZ R1 LOOP2
        SUBI R0 R0 2
    NT  BNEZ R0 LOOP
```

$$1+(1+1)\cdot\infty+\overset{NT\to T}{1}$$

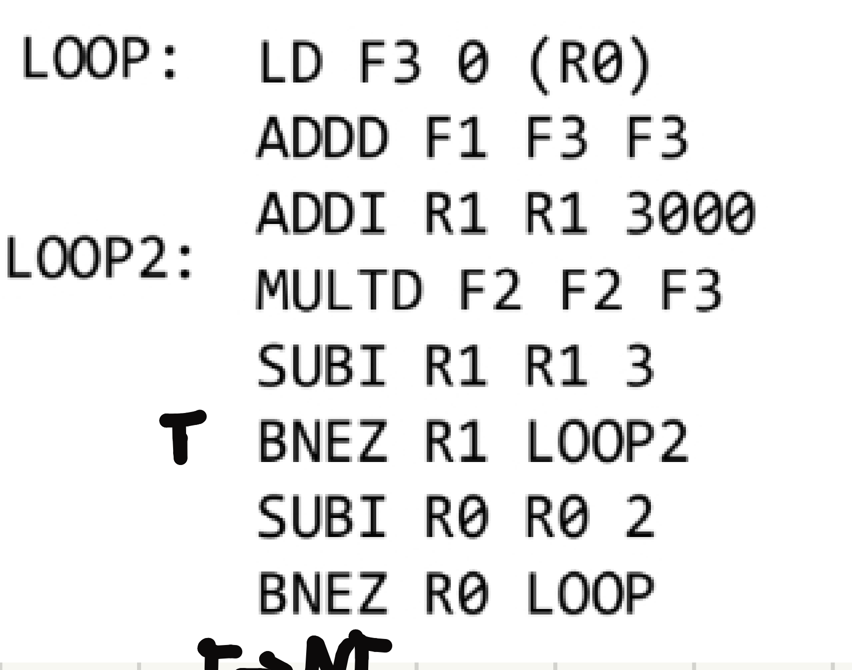
LOOP	NT
LOOP2	NT



```
LOOP:   LD F3 0 (R0)
        ADDD F1 F3 F3
        ADDI R1 R1 3000
LOOP2:  MULTD F2 F2 F3
        SUBI R1 R1 3
    NT  BNEZ R1 LOOP2
        SUBI R0 R0 2
    NT  BNEZ R0 LOOP
```

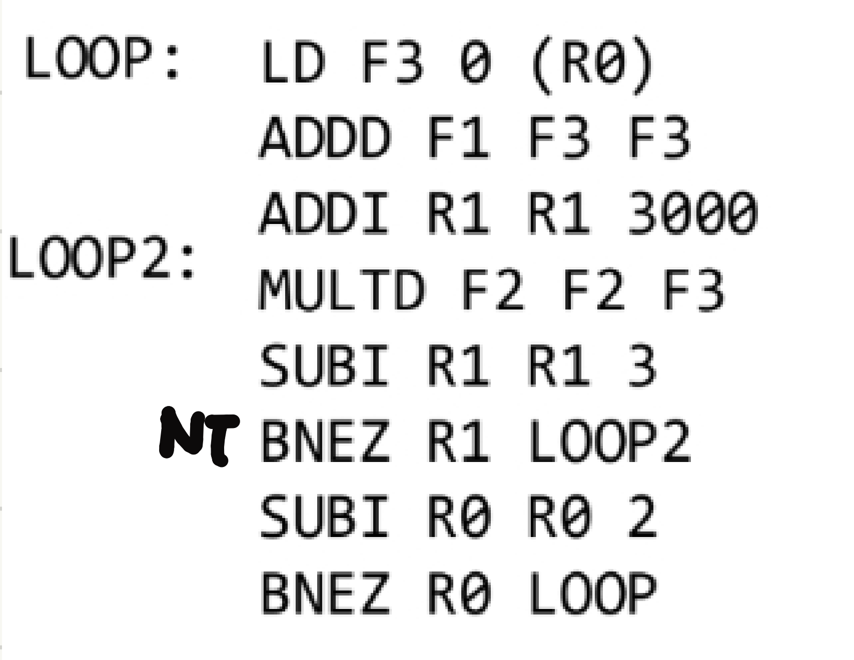
$$(1+1)\cdot\infty+1$$

1-bit BHT with collision



```
LOOP:   LD F3 0 (R0)
        ADDD F1 F3 F3
        ADDI R1 R1 3000
LOOP2:  MULTD F2 F2 F3
        SUBI R1 R1 3
     T  BNEZ R1 LOOP2
        SUBI R0 R0 2
        BNEZ R0 LOOP
```

$(\overset{T\to NT}{1} + \overset{NT\to T}{1})\cdot\infty$



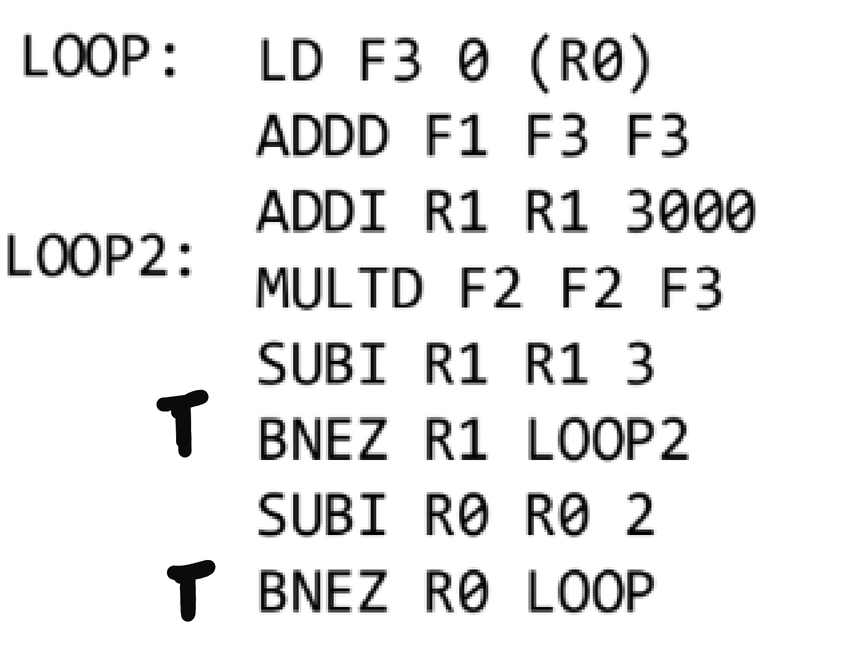
```
LOOP:   LD F3 0 (R0)
        ADDD F1 F3 F3
        ADDI R1 R1 3000
LOOP2:  MULTD F2 F2 F3
        SUBI R1 R1 3
    NT  BNEZ R1 LOOP2
        SUBI R0 R0 2
        BNEZ R0 LOOP
```

$(\overset{T\to NT}{1}+1+\overset{NT\to T}{1})\cdot\infty$

2-bit BHT with no collision

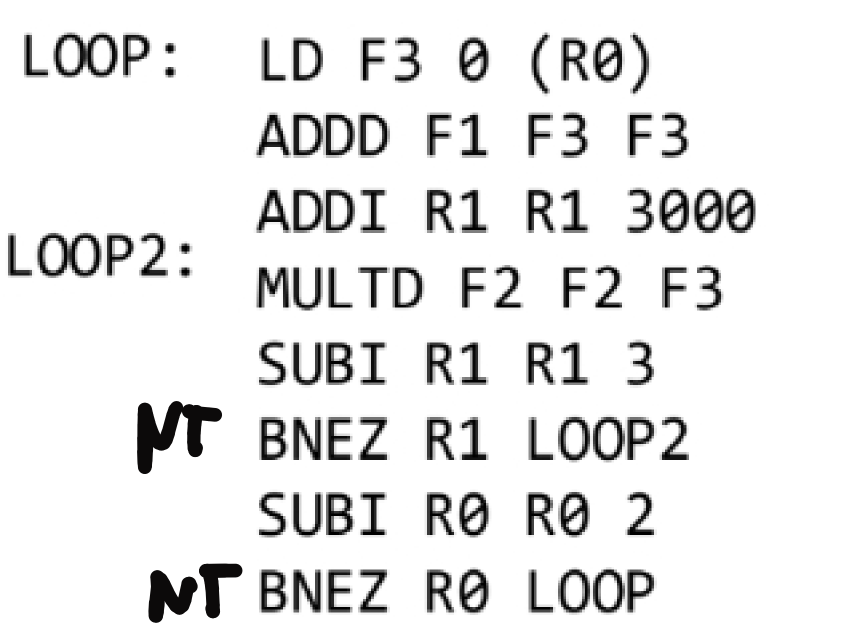
LOOP TT
LOOP2 TT

LOOP NT NT
LOOP2 NT NT



```
LOOP:   LD F3 0 (R0)
        ADDD F1 F3 F3
        ADDI R1 R1 3000
LOOP2:  MULTD F2 F2 F3
        SUBI R1 R1 3
     T  BNEZ R1 LOOP2
        SUBI R0 R0 2
     T  BNEZ R0 LOOP
```

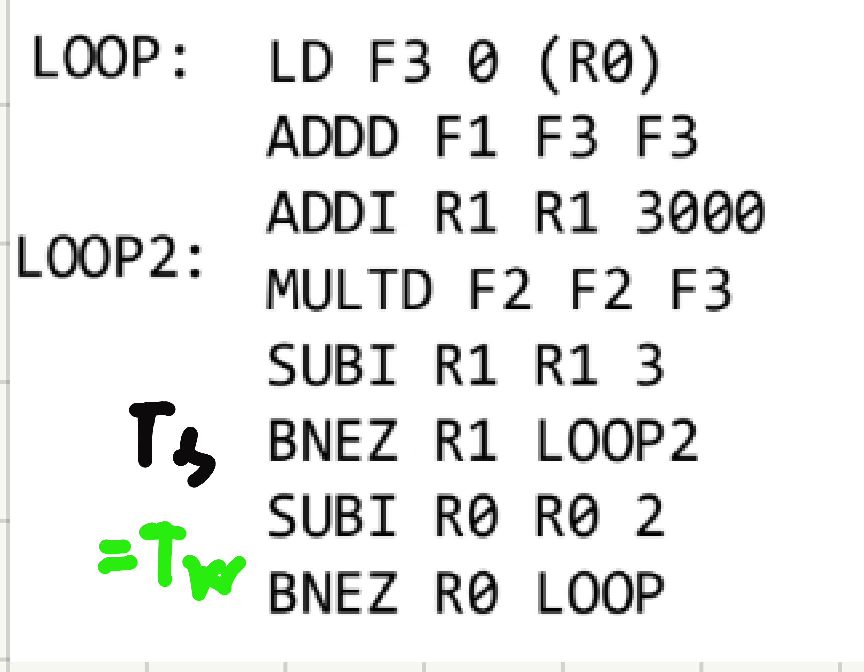
$\overset{T_s\to T_w}{1}\cdot\infty+0$



```
LOOP:   LD F3 0 (R0)
        ADDD F1 F3 F3
        ADDI R1 R1 3000
LOOP2:  MULTD F2 F2 F3
        SUBI R1 R1 3
    NT  BNEZ R1 LOOP2
        SUBI R0 R0 2
    NT  BNEZ R0 LOOP
```

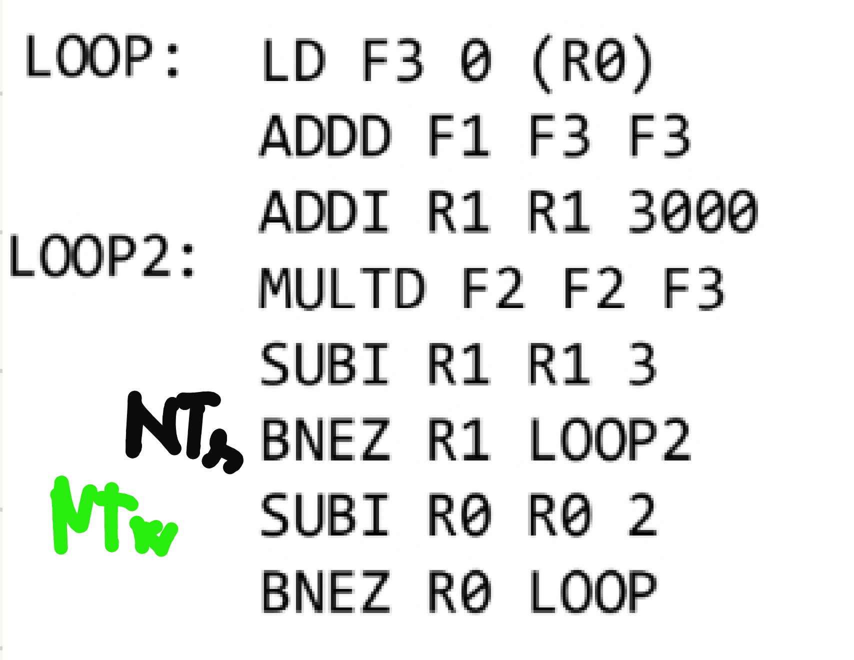
$(\overset{NT\to T}{\overbrace{1+1}}+\overset{T_s\to T_w}{1})+\overset{T_s\to T_w}{1}\cdot\infty+(\overset{NT_s\to NT_w}{1}+\underset{NT_w\to T}{1})$

2-bit BHT with collision



```
LOOP:   LD F3 0 (R0)
        ADDD F1 F3 F3
        ADDI R1 R1 3000
LOOP2:  MULTD F2 F2 F3
        SUBI R1 R1 3
    Ts  BNEZ R1 LOOP2
        SUBI R0 R0 2
   =Tw  BNEZ R0 LOOP
```

$\overset{T_s\to T_w}{1}\cdot\infty+0$



```
LOOP:   LD F3 0 (R0)
        ADDD F1 F3 F3
        ADDI R1 R1 3000
LOOP2:  MULTD F2 F2 F3
        SUBI R1 R1 3
   NTs  BNEZ R1 LOOP2
   NTw  SUBI R0 R0 2
        BNEZ R0 LOOP
```

$(\underbrace{\cancel{1}+1}_{NT\to T}+\underset{T_s\to T_w}{1})+0+\overset{T_s\to T_w}{1}\cdot\infty$