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Advanced Computer Architecture

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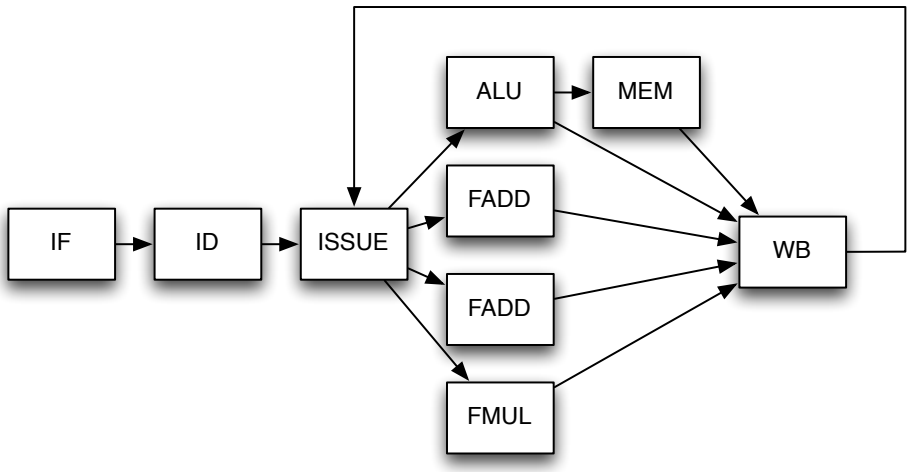
Name
Last Name

The student has to choose 2 out of the 3 exercises. If all the 3 exercises will be completed, just the 2 with the lowest score will be considered. This is an open book exam, which means the students can you use all their notes (we do not care of the format) but they cannot share their exams with anyone during the test.
At the end of the exam, when the professor will call it, each student has to upload at most 2 PDF files using the Microsoft Form share via the Zoom chat at the beginning of the exam: NOTE: if you are doing problem 1 and 3, upload your files using the corresponding box 1 and 3.
Few notes on the files:
1. You have to submit 1 PDF per question
2. Each PDF has to be max 10MB
3. Each PDF has to be named as codice persona plus the exe, e.g., 10000000_exe1.pdf
4. Each PDF has to report the name and the codice persone on each page
5. All these points are are in logic AND, if one of them will not be respected, the ENTIRE exam will not be evaluated

Problem 1 (50%)	
Problem 2 (50%)	
Problem 3 (50%)	
Total (100%)	

Problem 1

In this problem we will examine the execution of a code segment on the following single-issue out-of-order processor:



You can assume that:

- All functional units are pipelined
- ALU operations take 1 cycle
- Memory operations take 2 cycles (includes time in ALU)
- Floating-point add instructions take 3 cycles
- Floating-point multiply instructions take 4 cycles
- There is no register renaming
- Instructions are fetched, decoded and issued in order
- The issue stage is a buffer of unlimited length that holds instructions waiting to start execution
- An instruction will only enter the issue stage if it does not cause a WAR or WAW hazard
- Only one instruction can be issued at a time, and in the case multiple instructions are ready, the oldest one will go first

For this problem we will be using the following code:

```
I1      L.D    F0, 0(R0)
I2      MUL.D  F0, F1, F1
I3      ADD.D  F2, F1, F1
I4      ADD.D  F4, F3, F3
I5      ADDI   R1, R3, 8
I6      ADD.D  F6, F0, F0
```

Question1 - Fill in the following table to indicate how the given code will execute. Assume all register values are available at the start of execution.

Cycle / Inst	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
I1																				
I2																				
I3																				
I4																				
I5																				
I6																				

Problem 2

Assume that the following code has been executed on a CPU with SCOREBOARD.

	Issue	Read Op	Exec Co.	Write R.
LD F6 32+ R2	1	2	3	4
LD F2 45+ R3	5	6	7	8
MULTD F0 F4 F2	6	9	19	20
ADD F2 F8 F6	8	9	10	11
DIVD F12 F0 F6	7	21	31	32
SUBD F6 F8 F2	9	10	11	12

Question A. Is there a "configuration" that can respect the shown execution? If the previous answer was positive, how many units? Which kind? What latency?

Question B. If the previous table was not correct, please, write the right one and specify the number, kind and latency for each unit.

Problem 3

The Cell and Xenon processors are both examples of MIMD. Please effectively support your answer!

1

```
I1      L.D    F0  0(R0)
I2      MUL.D  F0, F1, F1
I3      ADD.D  F2, F1, F1
I4      ADD.D  F4, F3, F3
I5      ADDI   R1, R3, 8
I6      ADD.D  F6, F0, F0
```

ALU 1cc MEM 2cc
FP+ 3cc FP· 4cc

WAW. F0 11-12

RAW F0 12-16

Cycle / Inst	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
I1	F	D	I	E	E	W														
I2		F	↓	↓	D	↓	I	E	E	E	E	W								
I3					F	D	↓	I	E	E	E	↓	W							
I4						F	D	↓	I	E	E	E	↓	W						
I5							F	D	↓	I	E	↓	↓	↓	W					
I6								F	D	↓	↓	I	E	E	E	W				

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	Issue	Read Op	Exec Co.	Write R.
LD F6 32+ R2	1	2	3	4
LD F2 45+ R3	5	6	7	8
MULTD F0 F4 F2	6	9	19	20
ADD F2 F8 F6	8	9	10	11
DIVD F12 F0 F6	7	21	31	32
SUBD F6 F8 F2	9	10	11	12

THIS ANALYSIS IS ENOUGH TO STATE THAT GIVEN EXECUTION IS NOT CORRECT

LD F6 32+ R2

LD F2 45+ R3

MULTD F0 F4 F2

ADD F2 F8 F6

DIVD F12 F0 F6

SUBD F6 F8 F2

RAW F6 12-14
RAW F6 11-15
WAW F6 11-16

RAW F2 14-16

WAR F6 14-16

WAR F6 15-16

RAW F2 12-13

WAW F2 12-14

RAW F0 13-15

WAR F2 13-14

POSSIBLE CONFIGURATION CAN BE:

- 1 MEM 1CC
- 1 FADD 1CC
- 1 FMUL 10CC
- 1 FDIV 10CC

	Issue	Read Op	Exec Co.	Write R.
LD F6 32+ R2	1	2	3	4
LD F2 45+ R3	5	6	7	8
MULTD F0 F4 F2	6	9	19	20
ADD F2 F8 F6	9	10	11	12
DIVD F12 F0 F6	10	21	31	32
SUBD F6 F8 F2	11	13	14	22

> 9 ✓

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THEY ARE EXAMPLES OF MIMD ARCHITECTURES, AND IN PARTICULAR THEY COMPARE HOW A HOMOGENEOUS ARCHITECTURE BASED ON 3 CORES (XENON) AND AN HETEROGENEOUS ARCHITECTURE THAT COMBINES 8 SIMD "SUB-ARCHITECTURES" (CELL) CAN BE EXPLOITED TO PERFORM THE SAME TASKS