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Advanced Computer Architecture

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Name
Last Name
Professor:

Problem 1 (20%)	
Problem 2 (20%)	
Problem 3 (20%)	
Problem 4 (20%)	
Problem 5 (20%)	
Total (100%)	

Problem 1

We are evaluating the possibility to increase the CPU speed 6x (with a 10x cost), knowing that the CPU is used the 70% of time and that the cost of the CPU is ½ the cost of the system. According to the Amdahl's law, compare speedup and cost and evaluate if the upgrade is worth it.
Circle the bullet of the right answer(s)

- The upgrade is convenient because the cost is higher than the speedup
- Speedup and cost are not related but the real speedup is lower than 10x
- The upgrade is not convenient because the cost is higher than the speedup
- The upgrade is convenient because the cost is lower than the speedup

Problem 2

In a 5-stage pipeline MIPS architecture, it is possible to forward a data twice from stage-i to stage-j.
As an example, given the following code:

I1 ADDD F2, F4, F6
I2 ADDD F4, F2, F26
I3 ADDD F6, F2, F4

F2 will be forwarder from I1 to both I2 and I3 by using the EX->EX forwarding path
Circle the bullet of the right answer

- Yes
- No

Problem 3

Assume that a given 5 stage pipeline MIPS architecture is working with a clock cycle equal to 2 ns.
Considering the proposed MIPS code and a pipeline with NO path forwarding.

I1: add $s4, $s2, 6
I2: add $s8, $s4, $s7
I3: sub $s2, $s4, $s8

We are proposing the solution in the picture based only on pipeline stalls/bubbles.

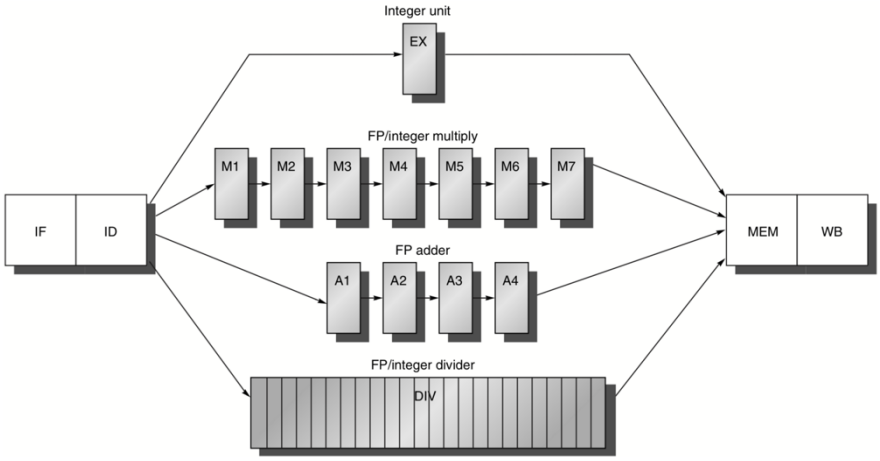
	Clk 1	Clk 2	Clk 3	Clk 4	Clk 5	Clk 6	Clk 7	Clk 8	Clk 9
I1	IF	ID	EXE	MEM	WB				
I2		IF	IFs	IFs	ID	EXE	MEM	WB	
I3					IF	ID	EXE	MEM	WB

Is it correct? Circle the bullet of the right answer

- Yes
- No

Problem 4

Considering the pipeline with multiple floating-point functional units, in which the EX cycle is repeated as many time as needed to complete the operations (as shown in the following figure).



Which of the following statements are TRUE? We may have more than a single TRUE statement. Only correct answers will be counted for the score.

Answer 1: Multiple instructions can be issued during the same clock cycle

Answer 2: Instructions cannot complete in different order in which they were issued

Answer 3: The number of registers write required in a cycle can be greater than 1

Answer 4: Requires the introduction of additional pipeline registers

Problem 5

Design and describe (all the decisions have to be motivated) a 1-BHT and a 2-BHT able to execute the following assembly code.
(R0 is set to 100, R1 is set to 0)

```
LOOP:   LD      F3   0     R0
        ADDD    F1   F3    F3
        MULTD   F2   F3    F1
        ADDI    R1   R1    1000
LOOP2:  LD      F3   0     R1
        MULTD   F2   F2    F3
        SUBI    R1   R1    10
        BNEZ    R1   LOOP2
        SUBI    R0   R0    10
        BNE     R0   R1    LOOP
```

The obtained result, in terms of miss predictions, is inline with theoretical characteristics of the two predictors? Please effectively support your answer.

Problem 1

We are evaluating the possibility to increase the CPU speed 6x (with a 10x cost), knowing that the CPU is used the 70% of time and that the cost of the CPU is ½ the cost of the system. According to the Amdahl's law, compare speedup and cost and evaluate if the upgrade is worth it.

Circle the bullet of the right answer(s)

- The upgrade is convenient because the cost is higher than the speedup
- Speedup and cost are not related but the real speedup is lower than 10x
- The upgrade is not convenient because the cost is higher than the speedup
- The upgrade is convenient because the cost is lower than the speedup

$$COST = \frac{70}{100} \cdot 10 + \frac{30}{100} \cdot 1 = 7{,}3$$

$$SPEEDUP = \frac{1}{1 - 0{,}7 + \frac{0{,}7}{6}} = 2{,}4$$

⇒ UPGRADE NOT CONVENIENT

Problem 2

In a 5-stage pipeline MIPS architecture, it is possible to forward a data twice from stage-i to stage-j.

As an example, given the following code:

I1 ADDD F2, F4, F6
I2 ADDD F4, F2, F26
I3 ADDD F6, F2, F4

F2 will be forwarder from I1 to both I2 and I3 by using the EX->EX forwarding path

Circle the bullet of the right answer

- Yes
- No ✓

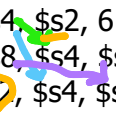
USING E→E FROM I1 TO I2, IF WE USE E→E TO I3 IT WILL RETURN F4 INSTEAD OF F2

Problem 3

Assume that a given 5 stage pipeline MIPS architecture is working with a clock cycle equal to 2 ns.

Considering the proposed MIPS code and a pipeline with NO path forwarding.

I1: add $s4, $s2, 6
I2: add $s8, $s4, $s7
I3: sub $s2, $s4, $s8



RAW RAW WAR RAW

We are proposing the solution in the picture based only on pipeline stalls/bubbles.

	Clk 1	Clk 2	Clk 3	Clk 4	Clk 5	Clk 6	Clk 7	Clk 8	Clk 9
I1	IF	ID	EXE	MEM	WB				
I2		IF	IFs	IFs	ID	EXE	MEM	WB	
I3					IF	ID	EXE	MEM	WB

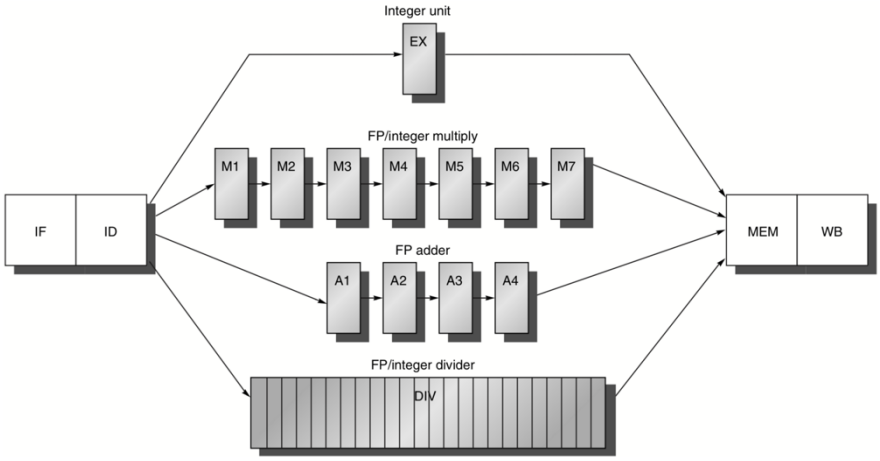
NOT MANAGED

Is it correct? Circle the bullet of the right answer

- Yes
- No

Problem 4

Considering the pipeline with multiple floating-point functional units, in which the EX cycle is repeated as many time as needed to complete the operations (as shown in the following figure).



Which of the following statements are TRUE? We may have more than a single TRUE statement. Only correct answers will be counted for the score.

F

Answer 1: Multiple instructions can be issued during the same clock cycle

Answer 2: Instructions cannot complete in different order in which they were issued F

Answer 3: The number of registers write required in a cycle can be greater than 1

SURE, IN CASE OF OVERLAPPED WRITES

Answer 4: Requires the introduction of additional pipeline registers

YES, TO ALLOW REPETITIONS

IMPORTANT THING IS TO PERFORM WB ON 1 CL

Problem 5

Design and describe (all the decisions have to be motivated) a 1-BHT and a 2-BHT able to execute the following assembly code.
(R0 is set to 100, R1 is set to 0)

R0=100 R1=0

```
LOOP:   LD      F3   0    R0
        ADDD    F1   F3   F3
        MULTD   F2   F3   F1
        ADDI    R1   R1   1000
LOOP2:  LD      F3   0    R1
        MULTD   F2   F2   F3
        SUBI    R1   R1   10
        BNEZ    R1   LOOP2
        SUBI    R0   R0   10
        BNE     R0   R1   LOOP
```

100 ITERATIONS

10 ITERATIONS

20 0

0 LAST

1-BHT NO COLLISION

```
LOOP:   LD      F3   0    R0
        ADDD    F1   F3   F3
        MULTD   F2   F3   F1
        ADDI    R1   R1   1000
LOOP2:  LD      F3   0    R1
        MULTD   F2   F2   F3
        SUBI    R1   R1   10
T       BNEZ    R1   LOOP2
        SUBI    R0   R0   10
T       BNE     R0   R1   LOOP
```

T→NT NT→T T→NT

1 + (1 + 1) · 9 + 1

= 20

2-BHT NO COLLISION

```
LOOP:   LD      F3   0    R0
        ADDD    F1   F3   F3
        MULTD   F2   F3   F1
        ADDI    R1   R1   1000
LOOP2:  LD      F3   0    R1
        MULTD   F2   F2   F3
        SUBI    R1   R1   10
T3      BNEZ    R1   LOOP2
        SUBI    R0   R0   10
T3      BNE     R0   R1   LOOP
```

$T_3 \to T_W$ $T_3 \to T_W$ LAST

1 · 10 + 1 = 11

```
LOOP:   LD      F3   0    R0
        ADDD    F1   F3   F3
        MULTD   F2   F3   F1
        ADDI    R1   R1   1000
LOOP2:  LD      F3   0    R1
        MULTD   F2   F2   F3
        SUBI    R1   R1   10
NT3     BNEZ    R1   LOOP2
        SUBI    R0   R0   10
NTW     BNE     R0   R1   LOOP
```

$NT_3 \to T$ $T_3 \to T_W$ $NT_3 \to T$ $T_3 \to T_W$

2 + 1 · 10 + 2 + 1 = 15

W.C. 2BHT > B.C. 1BHT ⇒ RESULT INLINE WITH THEORETICAL CHARACTERISTIC