



**POLITECNICO**  
**MILANO 1863**

**Embedded Systems (digital design)**

# Introduction

# Short bio - Prof. Davide Zoni, PhD

- **Current Position -**

- Assistant professor with tenure (RTDB), DEIB, Politecnico di Milano
- Contract professor, DIA, Università degli Studi di Parma
- Co-Founder @ Blue Signals, CEO @ Blue Signals

- **Research interests** - design and implementation of secure and efficient embedded systems with emphasis on low-power, crypto, hardware security, and machine learning

- **Visiting researcher (industry) -**

- arm ltd, Cambridge, UK, 2015
- IMEC (BE), STFC (UK)

- **Selected courses continuous training -**

- Advanced digital design IC Implementation, Europractice, 2022
- 4 courses targeting ASIC digital design using the Cadence Design Flow, Europractice, 2020-2022
- Verification with UVM, Europractice, 2019
- Comprehensive digital design IC Implementation and Sign-off, Europractice, 2018
- Essential verification with SystemVerilog and UVM, Europractice, 2017
- Digital Design with SystemVerilog, Europractice, 2015



- **Contacts**

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# **The digital design problem**

# The VLSI Evolution

## Very Large Scale Integrated (VLSI) Circuits

- Late 1970s: the process of creating an integrated circuit made of thousands of transistors into a single chip.
- The Moore's Law predict a double in the chip transistor count every 18months
  - Nowadays almost any reasonable complex digital design falls in the VLSI category

## INTegrated Electronics (Intel)

- 1968: founded by Moore and Noyce with a focus on memory chips
- 1971: Intel 4004, 4-bit datapath @ 108KHz. 2300 transistors @ 10um
- 1972: Intel 8008, 8-bit datapath. 3500 transistors
- 1974: intel 8080, 2MHz 6000 transistors @ 6um
- ...

## Technology Libraries

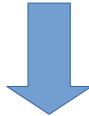
- Full Custom Cells
  - Huge effort to design the ad-hoc cells for each design
- Semi-Custom Cells
- Standard Cells
  - Design the technology library once, then move the optimization effort to the circuit design stage up to the place&route

# The need for a better HW description methodology

## CURRENT STATUS:

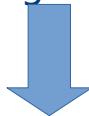
The increase in the transistor count in the same chip allows for:

- More functionalities
- More complex functions



## ISSUES:

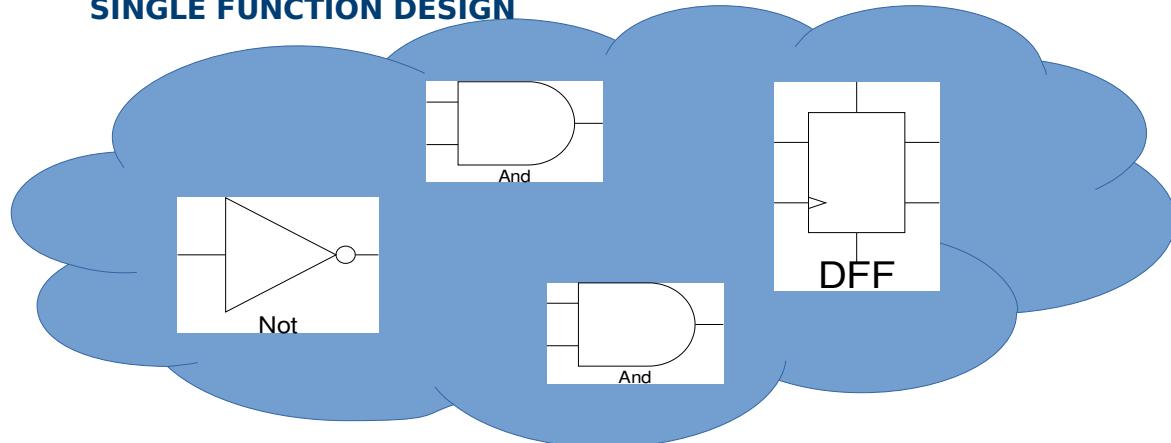
- The gate level design optimization (handmade) is not practical anymore
- (Possibly) design a custom cell for each gate of the design is not viable anymore



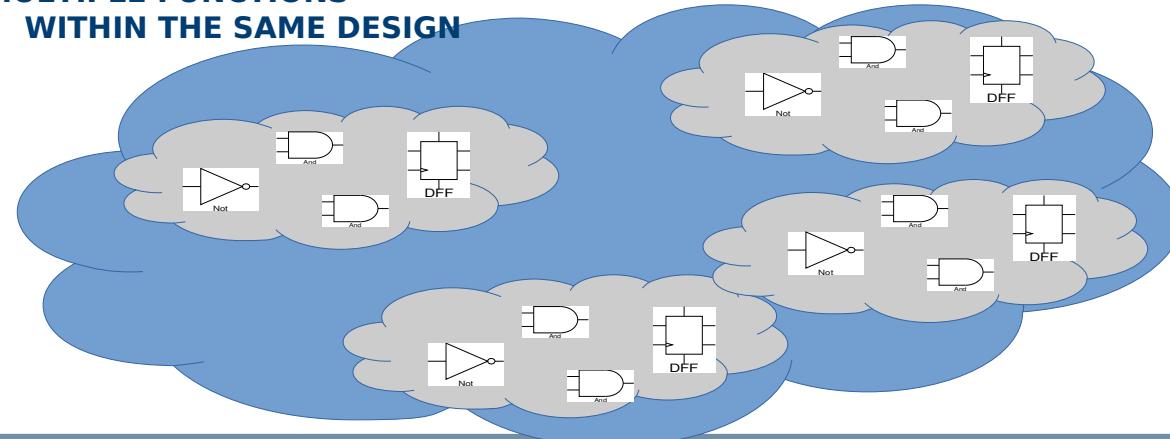
## NEW REQUIREMENTS:

- A flexible, scalable and maintainable way to describe the hardware, also easing the optimization design stage
- Possibly a verification language support can be a [huge] advantage

## SINGLE FUNCTION DESIGN



## MULTIPLE FUNCTIONS WITHIN THE SAME DESIGN

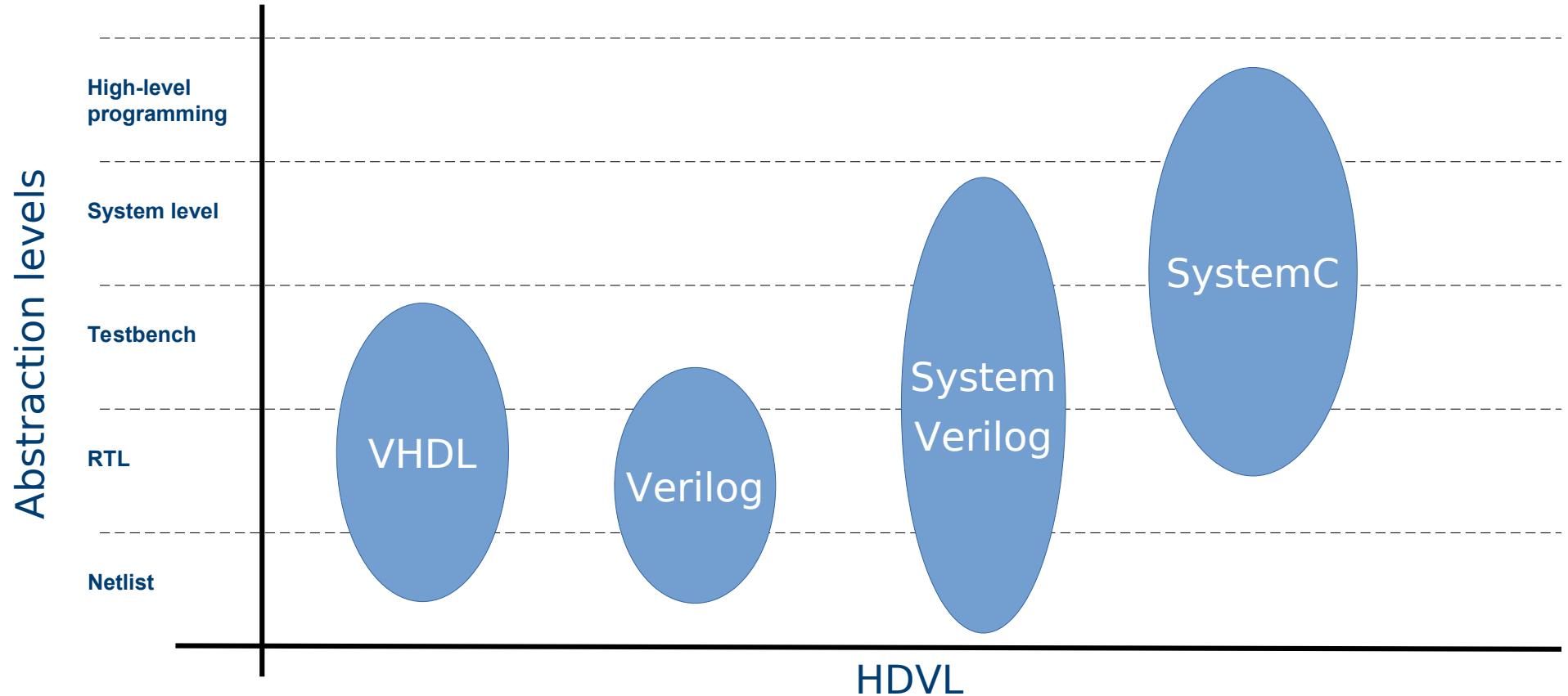


# SystemVerilog and VHDL: Dawn and Evolution

**WHY HDLs ? Hardware description language (HDL) is a device-independent representation of digital logic**

- **SystemVerilog is a hardware description (and verification) language**
  - Actually it is more than this, while we focus on a subset of the entire specification.
    - Keep an eye on the complexity
    - We explore the widely used parts, that allows the design up to a complete SoC
- **The History of Verilog:**
  - 1983: Gateway Design Automation invented Verilog
  - 1990: Cadence bought Verilog. Transferred into the public domain and became a standard IEEE STD. 1364-1995 aka Verilog-95
  - Later versions:
    - **Verilog 2001**
    - SystemVerilog/Verilog 2005, SystemVerilog 2008, **SystemVerilog 2012**, SystemVerilog 2018
- **VHDL (VHSIC Hardware Description Language)**
  - Published in 1987 with Dept. of Defence support as IEEE STD. 1076-1987
  - Later Versions: 1987, 1993, 2000, 2002, 2008, 2012, 2019
- **Verilog and VHDL share the same HDL opportunities**
  - Verilog is C-like
  - VHDL is Ada-like

# Abstract levels of Hardware Description and Verification Languages (HDVLs)

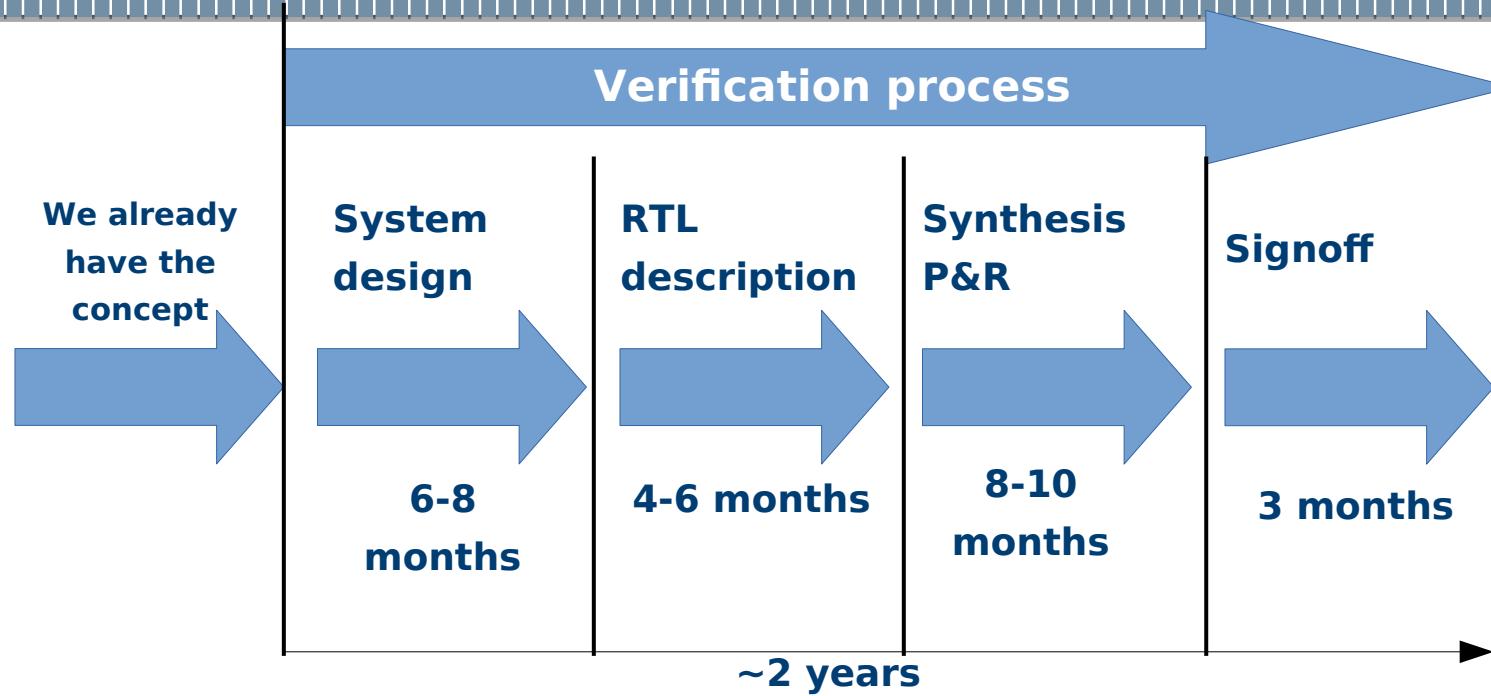


Source: IMEC, 2017

# Why digital design and verification?

- Why HDL (SV and VHDL)?
  - Why RTL design?
  - Why functional verification?
- Why using verification methodologies?

# Digital design and functional verification



## What is covered in this course?

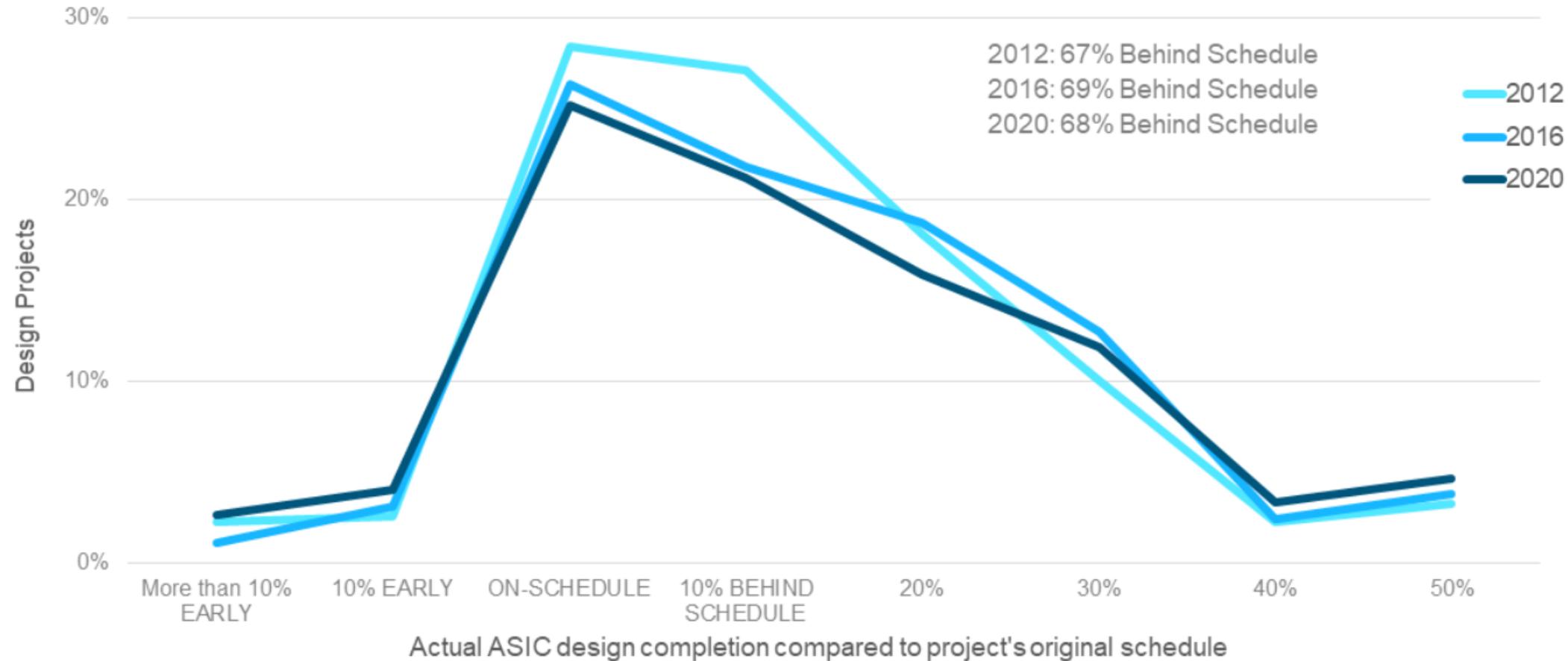
- Functional verification (RTL / Synthesis level)\*
  - Digital design at RTL level\*

\* SystemVerilog will be the reference HDVL

## **Time spent by engineers (and why)**

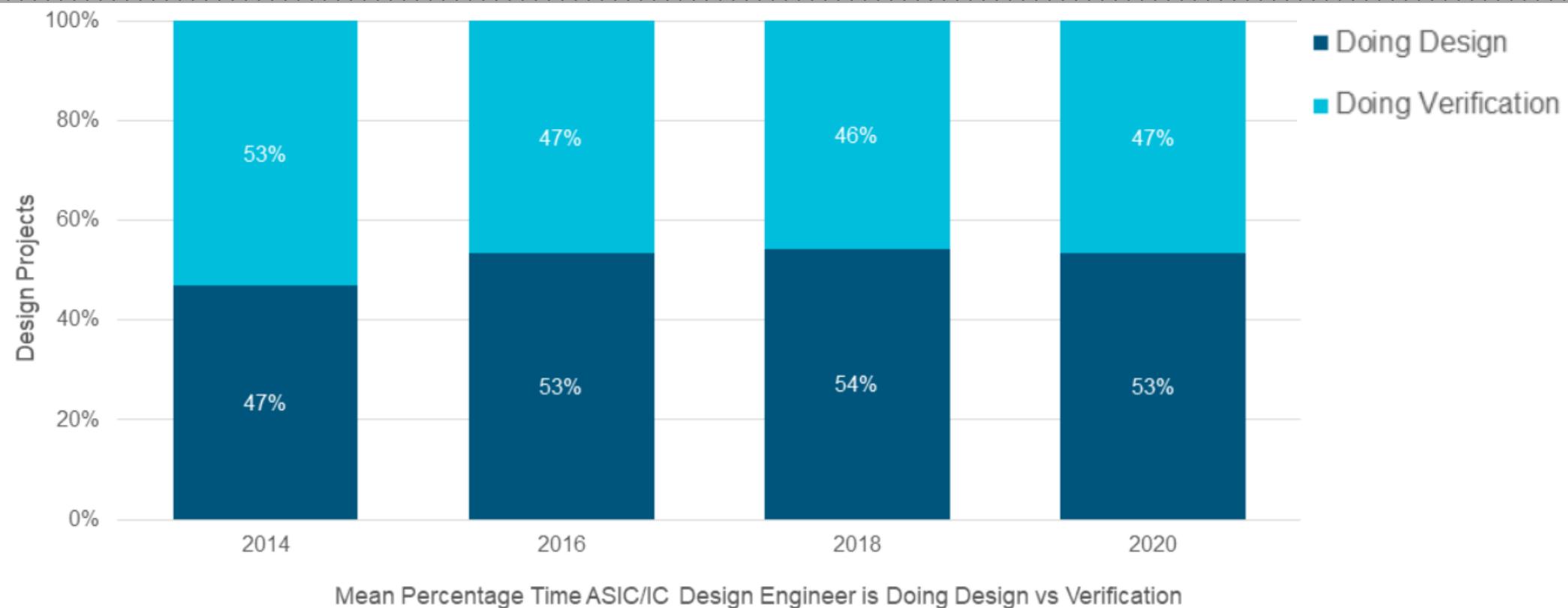
**- Design vs Verification -**

# ASIC project completion w.r.t. the original schedule



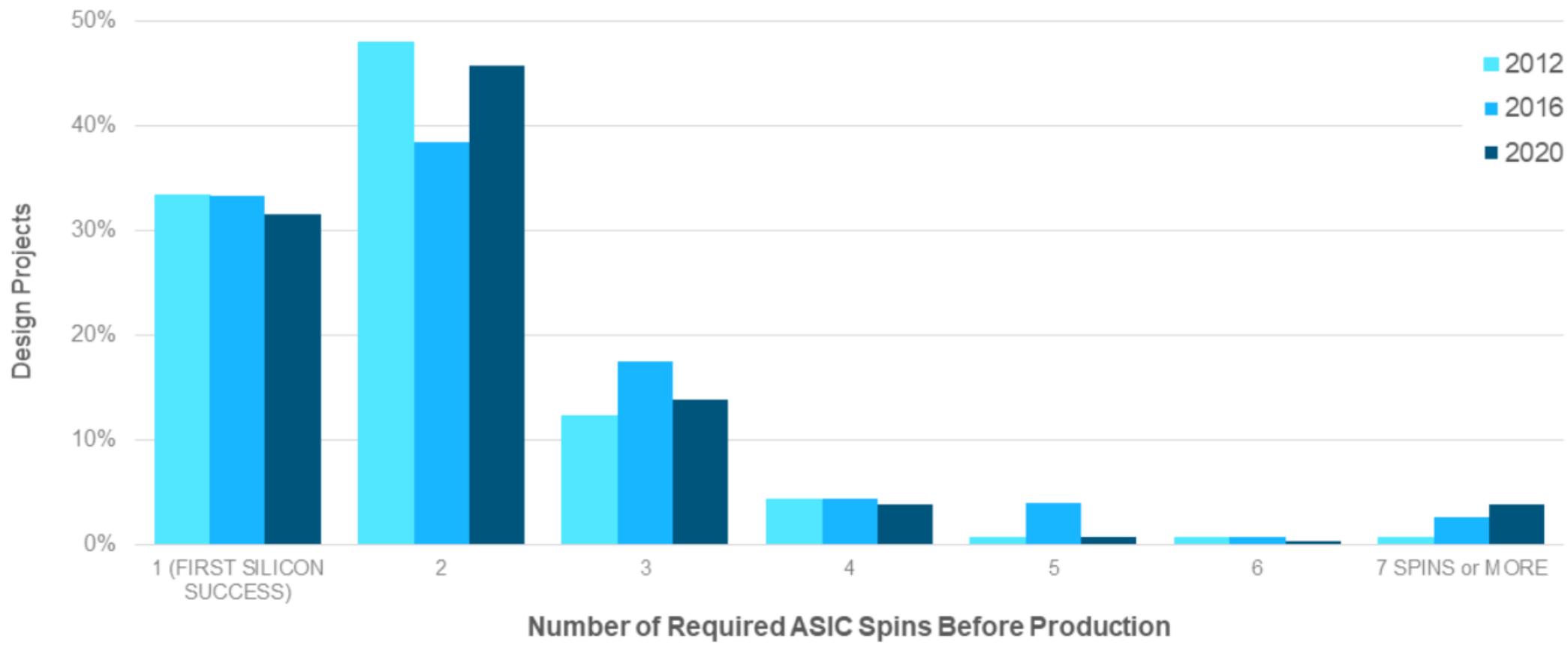
Source: WilsonResearchGroup and Mentor. A Siemens Business, 2020 Functional Verification Study

# Mean Time spent for ASIC/IC design vs verification



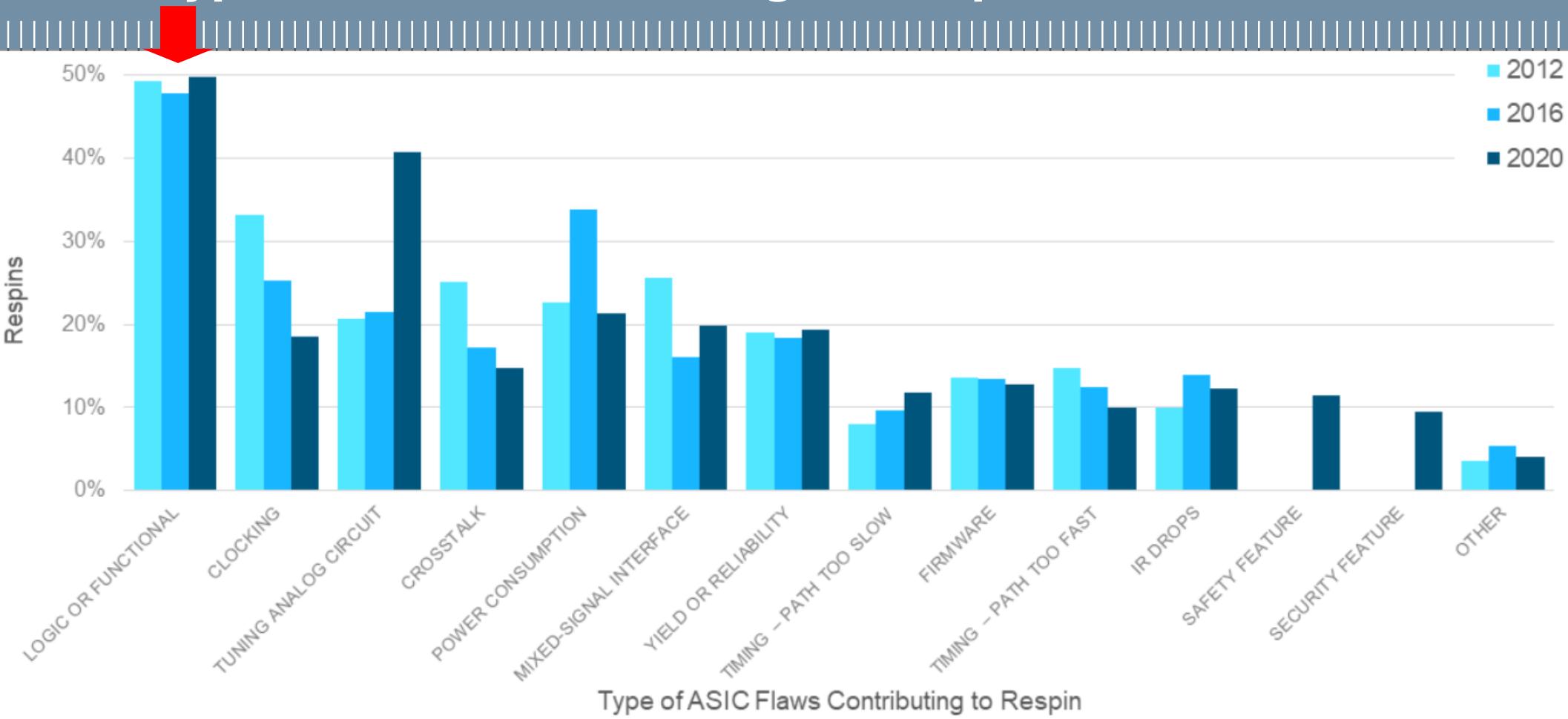
Source: WilsonResearchGroup and Mentor. A Siemens Business, 2020 Functional Verification Study

# ASIC number of required spins before production



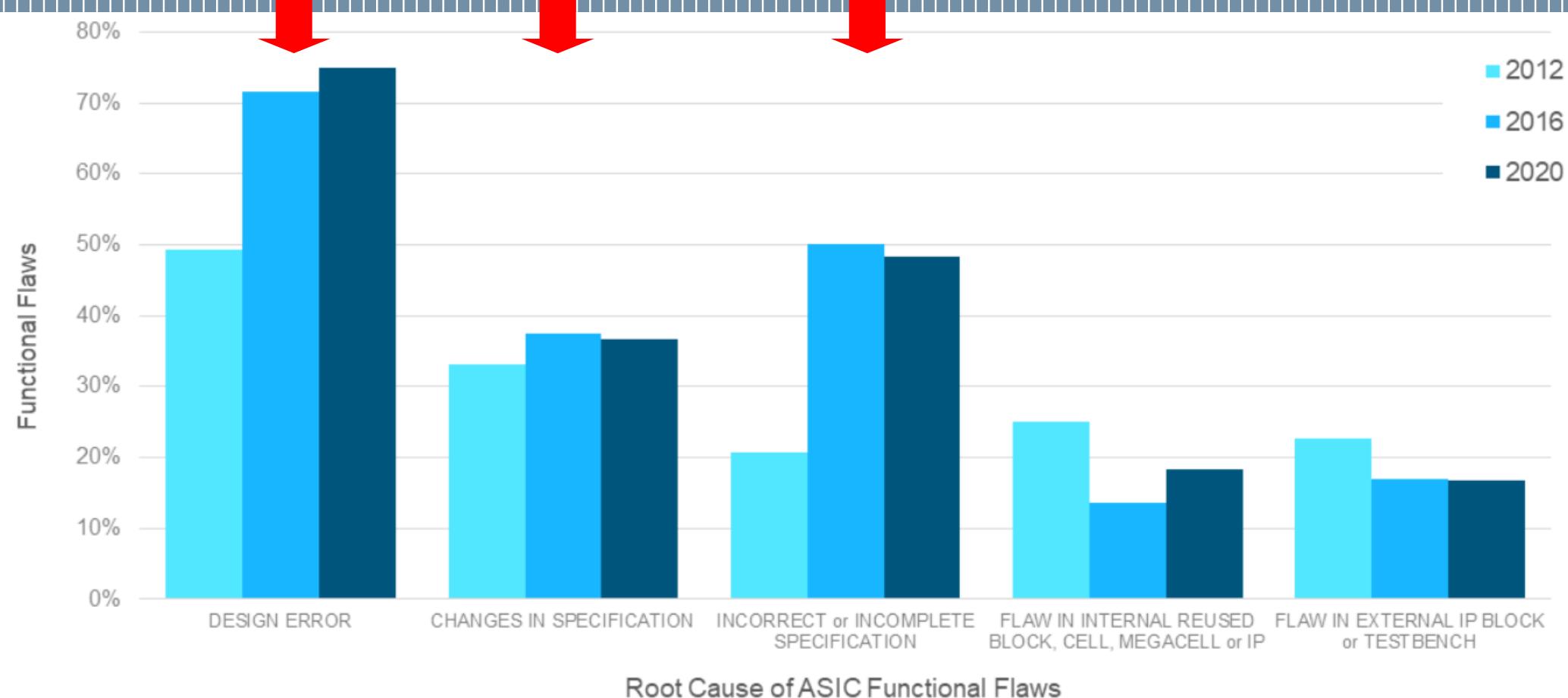
Source: WilsonResearchGroup and Mentor. A Siemens Business, 2020 Functional Verification Study

# ASIC type of flaws contributing to re-spin



Source: WilsonResearchGroup and Mentor. A Siemens Business, 2020 Functional Verification Study

# Root causes of ASIC functional flaws

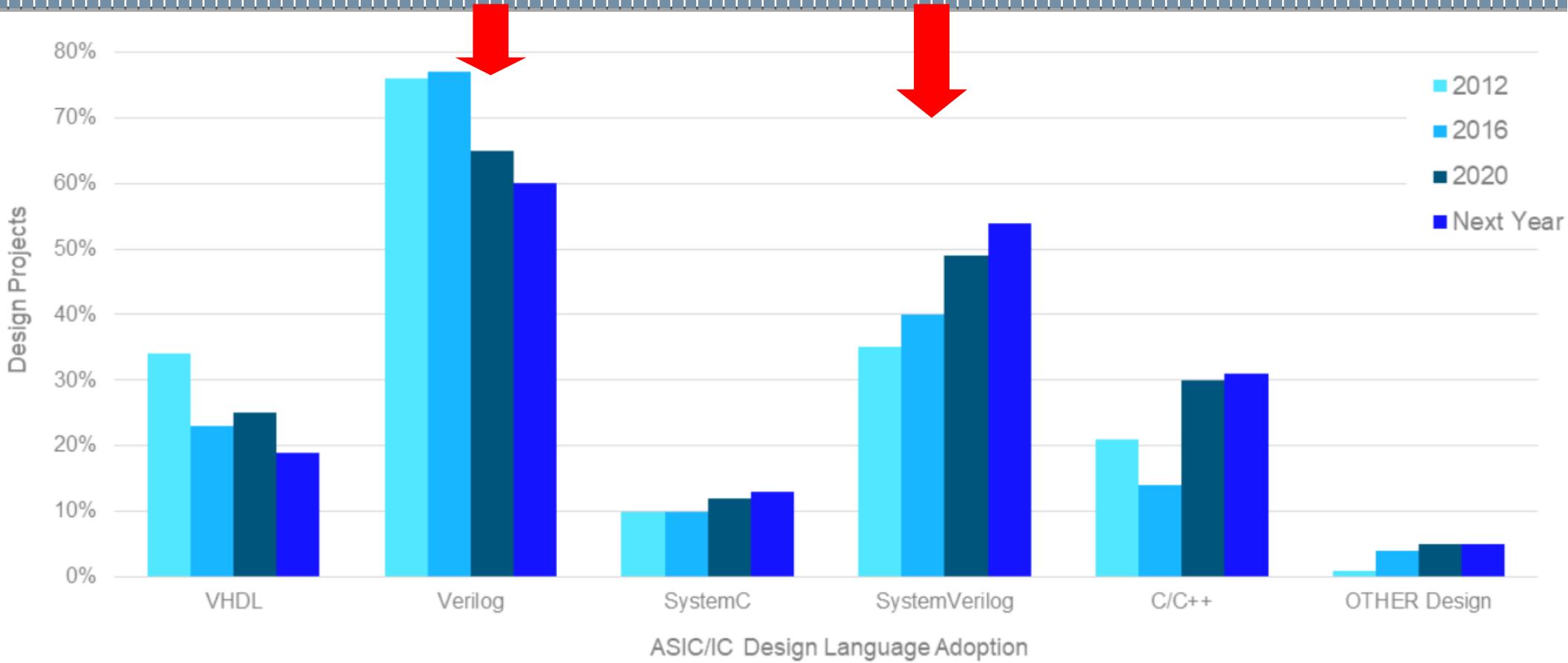


Source: WilsonResearchGroup and Mentor. A Siemens Business, 2020 Functional Verification Study

## **ASIC design and verification**

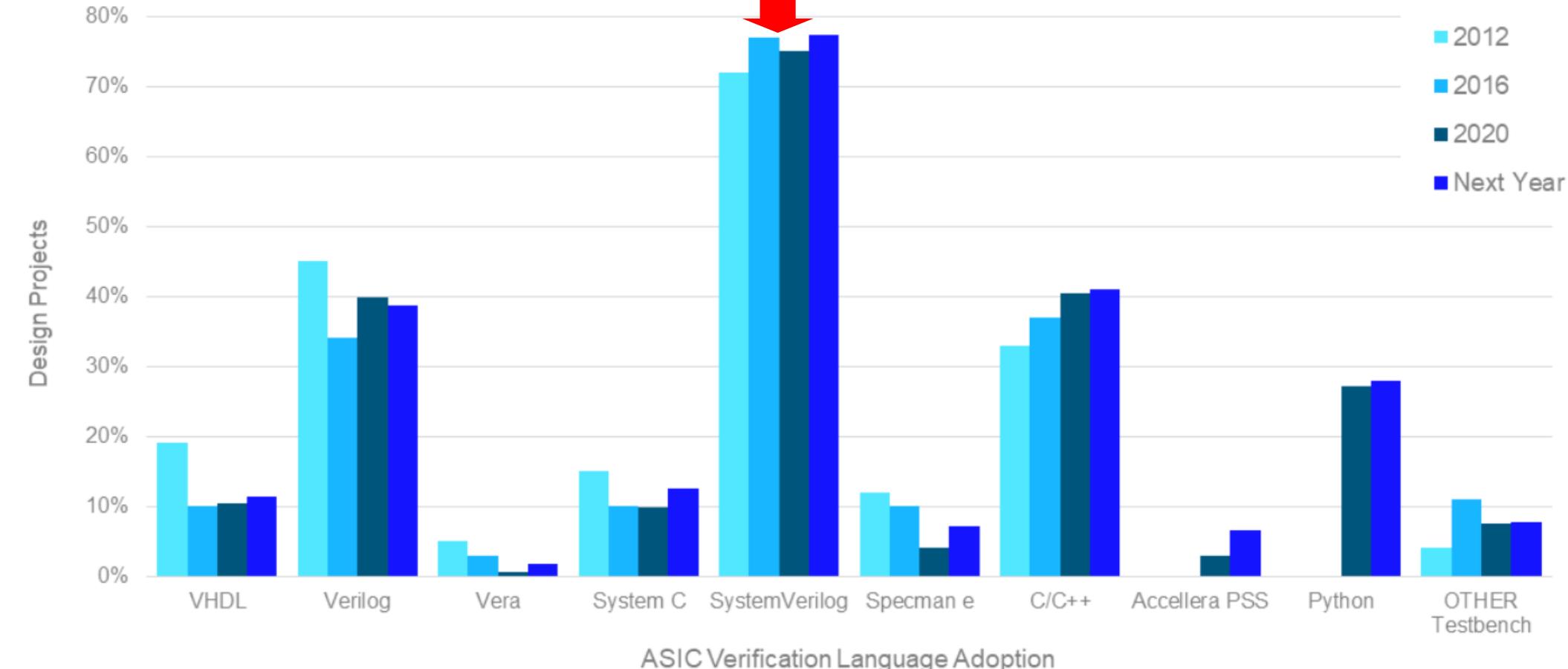
- (1) languages and (2) methodologies -

# ASIC Design Language Adoption Next 12 Months



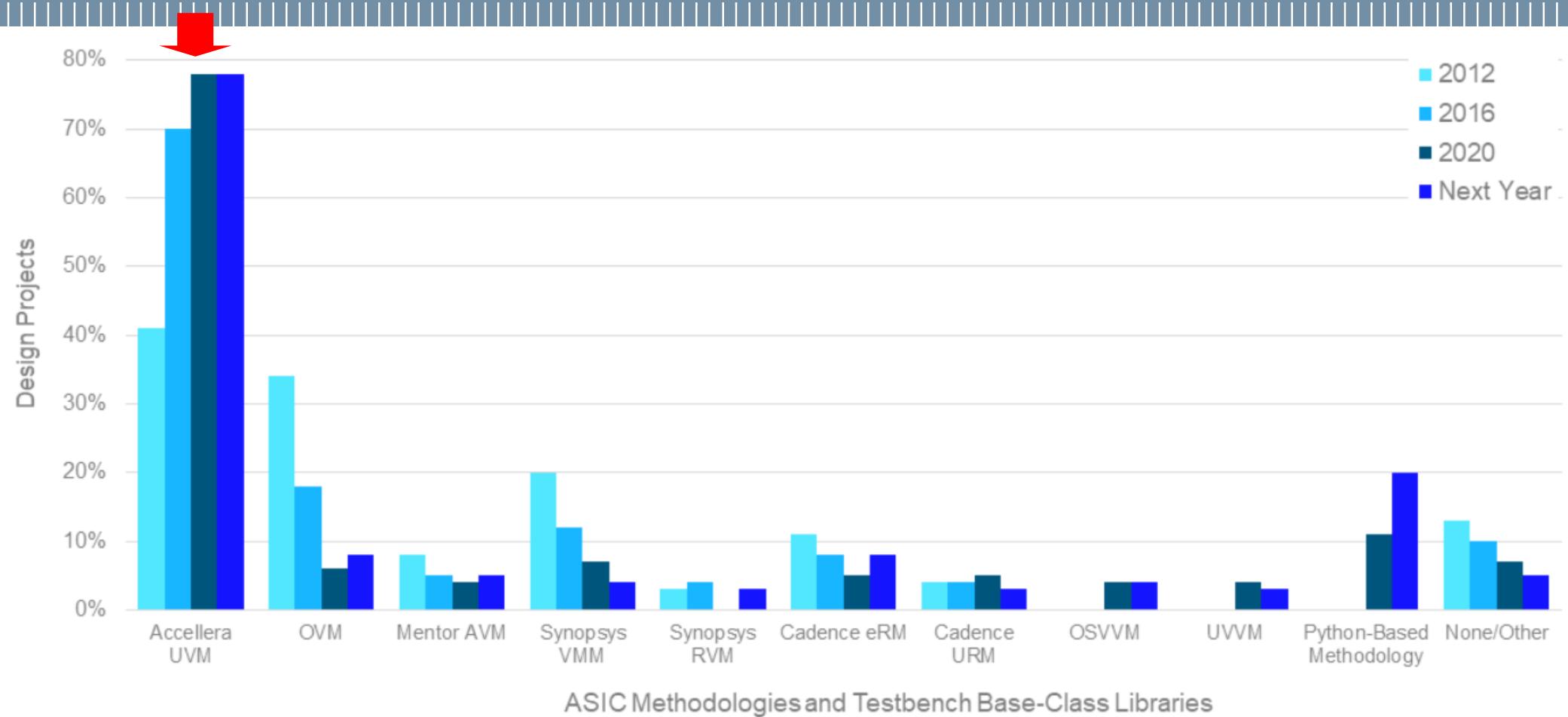
Source: WilsonResearchGroup and Mentor. A Siemens Business, 2020 Functional Verification Study

# ASIC Verification Language Adoption Next 12 Months



Source: WilsonResearchGroup and Mentor. A Siemens Business, 2020 Functional Verification Study

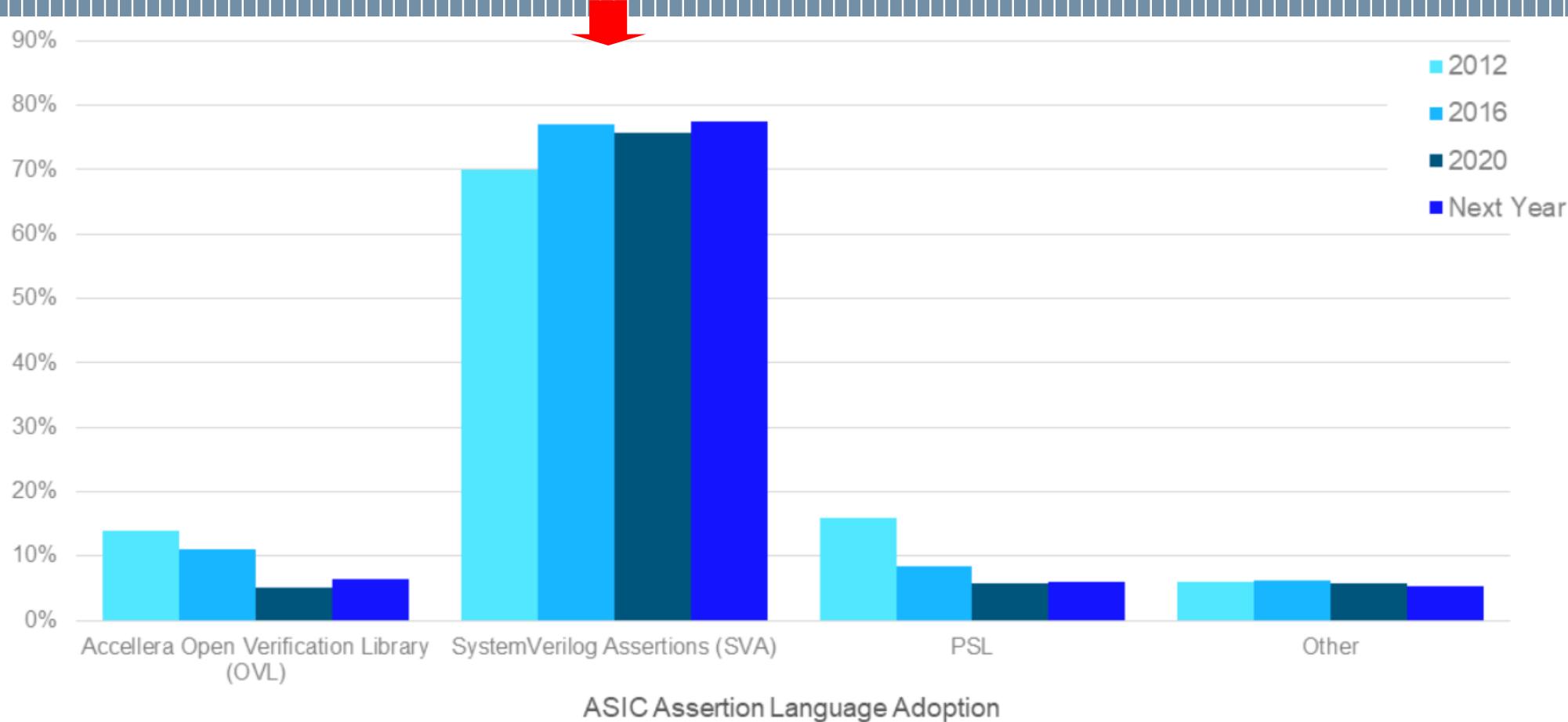
# ASIC Testbench Methodology Class Library Adoption Trends



ASIC Methodologies and Testbench Base-Class Libraries

Source: WilsonResearchGroup and Mentor. A Siemens Business, 2020 Functional Verification Study

# ASIC Assertion Language Adoption Next 12 Months



Source: WilsonResearchGroup and Mentor. A Siemens Business, 2020 Functional Verification Study

## **Structure of this part/classes**

– Which topics are we going to explore? –

# Lectures: 20 hours (2h/slot) + selected labs (20) for MSc studs

**Why participate** - overview on design and verification methodologies of digital systems using SV

**Objective - (1) faster design, (2) reusable components, (3) less errors:**

- **Design** - design, analyze, optimize, and extend complex digital systems
- **Design/Verification** - In-depth understanding of the simulation model
- **Verification** - create their own verification scenarios, and implement it in an effective and reusable way

**Xilinx toolchain**

- Xilinx Vivado

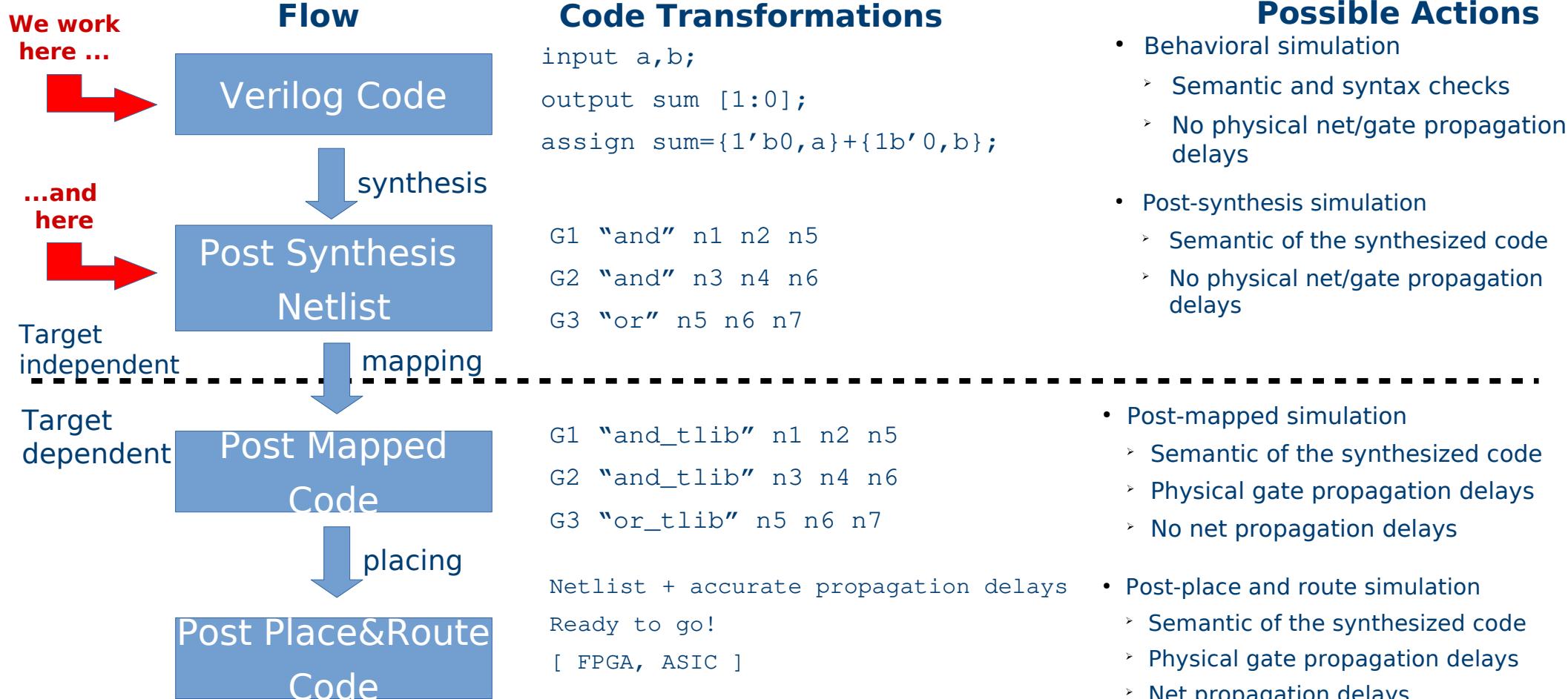
**Prerequisites and expected audience -**

- Familiar with VHDL or Verilog AND overview on object-oriented programming in C++ or Java
- The course is meant for **(1)** students willing to explore the design of digital systems, **(2)** for students with analog background willing to integrate digital design skills

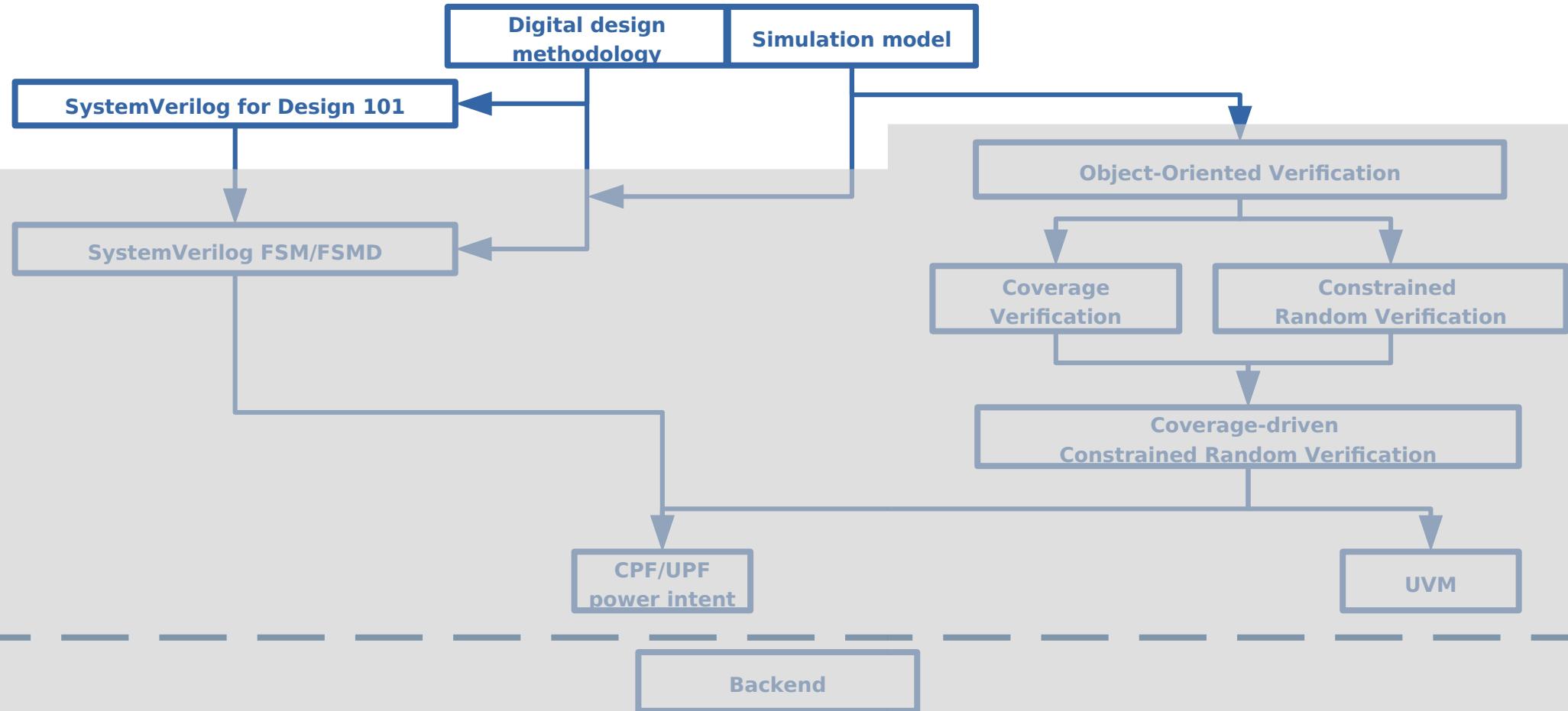
**When**

- Wednesdays and Thursdays 12.30pm - 2.15pm (from October 27, 2022 - to November 30, 2022)
- For any update - check-out the agenda of the course on WeBeep

# The (Simplified) Hardware Design Flow



# Digital design and verification - front-end flow



# SystemVerilog: pros and cons

## Pros

- SV is Object Oriented Language (OOP)
- Highly reusable and highly adopted infrastructures (UVM)
- SV can coexist with VHDL and Verilog
- DPI integration to use C-implemented golden models
- IEEE standard: all simulators support it in the same way
- Superset of Verilog: easy to follow for Verilog users

## Cons

- Too much to learn
  - we are going to cover a selected subset of features to make you productive
- Partly taking us to the software world: is that good for hardware people :P ?
- SV itself is not the solution: SV is just a tool. You always need to make the verification plan

# **Projects and Msc thesis (digital design)**

## We propose few projects related to digital design topics

### 1. Be aware!! - projects on digital design topics are not simple

- Especially if you just want to take the project and not the thesis
- Each project is a spin-off of a thesis

### 2. A student taking a project is strongly suggested to continue with the MSc thesis

- Additional training with hands-on and advanced lab sessions (20h)

### 3. You can find a list of the available topics for the projects/thesis <https://zoni.faculty.polimi.it>

- Find the link "**A list of available MSc theses [here]**"
- If you find a topic of interest we can discuss to frame a project
- The digital design projects give up to 10 points (added to the score of the written test with prof Fornaciari)