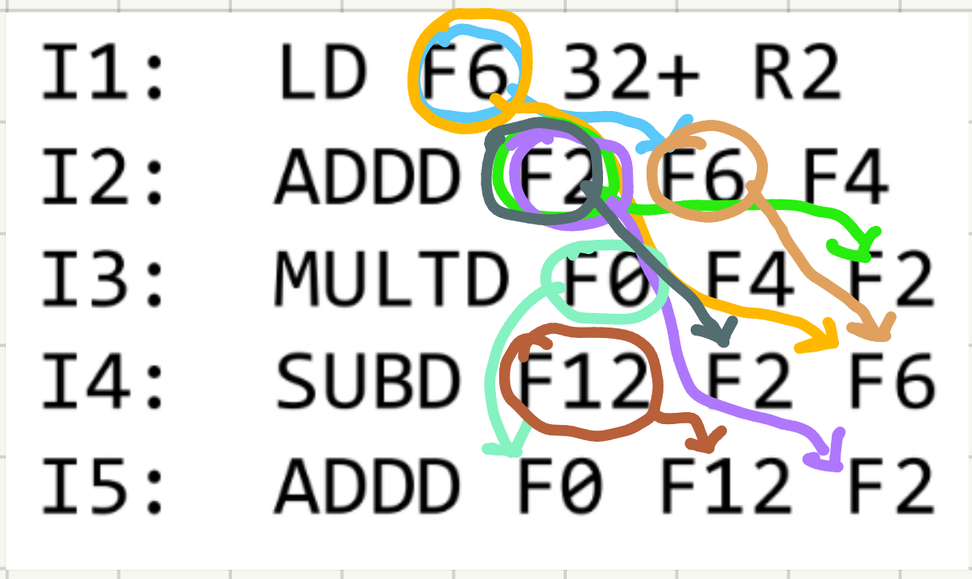
Exe 3 Scoreboard: the Code

```
I1:  LD F6 32+ R2
I2:  ADDD F2 F6 F4
I3:  MULTD F0 F4 F2
I4:  SUBD F12 F2 F6
I5:  ADDD F0 F12 F2
```

CONFLICTS



RAW F6 I1→I2

RAW F6 I1→I4

RAW F2 I2→I4

RAW F2 I2→I3

RAW F2 I2→I5

RAW F12 I4→I5

WAW F0 I3→I5

Exe 3.3 Scoreboard: CC 0

	Instruction	ISSUE	READ OPERAND	EXE COMPLETE	WB	Hazards	Unit
I1	LD F6 32+ R2						
I2	ADDD F2 F6 F4						
I3	MULTD F0 F4 F2						
I4	SUBD F12 F2 F6						
I5	ADDD F0 F12 F2						

F0	F2	F4	F6	F8	F10	F12	…	F30
P0	P2	P4	P6	P8	P10	P12	…	P30

Initialized Rename Table – registers from P32 in the free list

4 FPALU 3 cc latency, single write port for the pool
1 MEM 2 cc latency

Exe 3.3 Scoreboard:

	Instruction	ISSUE	READ OPERAND	EXE COMPLETE	WB	Hazards	Unit
I1	LD F6 32+ R2	1	2	4	5		M.U.
I2	ADDD F2 F6 F4	2	5+1=6	9	10	RAW F6 I1-I2	FP.U.1
I3	MULTD F0 F4 F2	3	11	14	15	RAW F2 I2-I3	FP.U.2
I4	SUBD F12 F2 F6	4	11	14	16	RAW F6 I1-I4 RAW F2 I2-I4	FP.U.3
I5	ADDD F0 F12 F2	5	17	20	21	WAW F0 I3-I5 RAW F12 I4-I5 STRUCT RF	FP.U.4

F0	F2	F4	F6	F8	F10	F12	…	F30
P0	P2	P4	P6	P8	P10	P12	…	P30

P34 P36 P33 P32 P35

Exe 4 Tomasulo with ROB: the Code

```
LOOP:I1: MULTD F2, F6, F8
     I2: ADDD F0, F6, F4
     I3: MULTD F10, F0, F2
     I4: ADDD F0, F12, F14
     I5: SUBI R0, R0, 4
     I6: BNEZ R0, LOOP
```

CONFLICTS

```
LOOP:I1:  MULTD F2, F6, F8
     I2:  ADDD F0, F6, F4
     I3:  MULTD F10, F0, F2
     I4:  ADDD F0, F12, F14
     I5:  SUBI R0, R0, 4
     I6:  BNEZ R0, LOOP
```

RAW F2 I1→I3

RAW F0 I2→I3

WAW F0 I2→I4

WAR F0 I3→I4

RAW R0 I5→I6

Exe.4 Tomasulo with ROB

- 3 RESERVATION STATIONS (RS1, RS2, RS3) + 3 MULT unit (MULT1,MULT2, MULT3) with latency 4
- 3 RESERVATION STATIONS (RS4, RS5, RS6) + 3 ADDD/SUBD (ADDD1, ADDD2, ADDD3) with latency 2
- 7-slot ROB
- Enough RS and FUs for integer operations, and separated CDB

To be clear, will show when the SUBI and BNEZ are issued

In the case of hazard on CDB, the oldest instruction has priority

Let's assume that we discover the BNEZ misprediction 5 clock cycles after the issue

Exe Tomasulo with ROB CC0

- 3 RESERVATION STATIONS (RS1, RS2, RS3) + 3 MULT unit (MULT1,MULT2, MULT3) with latency 4
- 3 RESERVATION STATIONS (RS4,RS5, RS6) + 3 ADDD/SUBD (ADDD1, ADDD2, ADDD3) with latency 2
- 7-slot ROB

Instruction	ISSUE	START EXE	WB	Commit	ROB idx	Hazards Type	RSi	Unit
It.1: MULTD F2, F6, F8								
It.1: ADDD F0, F6, F4								
It.1: MULTD F10, F0, F2								
It.1: ADDD F0, F12, F14								
It.2: MULTD F2, F6, F8								
It.2: ADDD F0, F6, F4								
It.2: MULTD F10, F0, F2								
It.2: ADDD F0, F12, F14								

Exe Tomasulo with ROB

- 3 RESERVATION STATIONS (RS1, RS2, RS3) + 3 MULT unit (MULT1,MULT2, MULT3) with latency 4
- 3 RESERVATION STATIONS (RS4,RS5, RS6) + 3 ADDD/SUBD (ADDD1, ADDD2, ADDD3) with latency 2
- 7-slot ROB

max(WB1, WB2)

Instruction	ISSUE	START EXE	WB	Commit	ROB idx	Hazards Type	RSi	Unit
It.1: MULTD F2, F6, F8	1	2	6*	7	0		RS1	MULT1
It.1: ADDD F0, F6, F4	2	3	5	8	1		RS4	ADDD1
It.1: MULTD F10, F0, F2	3	7	11	12	2	RAW F2 11-13 RAW F0 14-13	RS2	MULT2
It.1: ADDD F0, F12, F14	4	5	7		3		RS5	ADDD2
It.2: MULTD F2, F6, F8	6 t1=7	8			6		RS1	MULT1
It.2: ADDD F0, F6, F4	8	9	0		0	STRUCT CDB	RS4	ADDD1
It.2: MULTD F10, F0, F2	9				1		RS3	
It.2: ADDD F0, F12, F14						INSUFFICIENT ROB SLOTS STRUCT ROB		