UNIVERSITY OF GHANA

FACULTY OF ENGINEERING SCIENCES
FIRST SEMESTER EXAMINATIONS: 2012/2013
LEVEL 300: BACHELOR OF SCIENCE IN ENGINEERING

CPEN 303: Introduction to Computer Architecture [*3 Credits*]
TIME: 3 HOURS

INSTRUCTION: Attempt all questions

Question 1(40 marks)

a) Enumerate the three types of data dependencies in computer architecture and give an example for each. **[8 marks]**

b) State any three design specifications for memory in computer architecture with reasonable explanations. **[8 marks]**

c) Why is low power consumption important in computer architecture? Mention two (2) main approaches of reducing power consumption?**[4 marks]**

d) State the relationship between **Processor Performance** and **Instruction Per Cycle (IPC),Frequency,** and **Instruction Count.** Discuss how the performance could be improved as well as any limitations or challenges. **[8 marks]**

e) State the unique characteristics of RISC architecture that are being exploited in the current development of computer architecture. **[4 marks]**

f) State and explain briefly the three main differences between multi-computers and multiprocessors. **[8 marks]**

Question 2 (30 marks)

a. Formulate a four segment instruction pipeline for a computer. Specify and explain the operation to be performed in each segment. **[6 marks]**

b. Using 8-bit 2's complement representation of negative numbers, perform the following computations:
   (i) - 35 + (-11)
   (ii) 19 - (- 4) **[4 marks]**

c. What is a virtual memory? State briefly how it can be implemented **[4 marks]**

d. What are the main characteristics of the two mapping algorithms for cache memories: ***direct*** and ***associative***? Support your answer with diagrams. **[4 marks]**

e. What are the main characteristics of RISC architecture? **[4 marks]**

f. What is the purpose of instruction pipelining? How does a pipelined unit work?**[4marks]**

g. Why is the memory system of a computer organized as a hierarchy? **[4 marks]**

Question 3(27 marks)

(a) State Amdahl's law. **[2 marks]**

(b) Consider a machine for which a speedup of 30 is possible after applying an enhancement. If under certain conditions, the enhancement was only possible for 30% of the time, what is the speedup due to this partial application enhancement?**[3 marks]**

(c) Three enhancements with the following speedups are proposed for a new machine: Speedup (a) = 30, Speedup (b) = 20, and Speedup (c) = 15. Assume that for some set of programs, the fraction of use is 25% for enhancement (a), 30% for enhancement (b), and 45% for enhancement (c). If only one enhancement can be implemented, which should be chosen to maximize the speedup? If two enhancements can be implemented, which should be chosen, to maximize the speedup?**[6 marks]**

(d) A Pentium 4 system processor has two-level cache organization. The level L1 represents an 8KB data cache which is organized as a four-way set associative manner with a block size of 64bytes and the number of blocks per set as four. The advanced transfer cache L2 has a size of 256KB and it is organized as an eight-way set associative with 128-byte block size. The main memory size is 16MB.

(i) Sketch the system diagram indicating the memory interface. **[4 marks]**

(ii) Find the number of address lines that will be needed to address the main memory and the number of main memory blocks. **[4 marks]**

(iii) Find the length of the three fields of the main memory address. **[4 marks]**

(iv) Find the average access time of the system if the access times of the L1, L2, and main memory are 20ns, 100ns, and 1ms, respectively. Assume that the L1 cache has a hit ratio of 90% and the L2 hit ratio is 95%. **[4 marks]**

Question 4(23 marks)

(e) Consider having a program that runs in 50 s on computer A, which has a 500 MHz clock. We would like to run the same program on another machine, B, in 20 s. If machine B requires 2.5 times as many clock cycles as machine A for the same program, what clock rate must machine B have in MHz? **[6 marks]**

(f) Suppose that we have two implementations of the same instruction set architecture. Machine A has a clock cycle time of 50 ns and a CPI of 4.0 for some program and machine B has a clock cycle of 65 ns and a CPI of 2.5 for the same program. Which machine is faster and by how much?**[7 marks]**

(g) A compiler designer is trying to decide between two code sequences for a particular machine. The hardware designers have supplied the following facts:

Instruction Class	CPI of the Instruction Class
A	1
B	3
C	4

For a high level, the compiler writer is considering two sequences that require the following instruction sets

Code sequence	Instruction count in Millions		
	A	B	C
1	2	1	2
2	4	3	1

What is the CPI for each sequence? Which code sequence is faster? By how much? **[10 marks]**