



UNIVERSITY OF GHANA

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SCHOOL OF ENGINEERING SCIENCES
SECOND SEMESTER EXAMINATIONS: 2016/2017
LEVEL300: BACHELOR OF SCIENCE IN ENGINEERING
CPEN 302: COMPUTER SYSTEMS ENGINEERING [3 CREDITS]

TIME ALLOWED: 2 HOURS 30 MINUTES

INSTRUCTIONS:

ATTEMPT ALL QUESTIONS. [100 MARKS]

All abbreviations have their usual meaning.

1

- a. Explain two (2) detrimental effects caused by cross-talk in a multi-conductor system [4 marks]
- b. Assume the two-conductor system shown in the Figure 1, where $Z_o \approx 70 \Omega$, the termination resistor $R_T = 70 \Omega$, $V(\text{input}) = 1.0 \text{ V}$, Transmission rate $T_r = 100 \text{ ps}$, and the cable length $x = 2 \text{ inches}$. Determine the near- and far-end crosstalk magnitudes assuming the following capacitance and inductance matrices: [6 marks]

$$L(\text{in.}) = \begin{bmatrix} 9.869 \text{ nH} & 2.103 \text{ nH} \\ 2.103 \text{ nH} & 9.869 \text{ nH} \end{bmatrix}$$

$$C(\text{in.}) = \begin{bmatrix} 2.051 \text{ pF} & 0.239 \text{ pF} \\ 0.239 \text{ pF} & 2.051 \text{ pF} \end{bmatrix}$$

Note:

$$V(1) = \frac{V(\text{input})}{4} \cdot \left(\frac{L_{12}}{L} - \frac{C_{12}}{C} \right)$$

$$V(2) = \frac{V(\text{input}) \cdot x \cdot \sqrt{LC}}{2T_r} \cdot \left(\frac{L_{12}}{L} - \frac{C_{12}}{C} \right)$$

- c. Consider the same two-conductor system. If $R_1 = 45$ and $R_2 = 100 \Omega$, what are the respective near- and far-end crosstalk voltages? [6 marks]

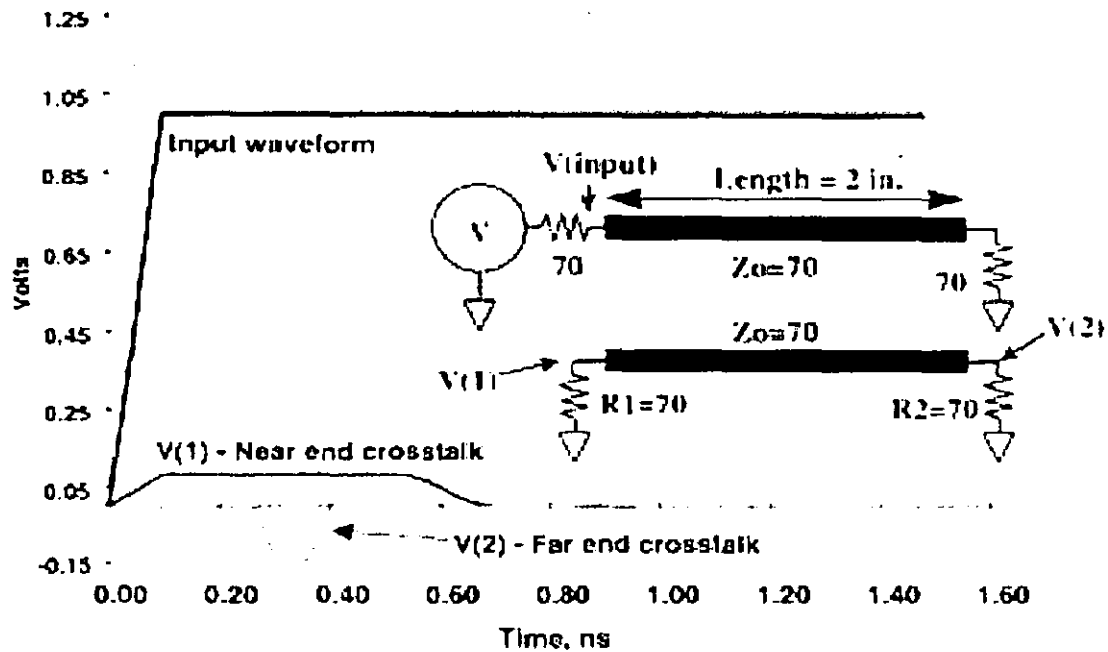


Figure 1: Proposed network for a two-conductor system

- d. Outline three (3) guidelines that can help reduce the effects of cross-talk during the design stage. [3 marks]
- e. Explain the following types of noise encountered in digital systems:
- i. Intersymbol interference [2 marks]
 - ii. Timing noise [2 marks]

2

For a transmission line geometry similar to the one provided in Figure 2, consider the following parameters: propagation velocity $v = 1.8 \times 10^8 \text{ m/s}$ and the time delay down the line connecting U1 and U2 is given as $TD = 1.42 \text{ ns}$.

- a. Calculate the steady state voltage V_{initial} , considering a source voltage of 2V, a source impedance of 75Ω and a line impedance of 50Ω . [2 marks]

- b. Calculate the source and load reflection coefficient considering that the line is terminated in open circuit. [4 marks]
- c. Sketch the lattice diagram and the response of the lattice diagram (V_{load} and V_{source} vs time) of this un-driven transmission line limited to the 5th reflection. [8 marks]

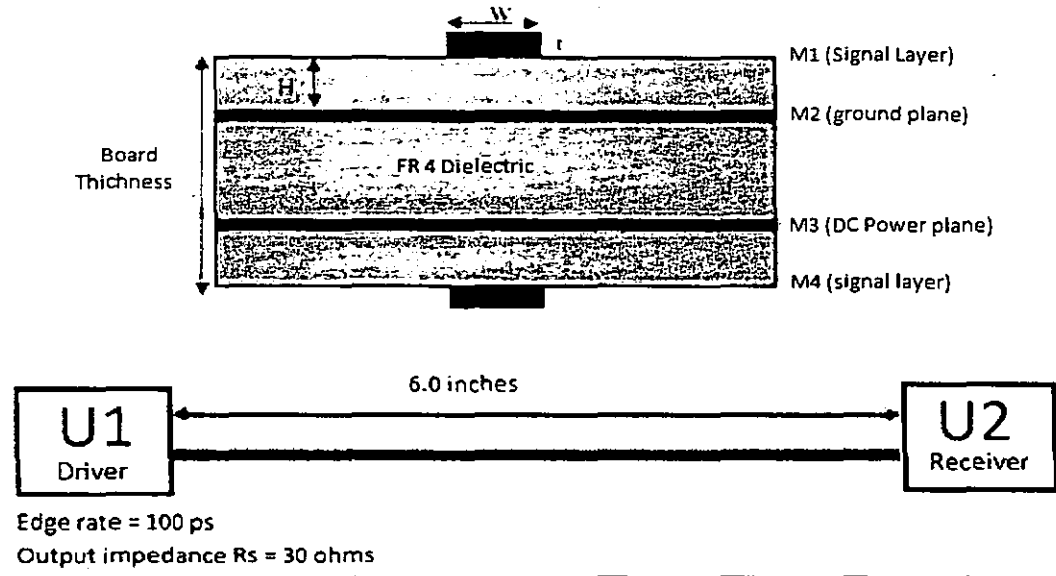


Figure 2: Sectional view of a standard four layer motherboard stackup

$$\epsilon_r = 4, t = 1, W = 0.6$$

3

- a. Differentiate between *microstrip* and *striplines*. [4 marks]
- b. With the help of Figure 3, show that the impedance of an infinite line is given by the equation [4 marks]

$$Z_0 = \left(\frac{R + Ls}{G + Cs} \right)^{1/2}$$

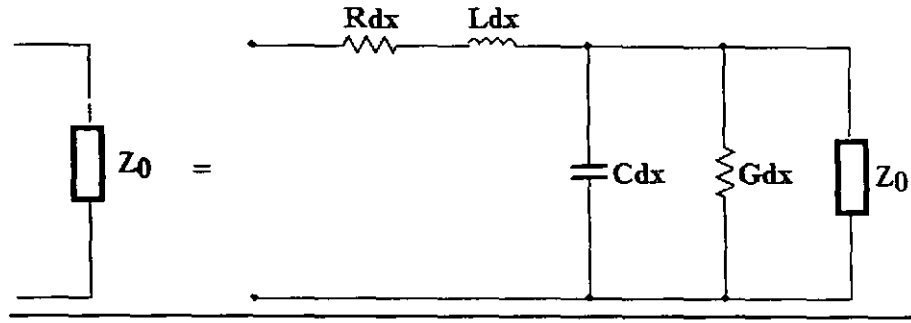


Figure 3: Model a differential section of a transmission line

- c. Considering the standard four layer motherboard stackup model depicted in Figure 2, determine the height H for a line impedance assuming $Z_0 = 50\Omega$,

Given that: $Z_{0_microstrip} = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln \left(\frac{5.98H}{0.8W + t} \right)$, $\epsilon_r = 4$, $t = 1$, and $W = 0.5$

[2 marks]

- d. Considering the value of H calculated in c.) and the formula provided below, evaluate the effective dielectric constant, the propagation velocity and the time delay

[5 marks]

$$\epsilon_e = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left(1 + \frac{12H}{W} \right)^{-1/2} + F - 0.217(\epsilon_r - 1) \frac{T}{\sqrt{WH}}$$

$$F = \begin{cases} 0.02(\epsilon_r - 1) \left(1 - \frac{W}{H} \right)^2 & \text{for } \frac{W}{H} < 1 \\ 0 & \text{for } \frac{W}{H} > 1 \end{cases}$$

4

- a. Explain four (4) system-level engineering issues encountered in digital systems. **[6 marks]**
- b. Describe a signaling convention and give two examples. **[4 marks]**

c. Describe timing convention and distinguish between synchronous and pipelined timing.

[4 marks]

d. Noise is a major concern in the engineering of digital systems that corrupts signals on channels between modules, disturbs the state of logic networks and memory cells, and adds jitter and skew to the timing of signals. Differentiate between jitter and skew.

[4 marks]