UNIVERSITY OF GHANA

BACHELOR OF SCIENCE IN ENGINEERING
SECOND SEMESTER EXAMINATIONS: 2014/2015
CPEN 402: ADVANCED COMPUTER ARCHITECTURE (3 Credits)

INSTRUCTIONS: *Answer all questions in Section A and Four (4) other questions in Section B.*

TIME ALLOWED: *THREE (3) HOURS*

SECTION A (40 Marks)

A1. Attempt all questions below.

a) List the three data dependencies that affect multi-processing of instruction by pipelining architecture. Which of these two are referred to as artificial dependencies? And why? [6 marks]

b) Briefly explain what is meant by the term 'windows of execution' in Superscalar Architectures. [4 marks]

c) State the dynamic power equation in the discussions of Computer architecture and explain the effect of any two of the parameters that contribute to power issues in architecture design [6 marks]

d) In the multiprocessor architecture, explain why **Dual core processor** will run far cooler than a **single core design** of equivalent performance running at double the clock speed. [4 marks]

e) Discuss any two schemes used in managing the RAM in Computers. [4 marks]

f) Explain why a Single embedded processors at clock frequencies of 1GHz and beyond are possible but not used in real architecture designs [4 marks]

g) Describe briefly by means of a diagram the main difference between **multiprocessor** and **multicomputer** design architecture and state two uses of each. [6 marks]

h) Show by means of a diagram how a pipeline execution with six instructions is executed by:

   i. A standard pipeline

ii. A super pipeline and

iii. A superscalar approach with the respective labels [6 marks]

SECTION B (60 Marks)

Answer any <u>Four (4)</u> Questions from this Section.

B1.

a) Explain why true data dependencies are intrinsic feature of the user's program. Can these dependencies be eliminated by either compiler or hardware techniques? Discuss and explain how they could be contained by means of illustrated instruction syntax [8 marks]

b) By means of a clearly labeled Memory Hierarchy diagram, discuss the strengths and limitations of the use of the various memory segments in the design and build of a personal computer. Pay attention to the use of various levels of caches and how these are implemented by different vendors. [7 marks]

B2. Consider the following program f: [10 marks]

```
program.f:
...
if CPU=a then
    low_limit=1
    upper_limit=50
elseif CPU=b then
    low_limit=51

upper_limit=100
end if
do  I  =  low_limit,
upper_limit
    work on A(I)
end do
...
end program
```

a) Show that this program could be executed by two CPUs in a parallel programing scenario by showing the programing outline in such a situation. Indicate the conditions that must be fulfilled for this to work.

b) Discuss briefly the use of parallel programming and indicate where these are useful. [5 marks]

B3.

a) Consider an architecture design employing a pipeline with **7** instructions each with execution time T_{ex}. They are executed by a **6**-stage pipeline. Pipeline overheads are ignored. How long does it take to execute the **7** instructions by the pipelined CPU? [make any suitable assumptions] Draw the figure. [7 marks]

b) In computer architecture, one popular classification divides the multiprocessor platform into symmetric multiprocessor (SMP) and asymmetric multiprocessor (AMP) systems. Explain in what situations each of these classifications is a better selection for a computer task. [8 marks]

B4.

a) Pollack's Rule states that the performance increase of a processor is roughly proportional to the square root of the increase in its complexity. Assume that the complexity is a function of the number of transistors denoted by **P(T)** and the performance of the increase in processor is denoted by **X(P).**

Prove that if the number of Transistors is **doubled**, the increase in the performance of the processor will be in the region of 40% and discuss the relevance of this mathematical observation to multi-processor computing architecture. [8 marks]

b) Name the three data dependencies that could be identified within the superscalar architecture and discuss their impact on computer architecture development by giving an example in each case. Which two of these three dependencies are referred to as artificial dependencies and why they are referred as such? [7 marks]

B5.

a) How much time would a program of ten thousand cycles be required to be completed if it were run on a **RISC** and **CISC** based computer architecture given the following parameters of information below. [6 marks]

i. Assume that **80%** of the instructions being executed are simple and **20%** complex.

ii. On a CISC machine simple instructions take **4 cycles**, complex instructions take **8 cycles**; cycle time is **100 ns** (10^{-7} **s**).

iii. On a RISC machine simple instructions are executed in **one cycle**; complex operations are implemented as a sequence of instructions; we consider on average **14 instructions (14 cycles)** for a complex operation; cycle time is **75 ns** ($0.75 * 10^{-7}$ **s**).

b) Explain the significance of the difference in the results from the two cases with respect to the two different platforms. [2 marks]

c) By means of two suitable diagrams, show Flynn's classifications of computer architectures for a Single Instruction Stream, Multiple Data stream (**SIMD**) with **Shared** and **without a Shared** memory. Discuss the usefulness of using each of the two computer architectures. [7 marks]