UNIVERSITY OF GHANA, LEGON

FIRST SEMESTER EXAMINATIONS, 2013/2014

LEVEL 200: BACHELOR OF SCIENCE IN ENGINEERING

CPEN 203: DIGITAL CIRCUITS.

INSTRUCTIONS: *Answer all questions.* **TIME ALLOWED: 3 hours**

Q1 (a) The key to the main entrance door of the Faculty of Engineering Sciences building of University of Ghana is to be replaced by an electronic key system. An electronic key that has four input knobs, *A, B, C, D* is to be used to generate the required output signal *Y* needed to open the door. Design a logic circuit for the electronic key, if the following conditions are required.

Y=1 when *A* and *B* are both 1, subjected to the conditions that *C* and *D* are both Low or both High [10 marks]

(b) List the systematic procedure used to achieve the designed logic circuit for the electronic key in Q1 (a) [7 marks]

(c) Identify the circuit in figure 1 and write the Boolean expression for the circuit, if ABCD are the address lines and a and b are the address select (control) lines [3marks]

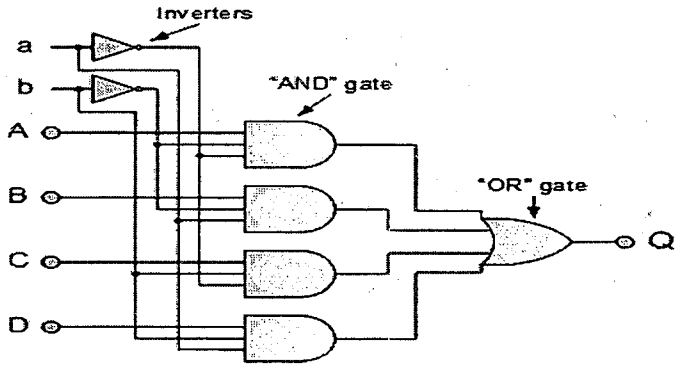

Figure 1

Examiner: Mr. Agyare Debra

Q2 (a) Compare CMOS ICs to TTL ICs in terms of the following parameters:

(i) Speed of operation [2 marks]

(ii) Noise immunity [2 marks]

(iii) Power dissipation [2 marks]

(b) Explain what a *high density* IC is, and give two advantages and two disadvantages of it. [6 marks]

(c) A NOR gate has an input voltage Vcc equal to 5V. The input current is 2.2mA for high output and 3.5mA for low output. Find the power dissipated for 50% duty cycle. [8 marks]

Q3 (a) With the aid of a circuit diagram show how four (4) flip-flops can be interconnected to reduce the normal 16 count to 10 count. [8 marks]

(b) Explain how the decade counter works. [5 marks]

(c) Give one advantage and one disadvantage of synchronous counter over asynchronous counter. [2 marks]

(d) A 4-bit asynchronous counter has a count of 1001 at any instant. What will be the count after 23 pulses. [5marks]

Q4

(a) Use Karnaugh map to simplify the function

$f(A,B,C,D)=\sum m(1,5,7,8,9,10,11,14,15)$ [10 marks]

(b)Draw a logic circuit to implement the simplified expression. [6 marks]

(c) Gives two reasons why many designers prefer to use either all NAND gates or all NOR gates in their circuits. [2 marks]

(d) Implement an Exclusive-NOR gate using only NAND gates. [2 marks]

Q5 (a) A 4-bit serial-in to serial-out shift register with a positive edge triggering clock pulse is fed at it's input with the data 1010

(i) Draw the circuit using either D or JK flip-flops [5marks]

(ii) Show the status of the register at the various clock pulses [10marks]

(b) State two applications of serial-in to serial-out shift register. [2marks]

(c) An 8-bit register has a clock frequency of 5MHz.

Calculate the delay time Δt introduced by the register. [3marks]