UNIVERSITY OF GHANA, LEGON

BACHELOR OF SCIENCE IN ENGINEERING
SECOND SEMESTER EXAMINATIONS, 2015/2016

DEPARTMENT OF COMPUTER ENGINEERING

CPEN 402: ADVANCED COMPUTER ARCHITECTURE (3 Credits)

INSTRUCTIONS:

ANSWER ALL QUESTIONS IN SECTION A AND FOUR (4) OTHER QUESTIONS IN SECTION B.

TIME ALLOWED: THREE (3) HOURS

SECTION A (40 Marks)

ANSWER ALL QUESTIONS IN THIS SECTION

1.

a. With the aid of a labelled diagram describe briefly the main difference between **multiprocessor** and **multicomputer** design architecture and state two uses of each. [6 marks]

b. By means of a suitable diagram, show how a CPU chip is interconnected to an I/O and a main memory in a simple Von Newman computer design bus system. [5 marks]

c. What is meant by the term '***windows of execution***' in Superscalar Architectures and mention any two constraints to the use of the information in the window? [4 marks]

d. Explain what is meant by the term '***Register naming***' in computer architecture and show by a sequence of program outline how this is achieved. [5 marks]

e. Explain why a Single embedded processor at clock frequencies of 1GHz and beyond are possible but not used in real architecture designs. [4 marks]

f. State two main advantages and disadvantages of VLIW as compared to Superscalar design in the theories of computer architectures. [4 marks]

g. Why is low power consumption important in computer architecture? [2 marks]

h. State Amdahl's law and briefly explain its relevance to multiprocessor architecture design of computers. [4 marks]

i. Show by means of well labelled diagrams how a pipeline execution with six instructions is executed by:
   i. A standard pipeline
   ii. A super pipeline and
   iii. A superscalar approach [6 marks]

SECTION B (60 Marks)
ANSWER ANY FOUR (4) QUESTIONS FROM THIS SECTION.

2.

a. By means of a clearly labelled Memory Hierarchy diagram, discuss the pros and cons of the use of the various memory segments in the design and build of a personal computer. [7 marks]

b. In computer architecture, one popular classification divides the multiprocessor platform into symmetric multiprocessor (SMP) and asymmetric multiprocessor (AMP) systems. Explain in what situations that each of these classifications are better selection for a computer task. [8 marks]

3.

Consider the following program f:

```
program.f:
...
if CPU=a then
  low_limit=1
  upper_limit=50
elseif CPU=b then
  low_limit=51
  upper_limit=100
end if
do I = low_limit, upper_limit
  work on A(I)
end do
....
end
```

a. Show that this program could be executed by two CPUs in a parallel programing scenario by showing the programing outline in such a situation. Indicate the conditions that must be fulfilled for this to work. [10 marks]

b. Discuss briefly the use of parallel programming and indicate where these are useful. [5 marks]

4.

a. Consider an architecture design employing a pipeline with 7 instructions each with execution time T_{ex}. They are executed by a 6-stage pipeline. Pipeline overheads are ignored. How long does it take to execute the 7 instructions by the pipelined CPU? [make any suitable assumptions] Draw the pipeline state diagram. [9 marks]

b. In the multiprocessor architecture, explain why **Dual-core processor** will run far cooler than a **single core design** of equivalent performance running at double the clock speed. [6 marks]

5.

a. Pollack's Rule says that the performance increase of a processor is roughly proportional to the square root of the increase in its complexity. Assume that the complexity is a function of the number of transistors denoted by **P(T)** and the performance of the increase in processor is denoted by **X(P)**.
Prove that if the number of Transistors is **doubled**, the increase in the performance of the processor will be in the region of 40% and discuss the relevance of this mathematical observation to multi-processor computing architecture with reference to cost. [7 marks]

b. By means of two suitable diagrams, show Flynn's classifications of computer architectures for a Single Instruction Stream, Multiple Data stream **(SIMD)** with **Shared** and **without a Shared** memory. Discuss the relevance between the two architectures with reference to computer design. [8 marks]

6.

a. How much time would a program of ten thousand cycles be required to be completed if it were run on a **RISC** and **CISC** based computers given the following parameters of information. [8 marks]

i. Assume that **80%** of executed instructions being simple and **20%** complex.
ii. On a CISC machine simple instructions take **4 cycles**, complex instructions take **8 cycles**; cycle time is **100 ns (10^{-7} s);**
iii. On a RISC machine simple instructions are executed in **one cycle**; complex operations are implemented as a sequence of instructions; we consider on average **14 instructions (14 cycles)** for a complex operation; cycle time is **75 ns ($0.75 * 10^{-7}$ s).**
iv. Explain the significance of the difference in the results from the two cases with respect to the two different architectures.

b. Name the three data dependencies that could be identified within the superscalar architecture and discuss their impact on computer architecture development by giving an example in each case. [5 marks]

c. Which two of the three dependencies in 6b above are referred to as artificial dependencies and why? [2 marks]