



UNIVERSITY OF GHANA

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BACHELOR OF SCIENCE IN ENGINEERING FIRST SEMESTER EXAMINATIONS: 2016/2017

DEPARTMENT OF COMPUTER ENGINEERING CPEN 403: EMBEDDED SYSTEMS (3 Credits)

INSTRUCTION: *Answer any five (5) Questions of your choice*

TIME ALLOWED: *THREE (3) HOURS*

1.
 - (a) What is an embedded system? List and define three main characteristics that distinguish such systems from other computing systems. [8 marks]
 - (b) Using the layered model and a diagram, briefly describe the architecture of a typical embedded system and explain the role of each layer in the model. [6 marks]
 - (c) List and briefly discuss three major challenges that confront embedded systems of today. [6 marks]

2.
 - (a) Suppose you have been tasked to design an embedded system for a tollbooth to monitor and control vehicular movement to and from the university. Describe the design steps you will follow to achieve your development. [6 marks]
 - (b) A temperature sensor monitoring the fuel production system at the TOR plant is connected to port P1 of a microcontroller while an LCD system is connected to port P2. Write a simple program to show how bytes of data captured from the plant on P1 can be written to the LCD. Illustrate with a simple diagram. [5 marks]
 - (c) Suppose in your design in 2(a) above, you decided to use software approach by writing to a microcontroller rather than FPGA hardware. If the microcontroller for the task has a clock speed of 500MHz and the number of instructions required for execution in the program is 400,000 (see Table 1 below), find the following:
 - (i) execution time and performance of the system. [4 marks]
 - (ii) MIPS/Watt and explain its relation to the performance of the system. Assume

the microcontroller is driven by 5V and draws a current of 3A.

[3 marks]

(iii) how much it will cost to implement the FPGA hardware option if the cost for the microcontroller based option is GHc800 and the cost per performance ratio is assumed to be the same for the two options. Assume the performance of the FPGA option is 1570 data/sec.

[2 marks]

Table 1 – Microcontroller operational data

No	Processor instructions	CPI	% Occurrence
1	ADD	3	25%
2	MUL	1	10%
3	SUB	2	15%
4	LOAD	4	18%
5	STORE	2	12%
6	BRANCH	-	20%
6b	BRANCH (taken)	1	55%
6a	BRANCH (not taken)	2	45%

- Q3. (a)** List four hardware components that make embedded systems what they are and briefly explain the function of each component on the embedded system. [4 marks]
- (b)** Explain the difference between a timer and a watchdog timer. Write a simple program to illustrate how a watchdog timer operates in ATM machines. [5 marks]
- (c)** Suppose a watchdog timer in an ATM machine is connected to a 12-bit counter that operates at a clock frequency of 16 MHz. Find the terminal count value that will be required to measure 3ms interval. [6 marks]
- (d)** A motor at the TOR plant operates at 5,000 revolutions per minute (rpm) when its input voltage is 3.5V. The microcontroller that controls the motor has a PWM whose output port can be set high (5V) or low (0V). Find the duty cycle that will be required to achieve the 5,000 rpm and the values of pulse width and period that will be required to achieve this duty cycle. [6 marks]
- 4. (a)** List four parameters you will consider necessary when selecting an ADC/DAC for use on an embedded board for ultrasound application. [4 marks]
- (b)** Suppose an analog input signal from the ultrasound machine in 4(a) has input range of 0 to 10 V. If the ADC uses a 10-bit encoding system, find the correct

encoding for an input of 4.2V.

[4 marks]

(c) Suppose the embedded board on the ultrasound machine is driven by a 10 MHz clock and 10-bit on-chip ADC. Suppose the ADC uses single ramp architecture for the conversion and the program that processes the input requires 100 instructions with an average execution time of 4 clocks per instruction. Find the conversion time required by the ADC for the conversion of the analog voltage signals, the maximum sampling rate of the signals, and the highest frequency that the sensor can monitor.

[6 marks]

(d) Suppose the DAC on the embedded board has a full scale of range of 30mV for 5V maximum output. Find the accuracy error of the DAC. Will you consider this error tolerable? Explain your answer.

[6 marks]

5. (a) Briefly discuss two synchronous communication interfaces on an embedded system that could be used to communicate with the real world. For each interface, give one common device that is capable of interfacing to the bus.

[4 marks]

(b) A 16 x 2 LCD system is integrated to an embedded board via UART to monitor the quality of power supply. The baud rate on the embedded board is set at 9600 bps. How long will the system take to display the information "voltage = 259.8V" on the LCD? Explain how you will increase the transmission duration for the information to be displayed much faster on the LCD.

[6 marks]

(c) Explain the difference between EEPROM and NVRAM. Which of the two memory types will you consider suitable for an embedded system if you want to store critical system information?

[4 marks]

(d) Describe the steps you will follow to test memory on an embedded board and explain whether the process will be suitable for RAM and EEPROM.

[5 marks]

(e) How will you test for missing memory chip on an embedded board? List and briefly describe any three common memory problems.

[5 marks]

6. (a) Explain the difference between hard real-time and soft real-time embedded systems.

[4 marks]

(b) What is the difference between fixed-priority and dynamic-priority real time scheduling algorithm? Briefly describe one fixed-priority and one dynamic-priority scheduling algorithm that may be used to schedule tasks in automobiles.

[6 marks]

(c) A real time embedded system has to execute four sets of tasks with execution times and deadlines shown in Table 2 below. The deadline of the tasks is assumed to be the same as the period.

- (i) Using the deadline monotonic scheduling priority scheme, indicate the order in which the tasks will be assigned for execution. [2 marks]
- (ii) Determine whether all the four task sets can be scheduled on time (justify your answer). Illustrate your tasks scheduling on a time diagram. [6 marks]
- (iii) Explain how the task sets can be made schedulable in case you found out that they are not schedulable. [2 marks]

Table 2 – Tasks sets scheduling information

Tasks	Execution time (ms)	Deadline (ms)
T1	20	100
T2	40	150
T3	60	200
T4	100	350