UNIVERSITY OF GHANA

SCHOOL OF ENGINEERING SCIENCES
SECOND SEMESTER EXAMINATIONS: 2016/2017
LEVEL400: BACHELOR OF SCIENCE IN ENGINEERING
CPEN 402: ADVANCED COMPUTER ARCHITECTURE [*3 CREDITS*]

TIME ALLOWED: *TWO AND HALF (2½) HOURS*

INSTRUCTIONS:
*Answer **ALL** questions in Section A and **THREE (3)** other questions in Section B.*

SECTION A [40 Marks]

*Answer **ALL** questions in this section.*

A1. Attempt all questions below.

a) Briefly explain what is meant by the term 'windows of execution' in Superscalar Architectures and indicate the issues associated with it. **[5 marks]**

b) State the dynamic power equation in the discussions of Computer architecture and explain the effect of any two of the parameters that contribute to power issues in architecture design. **[5 marks]**

c) In the multiprocessor architecture, explain why **Dual-core processor** will run far cooler than a **single core design** of equivalent performance running at double the clock speed. You may make any reasonable assumptions **[4 marks]**

d) Discuss any two schemes used in managing the RAM in Computers. **[4 marks]**

e) Explain why a Single embedded processor at clock frequencies of 1GHz and beyond are possible but not used in real architecture designs **[4 marks]**

f) Describe briefly by means of a diagram the main difference between multiprocessor and multicomputer design architecture and state two uses of each. **[6 marks]**

g) Show by means of a diagram how a pipeline execution with six instructions is executed by:
   i. A standard pipeline
   ii. A super pipeline and
   iii. A superscalar approach with the respective labels **[6 marks]**

h) The figure A1 below gives an example of potential hazards that occur in memory access in a typical computer.

Time	1	2	3	4	5	6	7	8	9	10	11
Ld F10,X	IF	ID	M	M	M	M	M	M	M	WB	
ADD F11,F10,F1		IF	stl	Stl	stl	stl	stl	Stl	stl	stl	Reg
MULT F1,F2,F3			IF	ID	M	M	M	MEM	WB		
ADD F1,F4,F5				IF	ID	A1	MEM	WB			

Figure: A1

EXAMINER: Mr. F. Boachie

i. Explain the hazard that has occurred in the second instruction (first ADD instruction) **[3 marks]**

ii. Explain what type of hazard is happening between the **second ADD** and the **MULT** instruction **[3 marks]**

SECTION B [60 Marks]

*Answer any **THREE (3)** questions from this section.*

B1. Consider the following program f: **[10 marks]**

```
program.f:
...
if CPU=a then
  low_limit=1
  upper_limit=50
elseif CPU=b then
  low_limit=51
  upper_limit=100
end if
do I = low_limit, upper_limit
  work on A(I)
end do
...
end program
```

a) Show that this program could be executed by two CPUs in a parallel programing scenario by showing the programing outline in such a situation. Indicate the conditions that must be fulfilled for this to work.

b) Discuss briefly the use of parallel programming and indicate where these are useful. **[5 marks]**

c) Describe briefly the importance of the memory hierarchy as it applies to computer architecture. **[5 marks]**

B2.

a) Consider an architecture design employing a pipeline with 8 instructions each with execution time T_{ex}. They are executed by a 6-stage pipeline. Pipeline overheads are ignored. How long does it take to execute the 8 instructions by the pipelined CPU? [make any suitable assumptions] Draw the figure. **[10 marks]**

b) In computer architecture, one popular classification divides the multiprocessor platform into symmetric multiprocessor (SMP) and asymmetric multiprocessor (AMP) systems. Describe the situation in which each is suitable for a computer task and why? **[10 marks]**

B3.

a) Pollack's Rule says that the performance increase of a processor is roughly proportional to the square root of the increase in its complexity. Assume that the complexity is a function of the number of transistors denoted by **P(T)** and the performance of the increase in processor is denoted by **X(P).**

Prove that if the number of Transistors is **doubled**, the increase in the performance of the processor will be in the region of 40% and discuss the relevance of this mathematical observation to multi-processor computing architecture. **[10 marks]**

b) Name the three data dependencies that could be identified within the superscalar architecture and discuss their impact on computer architecture development by giving an example in each case. Which two of these three dependencies are referred to as artificial dependencies and why are they referred to as such? **[10 marks]**

B4.

a) How much time would a program of ten thousand cycles be required to be completed if it were run on a RISC and CISC based computer architecture given the following information below.

i. Assume that 80% of executed instructions being RISC and 20% complex

ii. On a CISC machine simple instructions take 4 cycles, complex instructions take 8 cycles; cycle time is 100 ns (10^{-7} s); **[3 marks]**

iii. On a RISC machine, simple instructions are executed in one cycle; complex operations are implemented as a sequence of instructions; we consider on average 14 instructions (14 cycles) for a complex operation; cycle time is 75 ns ($0.75 * 10^{-7}$ s). **[3 marks]**

iv. Explain the significance of the difference in the results from the two cases with respect to the two different platforms. **[2 marks]**

b) By means of two suitable diagrams, show Flynn's classifications of computer architectures for a Single Instruction Stream, Multiple Data stream (SIMD) with Shared and without a Shared memory. Discuss the relevance between the two architectures with reference to computer design. **[6 marks]**

c) State three advantages each of RISC and CISC as applied to computer architecture. **[6 marks]**