

UNIVERSITY OF GHANA

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SCHOOL OF ENGINEERING SCIENCES SECOND SEMESTER EXAMINATIONS: 2016/2017 LEVEL200: BACHELOR OF SCIENCE IN ENGINEERING CPEN 202: COMPUTER SYSTEM DESIGN [2 CREDITS]

TIME ALLOWED: TWO (2) HOURS

INSTRUCTION:

Answer ANY FIVE (5) questions

	Answer ANY <u>FIVE (3)</u> questions
1.	a) Implement the circuit with the following function:
	$g(x_1, x_5) = \sum_{i=1}^{n} m(0, 1, 2, 4, 5, 8, 14, 15, 16, 18, 20, 24, 26, 28, 31) + D(10, 10, 10, 10, 10, 10, 10, 10, 10, 10, $
	11, 12, 27). [8 marks]
	b) Redesign the circuit using NAND-Gates only. [4 marks]
	c) Write a VHDL code to implement your design. [8 marks]
2.	
	a) Explain the usefulness of a 74F85 4-bit comparator chip. [2 marks]
	b) Draw the IEC/IEEE symbol of 74F85 4-bit comparator chip. [3 marks]
	c) Draw the 4-bit magnitude comparator logic diagram. [5 marks] d) Write a VHDL code to implement 2(a) above. [8 marks]
	e) Explain how you would achieve more 4-bit comparators. [2 marks]
	c) Explain now you would achieve more 4-on comparators. [2 marks]
3.	
	a) From first principles, design a full Adder. [5 marks]
	b) Illustrate how a 4-bit full Adder may be constructed. [5 marks]
	c) Write a VHDL code to implement an 8-bit full Adder. [10 marks]
4.	a). Clearly draw and label the general block diagram of a
	a) Clearly draw and label the general block diagram of a synchronous sequential machine. [4 marks]
	b) Design the circuit for a sequential machine to detect 1010. [15 marks]
	c) Name the type of sequential machine you have designed. [1 mark]
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	a) With the help of specific diagrams explain hazard in systems design. [3 marks]
	b) Explain how a stuck-at-fault may be overcome. [3 marks]
	c) Using K-map or otherwise deduce how an extra component may help solve a
	typical design fault. [4 marks]
	d) Find a hazard-free minimum cost implementation of the function:
	$f(x_1,, x_5) = \sum m(1, 4, 5, 11, 17, 28) + D(10, 12, 14, 15, 20, 31).$ [10 marks]

- 6.
- a) Differentiate between synchronous and asynchronous sequential circuits.

 [5marks]
- b) Design an asynchronous sequential circuit from the function AB+By=Y using NAND-Gates only. [10 marks]
- c) State any two (2) disadvantages of asynchronous circuits, and with the aid of a suitable diagram explain how they can be avoided. [5 marks]