UNIVERSITY OF GHANA

BACHELOR OF SCIENCE IN ENGINEERING

SECOND SEMESTER EXAMINATIONS, 2011/2012

CPEN 202 DIGITAL SYSTEMS DESIGN (2 Credits)

TIME ALLOWED: *TWO (2) HOURS*

INSTRUCTION:

Answer ANY five (5) questions in your answer booklet.

Q1. Study the Truth Table below:

X_1	X_2	f
0	0	0
0	1	1
1	0	1
1	1	0

(i) Draw the circuit from this Truth Table. [7 Marks]
(ii) State one good use of this circuit. [3 Marks]
(iii) Write a VHDL code to implement your circuit. [10 Marks]

Q2. (i) Explain how a Digital Combination Lock works. [5 Marks]
(ii) Using AND-Gates and Inverters, design a Digital Combination Lock whose input is 0110. [10 Marks]
(iii) Draw a state diagram for 0110. [5 Marks]

Q3. (i) Draw and label the general block diagram of a synchronous sequential machine. [5 Marks]
(ii) Design the circuit for a sequential machine to detect 1010. [15 Marks]

Q4. (i) From first principles, design a full Adder. [5 Marks]
(ii) Illustrate how a 4-bit Adder may be constructed. [5 Marks]
(iii) Write a VHDL code to implement the 4-bit Adder. [10 Marks]

Q5. (i) Given the function $f(x_1, x_2, x_3) = \sum m\ (1, 4, 5, 6)$. Design a combinatorial circuit to implement this function. [10 Marks]
(ii) Write a VHDL code to implement your design. [10 Marks]

EXAMINER: PROSPER AFRIYIE

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Q6. Write short notes on the following:

(i) Testing. [4 Marks]

(ii) Stuck-at Fault. [4 Marks]

(iii) Fault Reductions. [4 Marks]

(iv) Fault Modeling and Testing. [4 Marks]

(v) Test Effectiveness. [4 Marks]

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