UNIVERSITY OF GHANA

BACHELOR OF SCIENCE IN ENGINEERING
SECOND SEMESTER EXAMINATIONS: 2014/2015
CPEN 202 COMPUTER SYSTEMS DESIGN (2 Credits)

INSTRUCTIONS: *Answer ANY five (5) questions.*
TIME ALLOWED: ***TWO (2) HOURS***

Q1. (i) A chemical process starts only if at least three out of four keys (X_1, X_2, X_3, X_4) are inserted. If a key is inserted and the main switch is *ON* the system produces a logic 1. Design a minimal circuit to produce this system using NAND-Gates only. (10 Marks)

(ii) Explain how Component and Signal are used to code the circuit in Q1 (i). (2 Marks)

(iii) Write a VHDL code to implement the system in Q1 (i). (8 Marks)

Q2. (i) Outline the steps in designing a synchronous sequential machine. (6 marks)

(ii) Draw and label the general block diagram of a synchronous sequential machine. (2 Marks)

(iii) Using either D-Type or JK flip-flops and any logic gates, design a synchronous error-checking circuit to detect the presence of the sequence **110** in a serial flow of binary data. (11 Marks)

(iv) Indicate the type of machine that Q2 (iii) represents in computer systems design. (1 Marks)

Q3. (i) From first principles, design a full Adder. (5 Marks)

(ii) Illustrate how an 8-bit Adder may be constructed. (5 Marks)

(iii) Write a VHDL code to implement the 8-bit Adder. (10 Marks)

Q4. (i) Using NAND-Gates draw and explain a two input asynchronous sequential circuit $Y = AB + By$ (5 Marks)

(ii) If the feedback path is disconnected draw an excitation map and a flow table for Y in Q4(i). (10 Marks)

(iii) Draw and explain the state diagram for Q4 (i) above. (5 Marks)

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Q5. (i) Explain the usefulness of a 74F85 4-bit comparator chip. (2 Marks)

(ii) Draw the IEC/IEEE symbol of 74F85 4-bit comparator chip. (3 Marks)

(iii) Draw the 4-bit magnitude comparator logic diagram. (5 Marks)

(iv) Write a VHDL code to implement the comparator logic in Q5 (iii). (8 Marks)

(v) Explain the technique you would use to increase the number of 4-bit comparators. (2 Marks)

Q6. (i) With the help of specific diagrams, discuss hazard in systems design. Illustrate your answers with specific examples. (10 Marks)

(ii) Find the hazard-free minimum cost implementation of the function $f(X_1, X_2, X_3, X_4) = \sum m\,(0, 4, 11, 13, 15) + d\,(2, 3, 5, 10)$. (10 Marks)