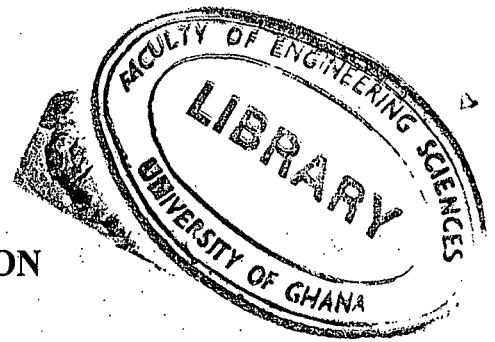




UNIVERSITY OF GHANA, LEGON

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BACHELOR OF SCIENCE IN ENGINEERING
FIRST SEMESTER EXAMINATIONS: 2015/2016

DEPARTMENT OF COMPUTER ENGINEERING

CPEN 303: COMPUTER ARCHITECTURE (3 CREDITS)

INSTRUCTION: Answer any four (4) Questions of your choice.

TIME ALLOWED: Two and half (2 1/2) hours

1.

Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs:

Instruction Type	Instruction Count (millions)	Cycles per Instruction
Machine A		
ALU	8	1
LOAD and STORE	4	3
BRANCH	2	4
Others	4	3
Machine B		
ALU	10	1
LOAD and STORE	8	2
BRANCH	2	4
Others	4	3

(a) Calculate the following for each of the machines: [12 marks]

- Calculate the effective Cycles Per Instruction (CPI)
- Millions of Instruction Per Second (MIPS)
- Execution time (CPU).

(b) Based on your result in 1(a) above, which machine will you prefer and give reasons for your choice. [3 marks]

(c) On the IAS (Von Neumann), describe the process that the CPU must undertake to read a value from memory and to write a value to memory in terms of what is put into the MAR, MBR, address bus, data bus and control bus. [10 marks]

Useful formulae

$$CPI = \frac{\sum_{i=1}^n (CPI_i \times I_i)}{I_c}$$

I_i = Number of executed instructions of type i for a given program

I_c = Instruction Count

f = Frequency

$$\text{MIPS rate} = \frac{f}{CPI \times 10^6}$$

$$CPU = \frac{I_c \times CPI}{f}$$

2.

- (a) Suppose we have four machines comprising: 0-address, 1-address, 2-address, and 3-address, respectively. Use each machine to compute the expression below and give a brief comment on your result. [10 marks]

$$X = (A + B \times C) / (D - E \times F)$$

- (b) The diagram in figure 1 below shows the order of execution of a program in six steps. Describe this execution order using Memory Address Register (MAR) and Memory Buffer Register (MBR). [10 marks]

- (c) List five (5) ways by which computer architecture can be designed to improve system performance. [5 marks]

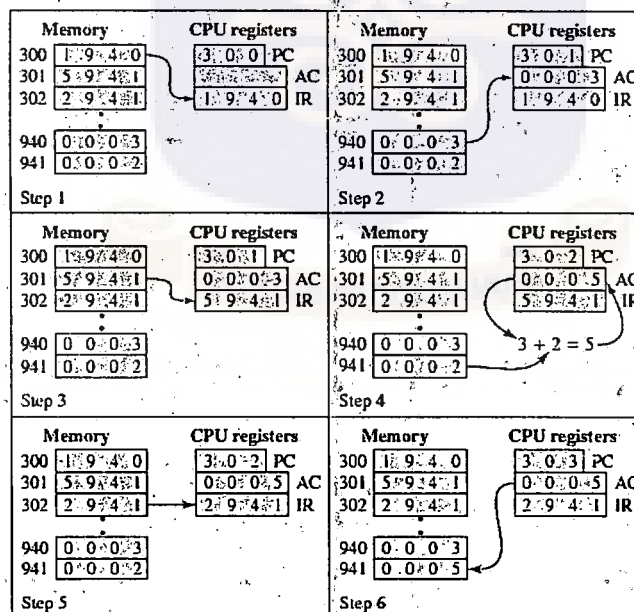


Figure 1

3.

(a) Represent the following decimal numbers in both binary sign-magnitude and in two's (2's) complement using 16 bits: [6 marks]

(i) +600

(ii) -200

(b) Use the unsigned binary multiplication block diagram in Figure 2 below to multiply 11 (multiplicand) by 13 (multiplier), where each number is represented using 4 bits. [7 marks]

(c) Convert the following floating point numbers to its binary representation using IEEE Standard 754. [8 marks]

(i) 1.638125×2^{-20}

(ii) -1.638125×2^{-20}

(d) How can we store 12345678 (32 bit hexadecimal) using 4 x 8-bit address locations in memory using: [4 marks]

(i) Little-Endian

(ii) Big-Endian

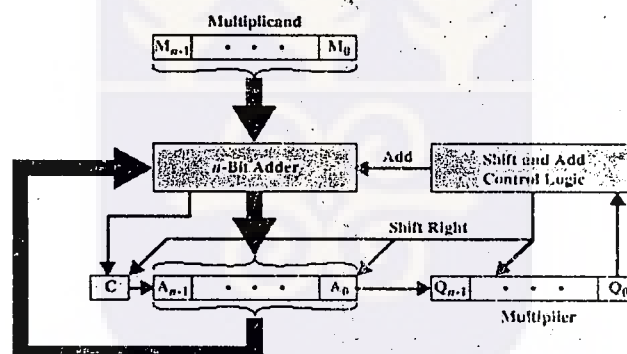
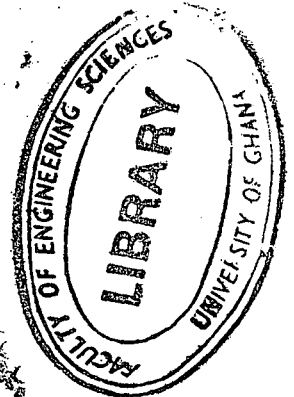


Figure 2



4.

(a) A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses. [5 marks]

(b) For a direct-mapped cache, a main-memory address is viewed as consisting of three fields. List and explain the three fields. [5 marks]

(c) What is the difference between DRAM and SRAM in terms of application, speed, size, and cost? [5 marks]

(d) Explain the two main types of memory errors. With a block diagram, how can error correcting code function work. [10 marks]

5.

EXAMINER: MR. GEORGE K. ANNI

(a) With the support of a diagram, explain the three techniques for performing data transfer between the processor and the Input- Output (I/O) devices. [10 marks]

(b) Define the following terms briefly as it applies to a magnetic disk. [10 marks]

- (i) Seek time
- (ii) Rotational delay
- (iii) Access time
- (iv) Track
- (v) Sector

(c) State five (5) major functions of a computer system? [5 marks]

