UNIVERSITY OF GHANA
BACHELOR OF SCIENCE IN ENGINEERING
FIRST SEMESTER EXAMINATION, 2018/2019
DEPARTMENT OF COMPUTER ENGINEERING
CPEN 303: COMPUTER ARCHITECTURE (3 Credits)

Instructions: Attempt all questions **Time Allowed: $2^{1/2}$ Hours**

All abbreviations have their usual meaning.

QUESTIONS

1.

a. What are the four main components of any general-purpose computer?

(4 Marks)

b. What is the key distinguishing feature of a microprocessor?

(3 Marks)

c. Consider two different machines, with two different instruction sets, both of which have a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs:

Instruction Type	Instruction Count (millions)	Cycles per Instruction
Machine A		
Arithmetic and logic	8	1
Load and store	4	3
Branch	2	4
Others	4	3
Machine A		
Arithmetic and logic	10	1
Load and store	8	2
Branch	2	4
Others	4	3

a. Determine the effective CPI, MIPS rate, and execution time for each machine.

(6 Marks)

b. Comment on the results. **(3 Marks)**

2. A microprocessor has a memory write timing as shown in Figure 1. Its manufacturer specifies that the width of the Write signal can be determined by T-50, where T is the clock period in ns.

   a. What width should we expect for the Write signal if bus clocking rate is 5 MHz?

   (4 Marks)

   b. The data sheet for the microprocessor specifies that the data remain valid for 20 ns after the falling edge of the Write signal. What is the total duration of valid data presentation to memory?

   (6 Marks)

   c. How many wait states should we insert if memory requires valid data presentation for at least 190 ns?

   (4 Marks)

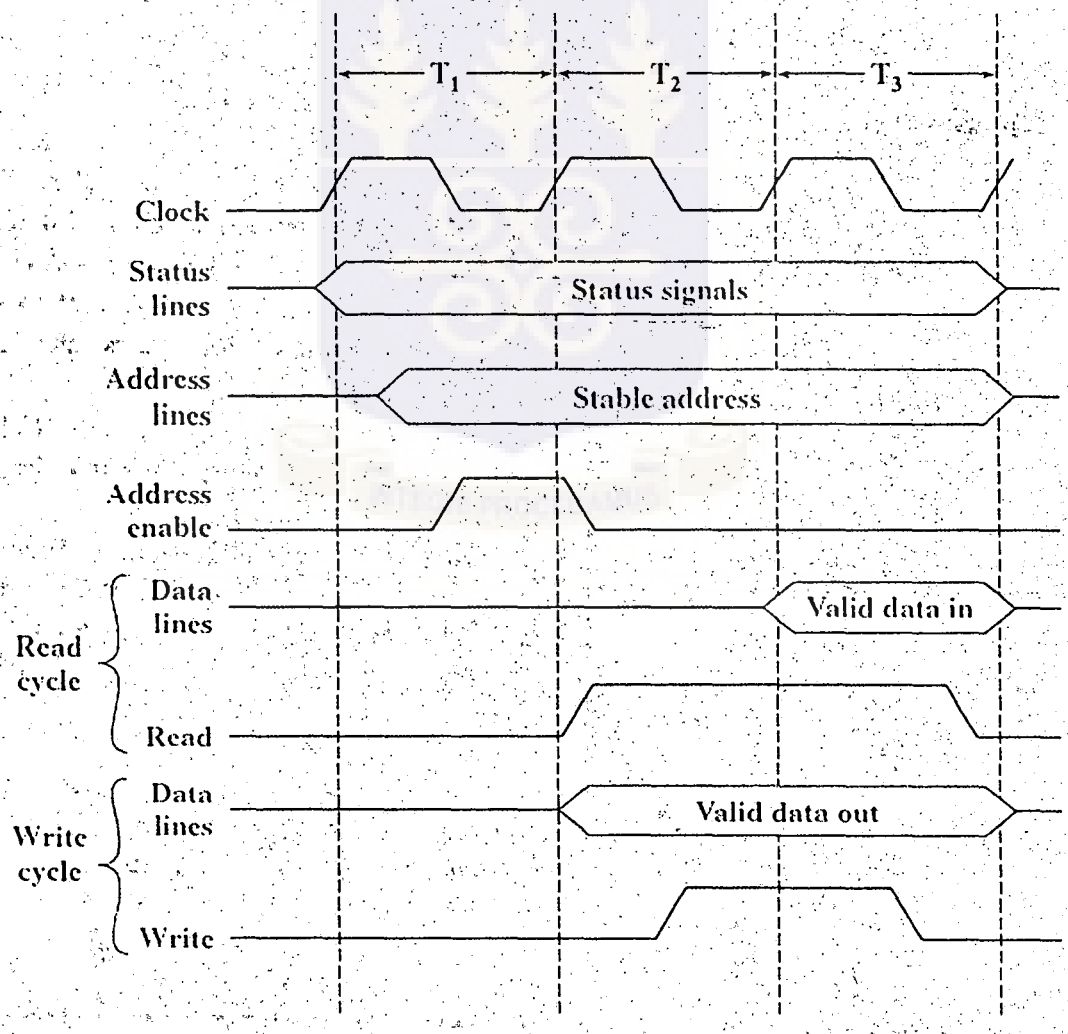

Figure 1. Timing of Synchronous Bus Operations

3.

a. What is the difference between DRAM and SRAM in terms of characteristics such as speed, size, and cost?

(6 Marks)

b. What are the differences among EPROM, EEPROM, and flash memory?

(6 Marks)

c. For the 8-bit word 00111001, the check bits stored with it would be 0111. Suppose when the word is read from memory, the check bits are calculated to be 1101. What is the data word that was read from memory?

(4 Marks)

d. A DMA module is transferring characters to memory using cycle stealing, from a device transmitting at 9600 bps. The processor is fetching instructions at the rate of 1 million instructions per second (1 MIPS). By how much will the processor be slowed down due to the DMA activity?

(4 Marks)

4.

a. What are the major functions of an I/O module?

(3 Marks)

b. List and briefly define three techniques for performing I/O.

(6 Marks)

c. A microprocessor scans the status of an output I/O device every 20 ms. This is accomplished by means of a timer alerting the processor every 20 ms. The interface of the device includes two ports: one for status and one for data output. How long does it take to scan and service the device given a clocking rate of 8 MHz? Assume for simplicity that all pertinent instruction cycles take 12 clock cycles.

(3 Marks)

d. Consider a system employing interrupt-driven I/O for a particular device that transfers data at an average of 8 KB/s on a continuous basis.

i. Assume that interrupt processing takes about 100 s (i.e., the time to jump to the interrupt service routine (ISR), execute it, and return to the main program). Determine the fraction of processor time consumed by this I/O device if it interrupts for every byte. **(4 Marks)**

ii. Now assume that the device has two 16-byte buffers and interrupts the processor when one of the buffers is full. Naturally, interrupt processing takes longer, because the ISR must transfer 16 bytes. While executing the ISR, the processor takes about 8 s for the transfer of each byte. Determine what fraction of processor time is consumed by this I/O device in this case. **(4 Marks)**