UNIVERSITY OF GHANA
COLLEGE OF BASIC AND APPLIED SCIENCES
SCHOOL OF ENGINEERING SCIENCES
FIRST SEMESTER EXAMINATIONS, 2014/2015
LEVEL 200: BACHELOR OF SCIENCE IN ENGINEERING
CPEN 203: DIGITAL CIRCUITS (3 Credits).

INSTRUCTIONS: *Answer all five (5) questions.*

TIME ALLOWED: *TWO (2) HOURS THIRTY (30) MINUTES*

Q1 Assume that the School of Engineering Sciences of the University of Ghana has four departments *A,B,C,D*. Facilities in the School are shared in proportion to the number of students in each department by a voting system. The percentage of shares held by the four departments *A,B,C,D* are 40%, 30% ,20% and 10% respectively. Any major decision at the School must have a minimum of 50% of the total votes.

(a) Design a suitable logic circuit to implement the voting system. [13 marks]

(b) If NAND gates are the only gates available show how the circuit in Q1 (a) will be implemented. [5 marks]

(c) Why are NAND gates classified as Universal Gates? [2 marks]

Q2 (a) Explain with the aid of a logic diagram and truth table the operation of Master–Slave J-K flip-flop. [14 marks]

(b) State the main advantage of Master-Slave flip-flop as compared to other flip-flops. [2 marks]

(c) Explain the problem of Race conditions associated with flip-flops. [2 marks]

(d) Explain the functions of the asynchronous inputs of flip-flops. [2 marks]

Q3 (a) A logic gate has its output at logical 0 when any one or more of its inputs is at logical 1. Write the Boolean expression describing this circuit. [2 marks]

(b) Use a Karnaugh map to simplify the expression:

$f(A,B,C)=\sum m(0,4,10,11,14,15)$ [10 marks]

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(c) Draw a logic circuit to implement the results obtained. [8 marks]

Q4 (a) Construct a 4- bit asynchronous (ripple) binary counter using either D or J-K flip-flop. [5 marks]

(b) Eplain how the circuit in **Q4 (a)** works. [8 marks]

(c) With the aid of a circuit diagram explain how the circuit in **Q4(a)** can be converted to a Decade counter. [7marks]

Q5 (a) State two functions of a Shift Register. [2marks]

(b) A Serial-in Serial-out Shift Register with a positive edge triggering clock pulse is fed at its input with the data 1011.

(i) Draw the circuit using either D or JK flip-flops [4marks]

(ii) Show the status of the register at the various clock pulses [12marks]

(c) Calculate the time delay introduced by a Mod-64 register if its clock frequency is 500kHz. [4marks]

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