UNIVERSITY OF GHANA

BACHELOR OF SCIENCE IN ENGINEERING

SECOND SEMESTER EXAMINATIONS, 2015/2016

DEPARTMENT OF COMPUTER ENGINEERING

CPEN 202: COMPUTER SYSTEMS DESIGN (2 Credits)

INSTRUCTION:

ANSWER ANY FIVE (5) QUESTIONS IN YOUR ANSWER BOOKLET.

TIME ALLOWED: TWO (2) HOURS

1.

a. Using AND-Gates and Inverters, design a Digital Combination Lock whose input is 0110. (10 marks)

b. A chemical process is activated only if at least three out of four keys are inserted. Assuming that an inserted key produces a logic 1, design a minimal logic circuit to achieve this using NAND gates only. (10 marks)

2.

a. Explain how you would design a 1-bit comparator. (5 marks)

b. How would you use it to construct a 4-bit comparator? (5 marks)

c. Write a VHDL code for a 12-bit Comparator. (10 marks)

3.

a. Draw and label the general block diagram of a synchronous sequential machine. (2 marks)

b. Using either D-Type or JK flip-flops, and any logic gates, design a synchronous error-checking circuit to detect the presence of the sequence 1010 in a serial flow of binary data. (16 marks)

c. Indicate the type of machine 3.b. represents in digital systems design. (2 marks)

4.

a. From first principles, design a full Adder. (5 marks)

b. Illustrate how an 8-bit Adder may be constructed. (5 marks)

c. Write a VHDL code to implement an 8-bit Adder. (10 marks)

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a. Briefly outline any six steps needed to design an asynchronous circuit. (6 marks)
b. Explain the terms *stable* and *unstable* in asynchronous systems design. (4 marks)
c. Design an asynchronous circuit for the function $Y = AB + By$ (10 marks)

6.

a. Given the function $f(x_1, x_2, x_3) = \sum m\ (1, 4, 5, 6)$. Design a circuit for this function. (8 marks)
b. Explain how you could use *Component* and *Signal* to code your circuit. (4 marks)
c. Write a VHDL code to implement your design. (8 marks)