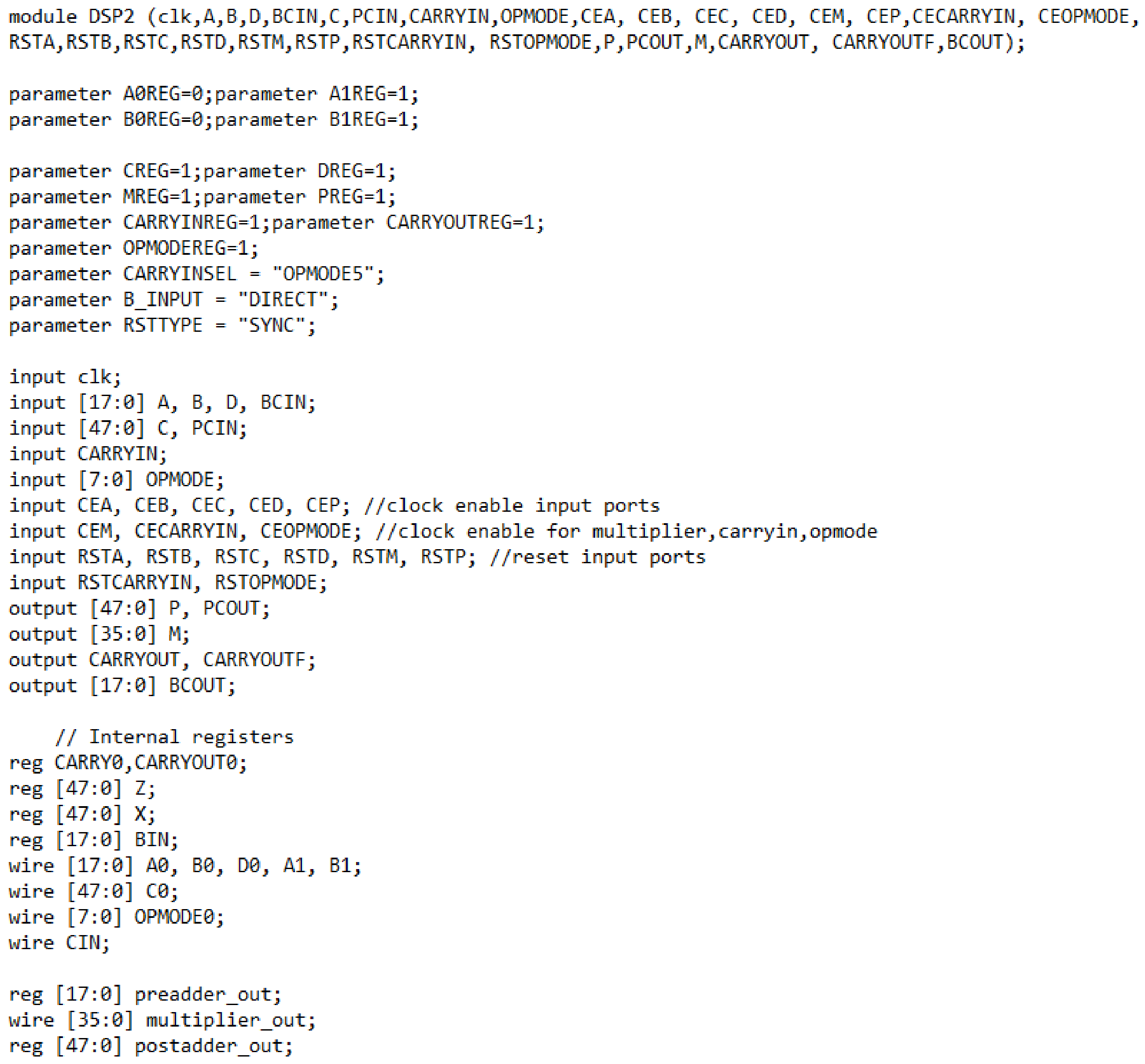
Name: Yousef Wael Mahmoud Alkattan

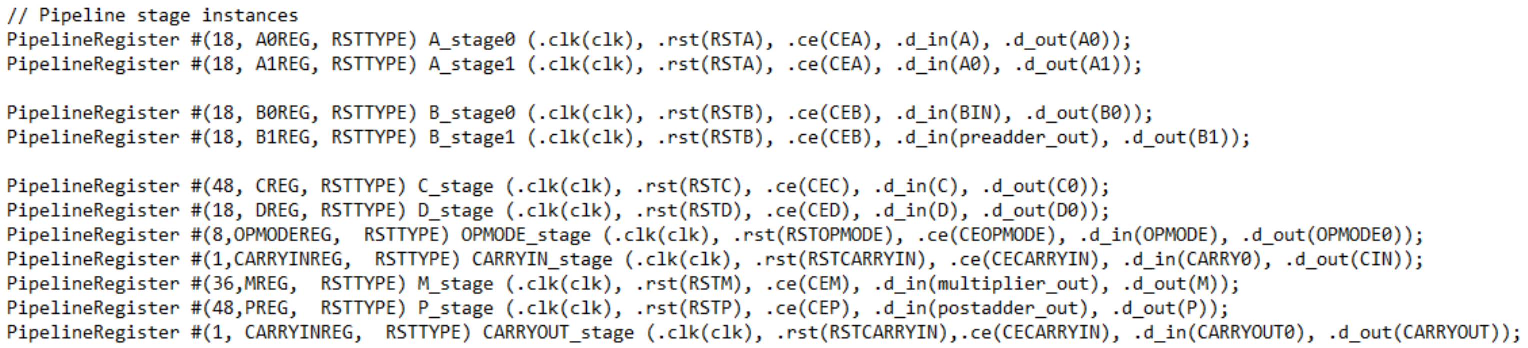
PROJECT1: DSP48A1

1. Design

Input & Output & Internal Registers

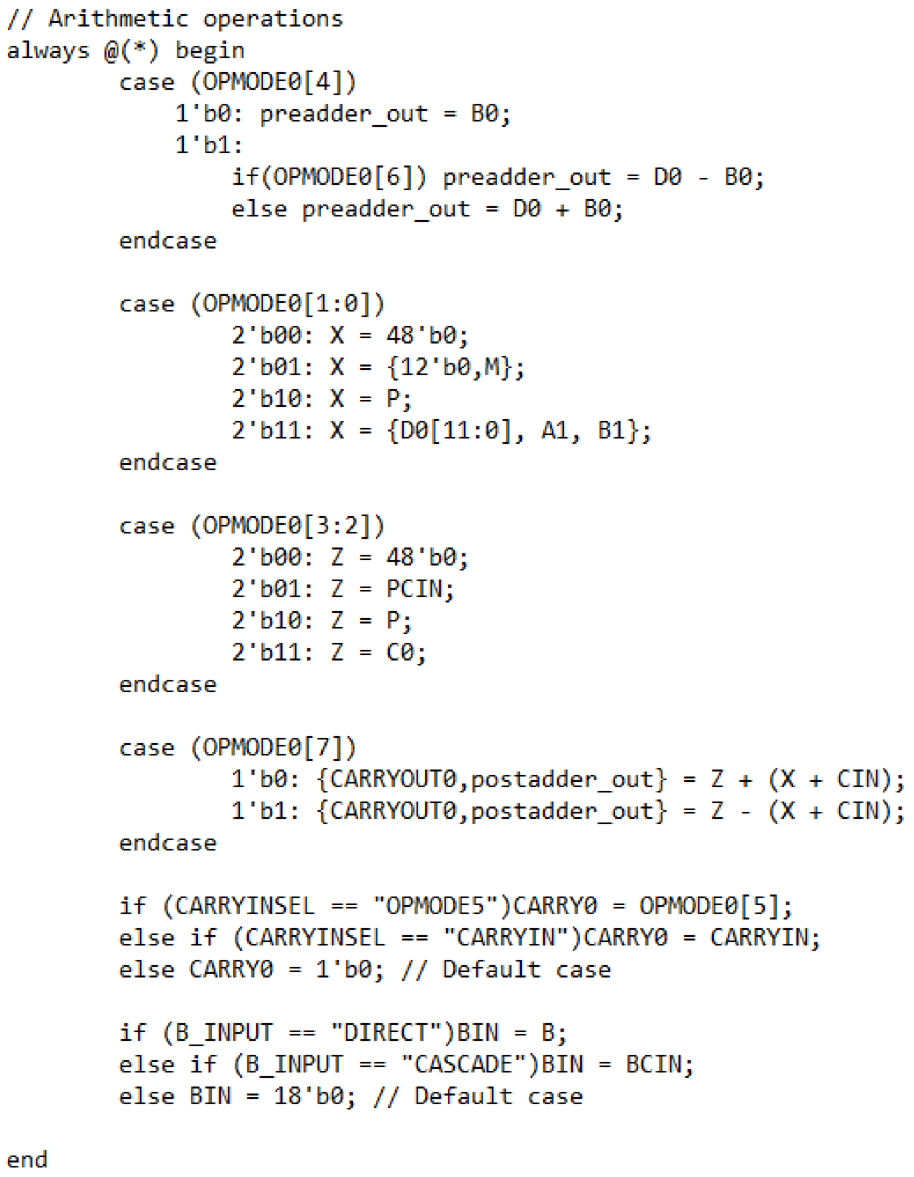


```
module DSP2 (clk,A,B,D,BCIN,C,PCIN,CARRYIN,OPMODE,CEA, CEB, CEC, CED, CEM, CEP,CECARRYIN, CEOPMODE,
RSTA,RSTB,RSTC,RSTD,RSTM,RSTP,RSTCARRYIN, RSTOPMODE,P,PCOUT,M,CARRYOUT, CARRYOUTF,BCOUT);

parameter A0REG=0;parameter A1REG=1;
parameter B0REG=0;parameter B1REG=1;

parameter CREG=1;parameter DREG=1;
parameter MREG=1;parameter PREG=1;
parameter CARRYINREG=1;parameter CARRYOUTREG=1;
parameter OPMODEREG=1;
parameter CARRYINSEL = "OPMODE5";
parameter B_INPUT = "DIRECT";
parameter RSTTYPE = "SYNC";

input clk;
input [17:0] A, B, D, BCIN;
input [47:0] C, PCIN;
input CARRYIN;
input [7:0] OPMODE;
input CEA, CEB, CEC, CED, CEP; //clock enable input ports
input CEM, CECARRYIN, CEOPMODE; //clock enable for multiplier,carryin,opmode
input RSTA, RSTB, RSTC, RSTD, RSTM, RSTP; //reset input ports
input RSTCARRYIN, RSTOPMODE;
output [47:0] P, PCOUT;
output [35:0] M;
output CARRYOUT, CARRYOUTF;
output [17:0] BCOUT;

    // Internal registers
reg CARRY0,CARRYOUT0;
reg [47:0] Z;
reg [47:0] X;
reg [17:0] BIN;
wire [17:0] A0, B0, D0, A1, B1;
wire [47:0] C0;
wire [7:0] OPMODE0;
wire CIN;

reg [17:0] preadder_out;
wire [35:0] multiplier_out;
reg [47:0] postadder_out;
```

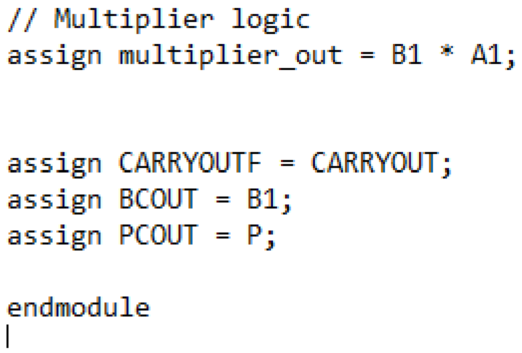


```
// Pipeline stage instances
PipelineRegister #(18, A0REG, RSTTYPE) A_stage0 (.clk(clk), .rst(RSTA), .ce(CEA), .d_in(A), .d_out(A0));
PipelineRegister #(18, A1REG, RSTTYPE) A_stage1 (.clk(clk), .rst(RSTA), .ce(CEA), .d_in(A0), .d_out(A1));

PipelineRegister #(18, B0REG, RSTTYPE) B_stage0 (.clk(clk), .rst(RSTB), .ce(CEB), .d_in(BIN), .d_out(B0));
PipelineRegister #(18, B1REG, RSTTYPE) B_stage1 (.clk(clk), .rst(RSTB), .ce(CEB), .d_in(preadder_out), .d_out(B1));

PipelineRegister #(48, CREG, RSTTYPE) C_stage (.clk(clk), .rst(RSTC), .ce(CEC), .d_in(C), .d_out(C0));
PipelineRegister #(18, DREG, RSTTYPE) D_stage (.clk(clk), .rst(RSTD), .ce(CED), .d_in(D), .d_out(D0));
PipelineRegister #(8,OPMODEREG,  RSTTYPE) OPMODE_stage (.clk(clk), .rst(RSTOPMODE), .ce(CEOPMODE), .d_in(OPMODE), .d_out(OPMODE0));
PipelineRegister #(1,CARRYINREG,  RSTTYPE) CARRYIN_stage (.clk(clk), .rst(RSTCARRYIN), .ce(CECARRYIN), .d_in(CARRY0), .d_out(CIN));
PipelineRegister #(36,MREG,  RSTTYPE) M_stage (.clk(clk), .rst(RSTM), .ce(CEM), .d_in(multiplier_out), .d_out(M));
PipelineRegister #(48,PREG,  RSTTYPE) P_stage (.clk(clk), .rst(RSTP), .ce(CEP), .d_in(postadder_out), .d_out(P));
PipelineRegister #(1, CARRYINREG,  RSTTYPE) CARRYOUT_stage (.clk(clk), .rst(RSTCARRYIN),.ce(CECARRYIN), .d_in(CARRYOUT0), .d_out(CARRYOUT));
```

Arithmetic Block

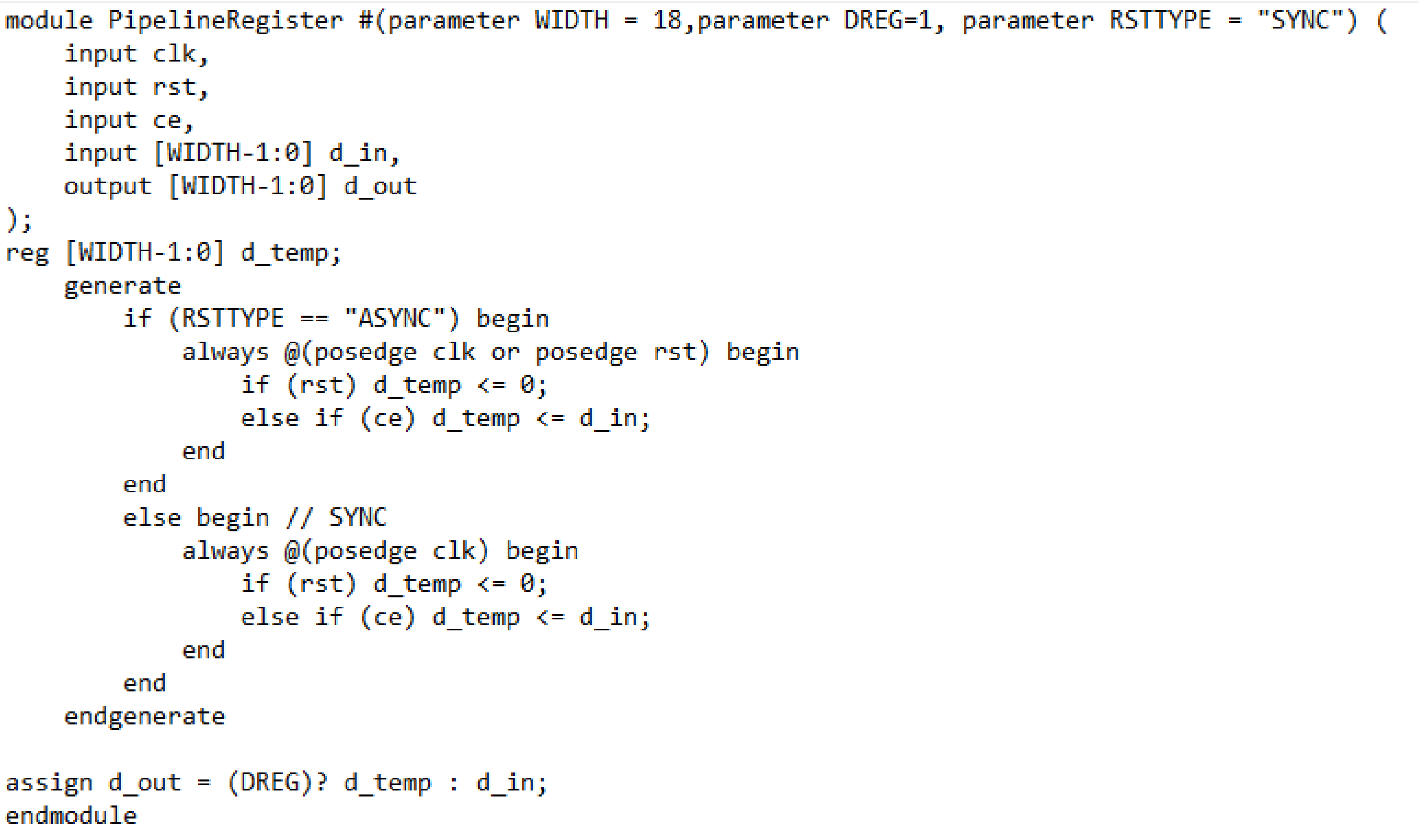


```
// Arithmetic operations
always @(*) begin
        case (OPMODE0[4])
            1'b0: preadder_out = B0;
            1'b1:
                if(OPMODE0[6]) preadder_out = D0 - B0;
                else preadder_out = D0 + B0;
        endcase

        case (OPMODE0[1:0])
                2'b00: X = 48'b0;
                2'b01: X = {12'b0,M};
                2'b10: X = P;
                2'b11: X = {D0[11:0], A1, B1};
        endcase

        case (OPMODE0[3:2])
                2'b00: Z = 48'b0;
                2'b01: Z = PCIN;
                2'b10: Z = P;
                2'b11: Z = C0;
        endcase

        case (OPMODE0[7])
                1'b0: {CARRYOUT0,postadder_out} = Z + (X + CIN);
                1'b1: {CARRYOUT0,postadder_out} = Z - (X + CIN);
        endcase

        if (CARRYINSEL == "OPMODE5")CARRY0 = OPMODE0[5];
        else if (CARRYINSEL == "CARRYIN")CARRY0 = CARRYIN;
        else CARRY0 = 1'b0; // Default case

        if (B_INPUT == "DIRECT")BIN = B;
        else if (B_INPUT == "CASCADE")BIN = BCIN;
        else BIN = 18'b0; // Default case

end
```



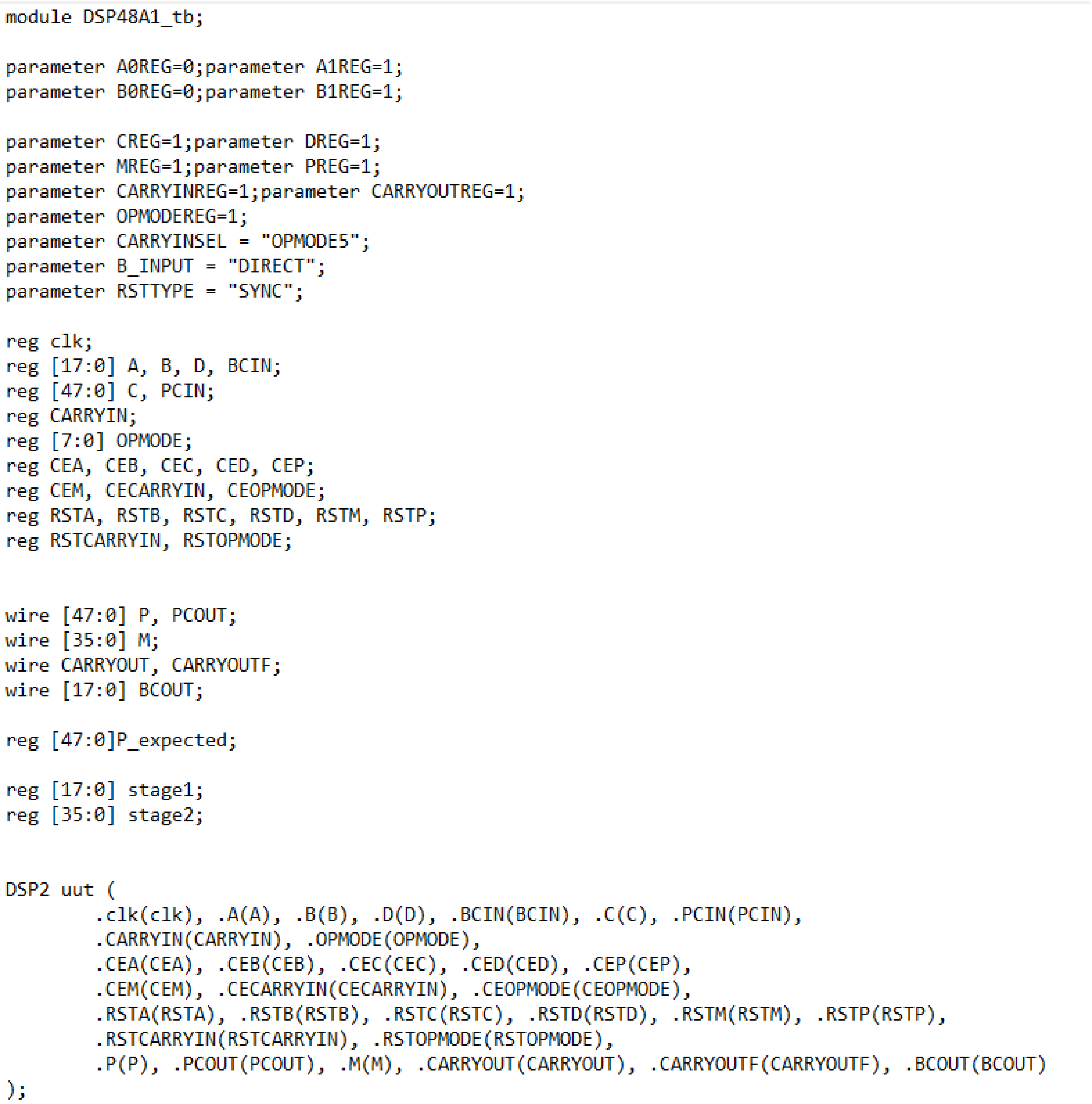
```
// Multiplier logic
assign multiplier_out = B1 * A1;


assign CARRYOUTF = CARRYOUT;
assign BCOUT = B1;
assign PCOUT = P;

endmodule
```

Register



```
module PipelineRegister #(parameter WIDTH = 18,parameter DREG=1, parameter RSTTYPE = "SYNC") (
    input clk,
    input rst,
    input ce,
    input [WIDTH-1:0] d_in,
    output [WIDTH-1:0] d_out
);
reg [WIDTH-1:0] d_temp;
    generate
        if (RSTTYPE == "ASYNC") begin
            always @(posedge clk or posedge rst) begin
                if (rst) d_temp <= 0;
                else if (ce) d_temp <= d_in;
            end
        end
        else begin // SYNC
            always @(posedge clk) begin
                if (rst) d_temp <= 0;
                else if (ce) d_temp <= d_in;
            end
        end
    endgenerate

assign d_out = (DREG)? d_temp : d_in;
endmodule
```

2. Testbench

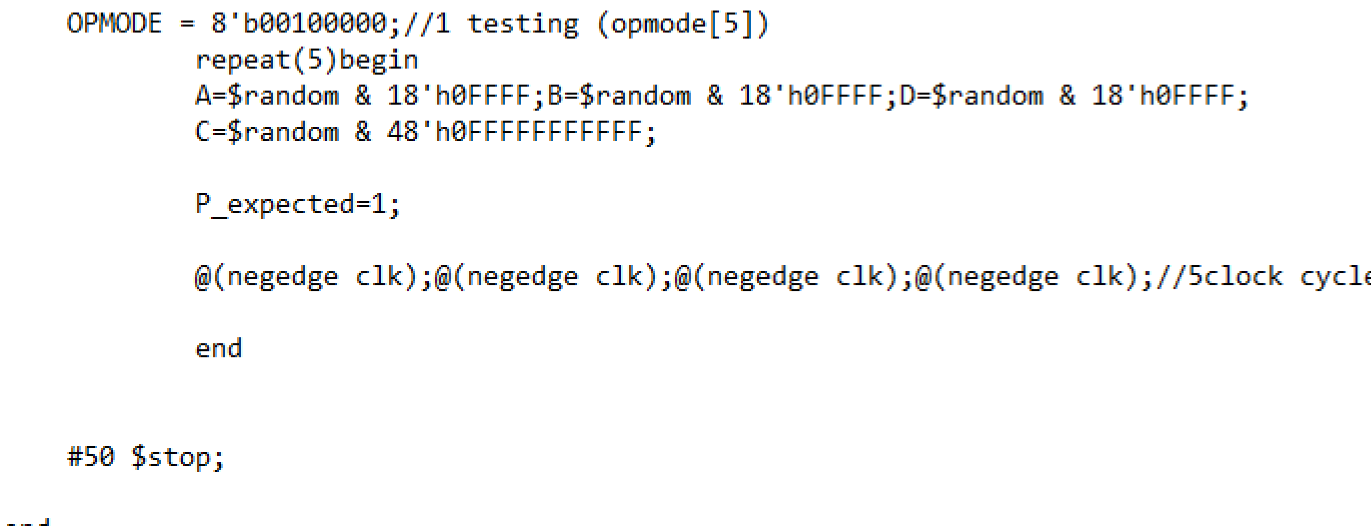


```
module DSP48A1_tb;

parameter A0REG=0;parameter A1REG=1;
parameter B0REG=0;parameter B1REG=1;

parameter CREG=1;parameter DREG=1;
parameter MREG=1;parameter PREG=1;
parameter CARRYINREG=1;parameter CARRYOUTREG=1;
parameter OPMODEREG=1;
parameter CARRYINSEL = "OPMODE5";
parameter B_INPUT = "DIRECT";
parameter RSTTYPE = "SYNC";

reg clk;
reg [17:0] A, B, D, BCIN;
reg [47:0] C, PCIN;
reg CARRYIN;
reg [7:0] OPMODE;
reg CEA, CEB, CEC, CED, CEP;
reg CEM, CECARRYIN, CEOPMODE;
reg RSTA, RSTB, RSTC, RSTD, RSTM, RSTP;
reg RSTCARRYIN, RSTOPMODE;


wire [47:0] P, PCOUT;
wire [35:0] M;
wire CARRYOUT, CARRYOUTF;
wire [17:0] BCOUT;

reg [47:0]P_expected;

reg [17:0] stage1;
reg [35:0] stage2;


DSP2 uut (
        .clk(clk), .A(A), .B(B), .D(D), .BCIN(BCIN), .C(C), .PCIN(PCIN),
        .CARRYIN(CARRYIN), .OPMODE(OPMODE),
        .CEA(CEA), .CEB(CEB), .CEC(CEC), .CED(CED), .CEP(CEP),
        .CEM(CEM), .CECARRYIN(CECARRYIN), .CEOPMODE(CEOPMODE),
        .RSTA(RSTA), .RSTB(RSTB), .RSTC(RSTC), .RSTD(RSTD), .RSTM(RSTM), .RSTP(RSTP),
        .RSTCARRYIN(RSTCARRYIN), .RSTOPMODE(RSTOPMODE),
        .P(P), .PCOUT(PCOUT), .M(M), .CARRYOUT(CARRYOUT), .CARRYOUTF(CARRYOUTF), .BCOUT(BCOUT)
);
```

```
initial begin
clk=0;
forever
#1 clk=~clk;
end

initial begin

        A = 18'd10; B = 18'd5; D = 18'd3; BCIN = 18'd2;
        C = 48'd20; PCIN = 48'd15;CARRYIN = 1'b0;
        OPMODE = 8'b00000001;

        RSTA = 1; RSTB = 1; RSTC = 1; RSTD = 1; RSTM = 1; RSTP = 1;
        RSTCARRYIN = 1; RSTOPMODE = 1;


@(negedge clk);
        RSTA = 0; RSTB = 0; RSTC = 0; RSTD = 0; RSTM = 0; RSTP = 0;
        RSTCARRYIN = 0; RSTOPMODE = 0;
        CEA = 1; CEB = 1; CEC = 1; CED = 1; CEP = 1;
        CEM = 1; CECARRYIN = 1; CEOPMODE = 1;

        // Apply various test cases for the first OPMODE


        //some initial indicaters to show they were used → constant
        PCIN = 48'hFFFF0000FFFF;BCIN = 18'd5;

        OPMODE = 8'b00000000; //p=0
                repeat(5)begin
                A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
                C=$random & 48'h0FFFFFFFFFFF;CARRYIN=$random;//avoiding overflow (preadder not optimized)

                P_expected=0;

                @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles
                                                                               ↳ 4
                end

        OPMODE = 8'b00000001; //p=M
                repeat(5)begin
                A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
                C=$random & 48'h0FFFFFFFFFFF;CARRYIN=$random;
                stage1= B;
                stage2= stage1*A;
                P_expected=stage2;

                @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

                end
```

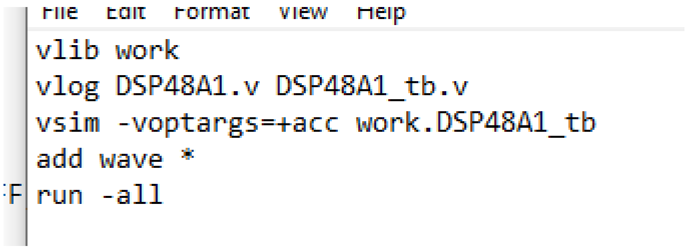
```
OPMODE = 8'b00000010;CARRYIN=0; //p=old p
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end

OPMODE = 8'b00000011;//p=concatenated
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;CARRYIN=$random;

        P_expected={D[11:0], A, B};

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end

OPMODE = 8'b00000111;//concatenated+pcin
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;CARRYIN=$random;

        P_expected={D[11:0], A, B}+PCIN;

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end

CARRYIN=0;//no longer randomizing carry
OPMODE = 8'b00001101;//M+C
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;
        stage1= B;
        stage2= stage1*A;
        P_expected=stage2+C;

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end
```

```
OPMODE = 8'b00011101;//((B+D)*A)+C
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;
        stage1= B+D;
        stage2= stage1*A;
        P_expected=stage2+C;

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end

OPMODE = 8'b01010101;//PCIN+((D-B)*A)
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;
        stage1= D-B;
        stage2= stage1*A;
        P_expected=PCIN+stage2;

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end

OPMODE = 8'b11010101;//PCIN-((D-B)*A)
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;

        stage1= D-B;
        stage2= stage1*A;
        P_expected=PCIN-stage2;

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end

OPMODE = 8'b10101101;//C-((B*A)+1)
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;

        stage1= B;
        stage2= stage1*A;
        P_expected=(C)-(stage2+1);

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end
```



```
    OPMODE = 8'b00100000;//1 testing (opmode[5])
            repeat(5)begin
            A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
            C=$random & 48'h0FFFFFFFFFFF;

            P_expected=1;

            @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycle

            end


    #50 $stop;

end
```

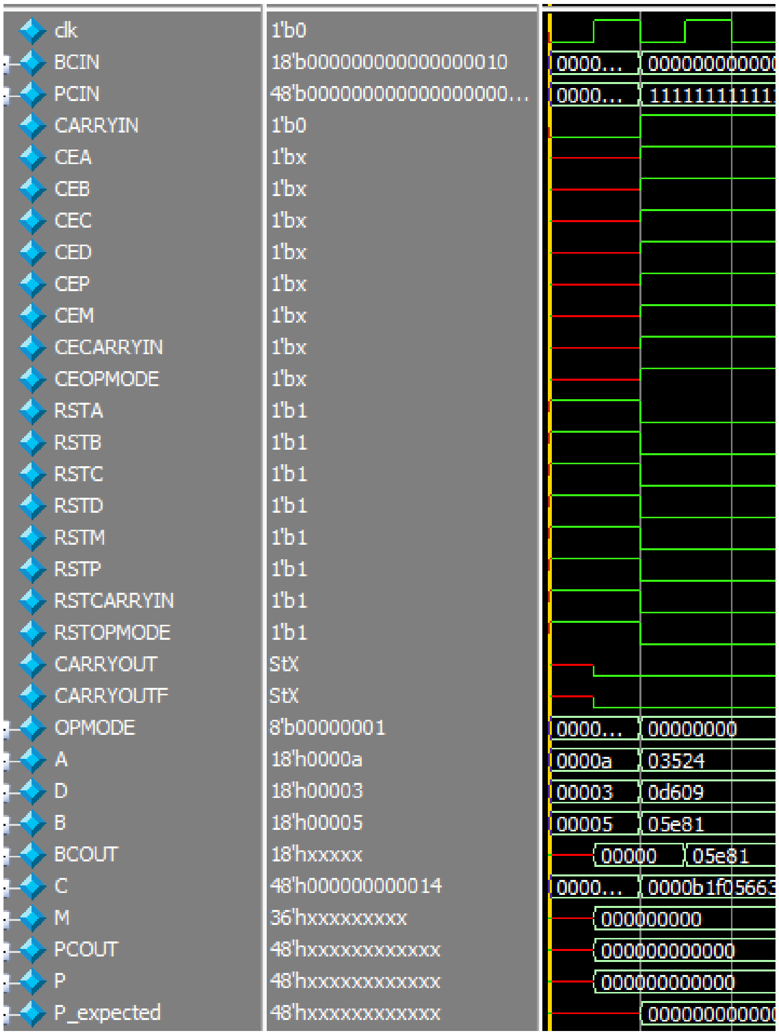
3. Do file



```
vlib work
vlog DSP48A1.v DSP48A1_tb.v
vsim -voptargs=+acc work.DSP48A1_tb
add wave *
run -all
```

4. QuestaSim waveform snippets

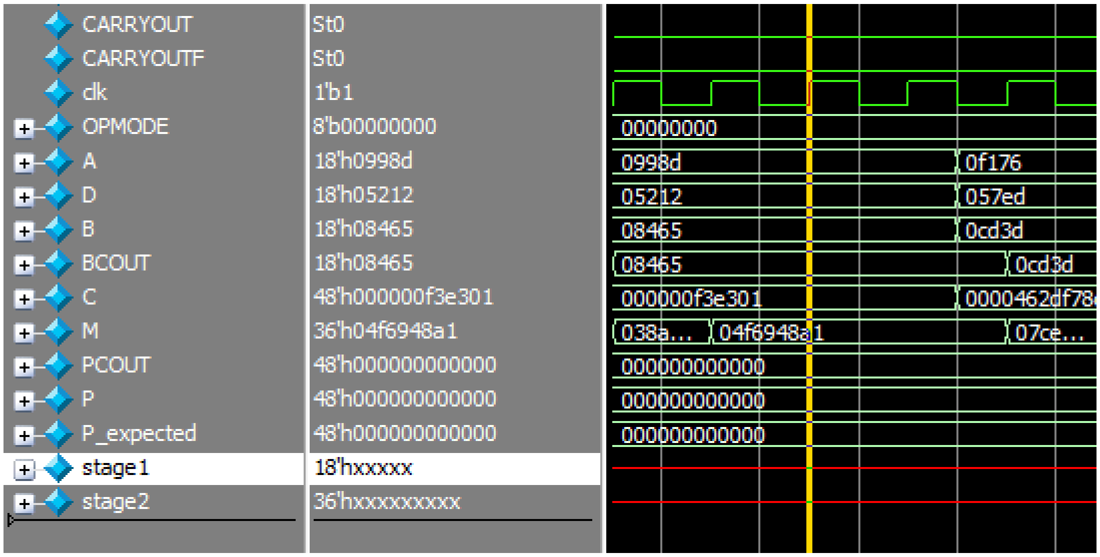
Reset



clk	1'b0
BCIN	18'b000000000000000010
PCIN	48'b0000000000000000000...
CARRYIN	1'b0
CEA	1'bx
CEB	1'bx
CEC	1'bx
CED	1'bx
CEP	1'bx
CEM	1'bx
CECARRYIN	1'bx
CEOPMODE	1'bx
RSTA	1'b1
RSTB	1'b1
RSTC	1'b1
RSTD	1'b1
RSTM	1'b1
RSTP	1'b1
RSTCARRYIN	1'b1
RSTOPMODE	1'b1
CARRYOUT	StX
CARRYOUTF	StX
OPMODE	8'b00000001
A	18'h0000a
D	18'h00003
B	18'h00005
BCOUT	18'hxxxxx
C	48'h000000000014
M	36'hxxxxxxxxx
PCOUT	48'hxxxxxxxxxxxx
P	48'hxxxxxxxxxxxx
P_expected	48'hxxxxxxxxxxxx

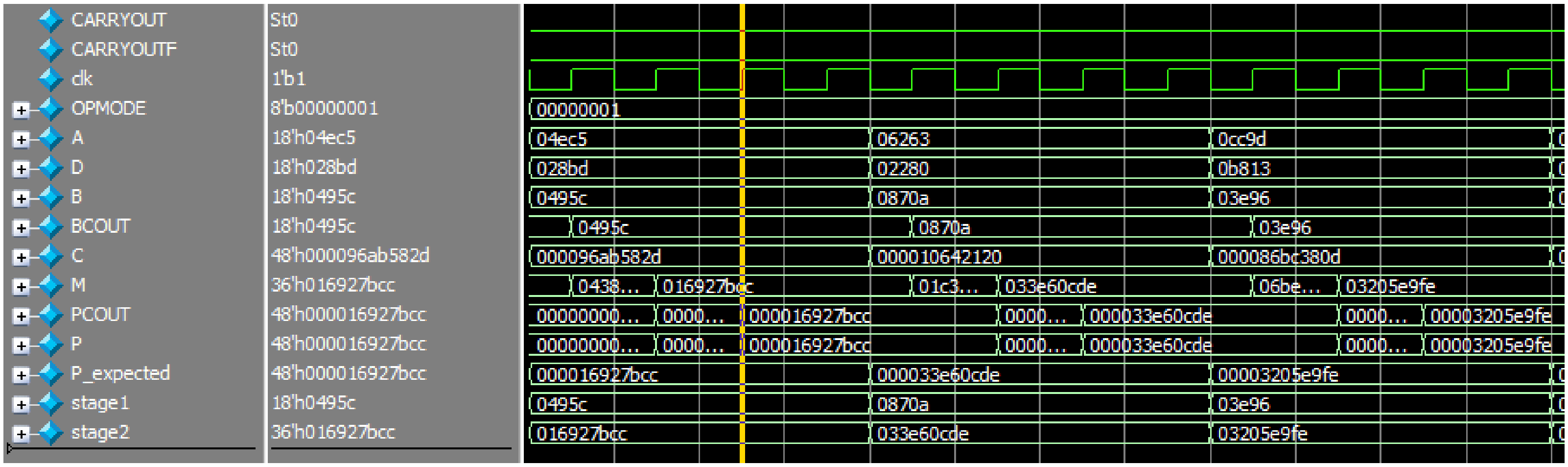
```
initial begin

        A = 18'd10; B = 18'd5; D = 18'd3; BCIN = 18'd2;
        C = 48'd20; PCIN = 48'd15;CARRYIN = 1'b0;
        OPMODE = 8'b00000001;

        RSTA = 1; RSTB = 1; RSTC = 1; RSTD = 1; RSTM = 1; RSTP = 1;
        RSTCARRYIN = 1; RSTOPMODE = 1;


@(negedge clk);
        RSTA = 0; RSTB = 0; RSTC = 0; RSTD = 0; RSTM = 0; RSTP = 0;
        RSTCARRYIN = 0; RSTOPMODE = 0;
        CEA = 1; CEB = 1; CEC = 1; CED = 1; CEP = 1;
        CEM = 1; CECARRYIN = 1; CEOPMODE = 1;
```

```
//some initial indicaters to show they were used
PCIN = 48'hFFFF0000FFFF;BCIN = 18'd5;

OPMODE = 8'b00000000; //p=0
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;CARRYIN=$random;//avoiding overflow (preadder not optimized)

        P_expected=0;

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end
```



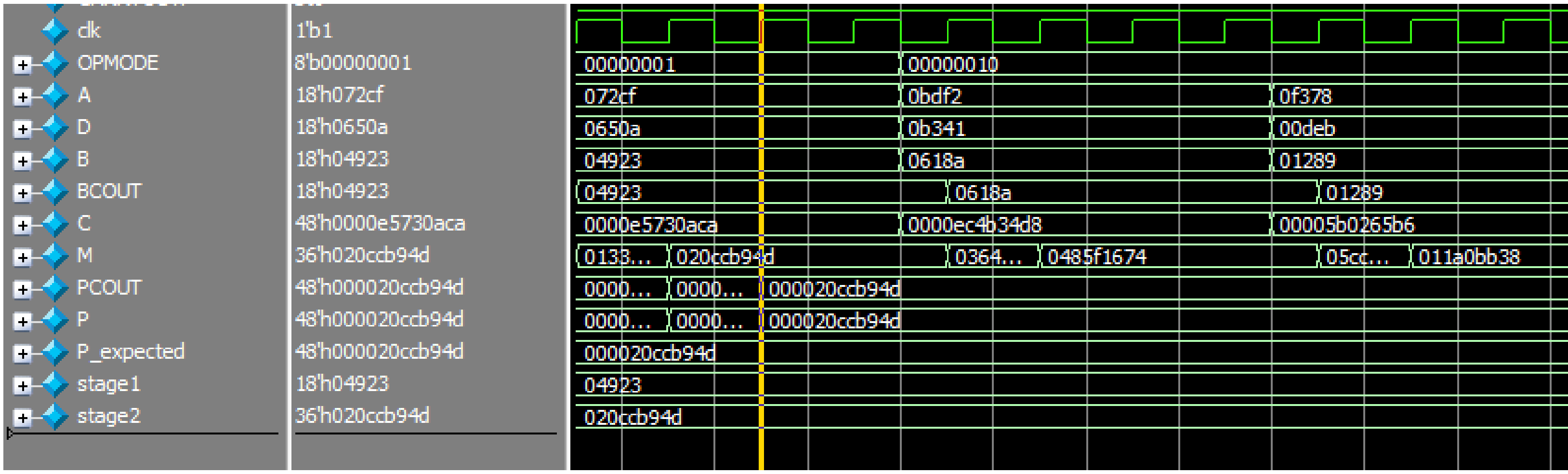
```
CARRYOUT     St0
CARRYOUTF    St0
clk          1'b1
OPMODE       8'b00000000
A            18'h0998d
D            18'h05212
B            18'h08465
BCOUT        18'h08465
C            48'h000000f3e301
M            36'h04f6948a1
PCOUT        48'h000000000000
P            48'h000000000000
P_expected   48'h000000000000
stage1       18'hxxxxx
stage2       36'hxxxxxxxxx
```

```
OPMODE = 8'b00000001; //p=M
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;CARRYIN=$random;
        stage1= B;
        stage2= stage1*A;
        P_expected=stage2;

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end
```



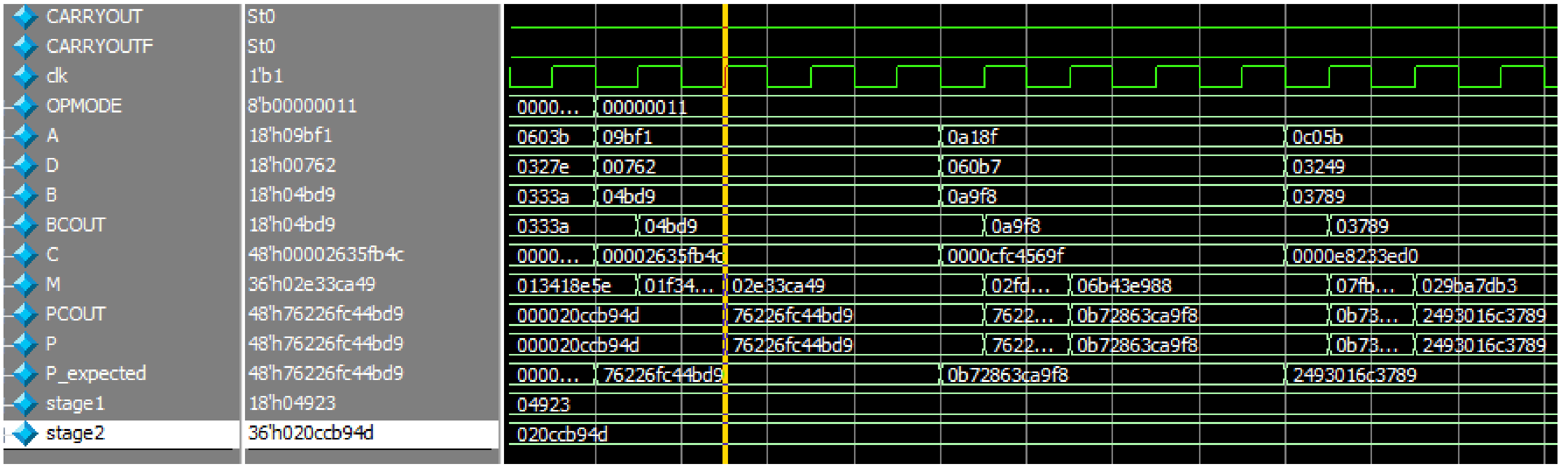
```
CARRYOUT     St0
CARRYOUTF    St0
clk          1'b1
OPMODE       8'b00000001         00000001
A            18'h04ec5           04ec5          06263          0cc9d
D            18'h028bd           028bd          02280          0b813
B            18'h0495c           0495c          0870a          03e96
BCOUT        18'h0495c           0495c          0870a          03e96
C            48'h000096ab582d    000096ab582d   000010642120   000086bc380d
M            36'h016927bcc       0438... 016927bcc   01c3... 033e60cde   06be... 03205e9fe
PCOUT        48'h000016927bcc    00000000... 0000... 000016927bcc   0000... 000033e60cde   0000... 00003205e9fe
P            48'h000016927bcc    00000000... 0000... 000016927bcc   0000... 000033e60cde   0000... 00003205e9fe
P_expected   48'h000016927bcc    000016927bcc   000033e60cde   00003205e9fe
stage1       18'h0495c           0495c          0870a          03e96
stage2       36'h016927bcc       016927bcc      033e60cde      03205e9fe
```

```
OPMODE = 8'b00000010;CARRYIN=0; //p=old p
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end
```



```
clk          1'b1
OPMODE       8'b00000001         00000001       00000010
A            18'h072cf           072cf          0bdf2          0f378
D            18'h0650a           0650a          0b341          00deb
B            18'h04923           04923          0618a          01289
BCOUT        18'h04923           04923          0618a          01289
C            48'h0000e5730aca    0000e5730aca   0000ec4b34d8   00005b0265b6
M            36'h020ccb94d       0133... 020ccb94d   0364... 0485f1674   05cc... 011a0bb38
PCOUT        48'h000020ccb94d    0000... 0000... 000020ccb94d
P            48'h000020ccb94d    0000... 0000... 000020ccb94d
P_expected   48'h000020ccb94d    000020ccb94d
stage1       18'h04923           04923
stage2       36'h020ccb94d       020ccb94d
```

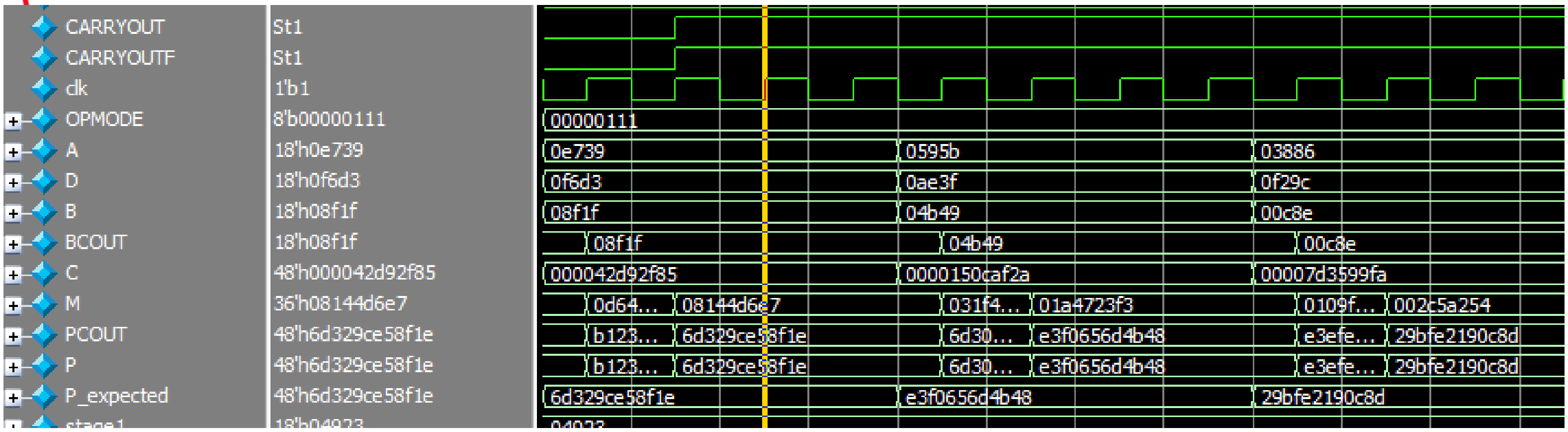
```
OPMODE = 8'b00000011;//p=concatenated
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;CARRYIN=$random;

        P_expected={D[11:0], A, B};

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end
```



```
CARRYOUT     St0
CARRYOUTF    St0
clk          1'b1
OPMODE       8'b00000011        0000...  00000011
A            18'h09bf1          0603b  09bf1  0a18f  0c05b
D            18'h00762          0327e  00762  060b7  03249
B            18'h04bd9          0333a  04bd9  0a9f8  03789
BCOUT        18'h04bd9          0333a  04bd9  0a9f8  03789
C            48'h00002635fb4c   0000...  00002635fb4c  0000cfc4569f  0000e8233ed0
M            36'h02e33ca49      013418e5e  01f34...  02e33ca49  02fd...  06b43e988  07fb...  029ba7db3
PCOUT        48'h76226fc44bd9   000020ccb94d  76226fc44bd9  7622...  0b72863ca9f8  0b73...  2493016c3789
P            48'h76226fc44bd9   000020ccb94d  76226fc44bd9  7622...  0b72863ca9f8  0b73...  2493016c3789
P_expected   48'h76226fc44bd9   0000...  76226fc44bd9  0b72863ca9f8  2493016c3789
stage1       18'h04923          04923
stage2       36'h020ccb94d      020ccb94d
```

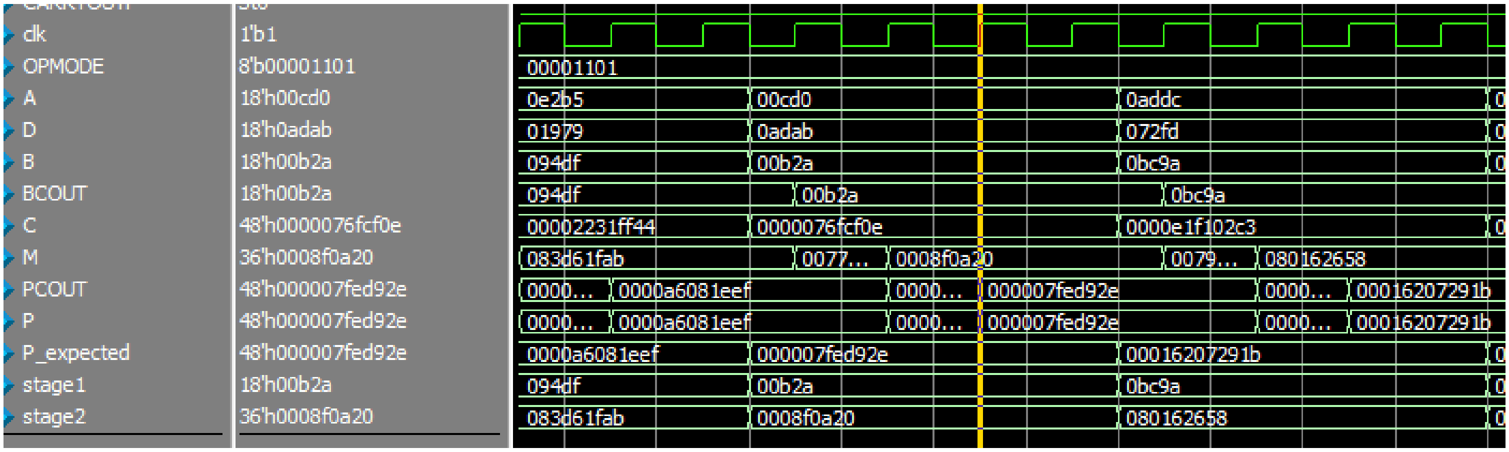
```
OPMODE = 8'b00000111;//concatenated+pcin
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;CARRYIN=$random;

        P_expected={D[11:0], A, B}+PCIN;

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end
```

1



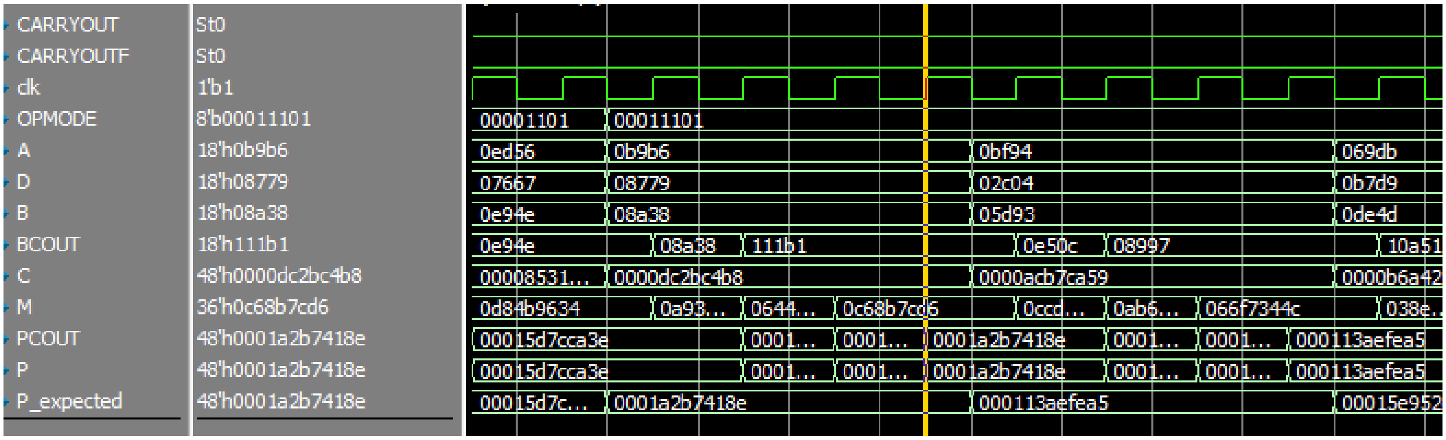
```
CARRYOUT     St1
CARRYOUTF    St1
clk          1'b1
OPMODE       8'b00000111        00000111
A            18'h0e739          0e739  0595b  03886
D            18'h0f6d3          0f6d3  0ae3f  0f29c
B            18'h08f1f          08f1f  04b49  00c8e
BCOUT        18'h08f1f          08f1f  04b49  00c8e
C            48'h000042d92f85   000042d92f85  0000150caf2a  00007d3599fa
M            36'h08144d6e7      0d64...  08144d6e7  031f4...  01a4723f3  0109f...  002c5a254
PCOUT        48'h6d329ce58f1e   b123...  6d329ce58f1e  6d30...  e3f0656d4b48  e3efe...  29bfe2190c8d
P            48'h6d329ce58f1e   b123...  6d329ce58f1e  6d30...  e3f0656d4b48  e3efe...  29bfe2190c8d
P_expected   48'h6d329ce58f1e   6d329ce58f1e  e3f0656d4b48  29bfe2190c8d
stage1       18'h04923          04923
```

```
CARRYIN=0;//no longer randomizing carry
OPMODE = 8'b00001101;//M+C
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;
        stage1= B;
        stage2= stage1*A;
        P_expected=stage2+C;

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end
```



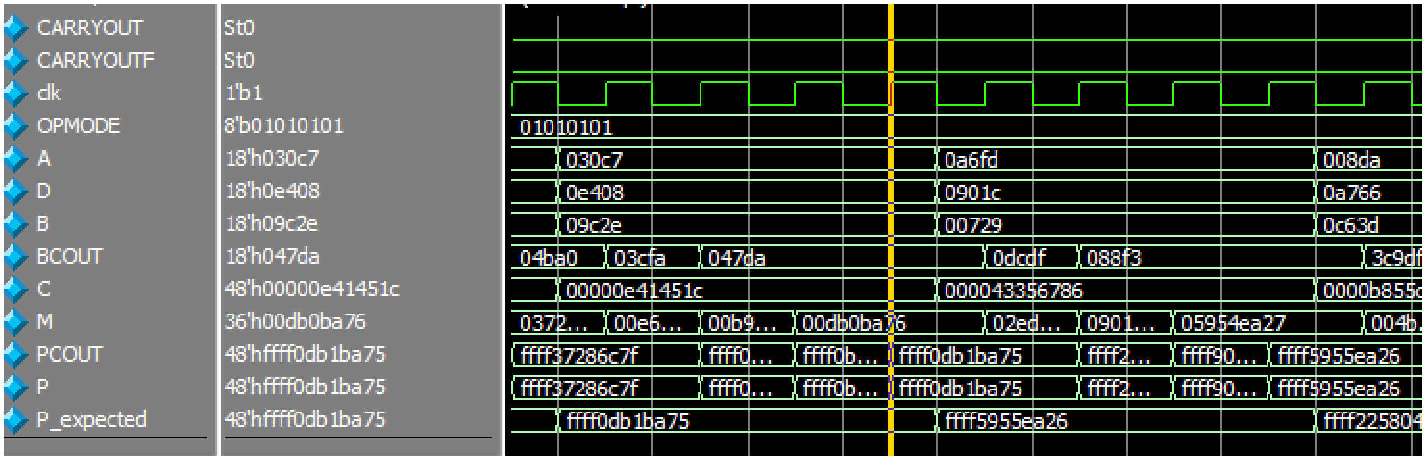
```
clk          1'b1
OPMODE       8'b00001101
A            18'h00cd0
D            18'h0adab
B            18'h00b2a
BCOUT        18'h00b2a
C            48'h0000076fcf0e
M            36'h0008f0a20
PCOUT        48'h000007fed92e
P            48'h000007fed92e
P_expected   48'h000007fed92e
stage1       18'h00b2a
stage2       36'h0008f0a20
```

```
OPMODE = 8'b00011101;//((B+D)*A)+C
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;
        stage1= B+D;
        stage2= stage1*A;
        P_expected=stage2+C;

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end
```



```
CARRYOUT     St0
CARRYOUTF    St0
clk          1'b1
OPMODE       8'b00011101
A            18'h0b9b6
D            18'h08779
B            18'h08a38
BCOUT        18'h111b1
C            48'h0000dc2bc4b8
M            36'h0c68b7cd6
PCOUT        48'h0001a2b7418e
P            48'h0001a2b7418e
P_expected   48'h0001a2b7418e
```

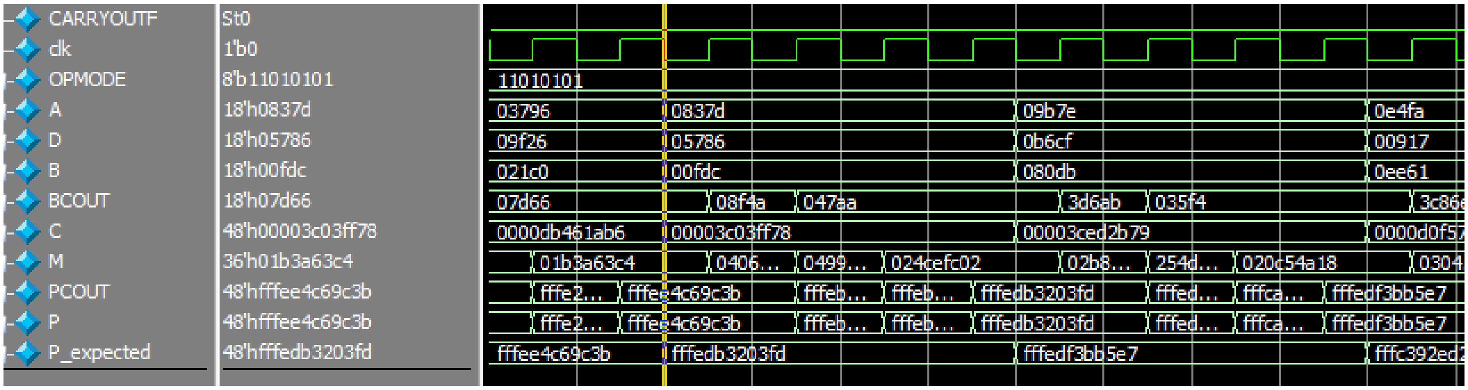
```
OPMODE = 8'b01010101;//PCIN+((D-B)*A)
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;
        stage1= D-B;
        stage2= stage1*A;
        P_expected=PCIN+stage2;

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end
```



```
CARRYOUT     St0
CARRYOUTF    St0
clk          1'b1
OPMODE       8'b01010101
A            18'h030c7
D            18'h0e408
B            18'h09c2e
BCOUT        18'h047da
C            48'h00000e41451c
M            36'h00db0ba76
PCOUT        48'hffff0db1ba75
P            48'hffff0db1ba75
P_expected   48'hffff0db1ba75
```

01010101
030c7 0a6fd 008da
0e408 0901c 0a766
09c2e 00729 0c63d
04ba0 03cfa 047da 0dcdf 088f3 3c9df
00000e41451c 000043356786 0000b855c
0372... 00e6... 00b9... 00db0ba76 02ed... 0901... 05954ea27 004b.
ffff37286c7f ffff0... ffff0b... ffff0db1ba75 ffff2... ffff90... ffff5955ea26
ffff37286c7f ffff0... ffff0b... ffff0db1ba75 ffff2... ffff90... ffff5955ea26
ffff0db1ba75 ffff5955ea26 ffff225804

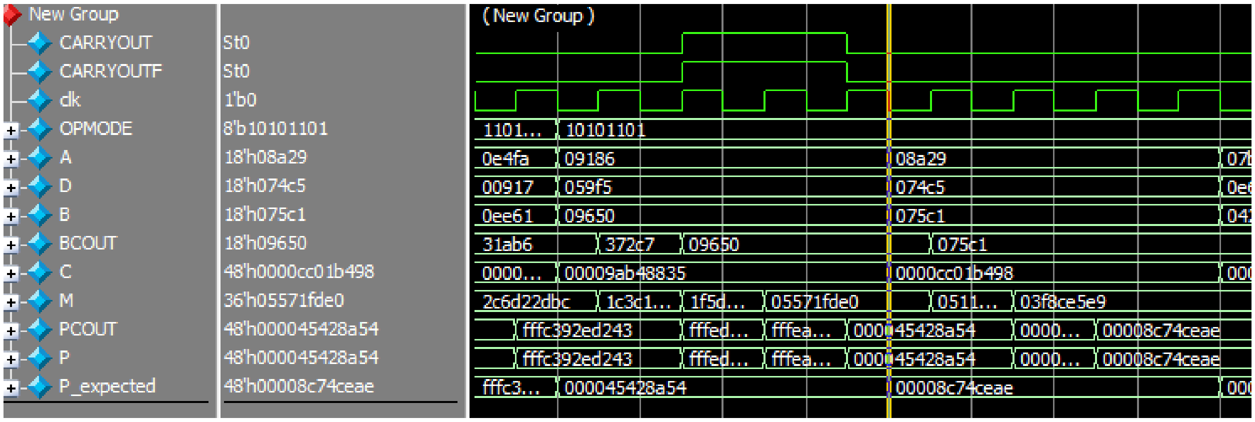
```
OPMODE = 8'b11010101;//PCIN-((D-B)*A)
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;

        stage1= D-B;
        stage2= stage1*A;
        P_expected=PCIN-stage2;

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end
```



```
CARRYOUTF    St0
clk          1'b0
OPMODE       8'b11010101
A            18'h0837d
D            18'h05786
B            18'h00fdc
BCOUT        18'h07d66
C            48'h00003c03ff78
M            36'h01b3a63c4
PCOUT        48'hfffee4c69c3b
P            48'hfffee4c69c3b
P_expected   48'hfffedb3203fd
```

11010101
03796 0837d 09b7e 0e4fa
09f26 05786 0b6cf 00917
021c0 00fdc 080db 0ee61
07d66 08f4a 047aa 3d6ab 035f4 3c86
0000db461ab6 00003c03ff78 00003ced2b79 0000d0f57
01b3a63c4 0406... 0499... 024cefc02 02b8... 254d... 020c54a18 0304
fffe2... fffee4c69c3b fffeb... fffeb... fffedb3203fd fffed... fffca... fffedf3bb5e7
fffe2... fffee4c69c3b fffeb... fffeb... fffedb3203fd fffed... fffca... fffedf3bb5e7
fffee4c69c3b fffedb3203fd fffedf3bb5e7 fffc392ed2

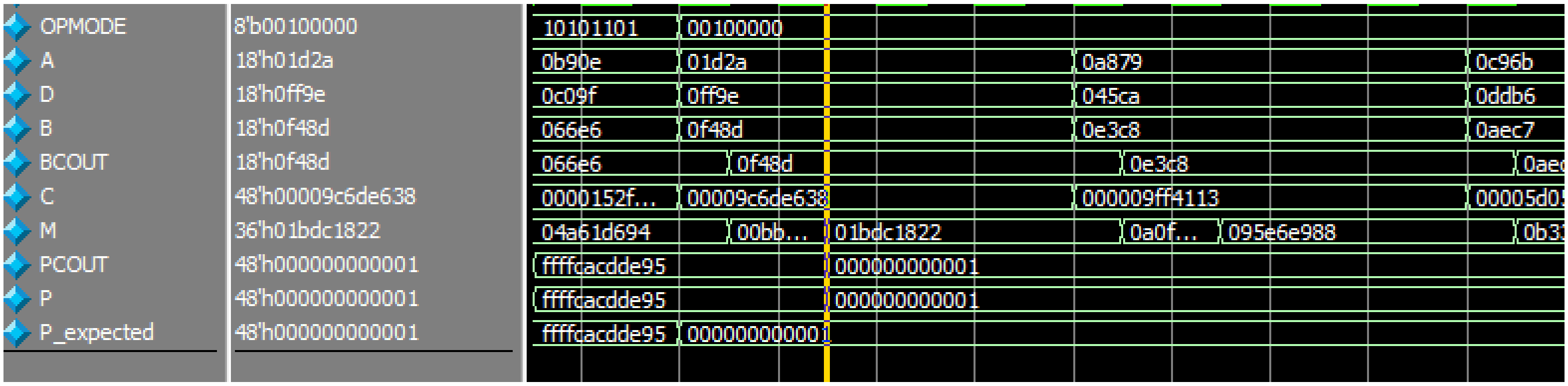
```
OPMODE = 8'b10101101;//C-((B*A)+1)
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;

        stage1= B;
        stage2= stage1*A;
        P_expected=(C)-(stage2+1);

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end
```



```
New Group
CARRYOUT      St0
CARRYOUTF     St0
clk           1'b0
OPMODE        8'b10101101
A             18'h08a29
D             18'h074c5
B             18'h075c1
BCOUT         18'h09650
C             48'h0000cc01b498
M             36'h05571fde0
PCOUT         48'h000045428a54
P             48'h000045428a54
P_expected    48'h00008c74ceae
```

(New Group)
1101... 10101101
0e4fa 09186 08a29 07b
00917 059f5 074c5 0e6
0ee61 09650 075c1 042
31ab6 372c7 09650 075c1
0000... 00009ab48835 0000cc01b498 000
2c6d22dbc 1c3c1... 1f5d... 05571fde0 0511... 03f8ce5e9
fffc392ed243 fffed... fffea... 000045428a54 0000... 00008c74ceae
fffc392ed243 fffed... fffea... 000045428a54 0000... 00008c74ceae
fffc3... 000045428a54 00008c74ceae 000

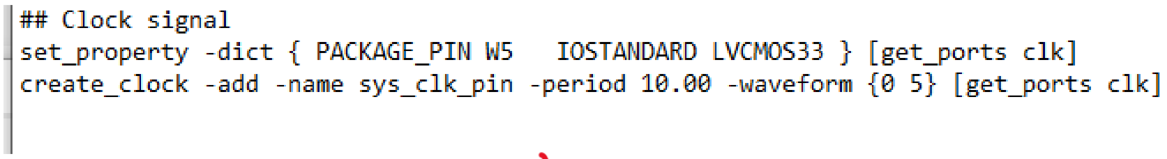
```
OPMODE = 8'b00100000;//1 testing (opmode[5])
        repeat(5)begin
        A=$random & 18'h0FFFF;B=$random & 18'h0FFFF;D=$random & 18'h0FFFF;
        C=$random & 48'h0FFFFFFFFFFF;

        P_expected=1;

        @(negedge clk);@(negedge clk);@(negedge clk);@(negedge clk);//5clock cycles

        end
```



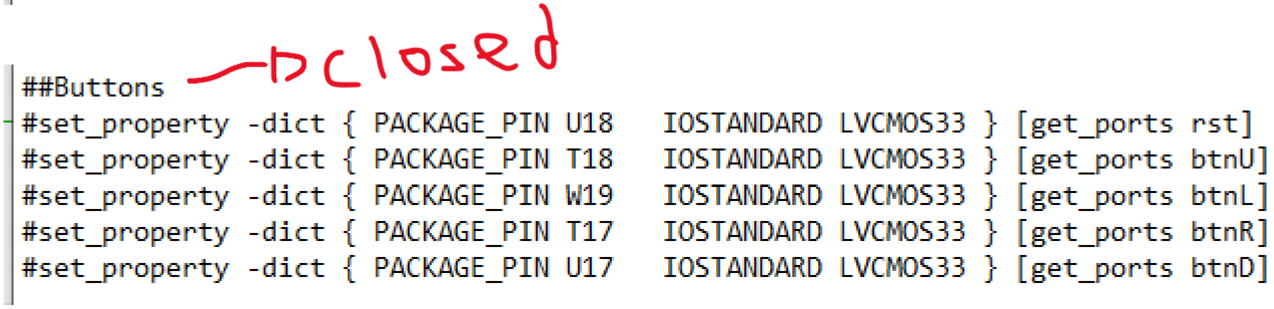
```
OPMODE        8'b00100000
A             18'h01d2a
D             18'h0ff9e
B             18'h0f48d
BCOUT         18'h0f48d
C             48'h00009c6de638
M             36'h01bdc1822
PCOUT         48'h000000000001
P             48'h000000000001
P_expected    48'h000000000001
```

10101101 00100000
0b90e 01d2a 0a879 0c96b
0c09f 0ff9e 045ca 0ddb6
066e6 0f48d 0e3c8 0aec7
066e6 0f48d 0e3c8 0aec
0000152f... 00009c6de638 000009ff4113 00005d0
04a61d694 00bb... 01bdc1822 0a0f... 095e6e988 0b3
ffffcacdde95 000000000001
ffffcacdde95 000000000001
ffffcacdde95 000000000001

5.Constraint File



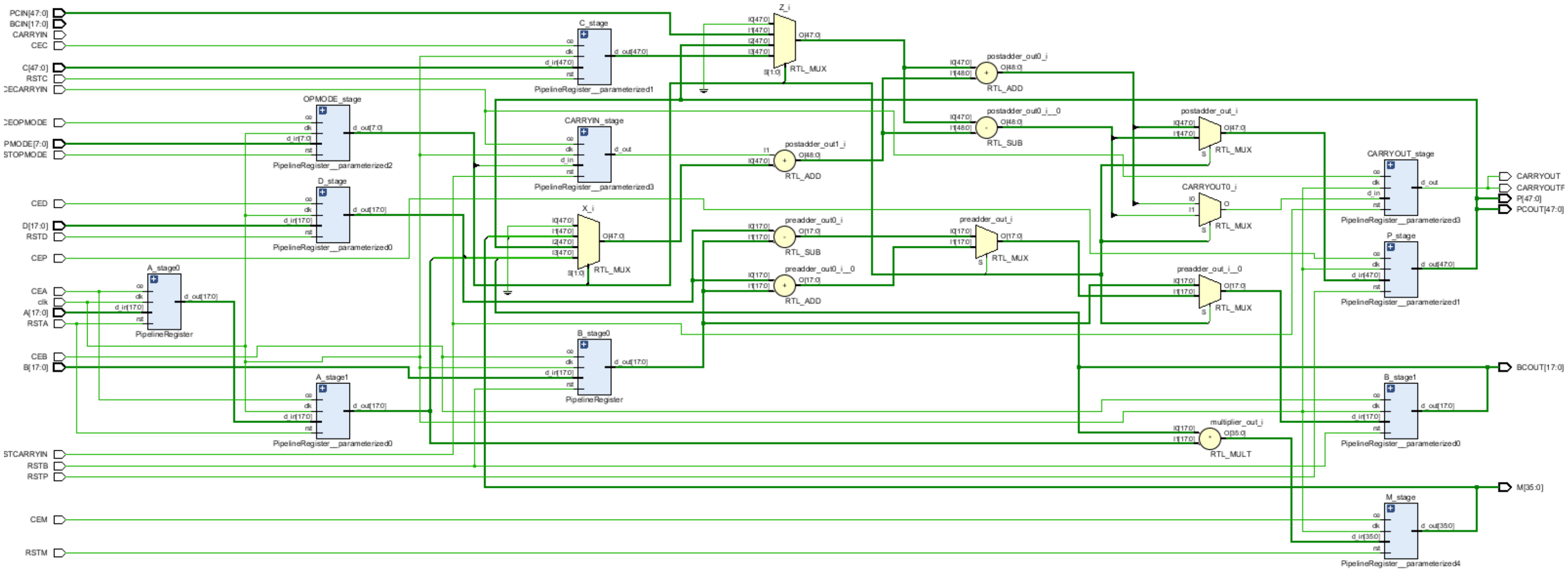
```
## Clock signal
set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports clk]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
```

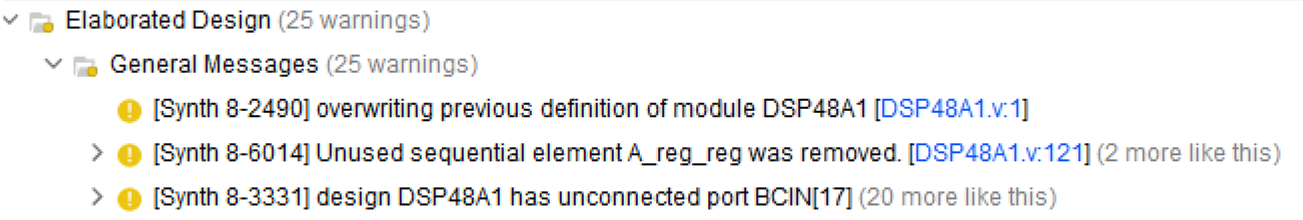


closed

```
##Buttons
#set_property -dict { PACKAGE_PIN U18   IOSTANDARD LVCMOS33 } [get_ports rst]
#set_property -dict { PACKAGE_PIN T18   IOSTANDARD LVCMOS33 } [get_ports btnU]
#set_property -dict { PACKAGE_PIN W19   IOSTANDARD LVCMOS33 } [get_ports btnL]
#set_property -dict { PACKAGE_PIN T17   IOSTANDARD LVCMOS33 } [get_ports btnR]
#set_property -dict { PACKAGE_PIN U17   IOSTANDARD LVCMOS33 } [get_ports btnD]
```

6.Elaboration





Elaborated Design (25 warnings)

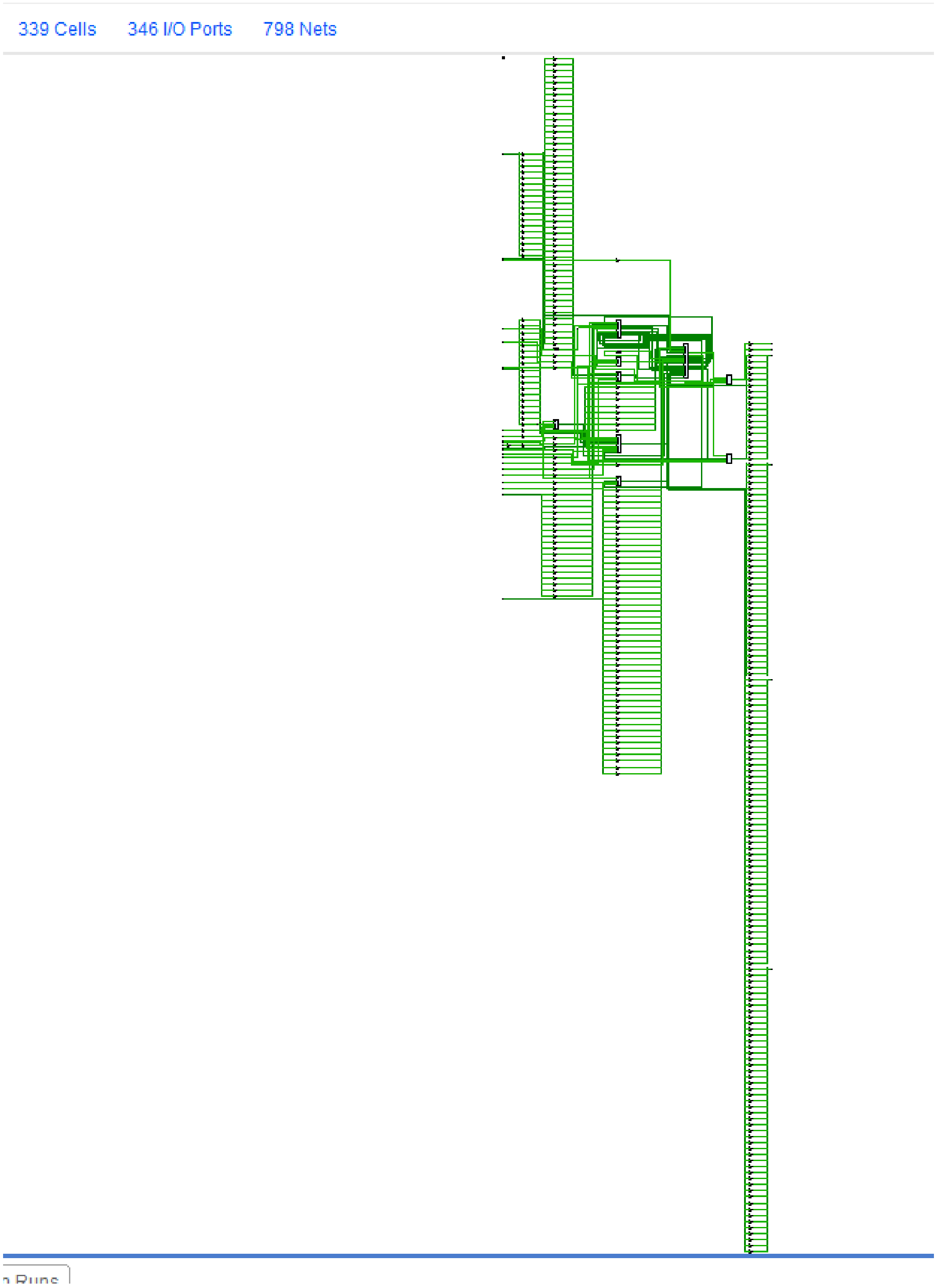
General Messages (25 warnings)

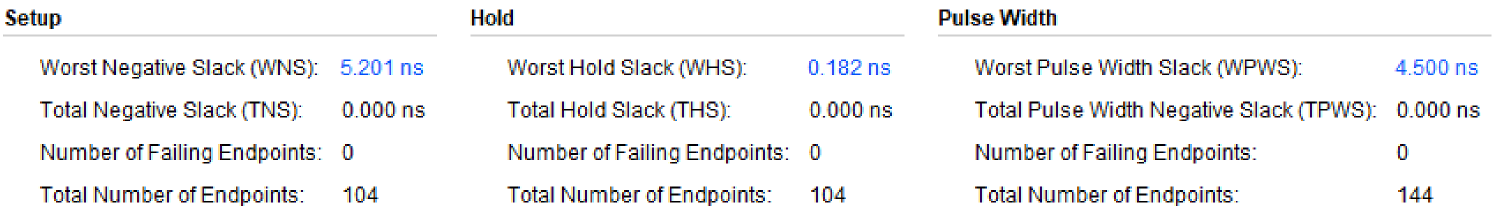
[Synth 8-2490] overwriting previous definition of module DSP48A1 [DSP48A1.v:1]

[Synth 8-6014] Unused sequential element A_reg_reg was removed. [DSP48A1.v:121] (2 more like this)

[Synth 8-3331] design DSP48A1 has unconnected port BCIN[17] (20 more like this)

7.Synthesis





Setup

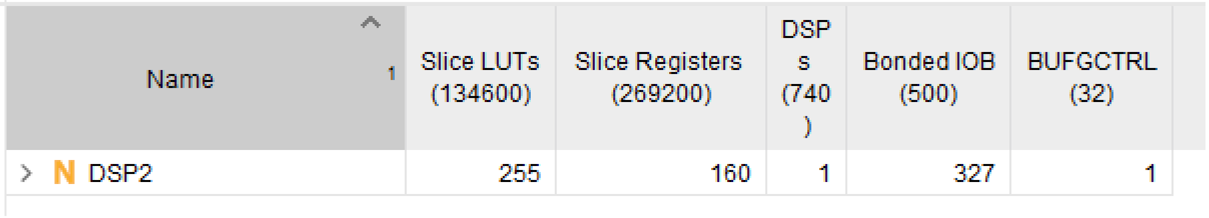
Worst Negative Slack (WNS):	5.201 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	104

Hold

Worst Hold Slack (WHS):	0.182 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	104

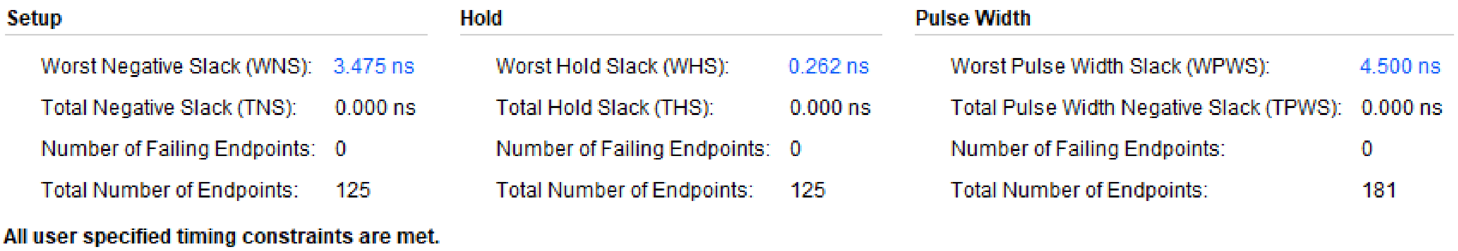
Pulse Width

Worst Pulse Width Slack (WPWS):	4.500 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	144



Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
› N DSP2	255	160	1	327	1

8.Implementation



Setup

Worst Negative Slack (WNS):	3.475 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	125

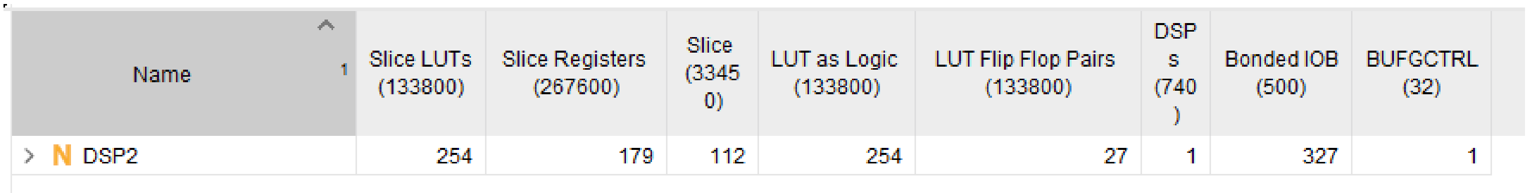
Hold

Worst Hold Slack (WHS):	0.262 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	125

Pulse Width

Worst Pulse Width Slack (WPWS):	4.500 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	181

All user specified timing constraints are met.



Name	Slice LUTs (133800)	Slice Registers (267600)	Slice (33450)	LUT as Logic (133800)	LUT Flip Flop Pairs (133800)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
› N DSP2	254	179	112	254	27	1	327	1