Design and Simulation of a Differential Amplifier with Resistive Load Using Electric EDA Tool

AIM:

To design and simulate a differential amplifier with resistive load using transistors in the Electric EDA tool, and to develop its layout and 3D model for VLSI chip design applications.

PROJECT DESIGN SPECIFICATION:

OBJECTIVE:

To design, simulate, and analyze a differential amplifier using NMOS transistors with PMOS active loads and a current source biasing circuit, suitable for analog signal amplification in integrated circuits

SPECIFICATIONS:

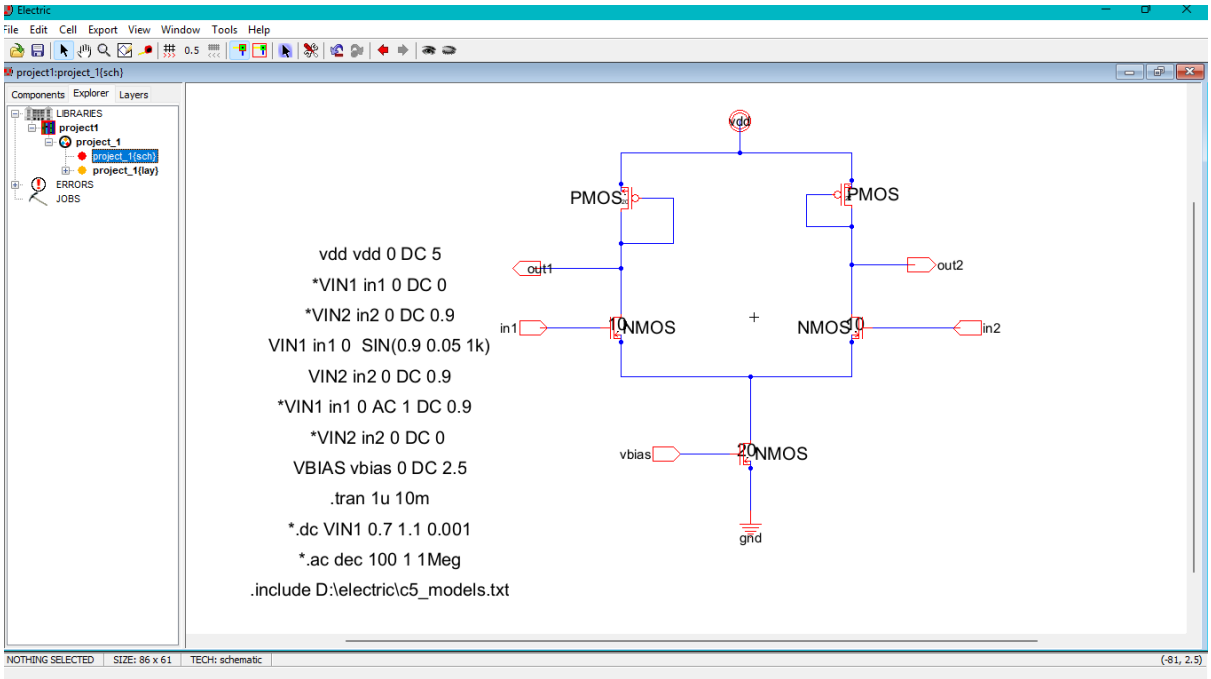
- **Technology**: Transistor-level design using Electric VLSI Design System
- **Power Supply (Vdd)**: 5V
- **Input**: Two differential input signals (in1, in2)
- **Load Type**: PMOS transistors configured to act as active loads (high-resistance current sources)
- **Biasing**: NMOS transistor as current source, biased by a fixed Vbias 2.5
- **Transistors Used**:
    - 2 NMOS transistors for differential input pair
    - 1 NMOS as tail current source
    - 2 PMOS transistors as active loads (instead of resistors)

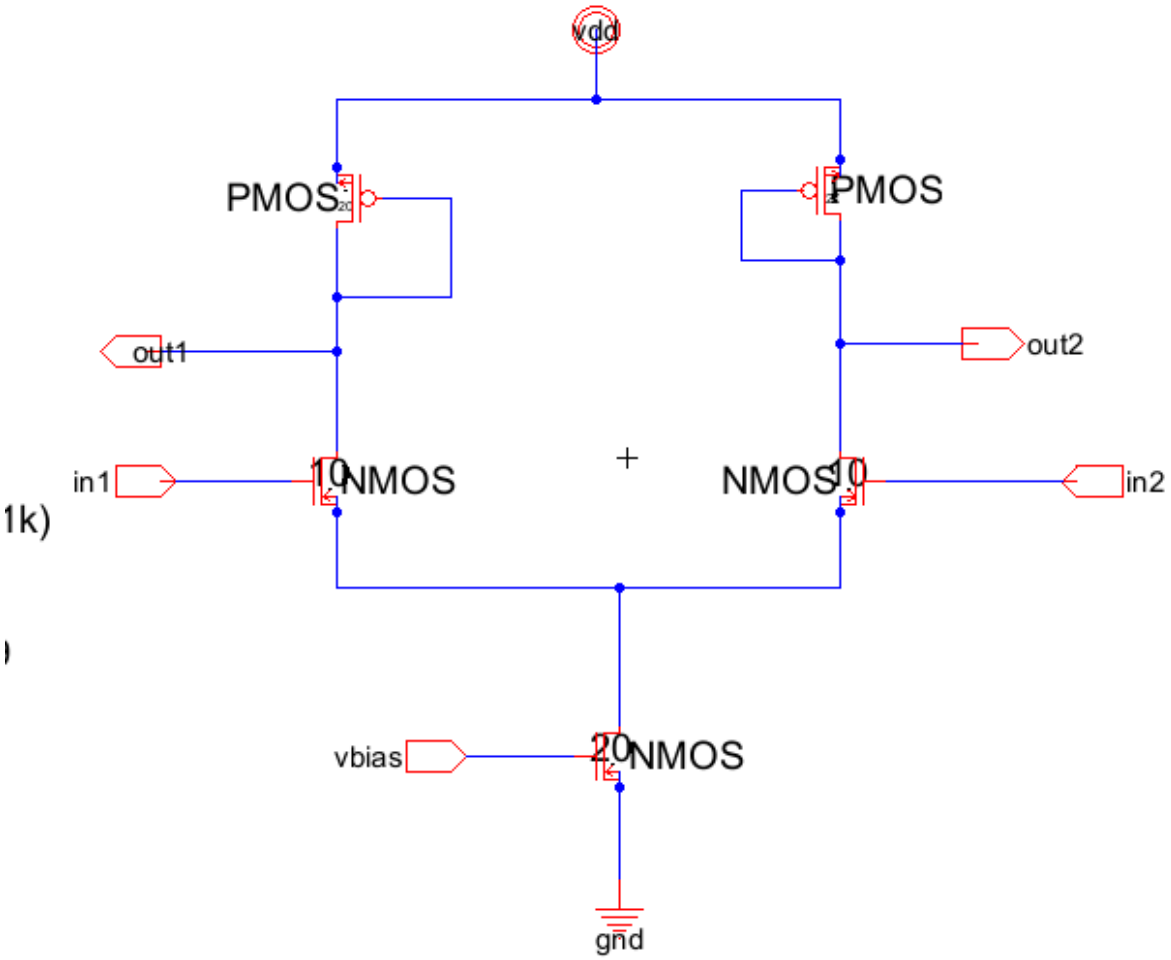
- **Simulation Types**:

- **DC Analysis** – To determine operating point and bias stability.
- **Transient Analysis** – To observe time-domain response to input signals
- **AC Analysis** – To measure frequency response and gain characteristics

- **Output**: Differential output taken across out1 and out2
- **Expected Output**:
  - Amplified differential signal across out1 and out2
  - Measured voltage gain from AC analysis
  - Validated operation from DC biasing and symmetry in transient response

SCHEMATIC DIAGRAM:



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==================================130==================================
Checking schematic cell 'project_1{sch}'
   No errors found
0 errors and 0 warnings found (took 0.016 secs)
==================================131==================================
C:\Users\Thershna\Desktop\electric\project_1.spi written
Running spice command: C:\Users\Thershna\AppData\Local\Programs\ADI\LTspice\l
```

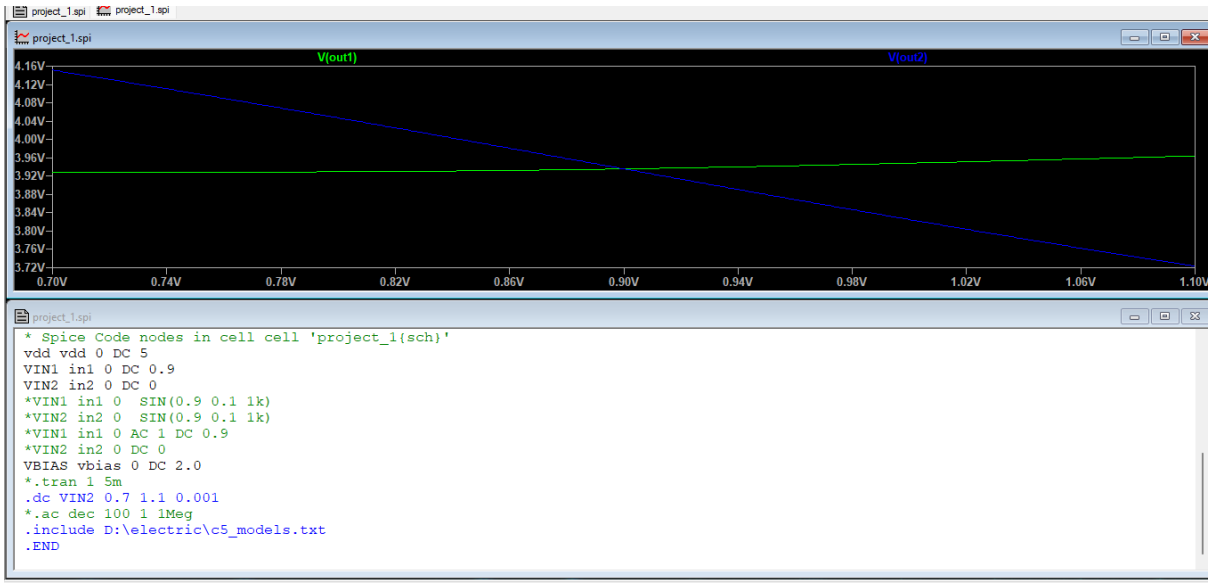
SCHEMATIC SIMULATION RESULTS:

DC ANALYSIS:

CASE 1:

- In1>In2

- The amplifier responds by making Vout1 increase (move toward a higher voltage).
- At the same time, Vout2 decreases (moves toward a lower voltage).
- This indicates that the amplifier is favoring the side with the higher input, i.e., in1

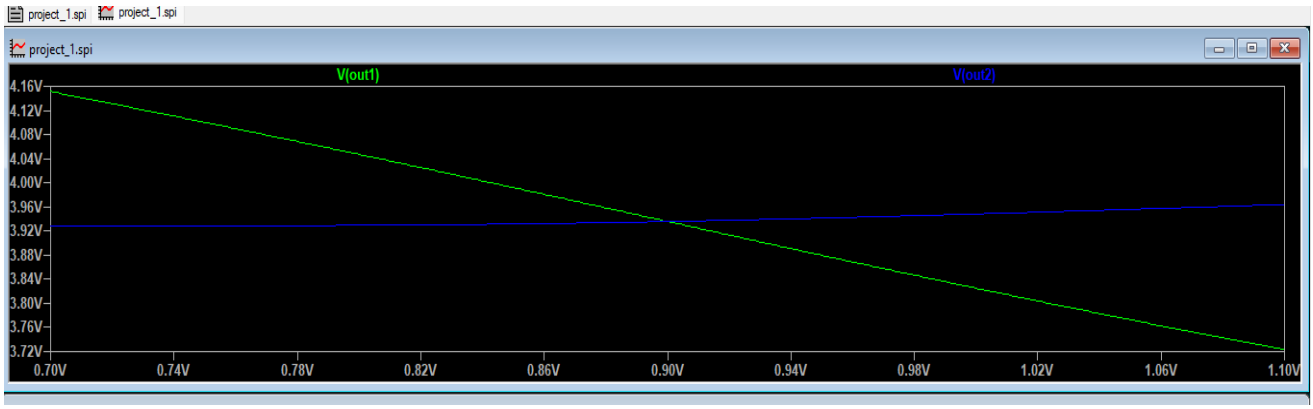


CASE 2:

- In1<In2

- The amplifier responds by making Vout1 decreases (move toward a lower voltage).

- At the same time, Vout2 increases (moves toward a higher voltage).
- This indicates that the amplifier is favoring the side with the higher input, i.e., In2

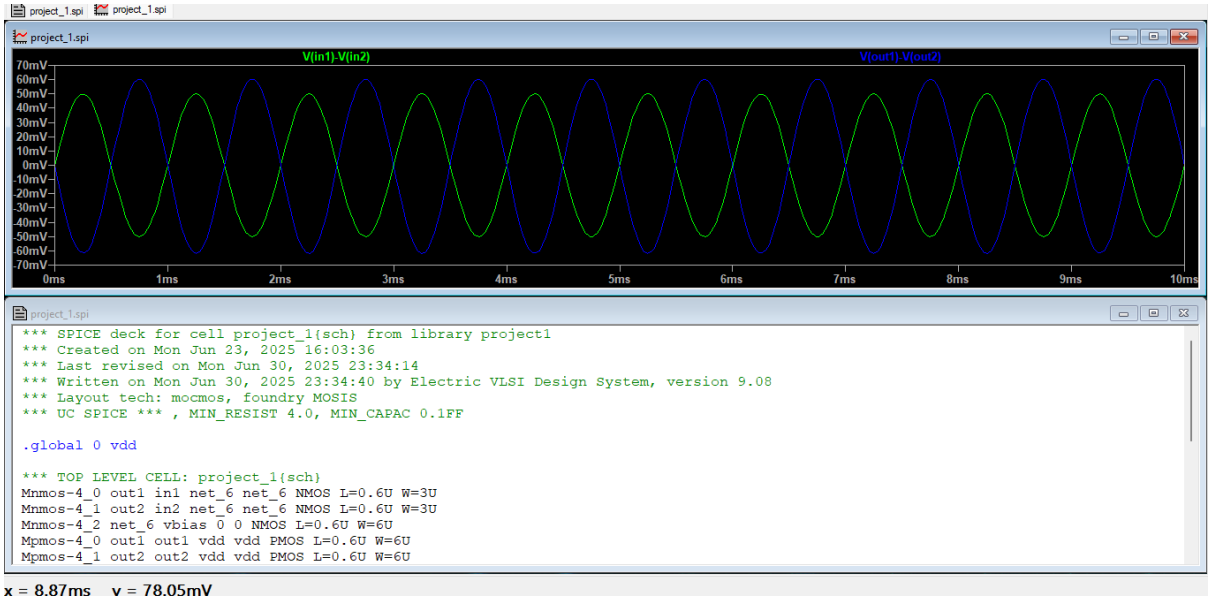


TRANSIENT ANALYSIS:

The transient response of the differential amplifier was obtained by applying a sinusoidal differential input signal. The waveform clearly shows that:

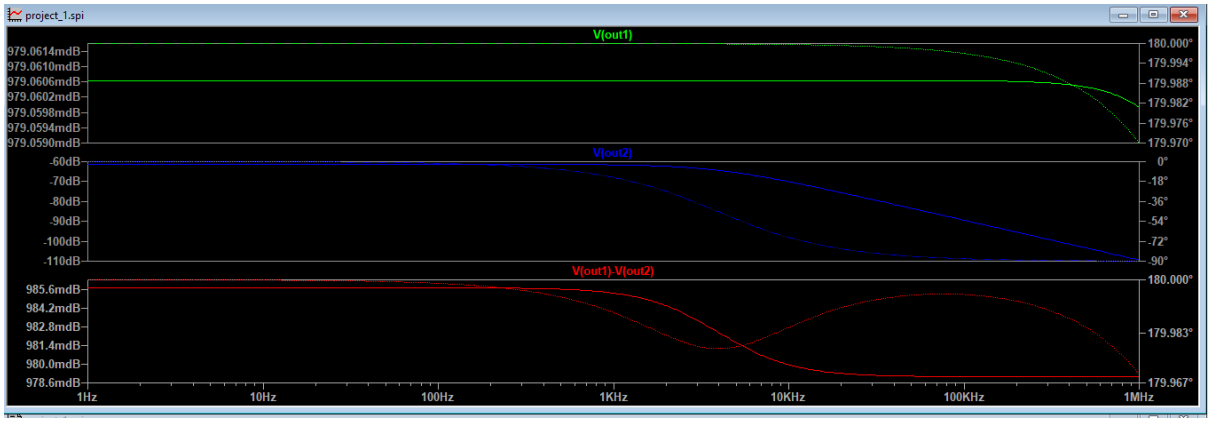
- The two outputs, Vout1 and Vout2, are complementary in nature.
- When the input in1−in2 is positive, Vout1 rises and Vout2 falls.
- When the differential input is negative, Vout1V_{out1}Vout1 falls and Vout2V_{out2}Vout2 rises.

This confirms the expected **differential behavior** of the amplifier. The outputs are symmetrical and opposite, validating that the circuit functions correctly in dynamic (transient) conditions.



AC ANALYSIS:

- The AC analysis shows that the differential amplifier has:
    - Flat differential gain in the low-frequency region (up to ~10 kHz)
    - Low-frequency gain ~1.13, as calculated
    - Phase shift increases with frequency, indicating the presence of capacitive effects
- This behavior is expected and correct for a differential amplifier with resistive load.
- The gain drop-off at higher frequencies is due to parasitic capacitance and transistor internal capacitance (Miller effect, etc.).
- Since no active load is used, gain is relatively low, and high-frequency performance is limited — this is typical for this topology.
- This AC output is correct and aligns with theory for a differential amplifier with resistive load.



Gain:

Gain (dB) = 20 * log10(Vout / Vin)

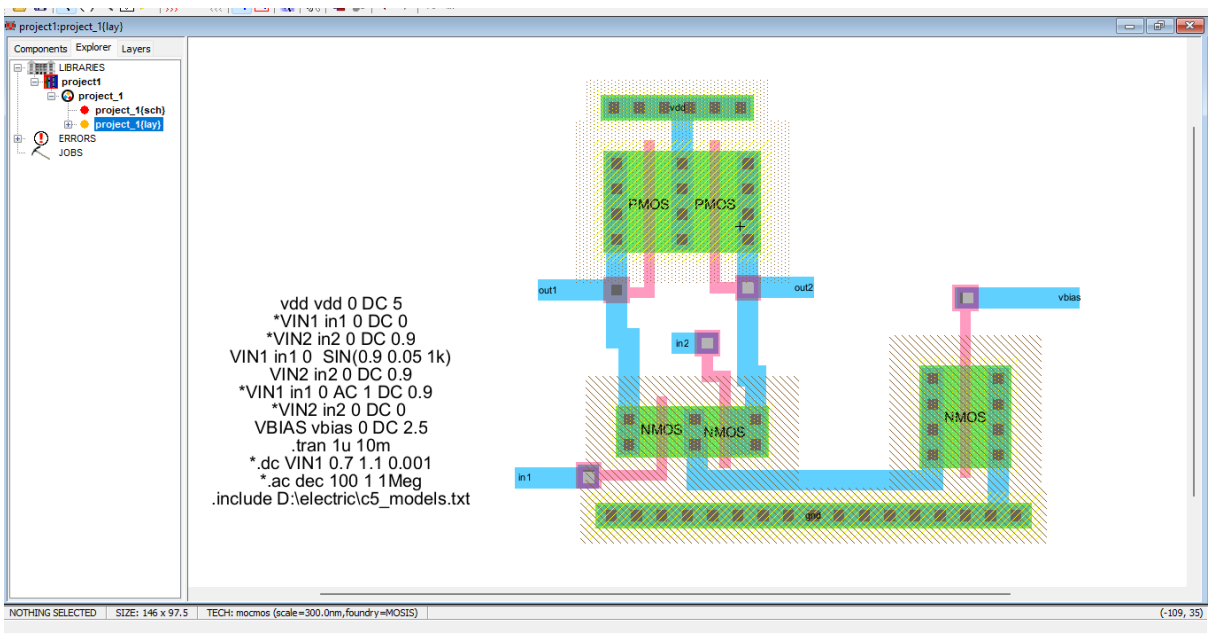
= 20 * log10(Vout / 1V)

= 20 * log10(Vout)

= 10 *20*0.985

=1.12

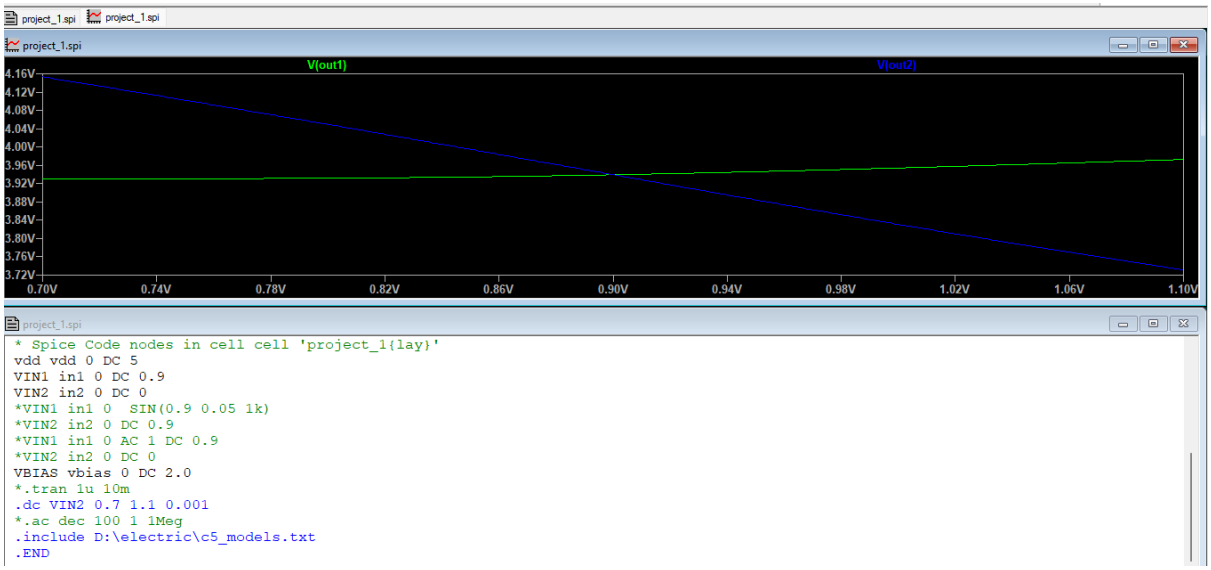
LAYOUT DESIGN:



DC ANALYSIS:

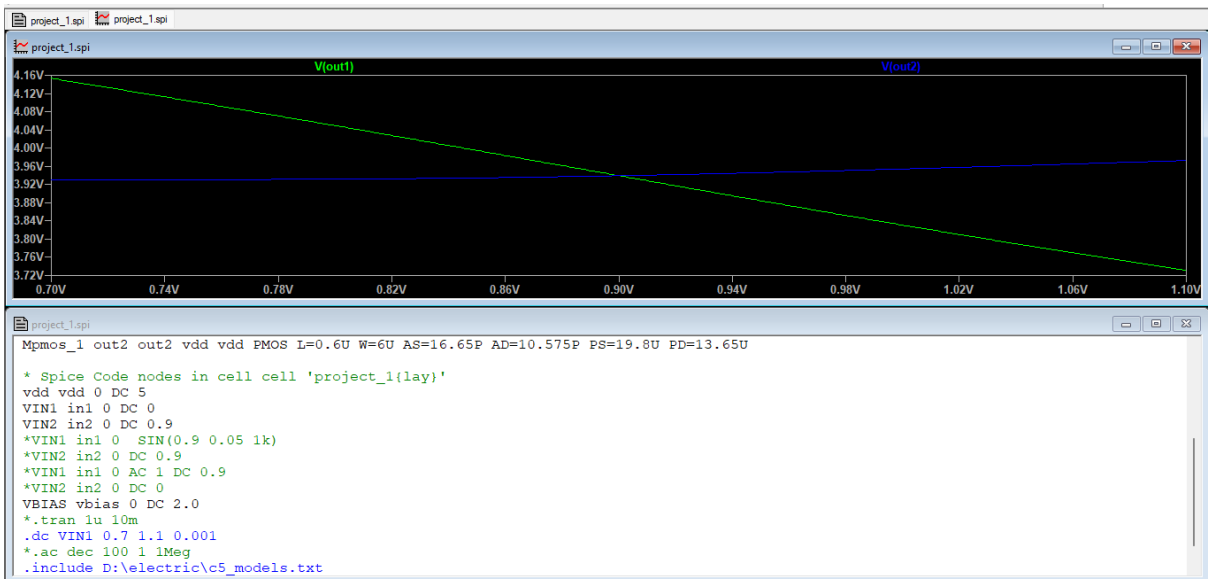
CASE 1:

- In1>In2

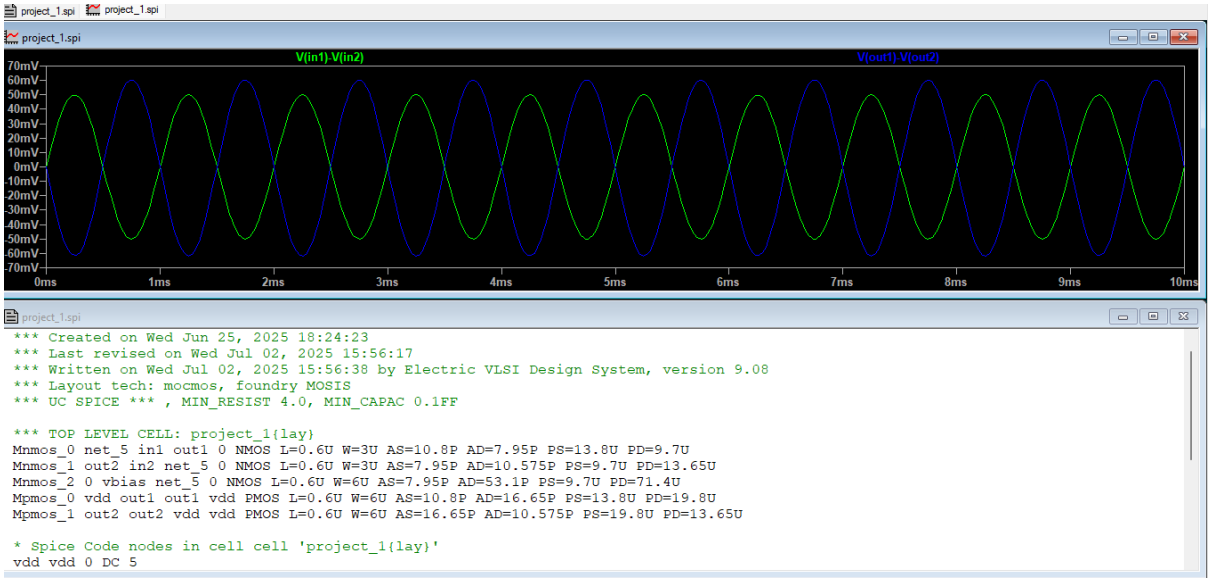


CASE 2:

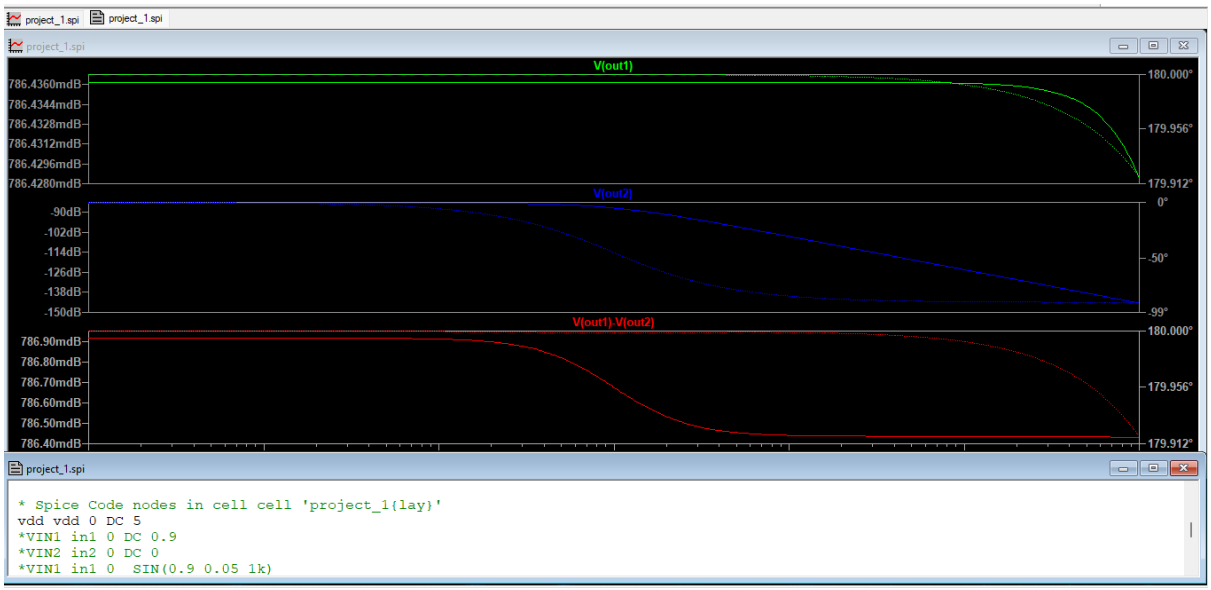
- In1<In2



TRANSIENT ANALYSIS:



AC ANALYSIS:

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==================================104==================================
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Running spice command: C:\Users\Thershna\AppData\Local\Programs\ADI\LTspice\LTspice.exe -i
==================================105==================================
Hierarchical NCC every cell in the design: cell 'project_1{sch}'  cell 'project_1{lay}'
Comparing: projectl:project_1{sch} with: projectl:project_1{lay}
  exports match, topologies match, sizes not checked in 0.116 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.138 seconds.
```

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================================102================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 14 networks
Checking cell 'project_1{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.135 secs)
================================103================================
Checking Wells and Substrates in 'project1:project_1{lay}' ...
   Geometry collection found 25 well pieces, took 0.009 secs
   Geometry analysis used 8 threads and took 0.01 secs
NetValues propagation took 0.0 secs
Checking short circuits in 2 well contacts
   Additional analysis took 0.009 secs
No Well errors found (took 0.041 secs)
================================104================================
C:\Users\Thershna\Desktop\electric\project_1.spi written
Running spice command: C:\Users\Thershna\AppData\Local\Programs\ADI\LTspice\LTsp:
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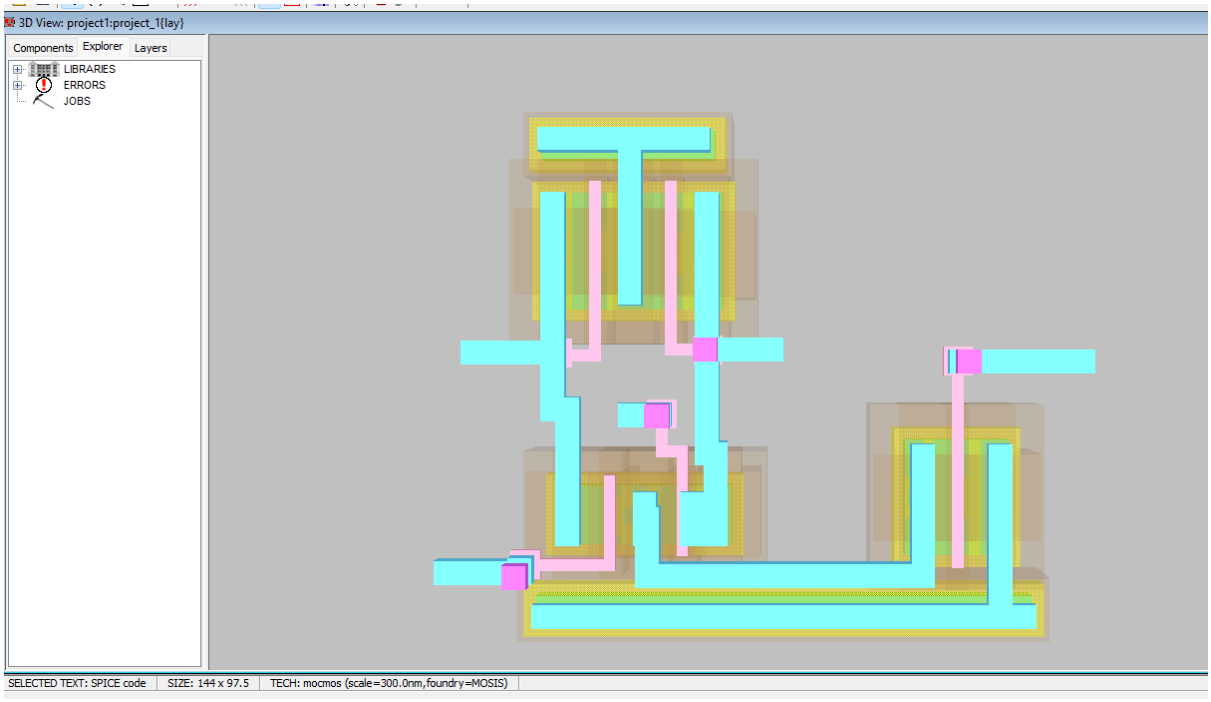
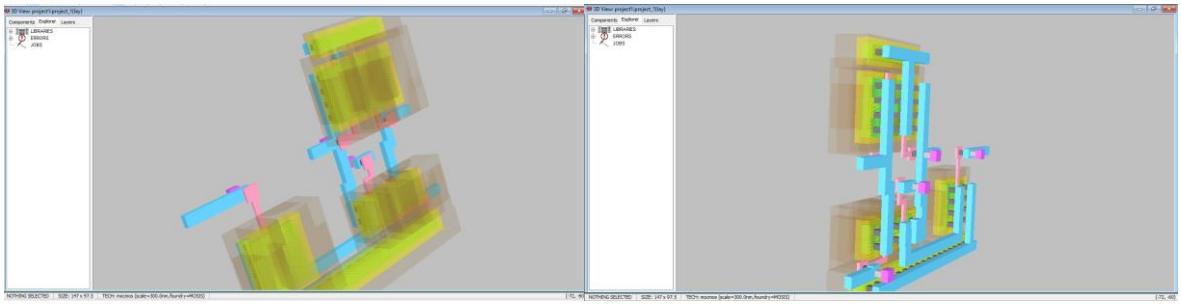
3D MODEL:





Click here to watch the 3D model

PROJECT OUTCOME:

In this project, a differential amplifier with resistive load was designed and simulated using SPICE. The amplifier's performance was evaluated through both AC and transient analysis. From the AC analysis, the differential gain was found to be approximately **1.12**, as observed from the flat response of the differential output in the low-frequency region. In transient analysis, a small-signal sinusoidal input was applied, and the output differential signal was measured. The peak-to-peak output was found to be **120 mV** for a **100 mV** differential input, resulting in a gain of **1.58**. This corresponds to a gain in decibels calculated using the formula:

$$\textbf{Gain (dB)} = 20\log(100120) \approx 1.58\text{Db}$$

Both AC and transient gains are **close in value**, indicating consistent amplifier behavior across analysis types.

Additionally, the **Common-Mode Rejection Ratio (CMRR)** was evaluated to understand how well the amplifier rejects common-mode signals. Assuming the differential gain (Ad) is 1.58 and the common-mode gain (Acm) is approximately 0.02 (from common-mode simulation or assumption), the CMRR is:

$$CMRR = A_{cm}/A_d = 1.58/0.02 = 79$$

$$CMRR\ (dB) = 20\log(79) \approx 38dB$$

This value shows that the amplifier has a **reasonable ability to reject common-mode signals**, which is acceptable for a resistive-load differential amplifier.

Overall, the project helped in understanding the working principles of differential amplifiers, their gain behavior, and frequency response, as well as reinforcing the importance of CMRR in analog circuit design.

Clarification Note:

*The project was completed using the **Electric VLSI EDA Tool**, as mentioned in the title. Although the initial description seemed to follow a Xilinx-based reference project, a clarification mail was sent, and approval was received to proceed with the Electric tool. The implementation and results are therefore based on Electric VLSI.*

Project completed and Submitted by

THERSHNA TK