

AN 13.10

USB3300 PHY Layout Guidelines

1 Introduction

The Universal Serial Bus (USB) is capable of operating at 480 Mbps. Excellent signal integrity is required to operate reliably at high-speed data rates. The PCB layout is a critical component in maintaining signal integrity. This document provides recommendations regarding the PCB layout.

1.1 Audience

This application note is written for a reader that is familiar with hardware design, USB protocols and the USB 2.0 specification. The goal of the application note is to provide information on sensitive areas of the PCB layout.

1.2 Overview

Following recommendations for PCB layout with SMSC parts is not the only way to layout our QFN. Every board designer will have his/her own preference. There are multiple ways to layout these parts which can be dependent on complexity and density of layout, board space, number and types of devices in circuit and the environment that the final product will reside in.

1.3 References

The following documents should be referenced when using this application note:

- SMSC USB3300 Datasheet
- SMSC EVB-USB3300 User Manual
- Universal Serial Bus Specification Revision 2.0

2 Review of Sensitive Circuits

This chapter provides guidelines for the sensitive circuits associated with the system application of the USB3300.

2.1 Controlled Impedance for USB Traces

The USB 2.0 specification requires the USB DP/DM traces maintain nominally 90 Ohms differential impedance (see USB specification Rev 2.0, paragraph 7.1.1.3 for more details). In this design the traces are 14 mil wide with minimum line spacing of 7 mils. These numbers are derived for 13 mil distance from ground reference plane. A continuous ground plane is required directly beneath the DP/DM traces and extending at least 5 times the spacing width to either side of DP/DM lines.

Maintain close to 90 Ohms differential impedance. For different dielectric thickness, copper weight or board stack-up, trace width and spacing will need to be recalculated.

Maintain symmetry between DP/DM lines in regards to shape and length.

Single ended impedance is not as critical as the differential impedance, a range of 42 to 78ohms is acceptable (equivalently, common mode impedance must be between 21 Ohms and 39 Ohms).

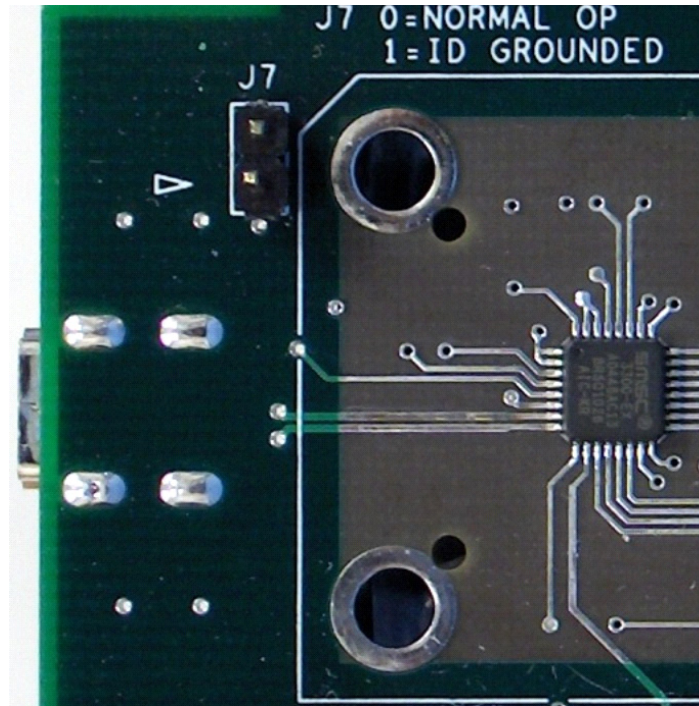


Figure 2.1 Example of Routing DP/DM to Type B Connector

Figure 2.1 shows DP/DM traces with approximately equal trace length and symmetry. It is important to maintain a conductor width and spacing that provides differential and common mode impedances compliant with the USB specification. Use 45 degree turns to minimize impedance discontinuities.

2.2 Isolation of DP/DM Traces

The DP/DM traces must be isolated from nearby circuitry and signals. Maintain a distance of parts to lines that is greater than or equal to 5 times the distance of the 7 mil spacing between the traces. Do not route differential pairs under parts. Do not cross DP/DM lines with other PCB traces unless the traces are on the opposite side of the ground plane from DP/DM. Route DP/DM traces over solid plane, not over power planes.

2.3 Isolated Shielding on the USB Connector.

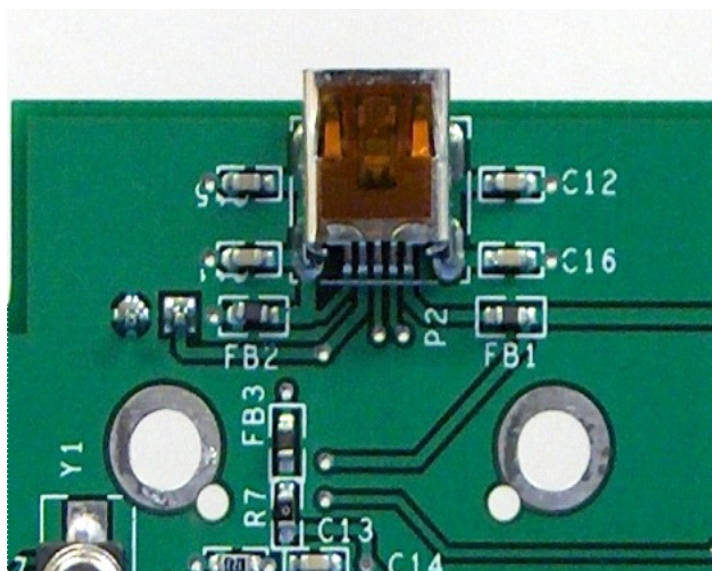


Figure 2.2 Connections to Shield of Type B USB Connector

The USB3300 fully supports USB On-the-Go (OTG) PHY. [Figure 2.2](#) shows the Mini-AB connector housing is AC coupled to the device ground. The housing is also DC coupled to ground through the ferrite bead, FB2. Industry convention is to ground only the host side of the cable shield. This is done to provide cable shielding while preventing possible ground currents from flowing in the USB cable if there happens to be a potential difference between the host and device grounds. If device only operation were desired, it would be advised to cut the trace between FB2 and the connector housing so that only AC grounding of the housing was present.

2.4 Crystal Oscillator

The crystal oscillator is sensitive to stray capacitances and noise from other signals. It can also disturb other signals and cause EMI noise. The load capacitors, crystal and parallel resistors should be placed close to each other. The ground connection for the load capacitors should be short and out of the way from return currents from USB, VBUS power lines. The load capacitors return path should be to the digital logic power supply.

Figure 2.3 shows a schematic of the crystal oscillator circuit.

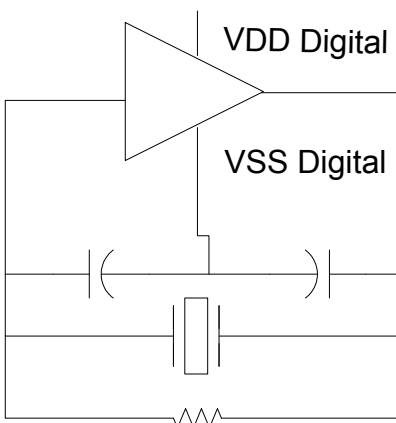


Figure 2.3 Crystal Oscillator Schematic

Figure 2.4 illustrates a suggested PCB layout of the crystal circuit. All components are far removed from USB lines.

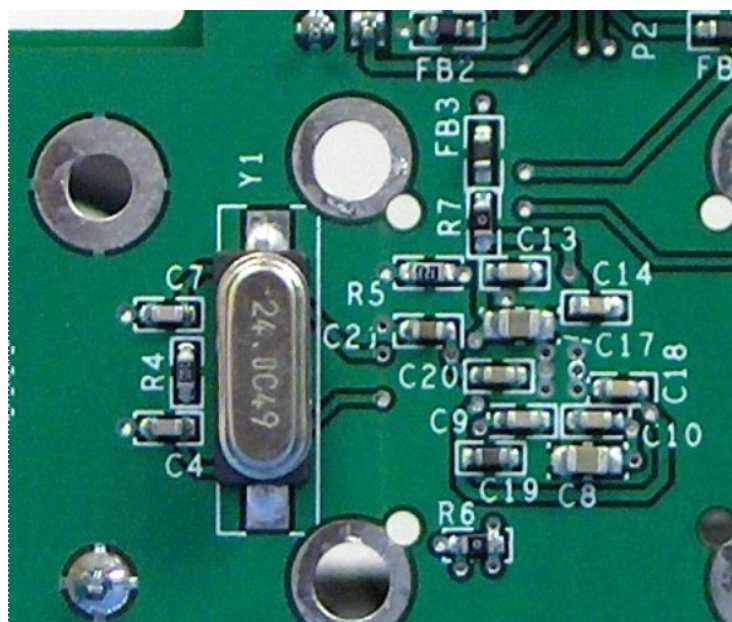


Figure 2.4 Crystal Oscillator Component Layout

2.5 RBIAS

The RBIAS resistor sets an internal current source reference. Thus, the RBIAS pin is a high impedance node and so any noise induced on the RBIAS traces will directly impact internal current references and negatively degrade eye-diagram quality. The RBIAS resistor should be placed close to the RBIAS

pin and the ground return should be short and direct to VSS with RBIAS placed the same way as bypass capacitors as described in paragraph 2.6. Traces for resistor should be very short and isolated from nearby traces if possible.

2.6 Power Supply Bypass Capacitors

Bypass capacitors should be placed close to the supply pins of the USB3300 and connected with short, wide traces. The USB3300 evaluation board has bypassing directly under part, with return current paths tied to bottom ground plane.

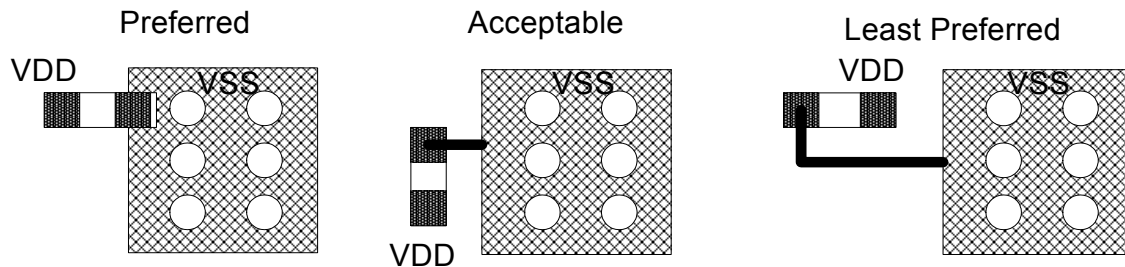


Figure 2.5 Placement of Bypass Capacitors

2.7 VIAS in Ground Flag

The die pad (flag) is 105 mils per side. A 15 mil via in a pattern of 2 X 3 grid has been used which resulted in excellent signal integrity performance. Ideally these vias would be plugged so that no solder will flow through which would result in less than ideal solder connection to flag.

3 Summary

Layout guidelines have been presented for the USB3300. SMSC has found these guidelines to be effective in creating a systems application circuit for the USB PHY.

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