



Circuitos Digitais I - 6878

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Bacharelado em Ciência da Computação

Aula de Hoje

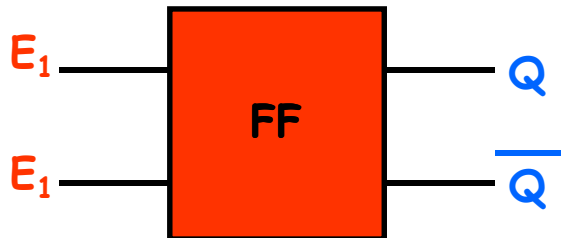
- **Circuitos Sequenciais:**
 - Flip-Flop Tipo RS
 - Flip-Flop Tipo D

Circuitos Sequenciais

Circuitos Sequenciais: As saídas dependem das entradas atuais e também das entradas anteriores.

Flip-Flops (FF): São circuitos sequenciais que podem ser usados como memória para armazenar 1 bit.

Símbolo



Condição do FF:

As saídas Q e \overline{Q} são complementares

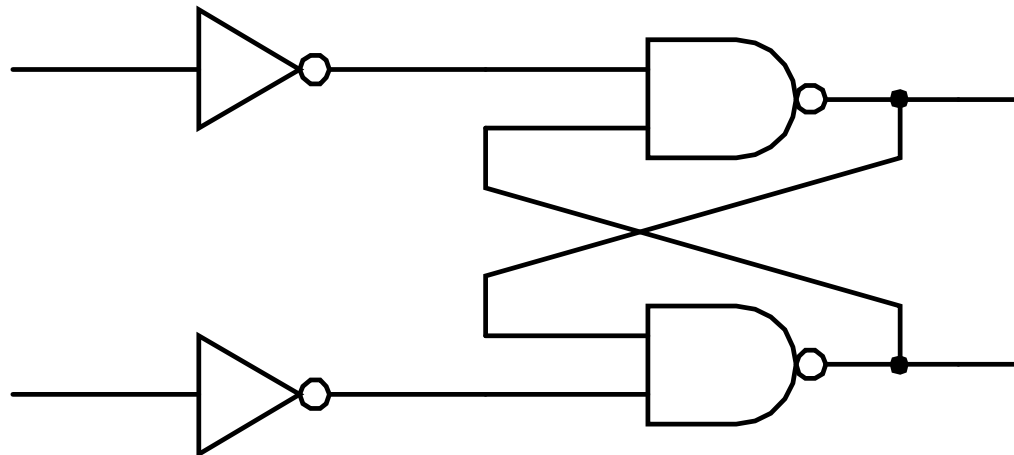
$$\text{Se } \begin{cases} Q=0 \Rightarrow \overline{Q}=1 \\ Q=1 \Rightarrow \overline{Q}=0 \end{cases}$$

Flip-Flop RS

TV da NAND

A	B	S
0	0	1
0	1	1
1	0	1
1	1	0

Circuito do FF RS



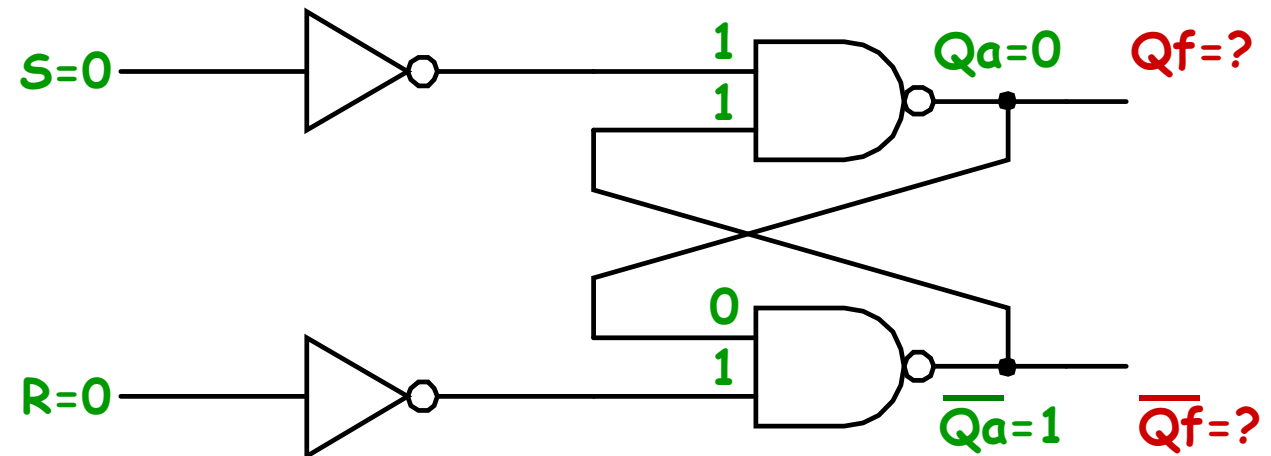
Flip-Flop RS

Nomenclatura

Q_a = saída anterior

Q_f = saída final

Estudo de Casos

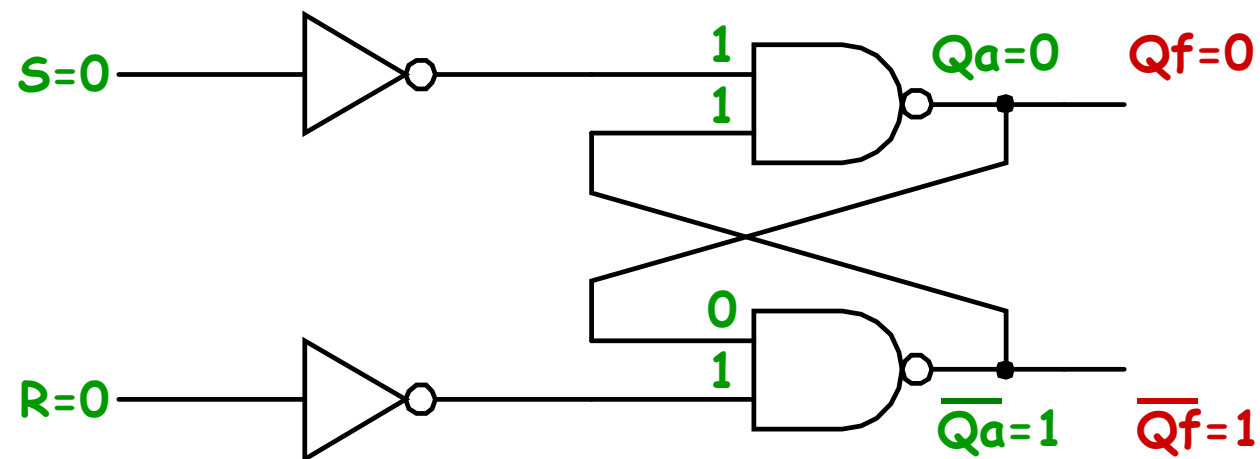


Caso 0

S	R	Q_a	\overline{Q}_a	Q_f	\overline{Q}_f
0	0	0	1		

Flip-Flop RS

Estudo de Casos



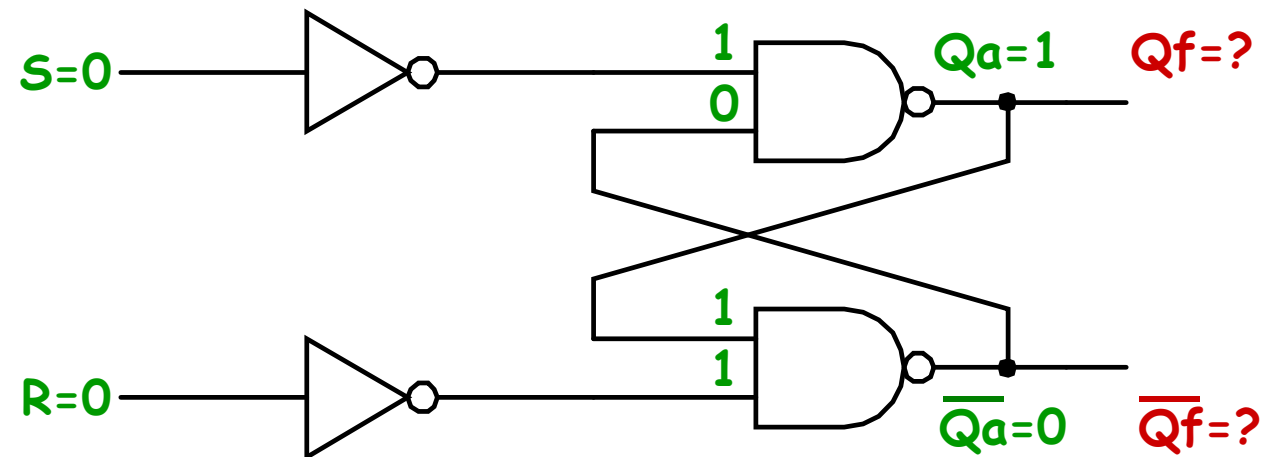
Caso 0

S	R	Q_a	\overline{Q}_a	Q_f	\overline{Q}_f
0	0	0	1	0	1

Manteve o estado anterior das saídas

Flip-Flop RS

Estudo de Casos

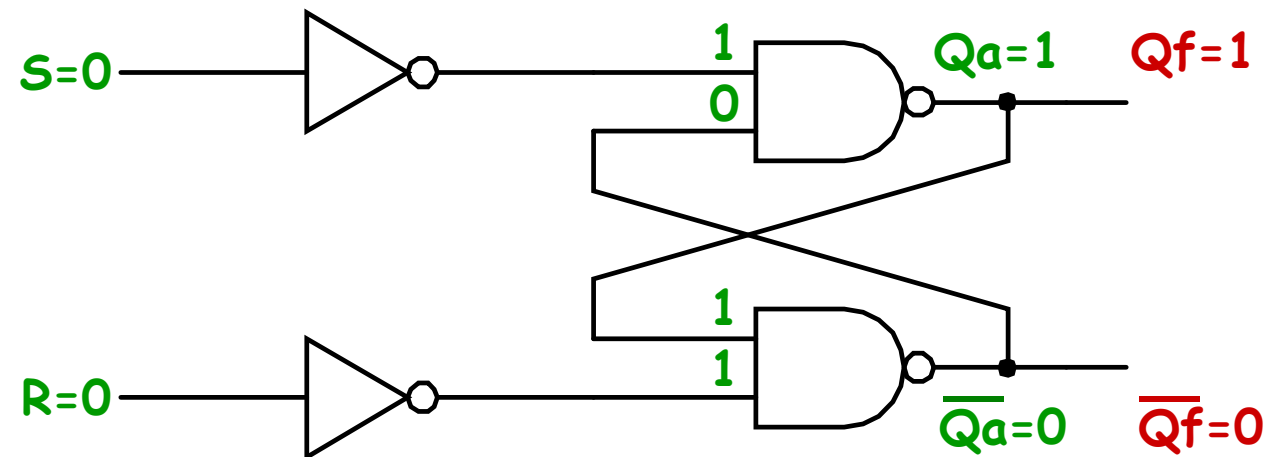


Caso 1

S	R	Q_a	\overline{Q}_a	Q_f	\overline{Q}_f
0	0	1	0		

Flip-Flop RS

Estudo de Casos



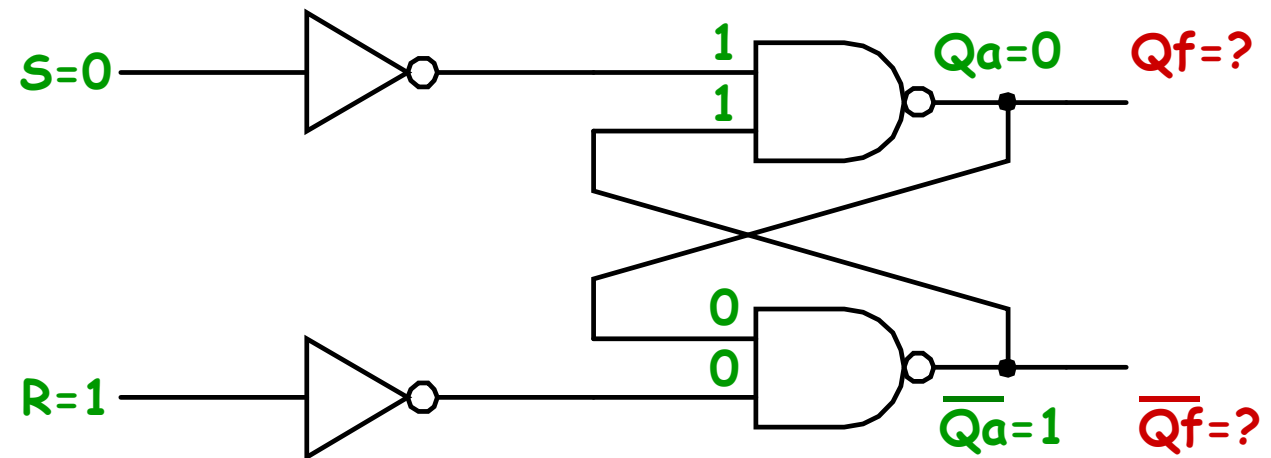
Caso 1

S	R	Q_a	\overline{Q}_a	Q_f	\overline{Q}_f
0	0	1	0	1	0

Manteve o estado anterior das saídas

Flip-Flop RS

Estudo de Casos

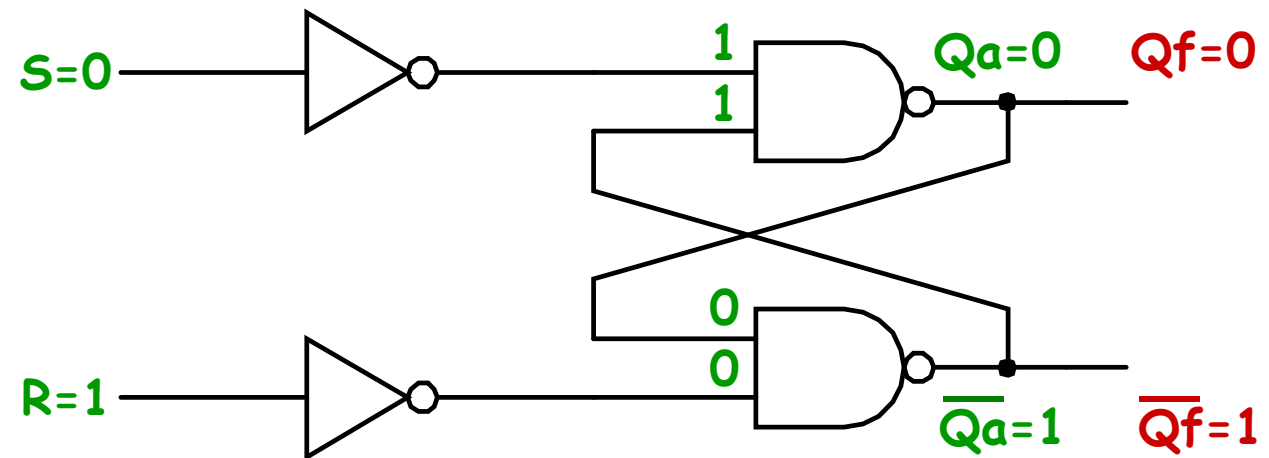


Caso 2

S	R	Q_a	\overline{Q}_a	Q_f	\overline{Q}_f
0	1	0	1		

Flip-Flop RS

Estudo de Casos



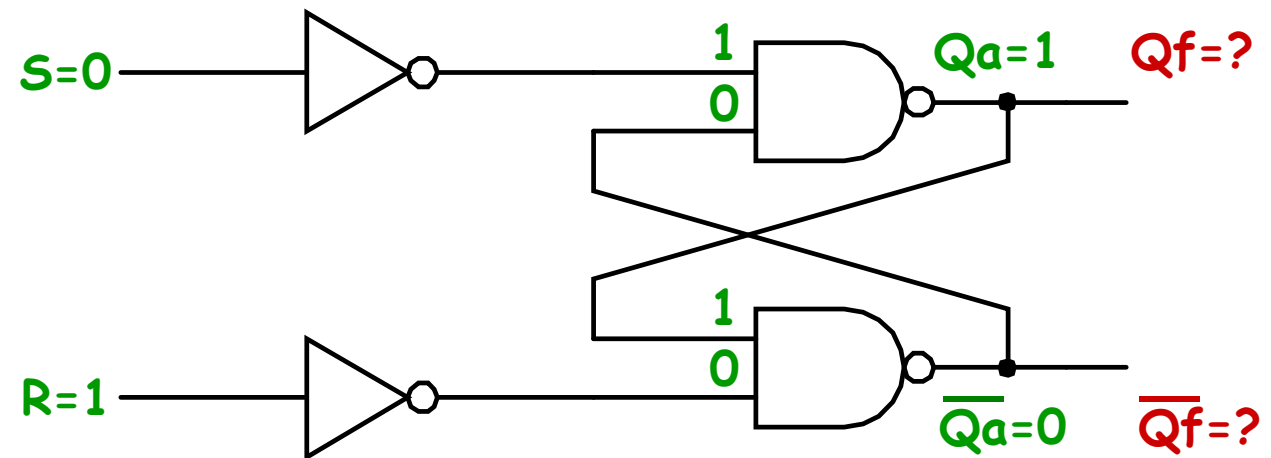
Caso 2

S	R	Q_a	$\overline{Q_a}$	Q_f	$\overline{Q_f}$
0	1	0	1	0	1

$Q_f=0 \Rightarrow$ Reset da saída

Flip-Flop RS

Estudo de Casos

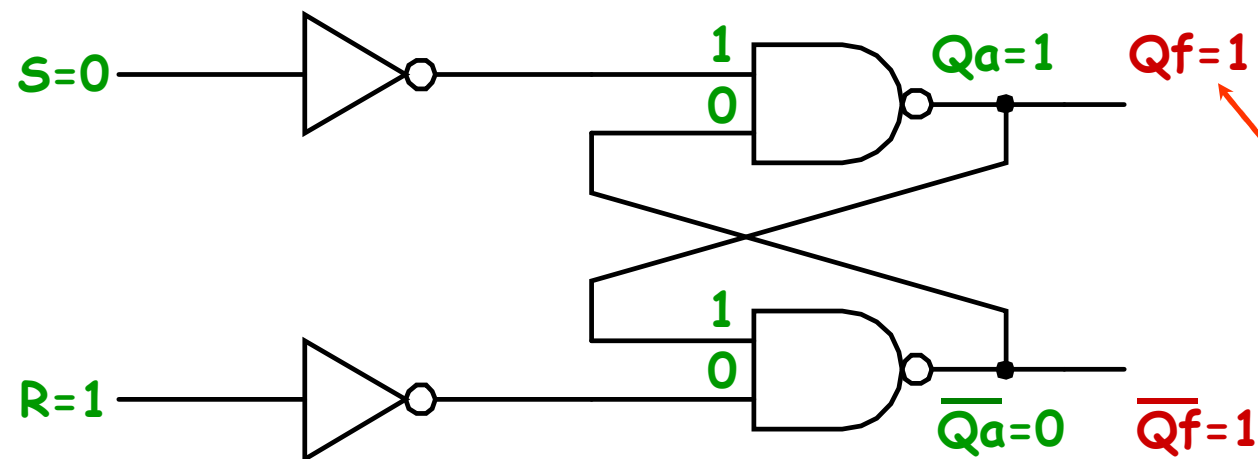


Caso 3

S	R	Q_a	\overline{Q}_a	Q_f	\overline{Q}_f
0	1	1	0		

Flip-Flop RS

Estudo de Casos



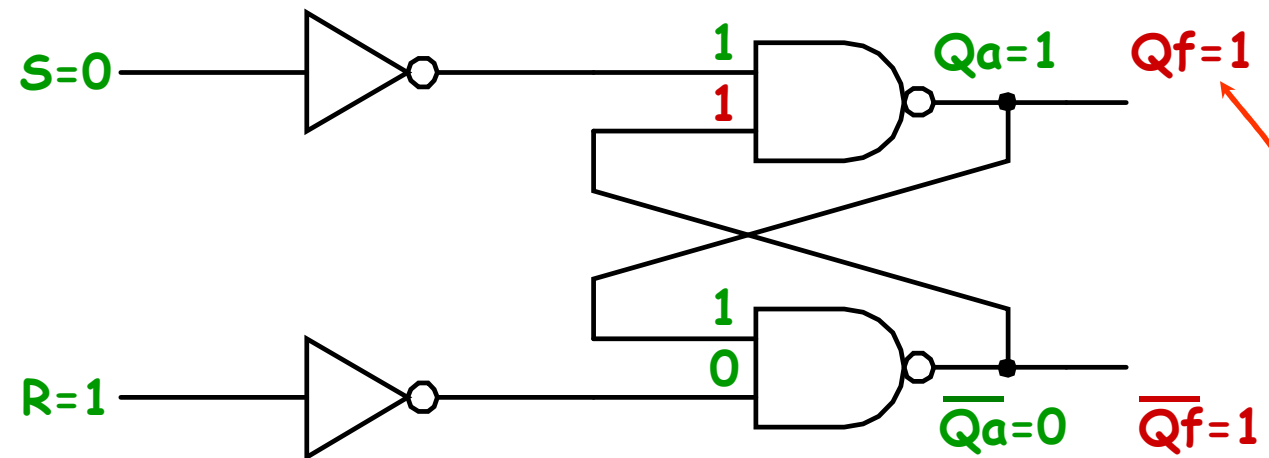
Caso 3

S	R	Q_a	$\overline{Q_a}$	Q_f	$\overline{Q_f}$
0	1	1	0		

Estado instável das saídas

Flip-Flop RS

Estudo de Casos



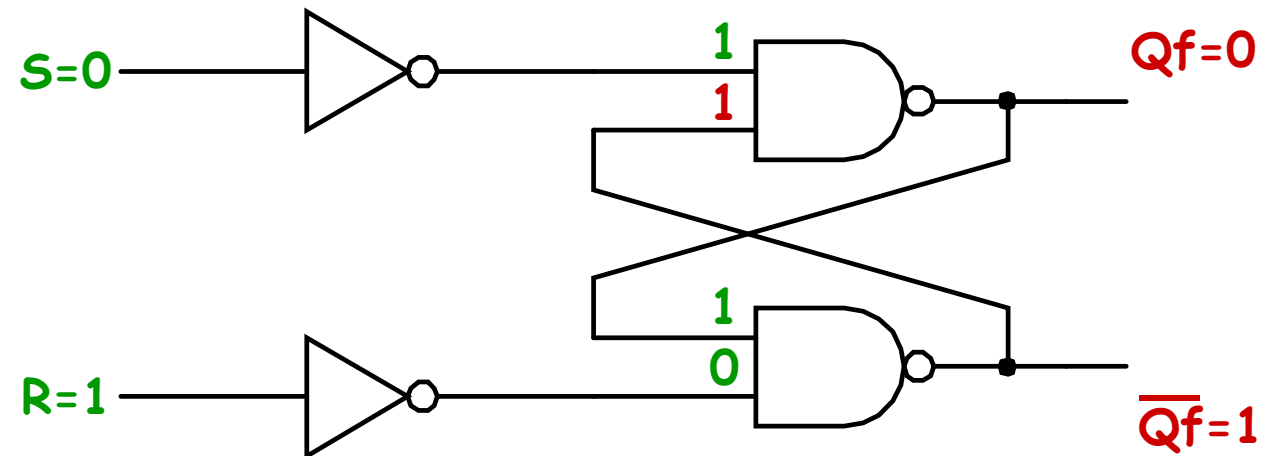
Caso 3

S	R	Q_a	$\overline{Q_a}$	Q_f	$\overline{Q_f}$
0	1	1	0		

Estado instável das saídas

Flip-Flop RS

Estudo de Casos

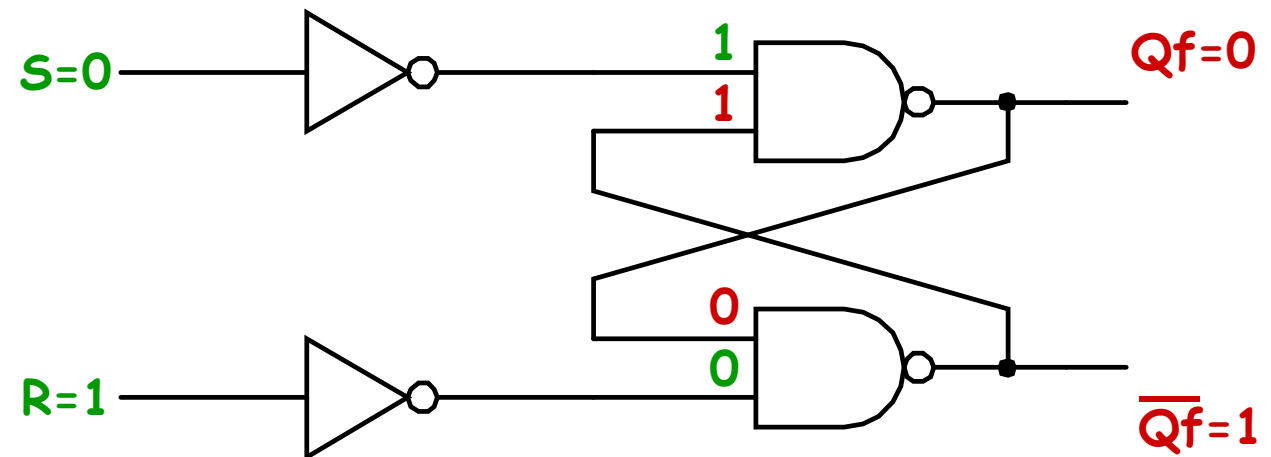


Caso 3

S	R	Q_a	$\overline{Q_a}$	Q_f	$\overline{Q_f}$
0	1	1	0		

Flip-Flop RS

Estudo de Casos



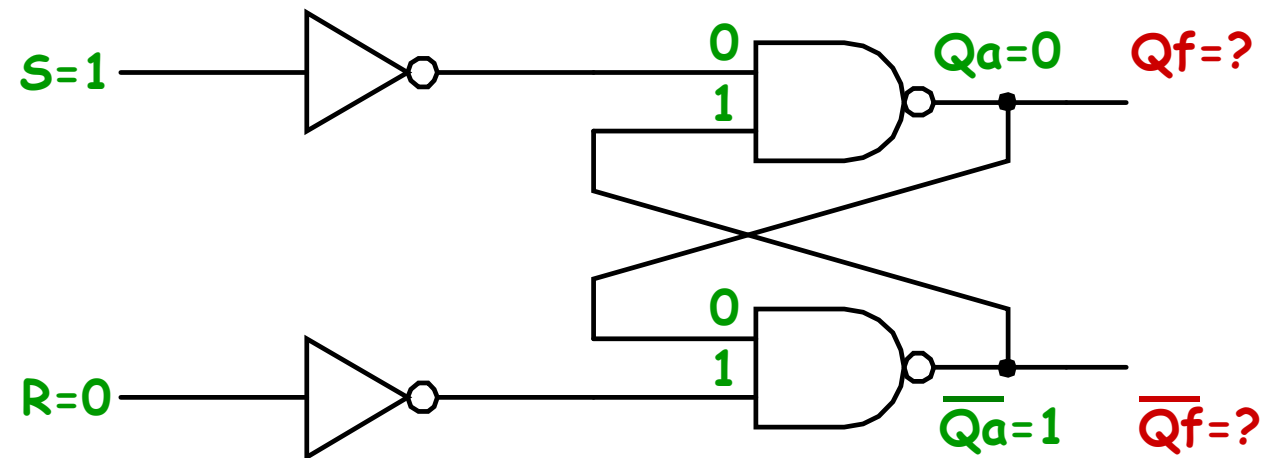
Caso 3

S	R	Q_a	\overline{Q}_a	Q_f	\overline{Q}_f
0	1	1	0	0	1

$Q_f=0 \Rightarrow$ Reset da saída

Flip-Flop RS

Estudo de Casos

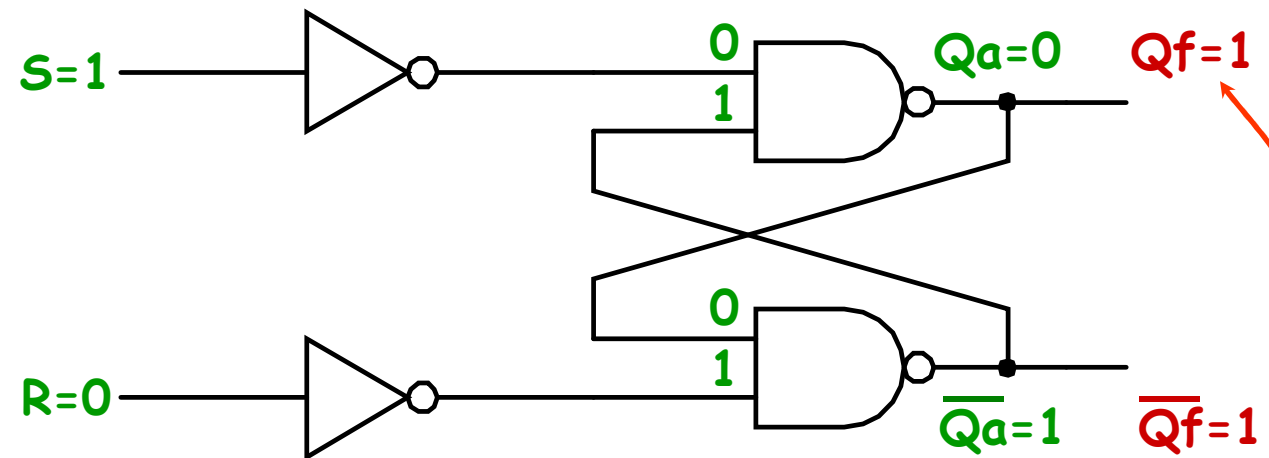


Caso 4

S	R	Q_a	\overline{Q}_a	Q_f	\overline{Q}_f
1	0	0	1		

Flip-Flop RS

Estudo de Casos



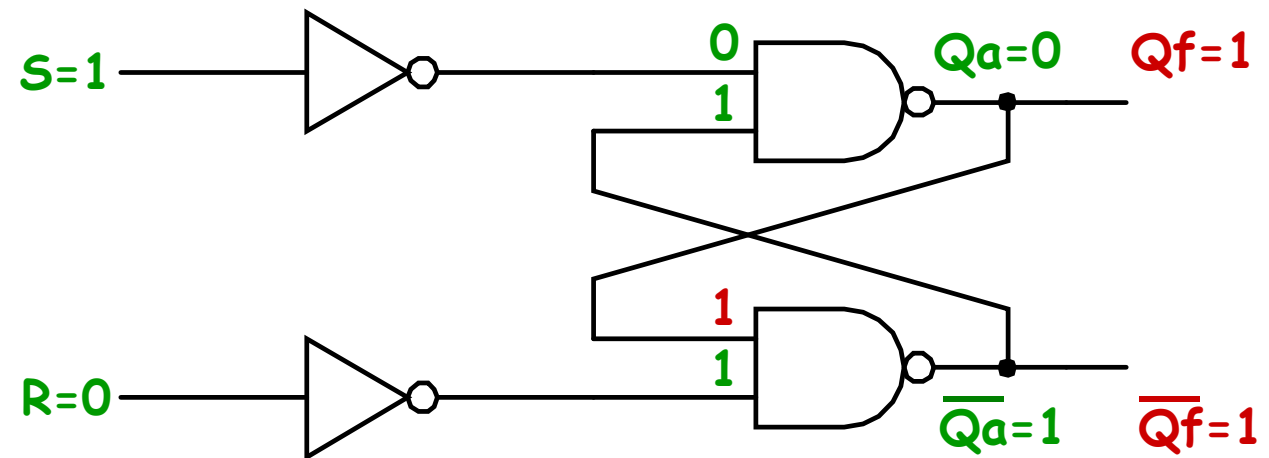
Caso 4

S	R	Q_a	\overline{Q}_a	Q_f	\overline{Q}_f
1	0	0	1		

Estado instável das saídas

Flip-Flop RS

Estudo de Casos

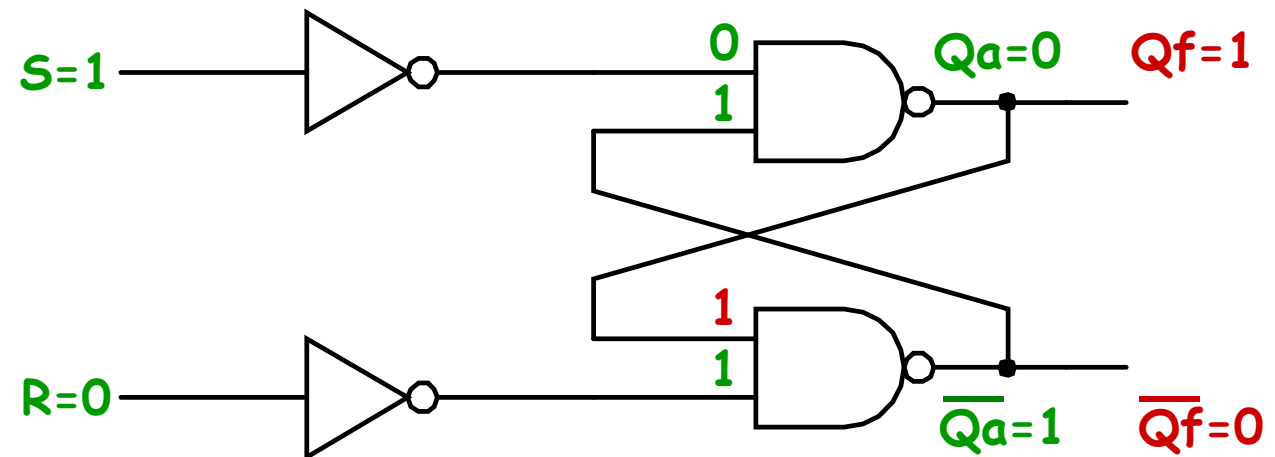


Caso 4

S	R	Q_a	\overline{Q}_a	Q_f	\overline{Q}_f
1	0	0	1		

Flip-Flop RS

Estudo de Casos

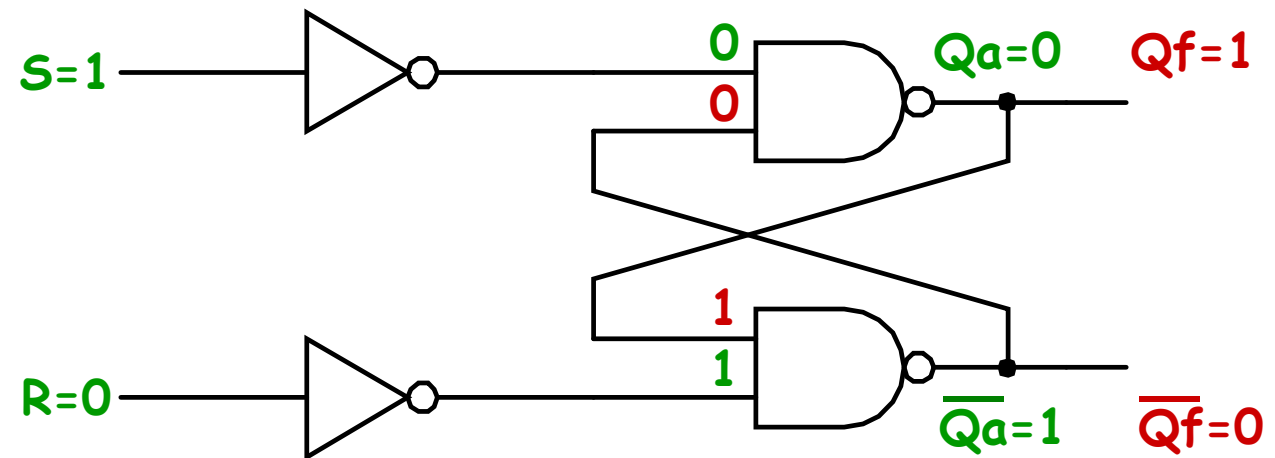


Caso 4

S	R	Q_a	\overline{Q}_a	Q_f	\overline{Q}_f
1	0	0	1		

Flip-Flop RS

Estudo de Casos

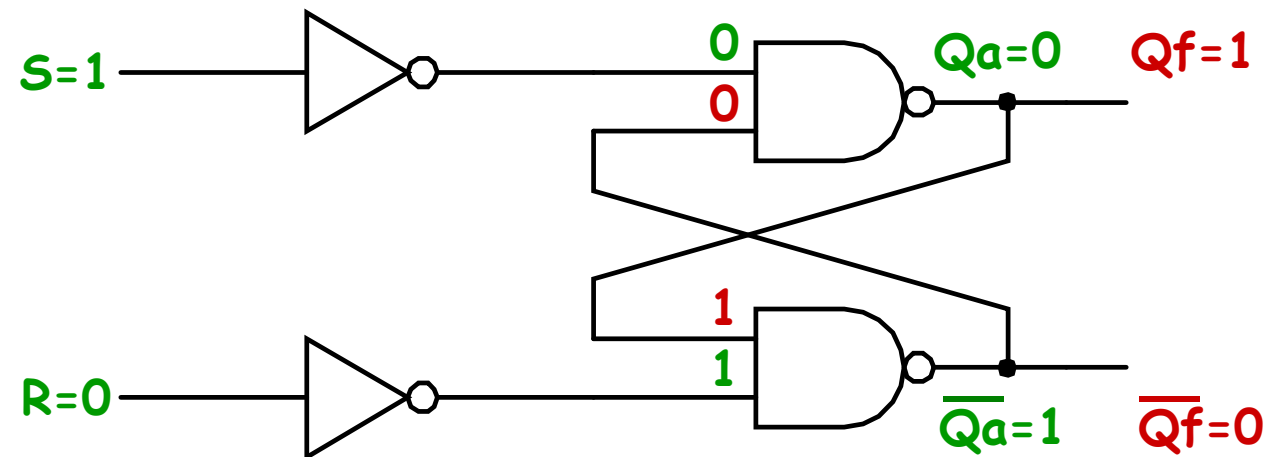


Caso 4

S	R	Q_a	\overline{Q}_a	Q_f	\overline{Q}_f
1	0	0	1		

Flip-Flop RS

Estudo de Casos



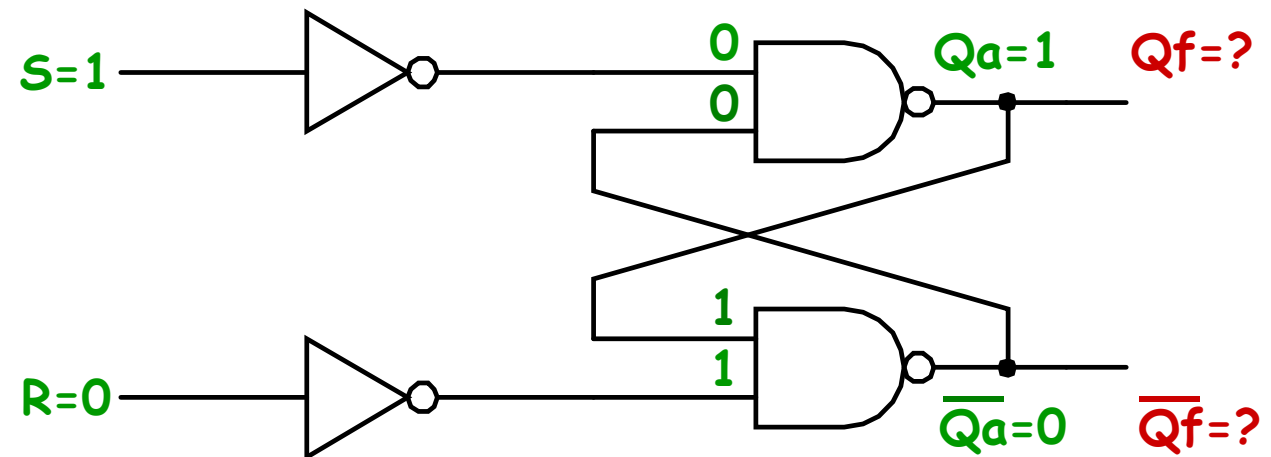
Caso 4

S	R	Q_a	\bar{Q}_a	Q_f	\bar{Q}_f
1	0	0	1	1	0

$Q_f=1 \Rightarrow$ Set da saída

Flip-Flop RS

Estudo de Casos

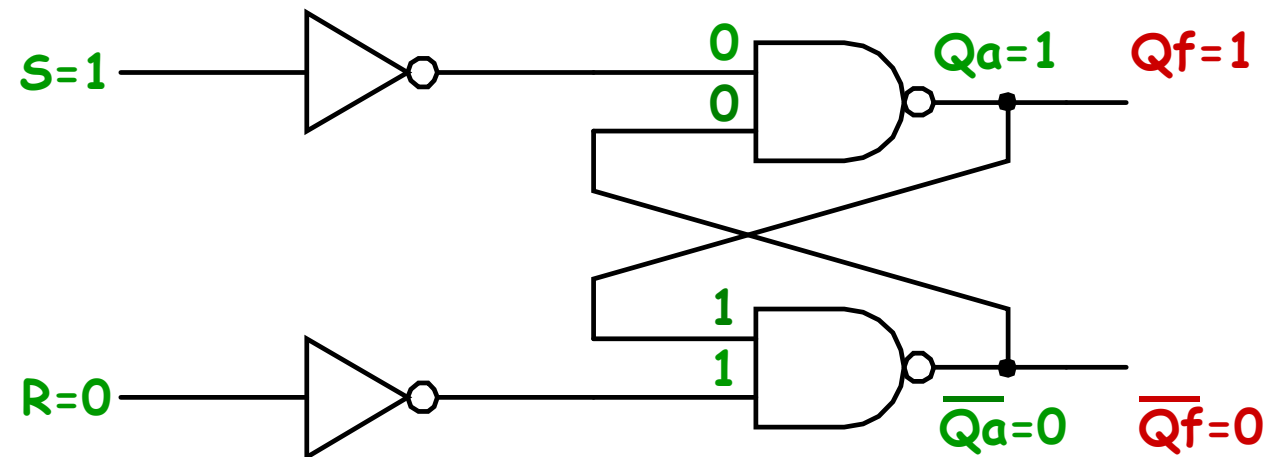


Caso 5

S	R	Q_a	\overline{Q}_a	Q_f	\overline{Q}_f
1	0	1	0		

Flip-Flop RS

Estudo de Casos



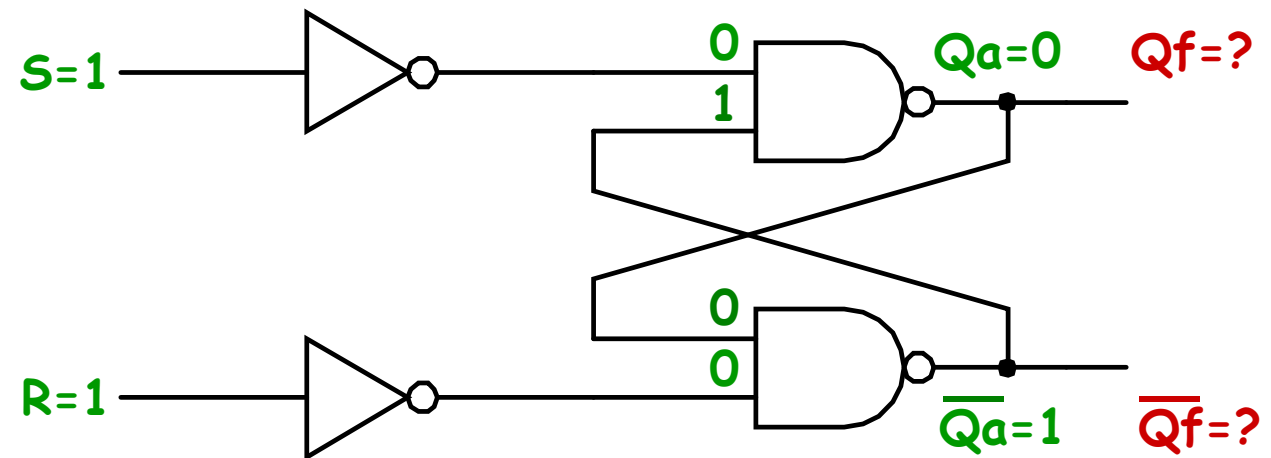
Caso 5

S	R	Q_a	\overline{Q}_a	Q_f	\overline{Q}_f
1	0	1	0	1	0

$Q_f=1 \Rightarrow$ Set da saída

Flip-Flop RS

Estudo de Casos

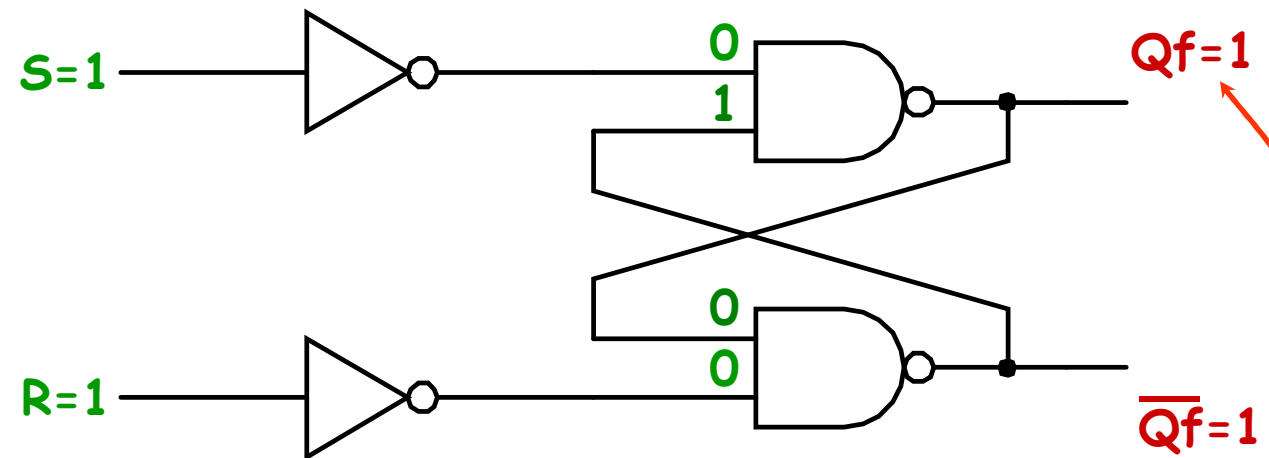


Caso 6

S	R	Q_a	\bar{Q}_a	Q_f	\bar{Q}_f
1	1	0	1		

Flip-Flop RS

Estudo de Casos



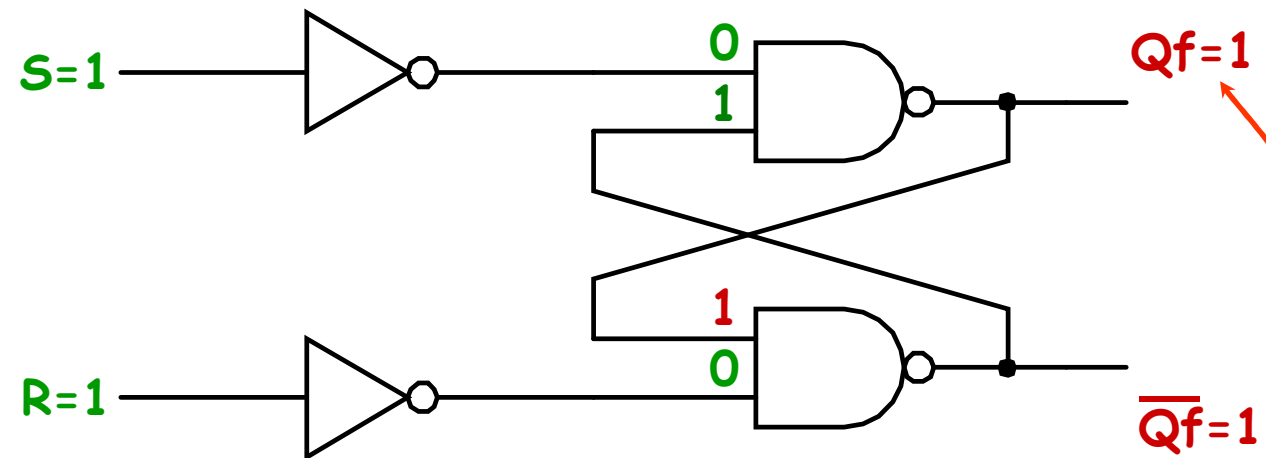
Caso 6

S	R	Qa	\overline{Qa}	Qf	\overline{Qf}
1	1	0	1		

Estado instável das saídas

Flip-Flop RS

Estudo de Casos



Caso 6

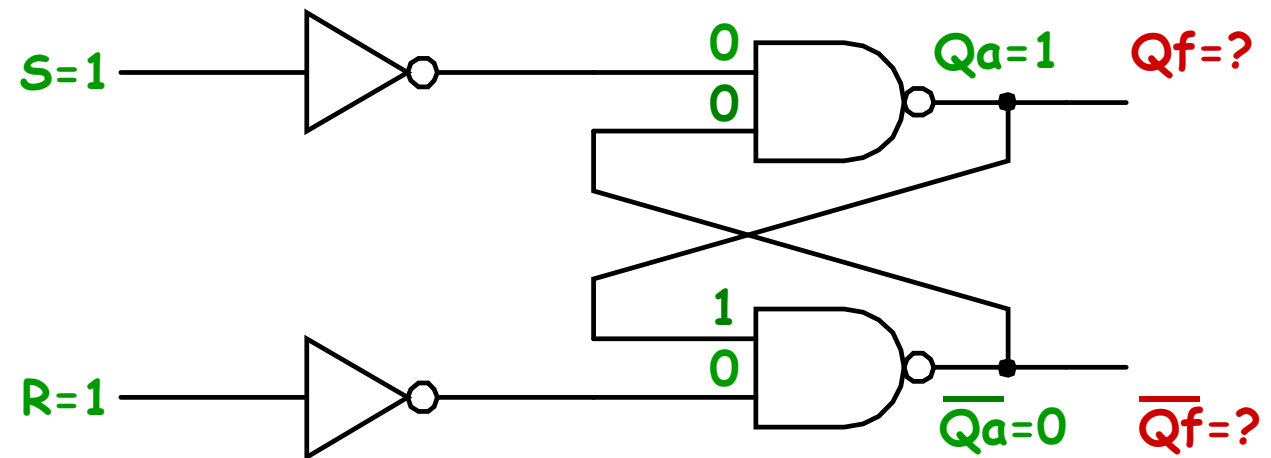
S	R	Q_a	$\overline{Q_a}$	Q_f	$\overline{Q_f}$
1	1	0	1	1	1

$Q_f = \overline{Q_f} = 1$ Viola a condição do FF RS

Estado instável das saídas

Flip-Flop RS

Estudo de Casos

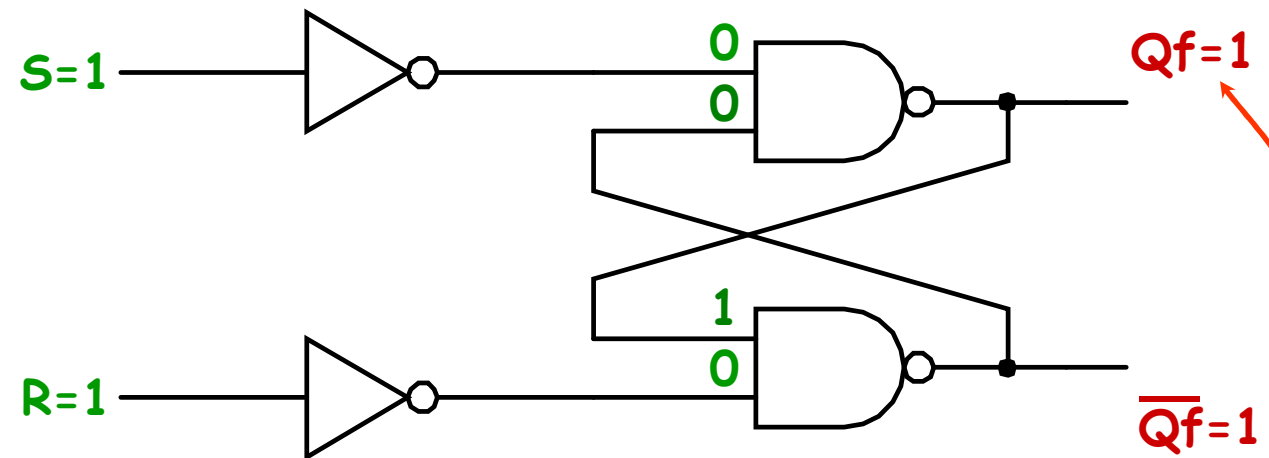


Caso 7

S	R	Q_a	\overline{Q}_a	Q_f	\overline{Q}_f
1	1	1	0		

Flip-Flop RS

Estudo de Casos

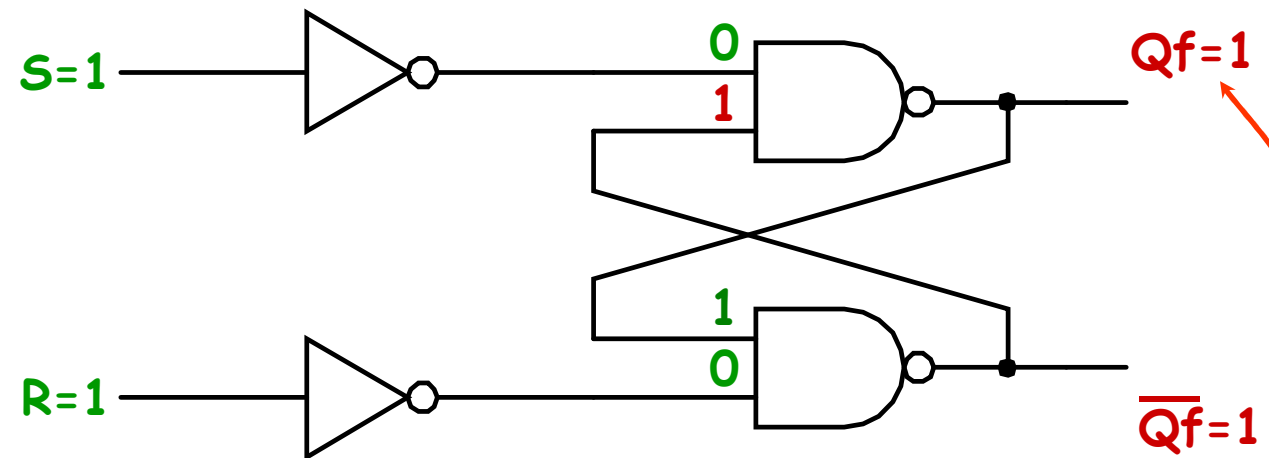


Caso 7

S	R	Q_a	\overline{Q}_a	Q_f	\overline{Q}_f
1	1	1	0		

Flip-Flop RS

Estudo de Casos



Caso 7

S	R	Qa	\overline{Qa}	Qf	\overline{Qf}
1	1	1	0	1	1

$Qf = \overline{Qf} = 1$ Viola a condição do FF RS

Flip-Flop RS

Tabela Verdade do FF RS

S	R	Q _a	Q _f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

Q_f=Q_a Mantém a saída anterior

Q_f=0 Reset da saída anterior

Q_f=1 Set da saída anterior

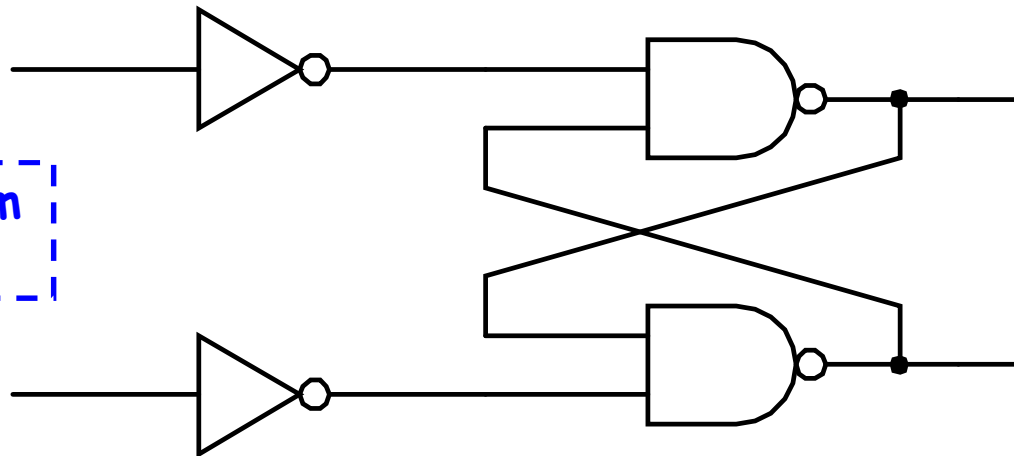
Entradas não permitidas

S	R	Q _f
0	0	Q _a
0	1	0
1	0	1
1	1	X

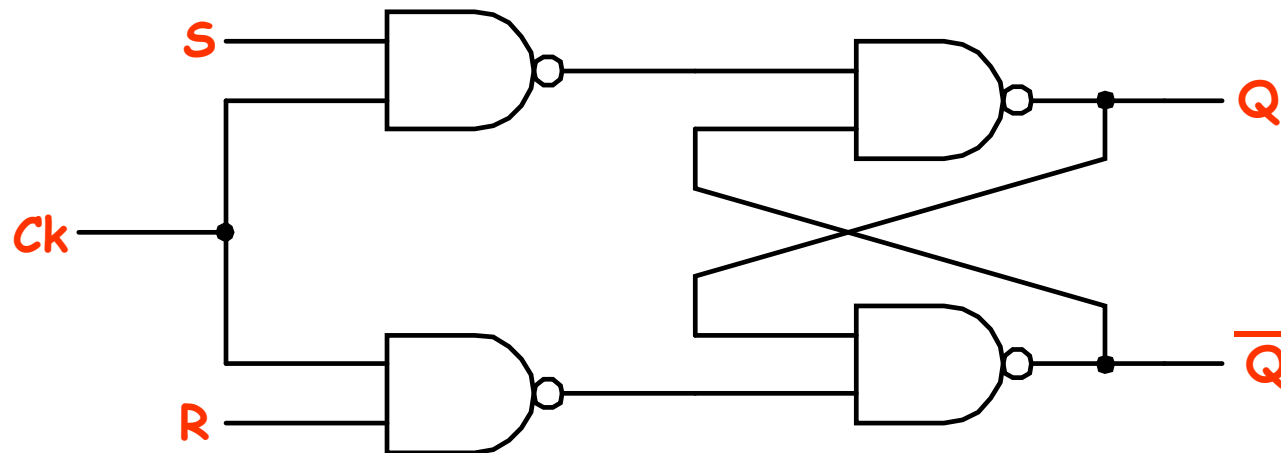
Flip-Flop RS - Sem Clock

Circuito do Latch ou FF RS

Enquanto as entradas variam
⇒ as saídas também variam



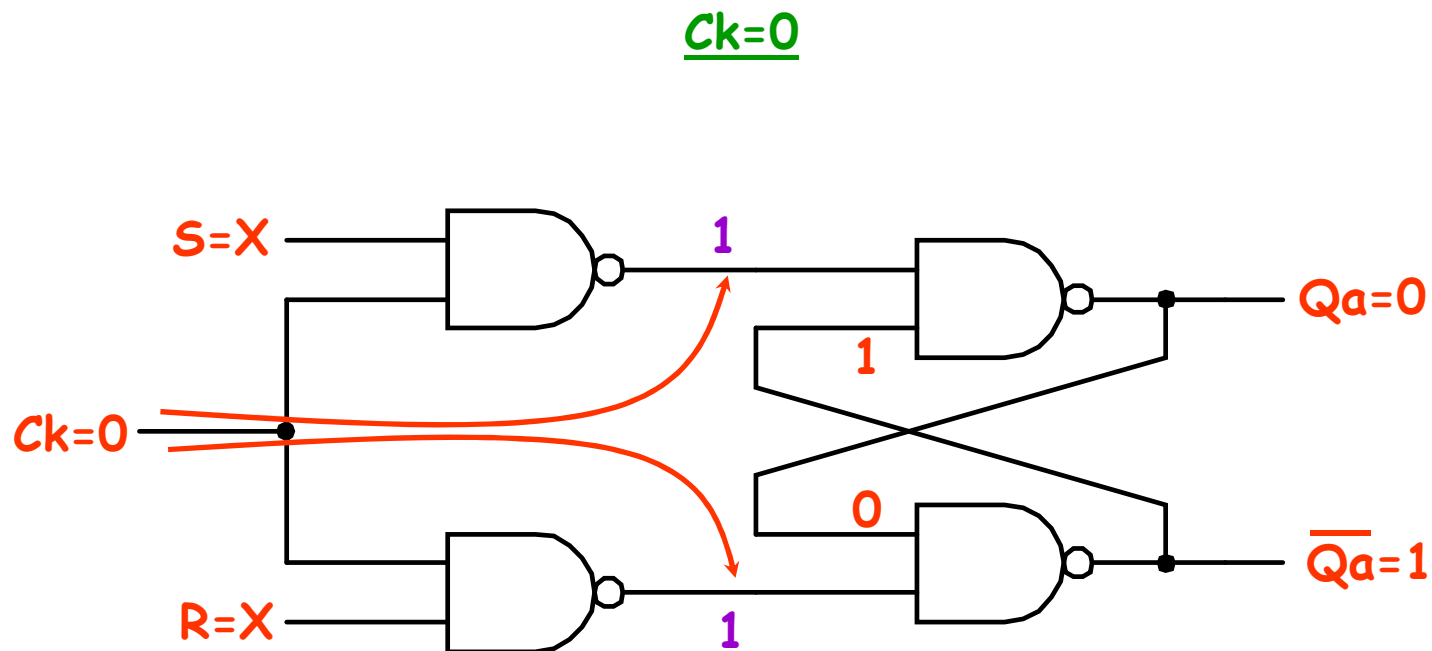
Flip-Flop RS com entrada clock



Se o clock=0 \Rightarrow FF permanece no seu estado anterior, mesmo que variem as entradas S e R

Se o clock=1 \Rightarrow FF funciona como um FF RS

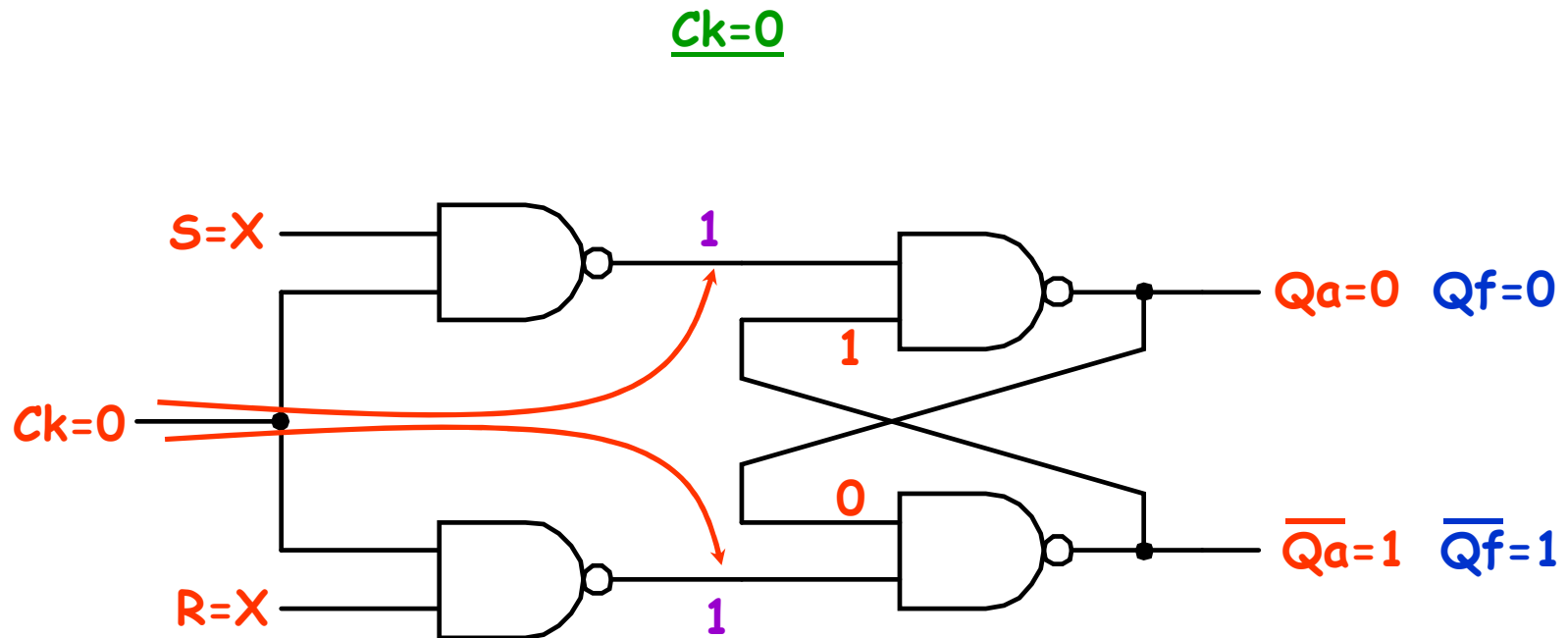
Flip-Flop RS com entrada clock



TV da NAND

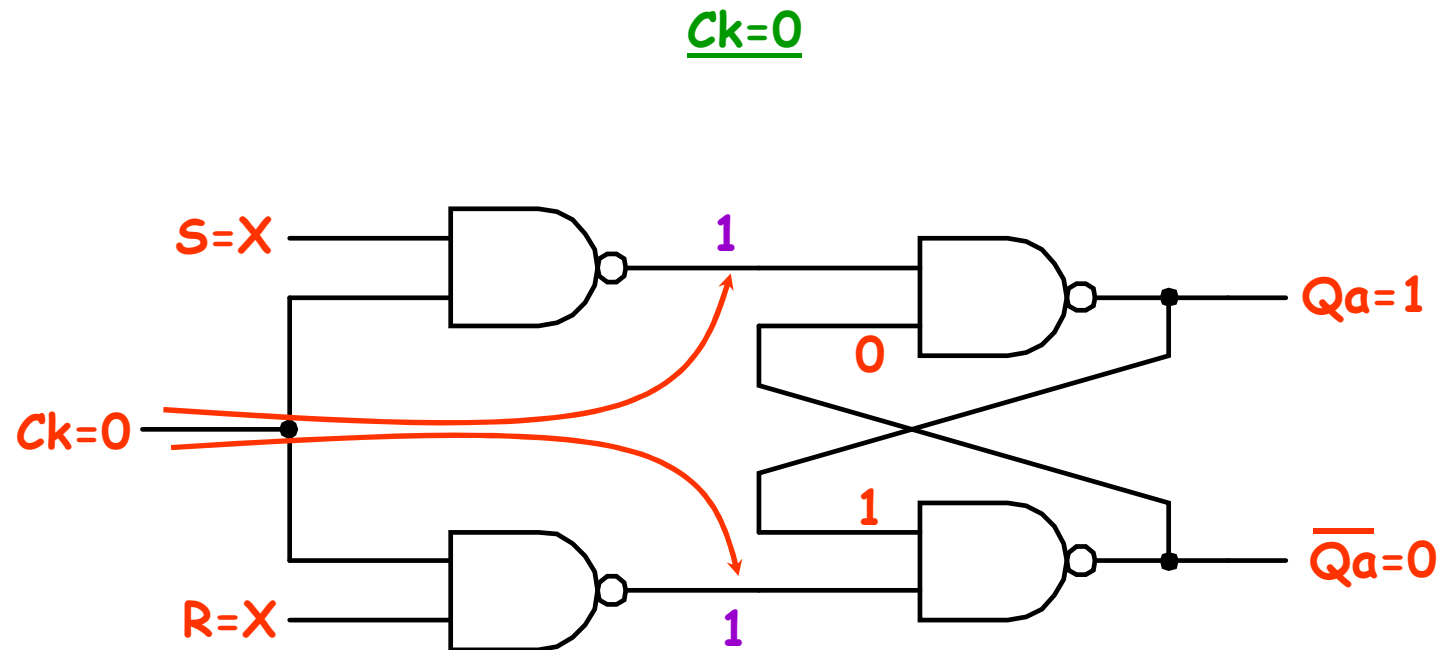
A	B	S
0	0	1
0	1	1
1	0	1
1	1	0

Flip-Flop RS com entrada clock

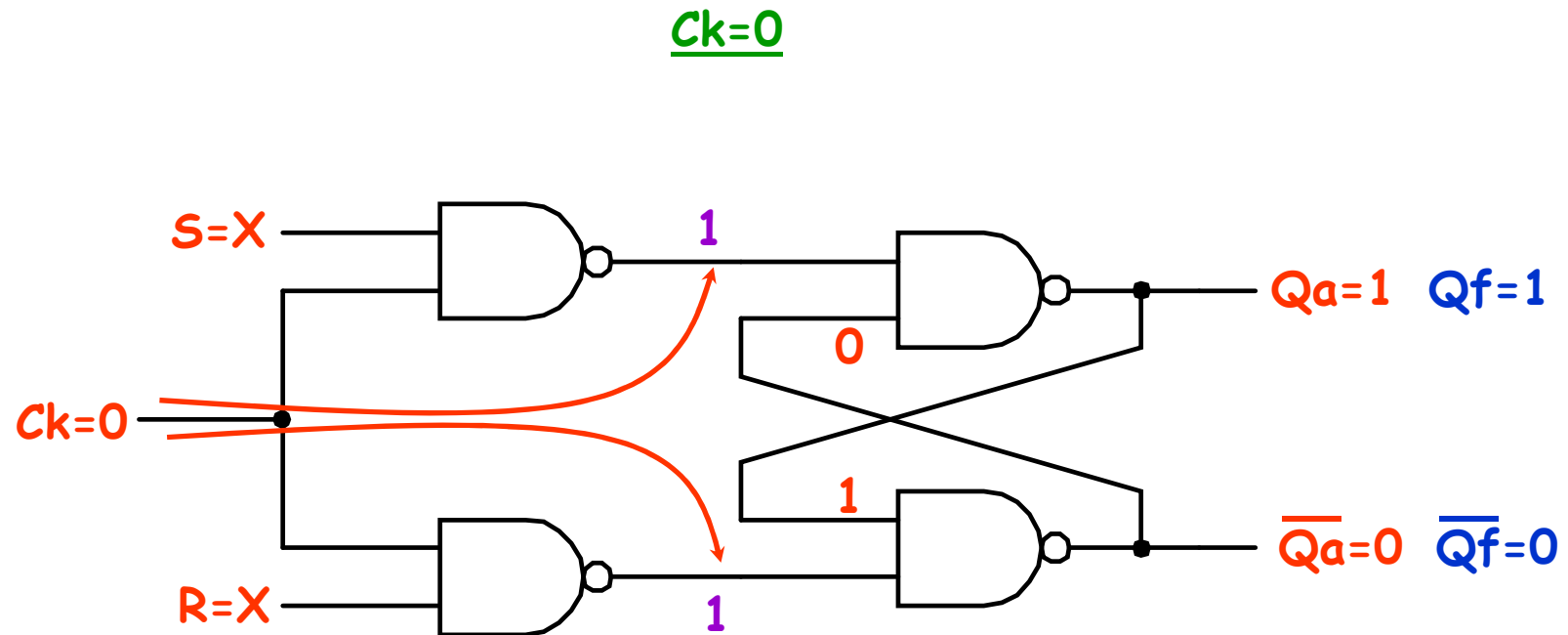


Para clock=0 \Rightarrow FF permanece no seu estado anterior

Flip-Flop RS com entrada clock



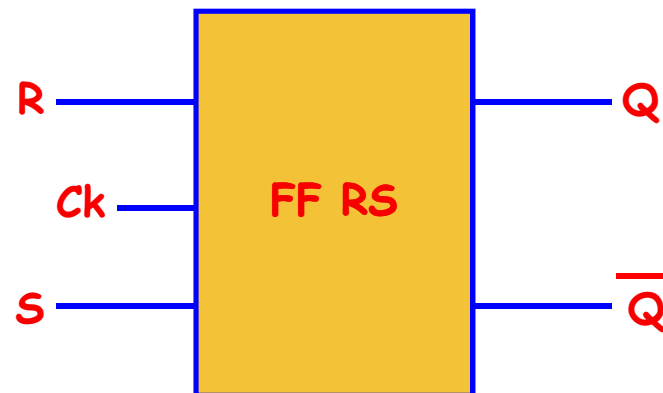
Flip-Flop RS com entrada clock



Para clock=0 \Rightarrow FF permanece no seu estado anterior

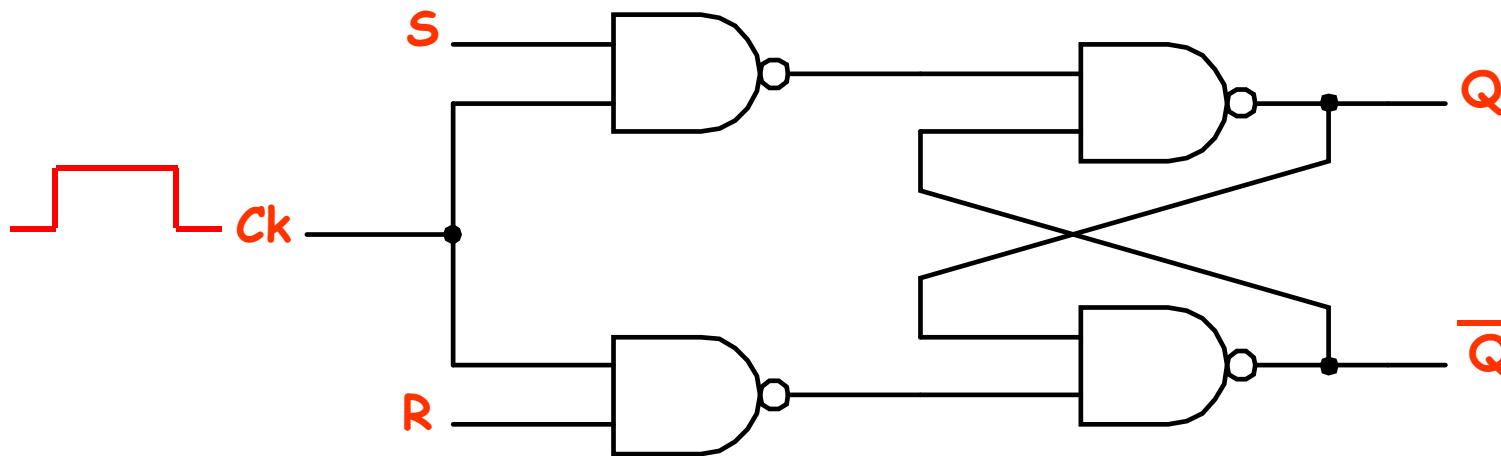
Flip-Flop RS com entrada clock

Símbolo FF RS com entrada clock



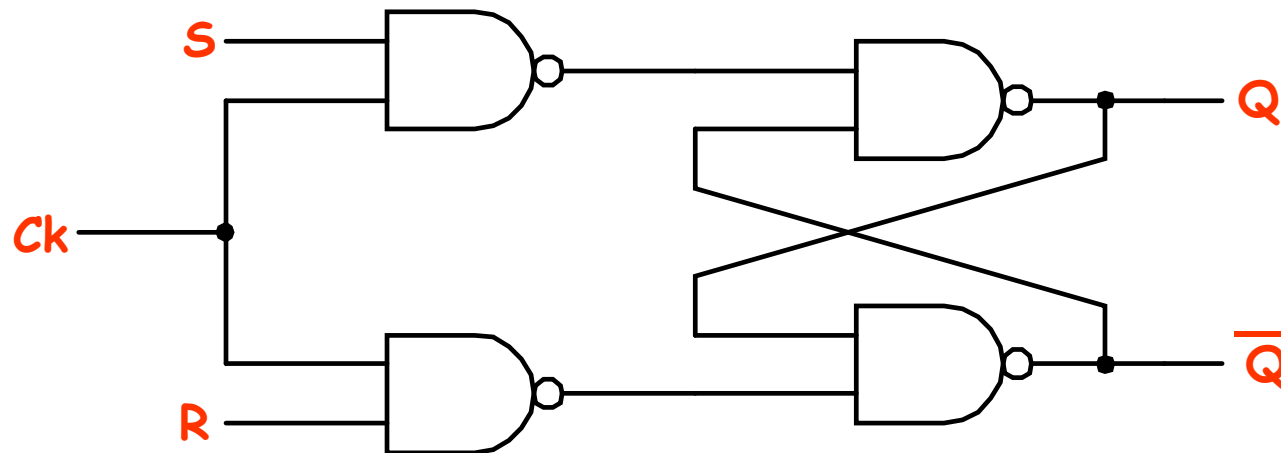
Flip-Flop sensível ao nível do clock

- Flip-Flop sensível ao nível do clock dispara sempre que o clock está num determinado estado lógico (chamado de LATCH)
- Alguns FFs são disparados pelo nível lógico 1 e alguns pelo nível lógico 0
- O FF abaixo é sensível ao nível porque ele responde às suas entradas R e S sempre que o clock está em ALTO



Tarefinha

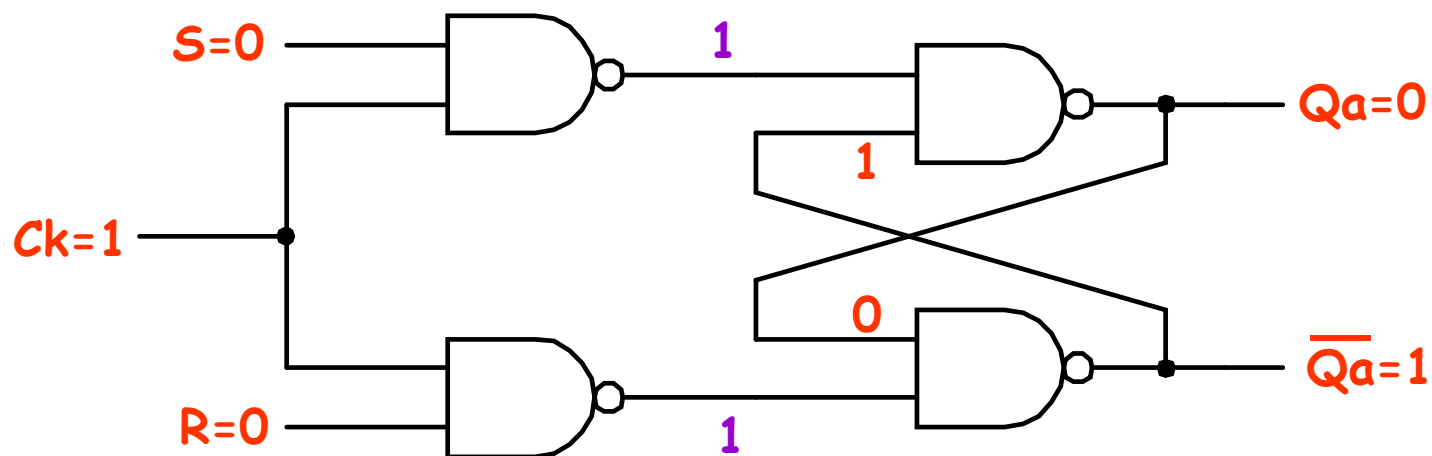
Mostre que o Flip-Flop RS com clock=1 opera normalmente como um FF RS



Solução

Ck=1

Caso 0



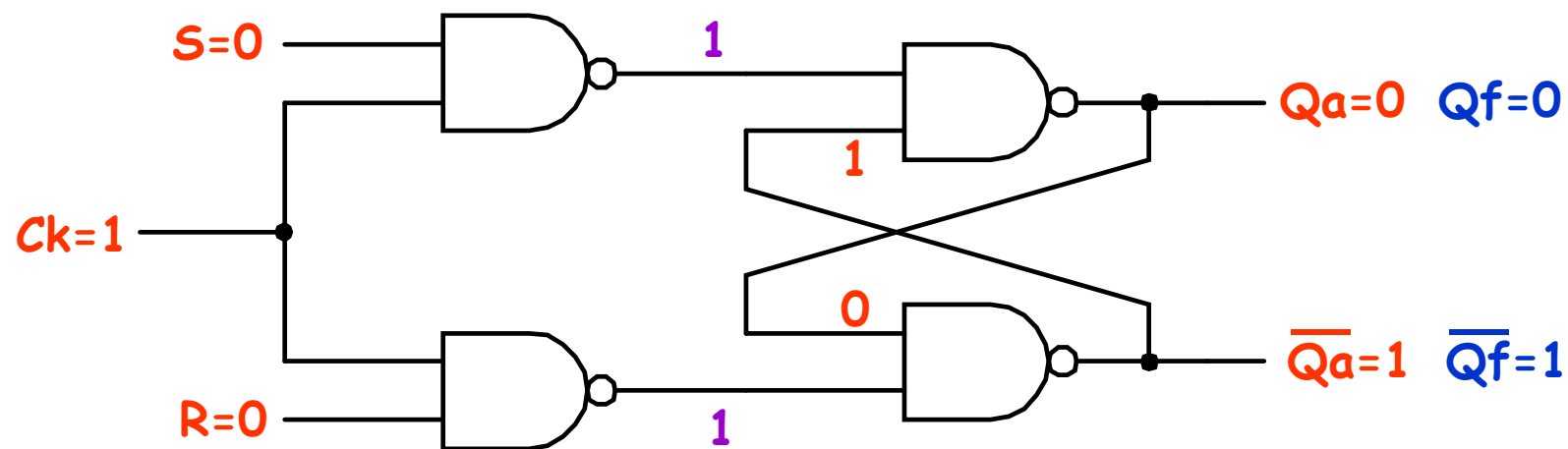
TV da NAND

A	B	S
0	0	1
0	1	1
1	0	1
1	1	0

Solução

Ck=1

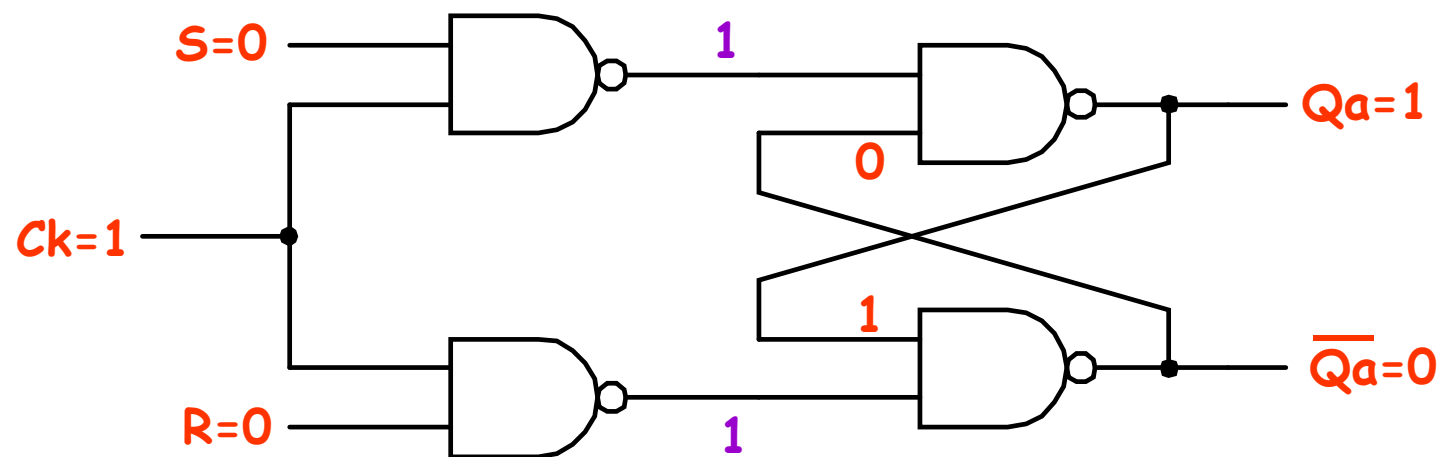
Caso 0



Solução

Ck=1

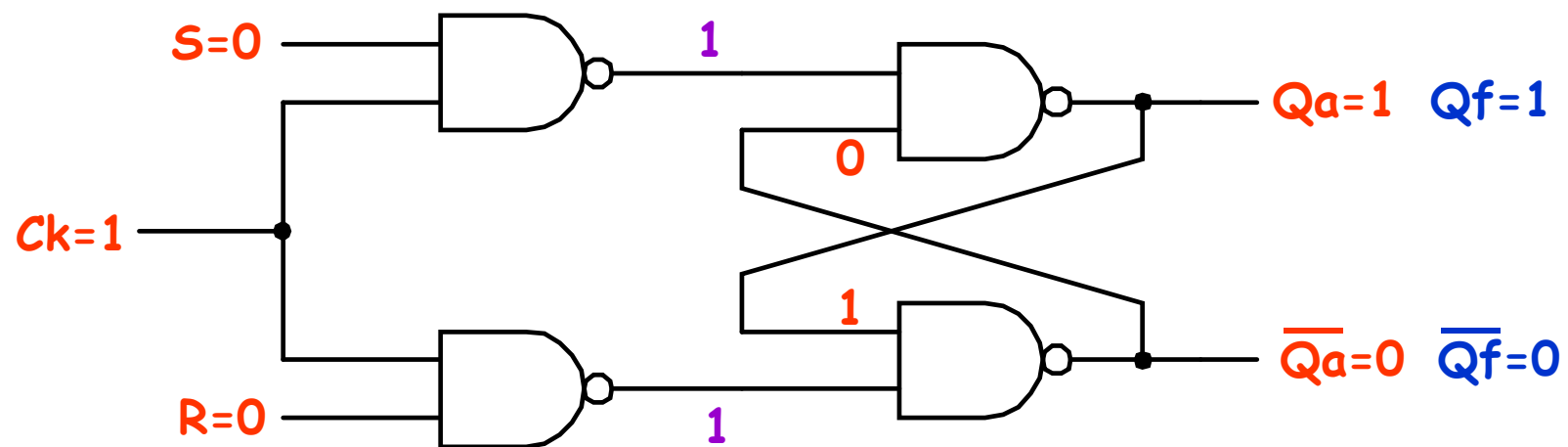
Caso 1



Solução

Ck=1

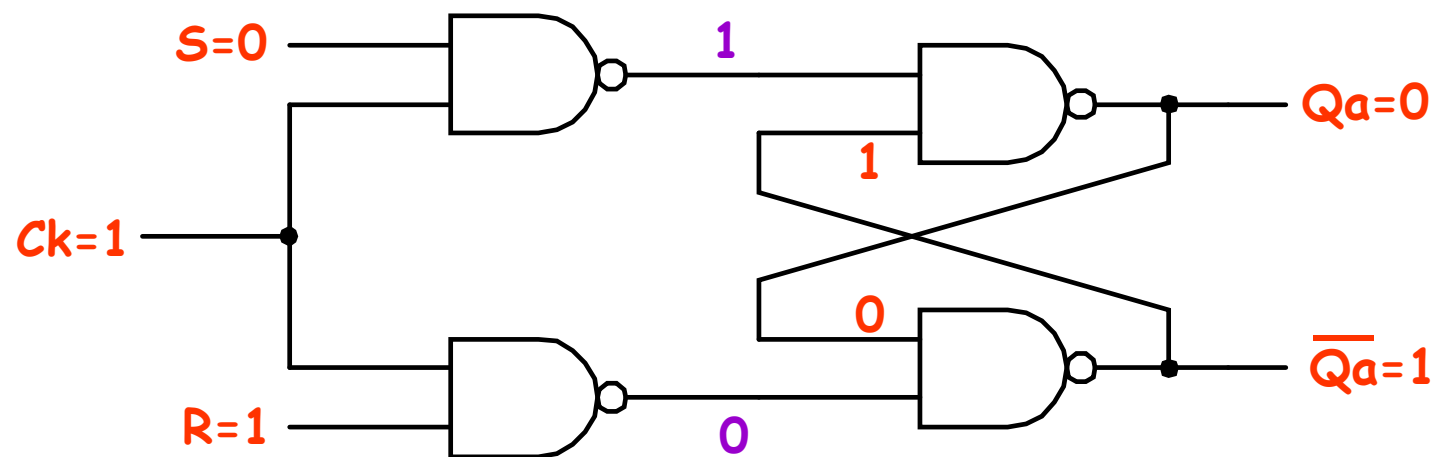
Caso 1



Solução

Ck=1

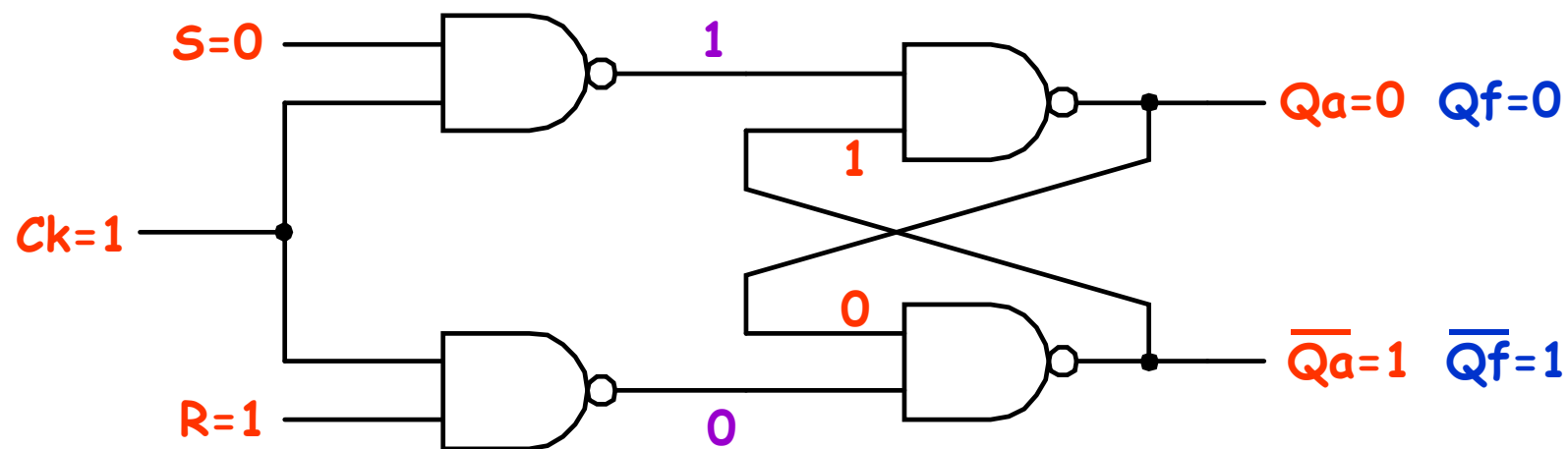
Caso 2



Solução

Ck=1

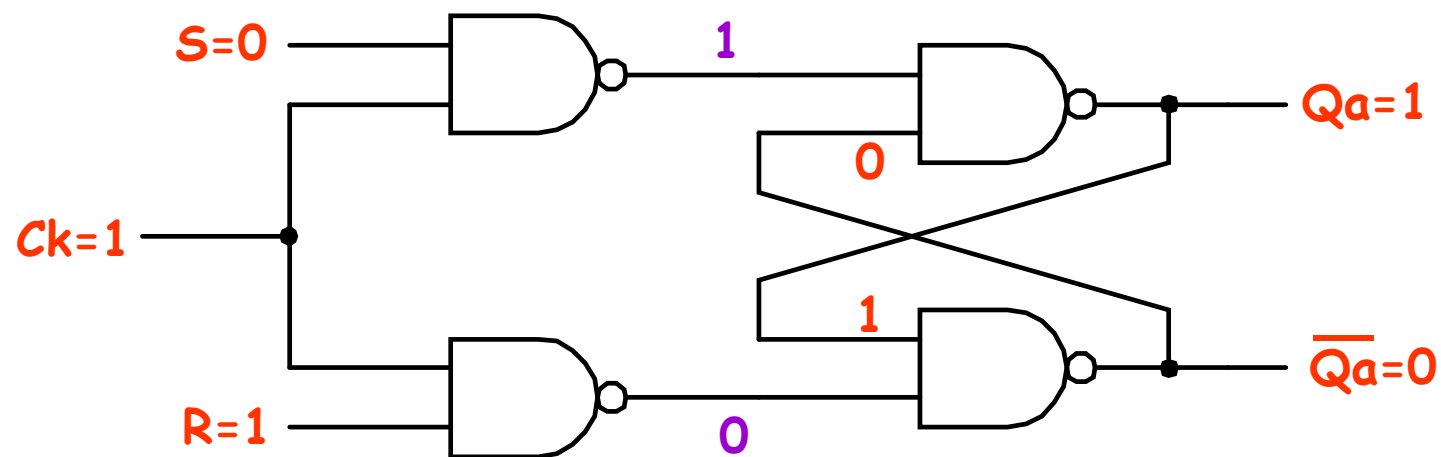
Caso 2



Solução

Ck=1

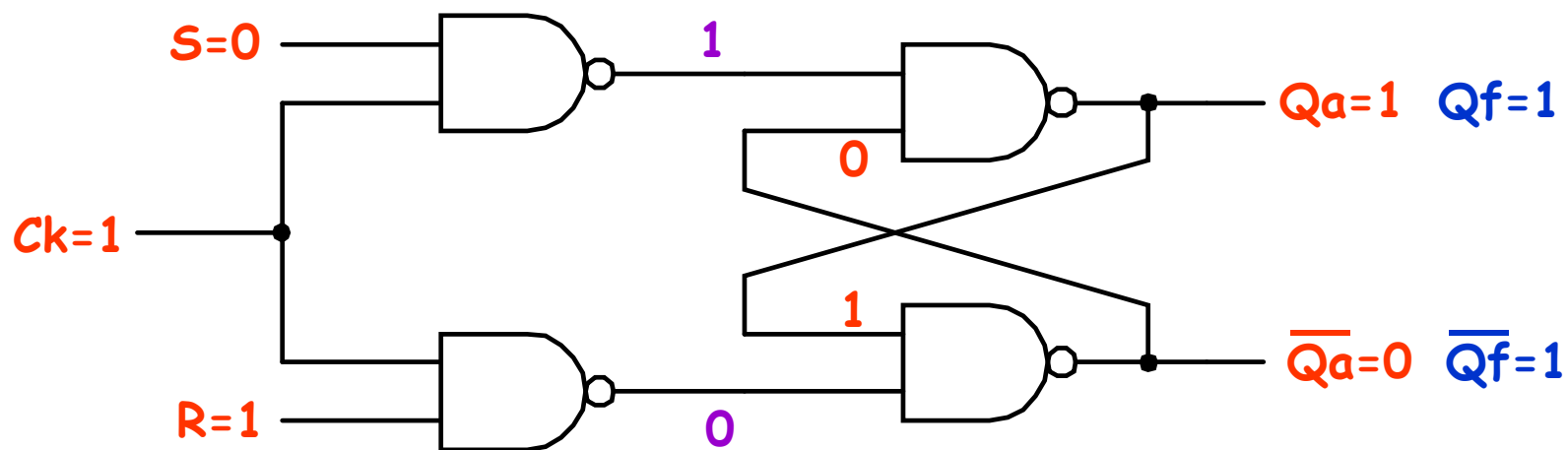
Caso 3



Solução

Ck=1

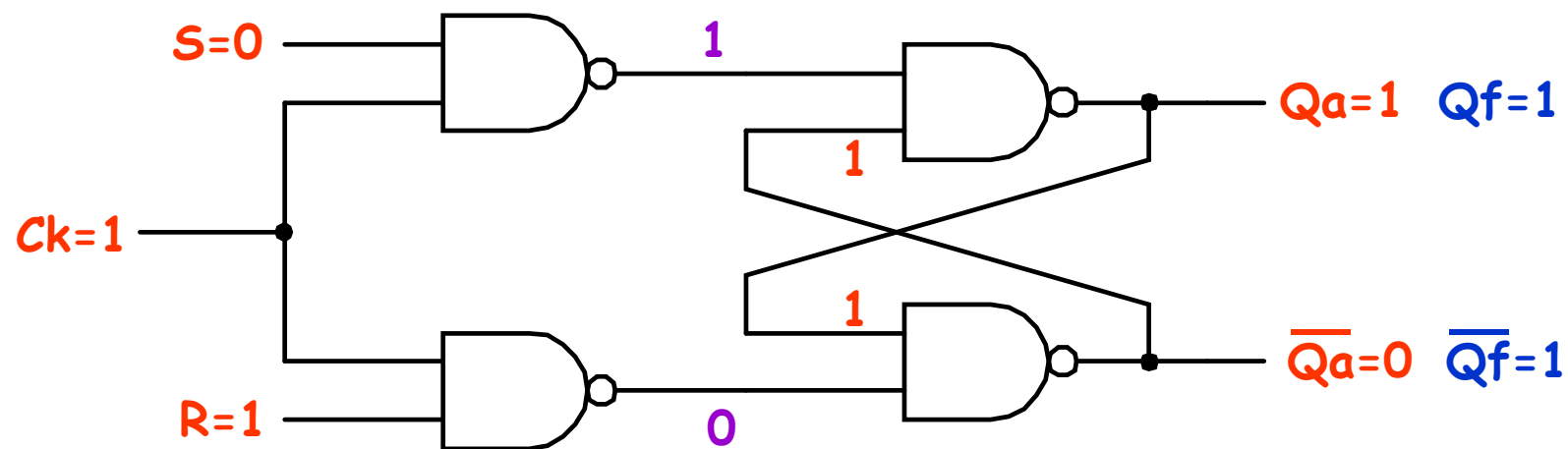
Caso 3



Solução

Ck=1

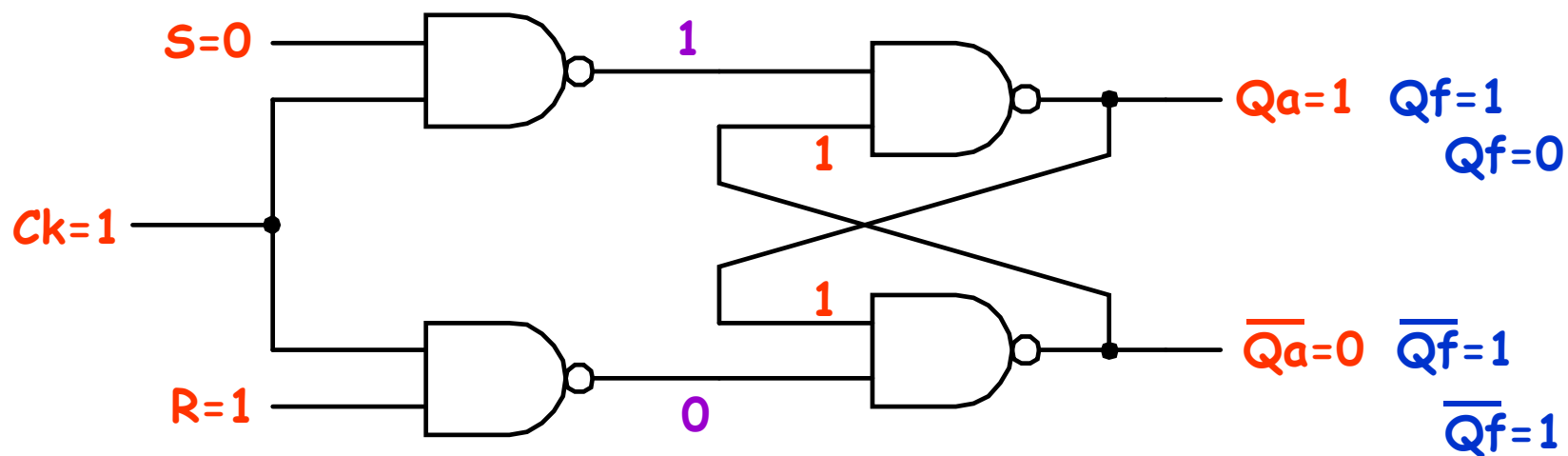
Caso 3



Solução

Ck=1

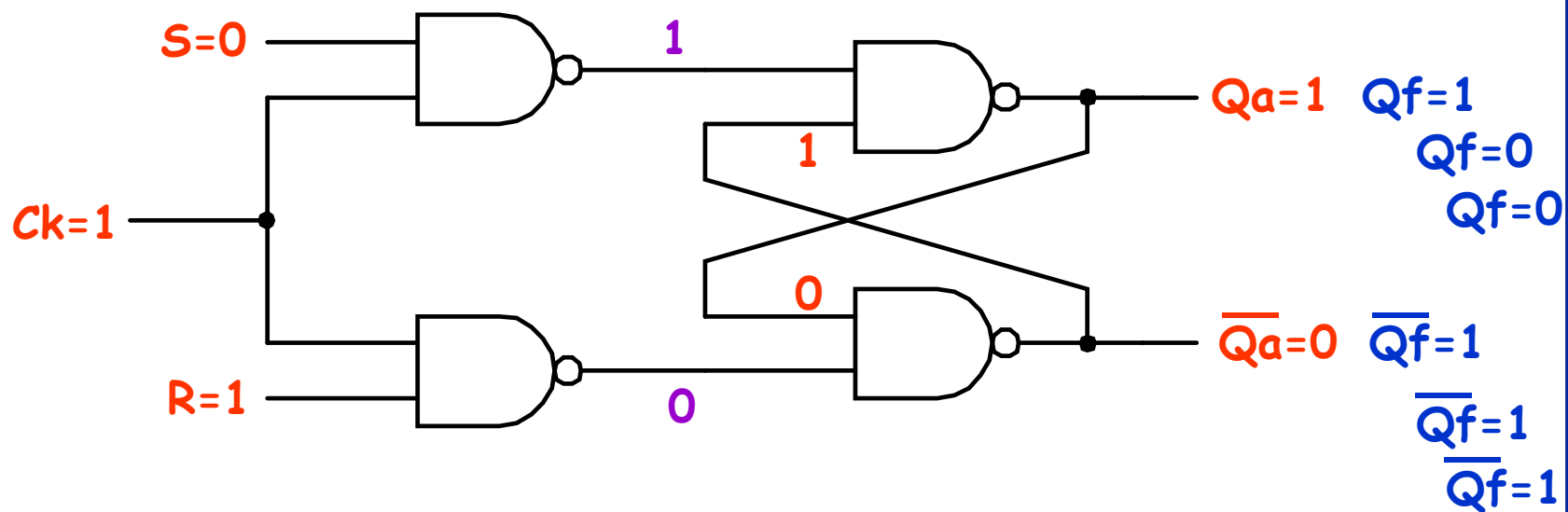
Caso 3



Solução

Ck=1

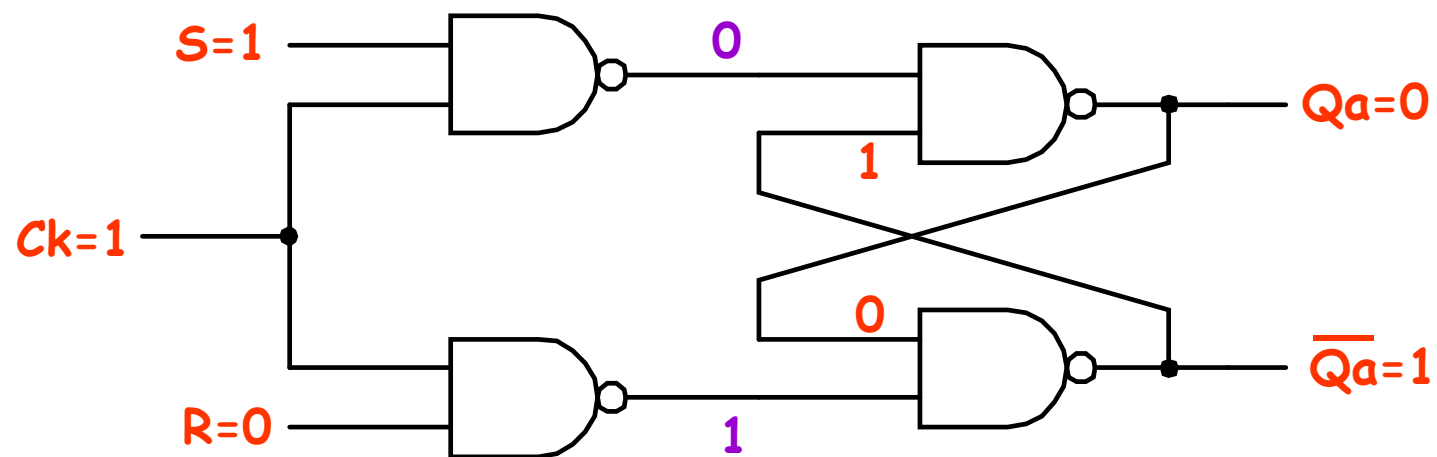
Caso 3



Solução

Ck=1

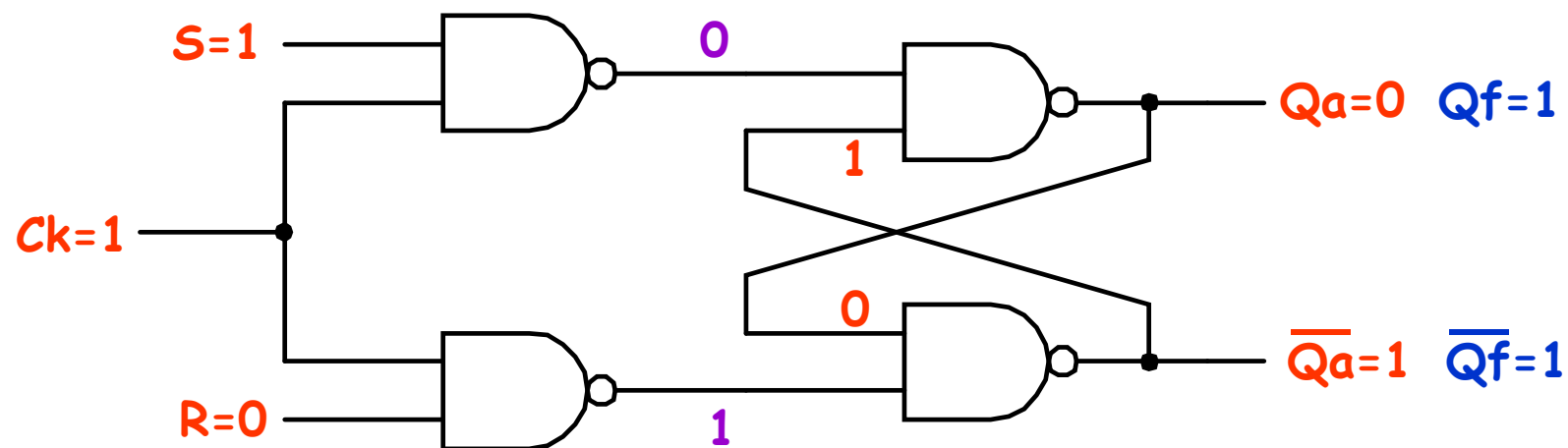
Caso 4



Solução

Ck=1

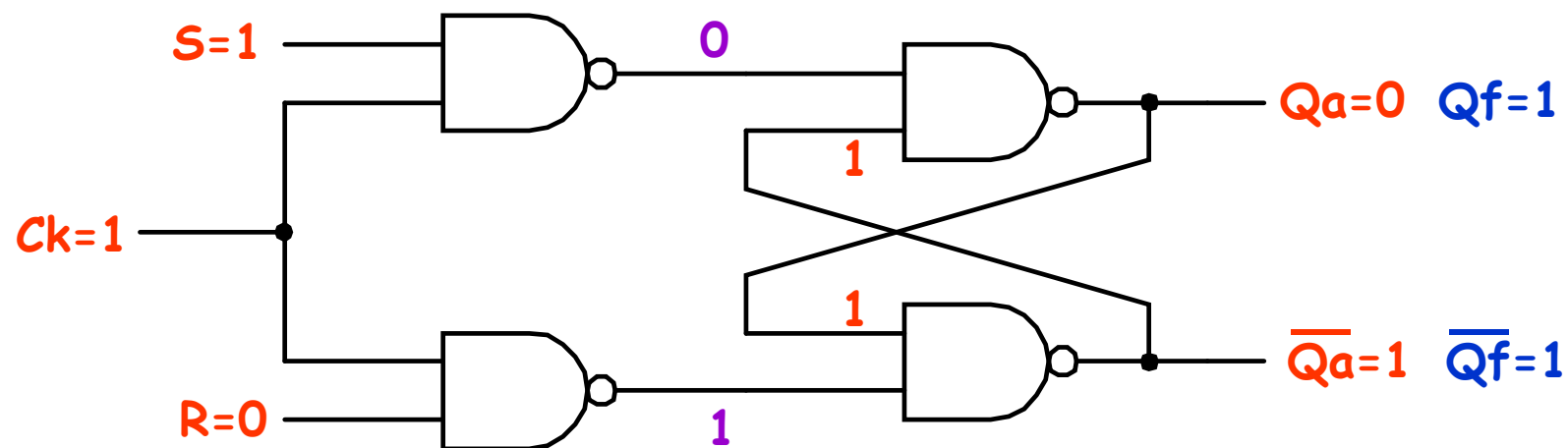
Caso 4



Solução

Ck=1

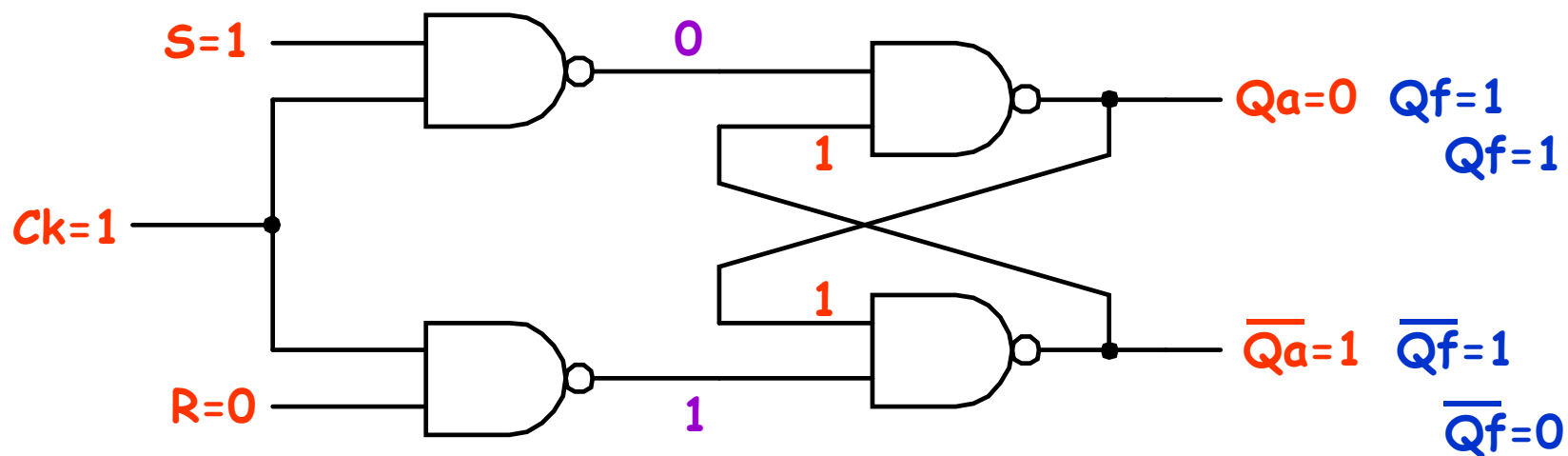
Caso 4



Solução

Ck=1

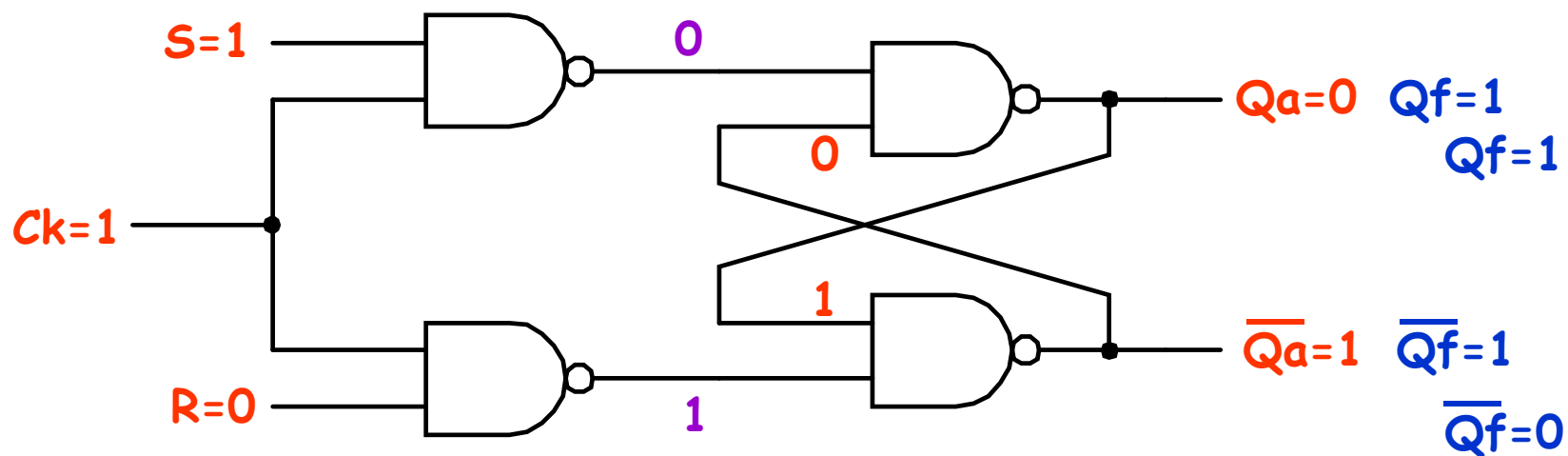
Caso 4



Solução

Ck=1

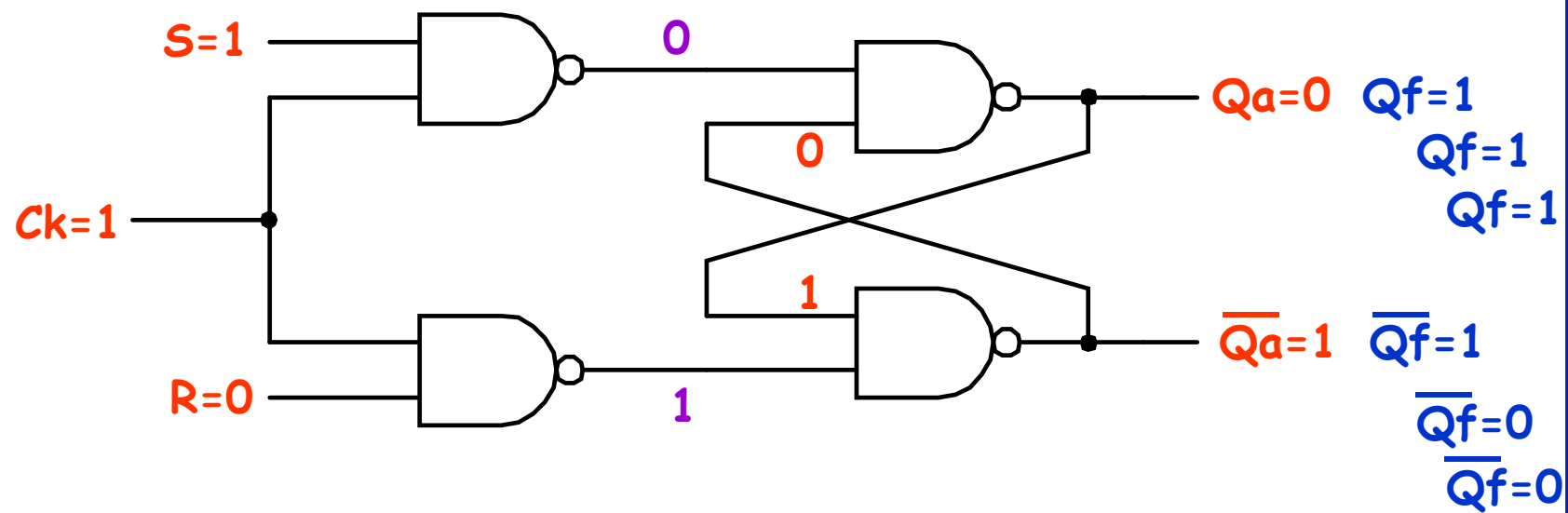
Caso 4



Solução

Ck=1

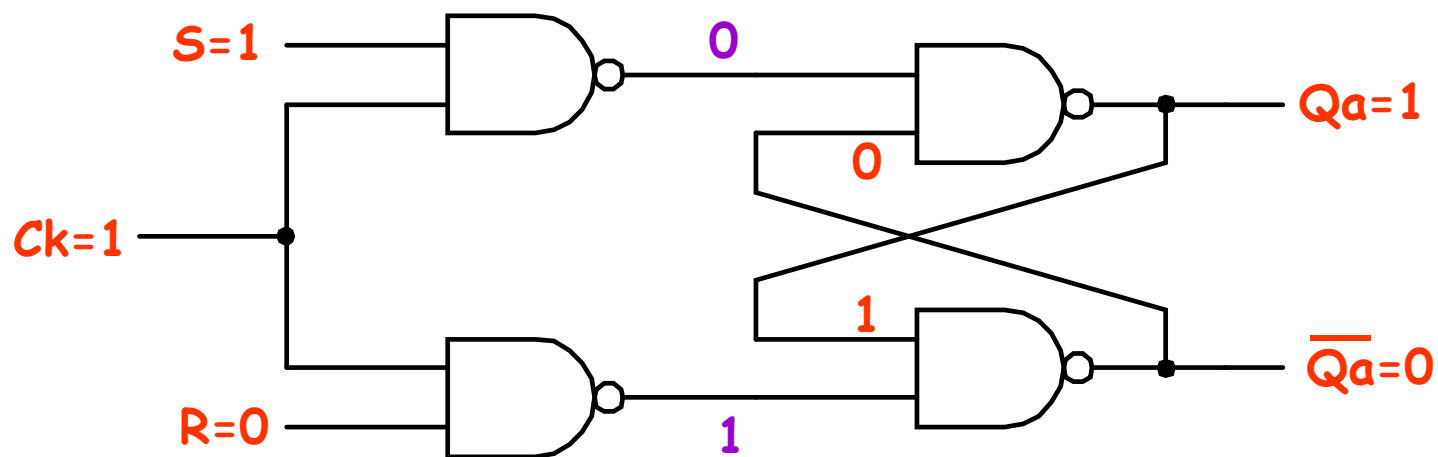
Caso 4



Solução

Ck=1

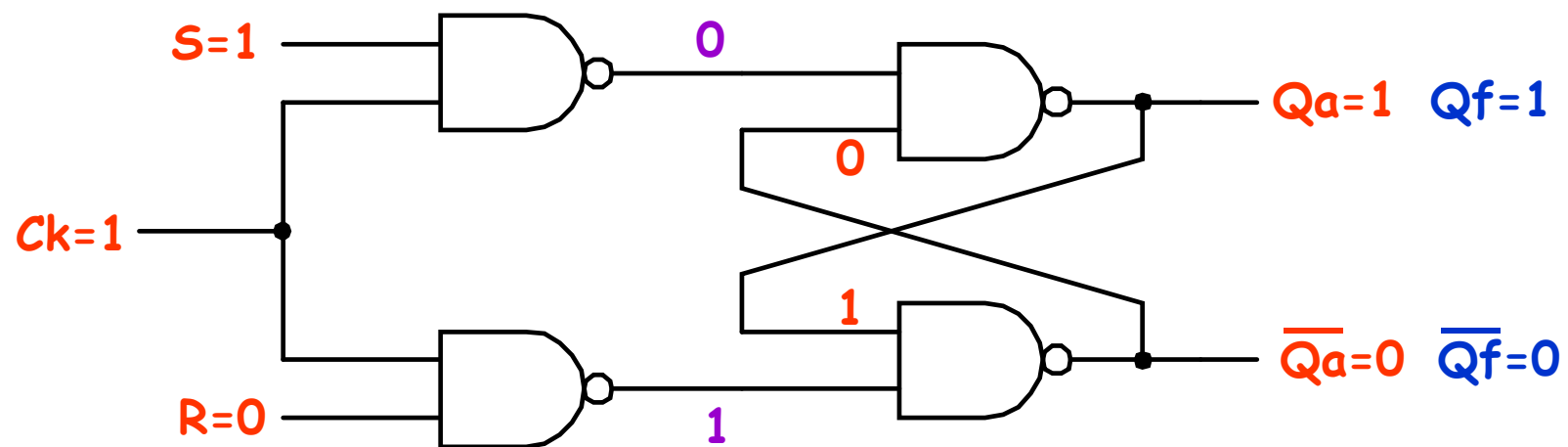
Caso 5



Solução

Ck=1

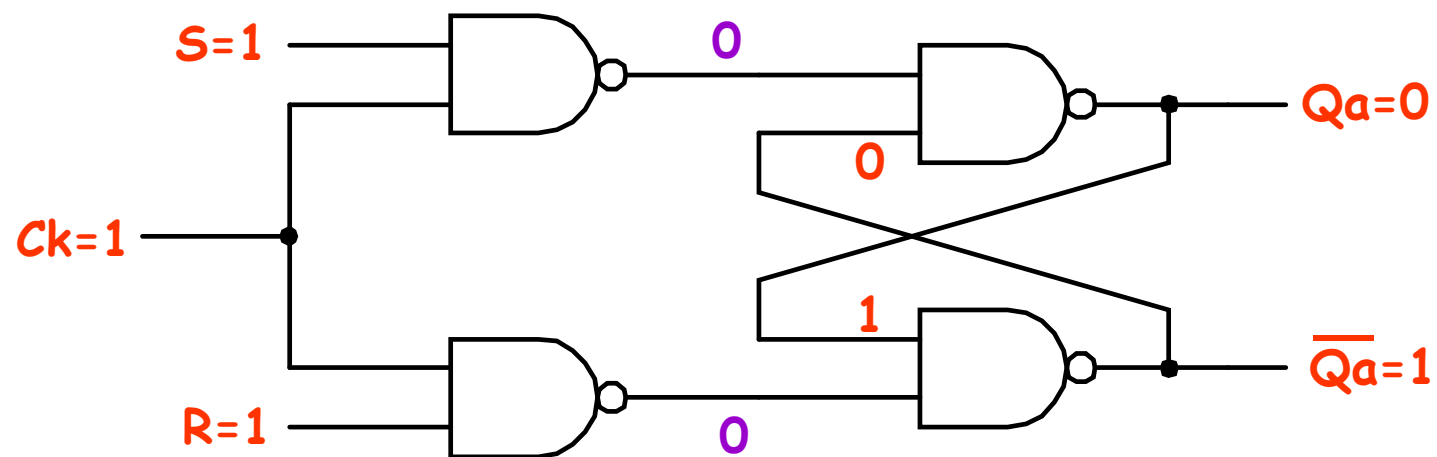
Caso 5



Solução

Ck=1

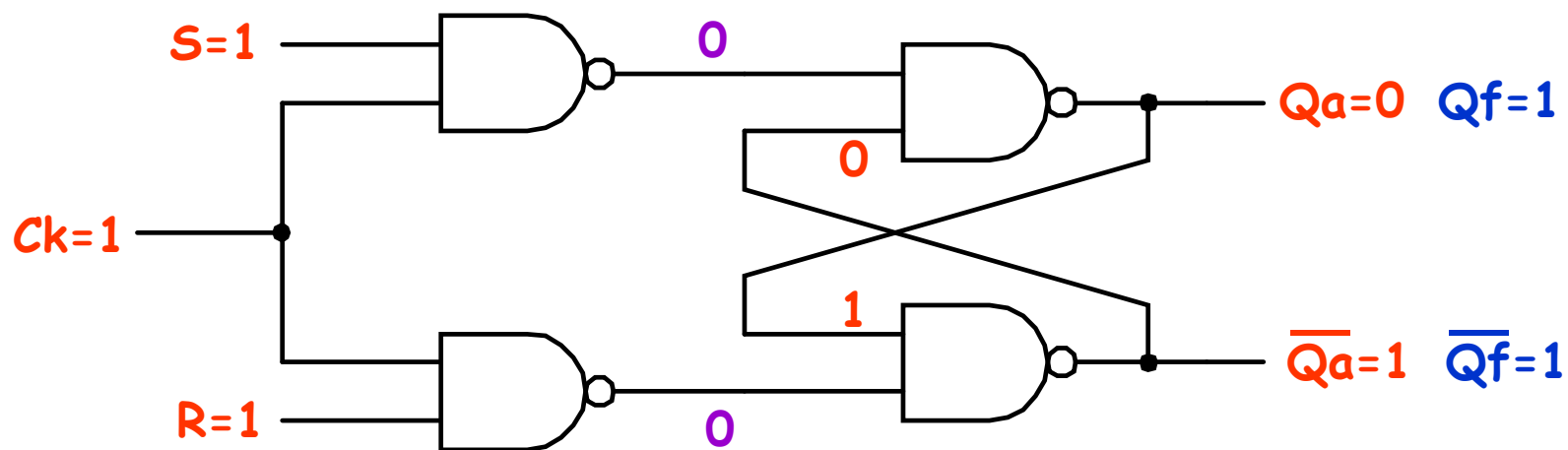
Caso 6



Solução

Ck=1

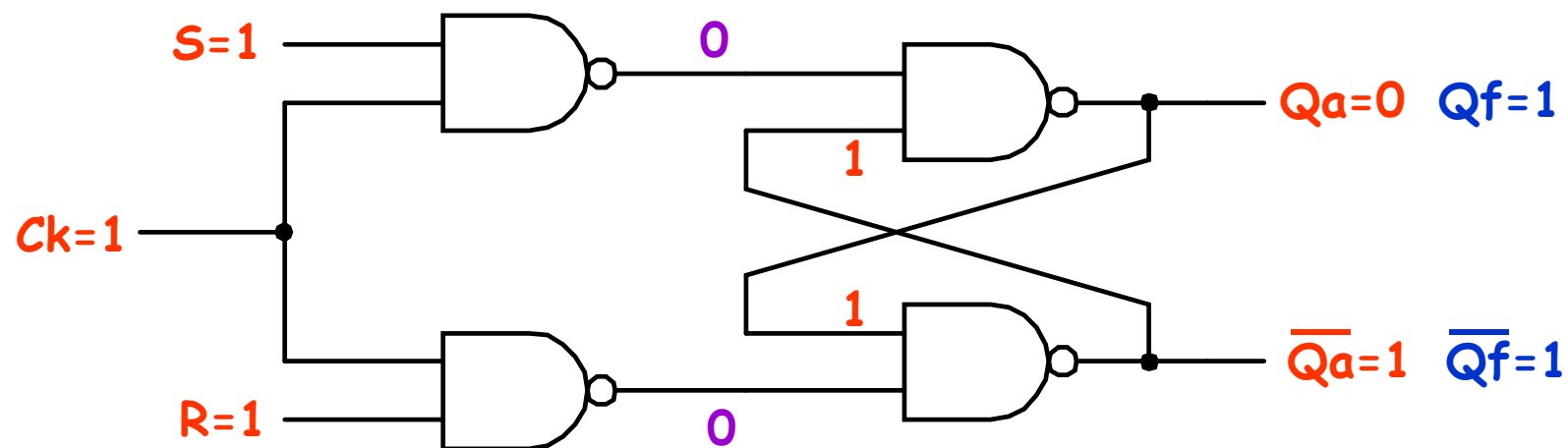
Caso 6



Solução

Ck=1

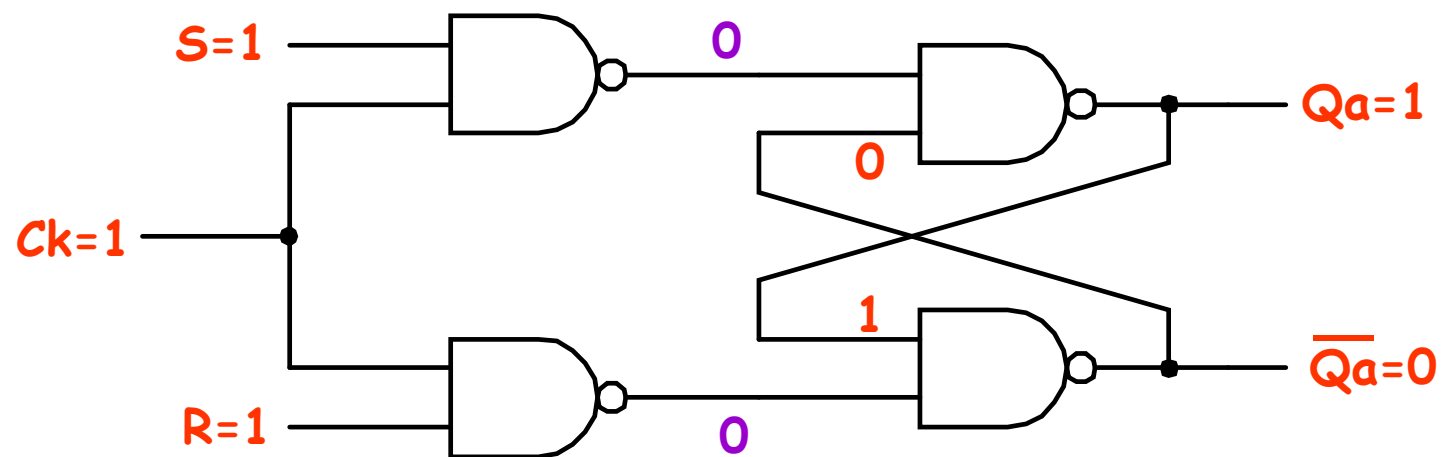
Caso 6



Solução

Ck=1

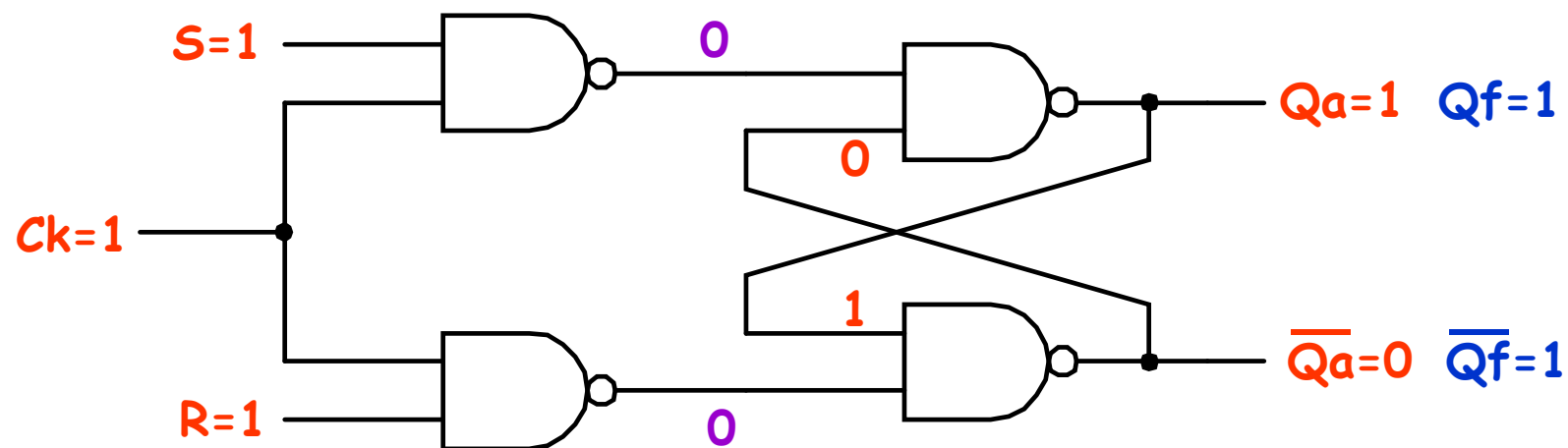
Caso 7



Solução

Ck=1

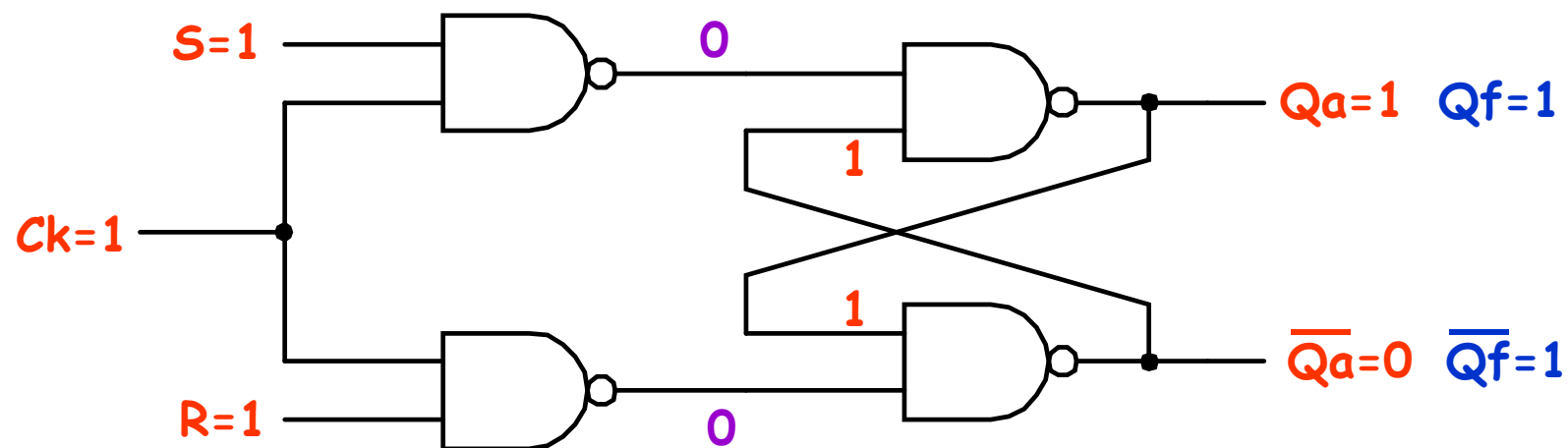
Caso 7



Solução

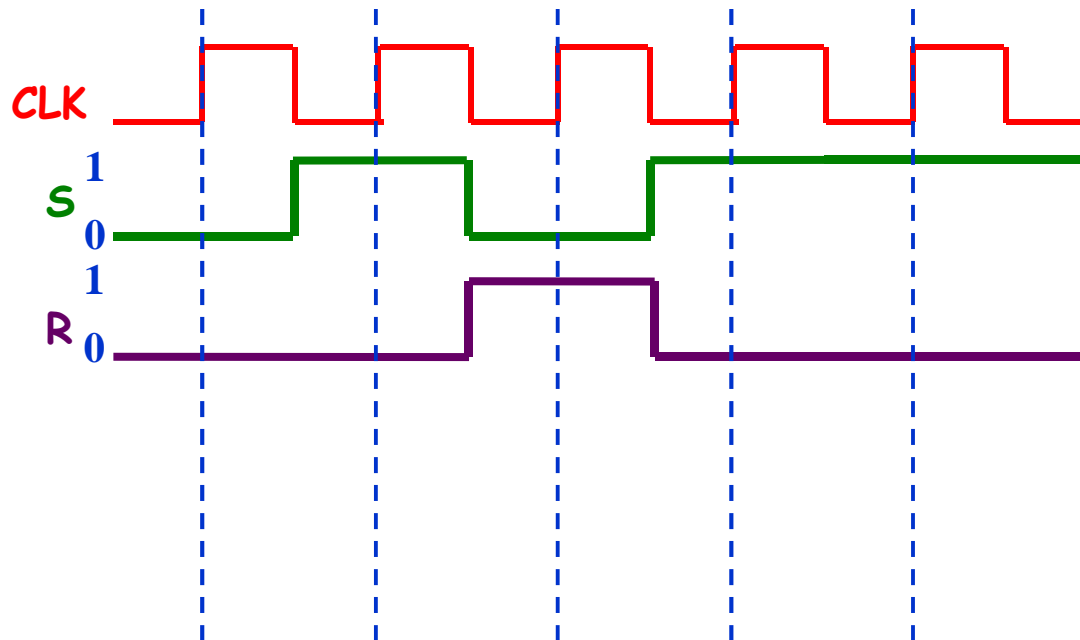
Ck=1

Caso 7



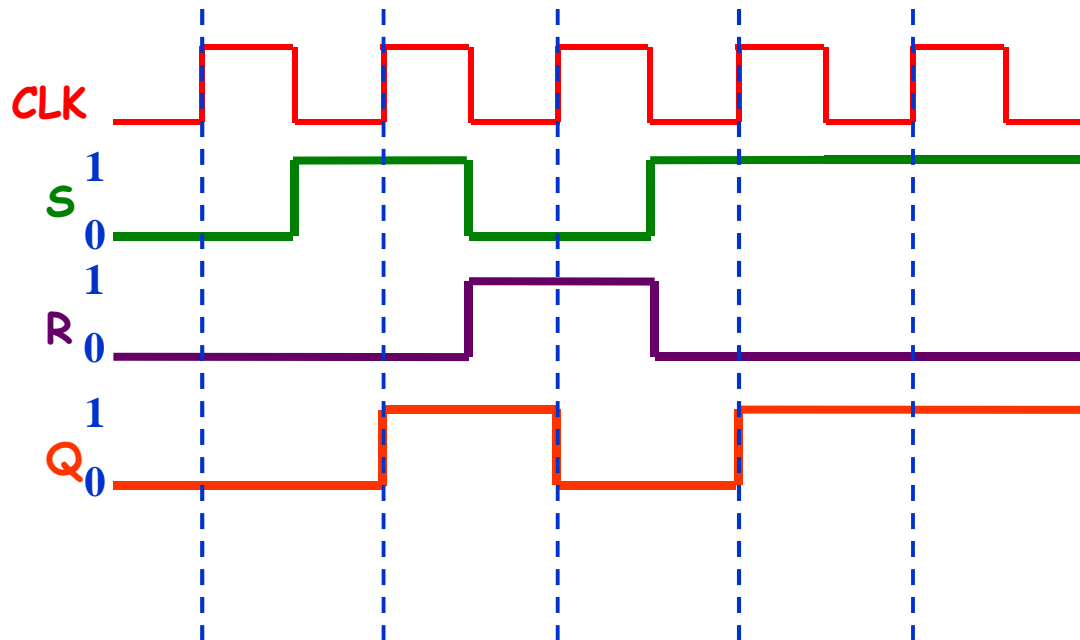
Exercício

1. Faça o diagrama de forma de onda da saída Q de um Flip-Flop RS com entrada clock igual a 1. Considere que a saída Q é inicialmente 0.

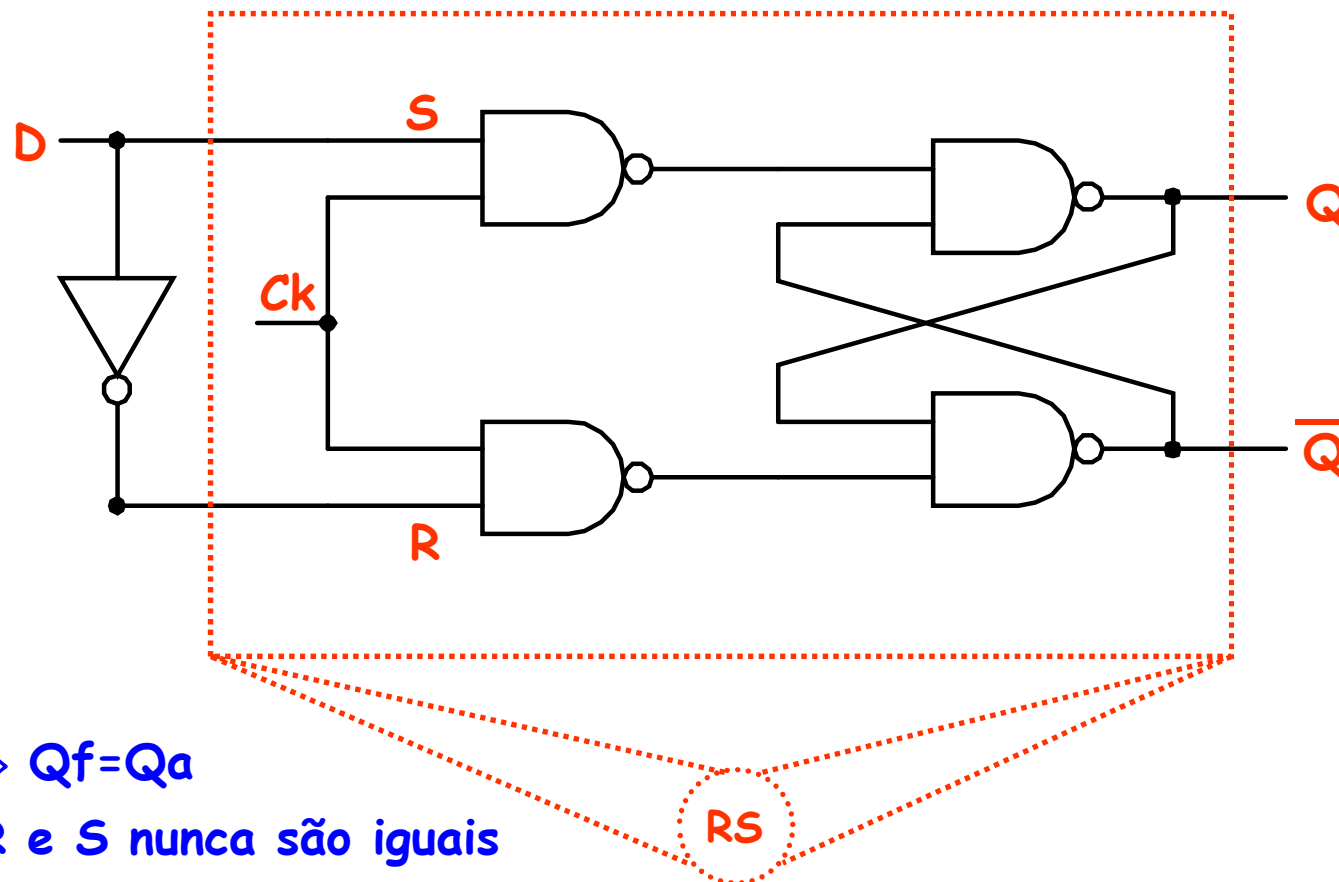


Solução

1. Faça o diagrama de forma de onda da saída Q de um Flip-Flop RS com entrada clock igual a 1. Considere que a saída Q é inicialmente 0.



Flip-Flop Tipo D com entrada clock

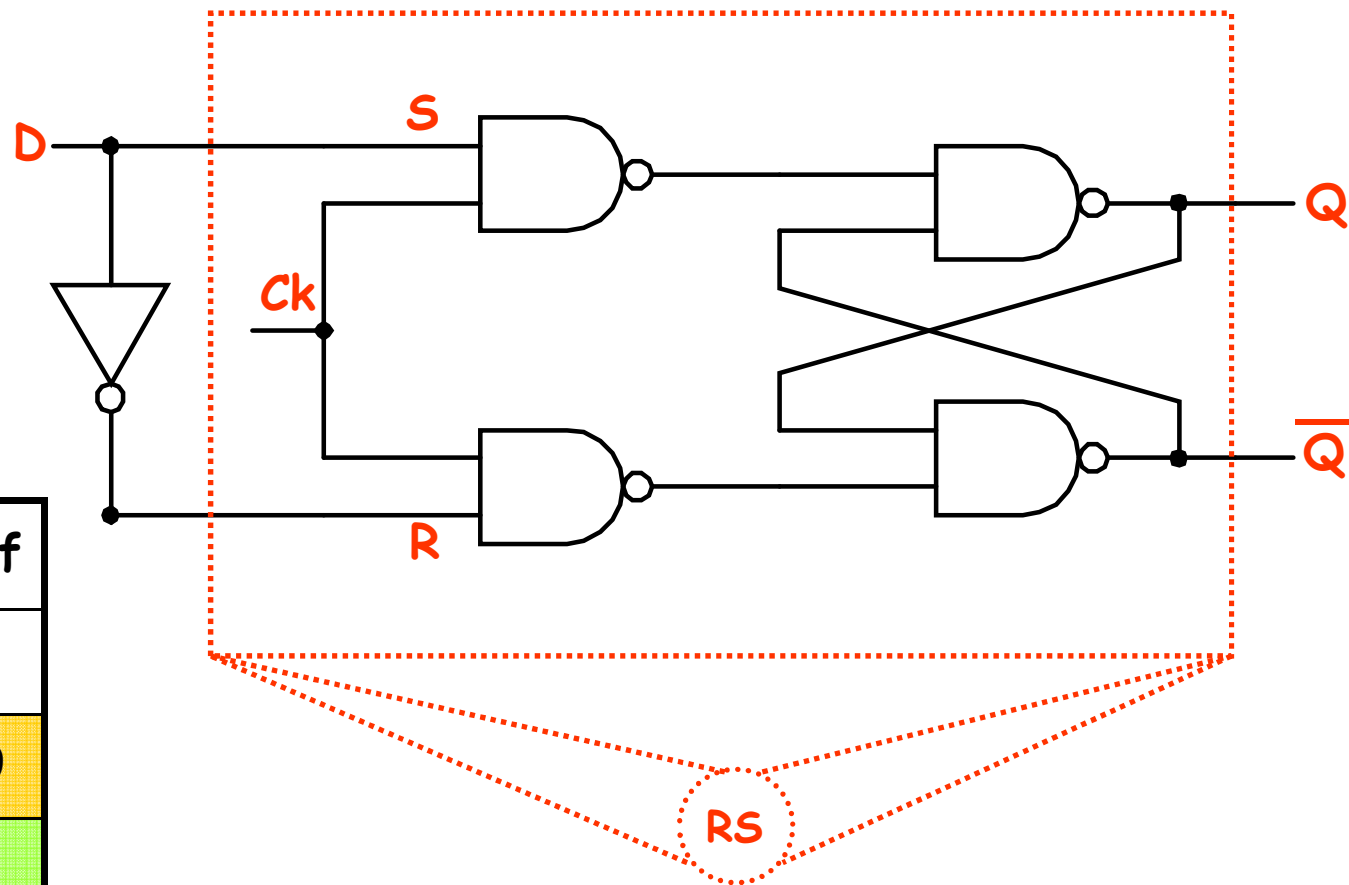


Se $Ck=0 \Rightarrow Q_f=Q_a$

Entradas R e S nunca são iguais

Flip-Flop Tipo D com entrada clock

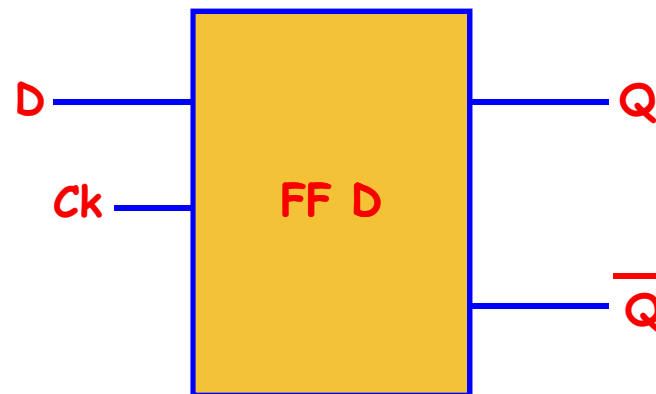
D	S	R	Qf
∅	0	0	-
0	0	1	0
1	1	0	1
∅	1	1	-



Flip-Flop Tipo D com entrada clock

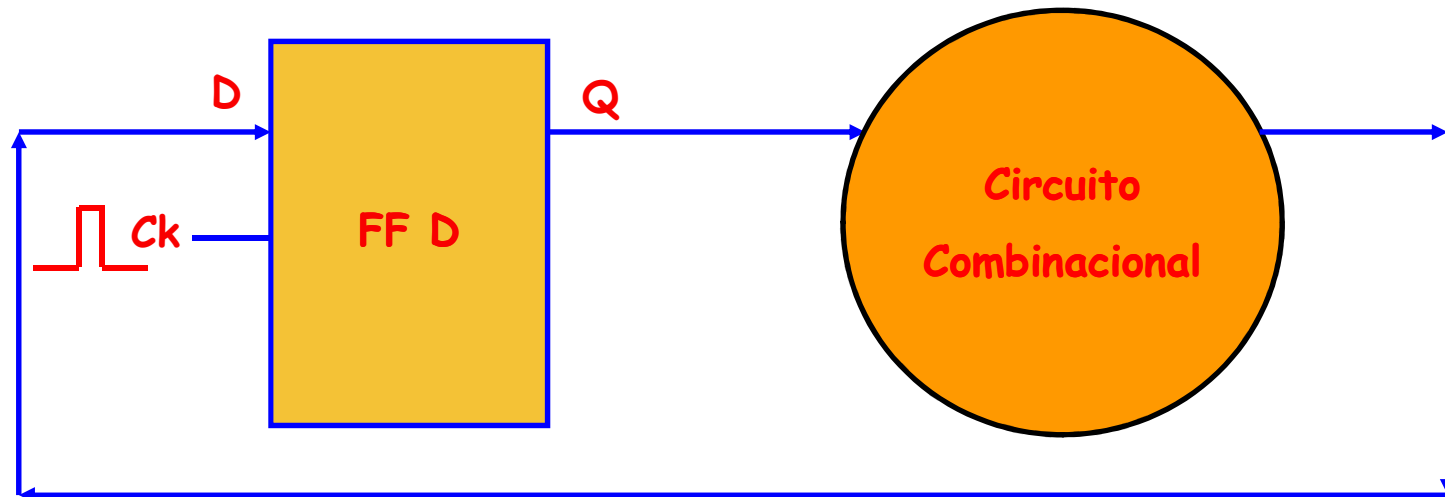
Símbolo FF Tipo D com entrada clock

D	Qf
0	0
1	1



FF sensível ao nível do clock

- **Problema:** Flip-Flop sensível ao nível do clock é instável para certas aplicações
- A saída atual do FF D (Q) é realimentada através de um circuito combinacional para gerar uma nova entrada D
- Quando o FF é disparado o valor de D é transferido para a saída para gerar novo valor de Q^+
- Se o clock é sensível ao nível então Q pode viajar pelo circuito combinacional e mudar o valor de D e conseqüentemente a saída Q
- Para evitar esse problema o pulso de clock deveria ser muito estreito



Resumo da Aula de Hoje

Tópicos mais importantes:

- **Circuitos Sequenciais:**
 - Flip-Flop Tipo RS
 - Flip-Flop Tipo D