12-Bit Binary Counter

The MC14040B 12-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range
- Common Reset Line
- Pin-for-Pin Replacement for CD4040B

MAXIMUM RATINGS (Voltages Referenced to VSS) (Note 2.)

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P _D	Power Dissipation, per Package (Note 3.)	500	mW
T _A	Ambient Temperature Range	-55 to +125	°C
T _{stg}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature (8–Second Soldering)	260	°C

- Maximum Ratings are those values beyond which damage to the device may occur.
- Temperature Derating: Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}.$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



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MARKING DIAGRAMS

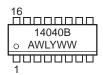


PDIP-16 P SUFFIX CASE 648





SOIC-16 D SUFFIX CASE 751B



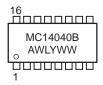


TSSOP-16 DT SUFFIX CASE 948F





SOEIAJ-16 F SUFFIX CASE 966



A = Assembly Location

WL or L = Wafer Lot YY or Y = Year WW or W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14040BCP	PDIP-16	2000/Box
MC14040BD	SOIC-16	2400/Box
MC14040BDR2	SOIC-16	2500/Tape & Reel
MC14040BDT	TSSOP-16	96/Rail
MC14040BF	SOEIAJ-16	See Note 1.
MC14040BFEL	SOEIAJ-16	See Note 1.

 For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

PIN ASSIGNMENT

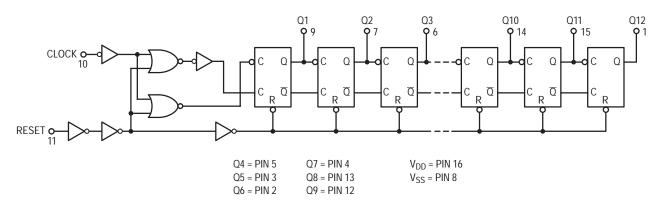
Q12 [1 ●	16	D V _{DD}
Q6 [2	15	Q11
Q5 [3	14	Q10
Q7 [4	13] Q8
Q4 [5	12	Q9
Q3 [6	11	R
Q2 [7	10] C
V _{SS} [8	9	Q1

TRUTH TABLE

Clock	Reset	Output State
	0	No Change
_	0	Advance to next state
Х	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

			V _{DD}	- 5	5°C		25°C		125	i°C	
Characteristic		Symbol	Vdc	Min	Max	Min	Typ ^(4.)	Max	Min	Max	Unit
Output Voltage " V _{in} = V _{DD} or 0	'0" Level	V _{OL}	5.0 10 15	_ _ _	0.05 0.05 0.05	_ _ _	0 0 0	0.05 0.05 0.05	_ _ _	0.05 0.05 0.05	Vdc
$V_{in} = 0 \text{ or } V_{DD}$	'1" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95	_ _ _	4.95 9.95 14.95	5.0 10 15	_ _ _	4.95 9.95 14.95	_ _ _	Vdc
Input Voltage " (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	'0" Level	V _{IL}	5.0 10 15	_ _ _	1.5 3.0 4.0	_ _ _	2.25 4.50 6.75	1.5 3.0 4.0	_ _ _	1.5 3.0 4.0	Vdc
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$	'1" Level	V _{IH}	5.0 10 15	3.5 7.0 11	_ _ _	3.5 7.0 11	2.75 5.50 8.25	_ _ _	3.5 7.0 11	_ _ _	Vdc
Output Drive Current $ (V_{OH} = 2.5 \text{ Vdc}) $ $ (V_{OH} = 4.6 \text{ Vdc}) $ $ (V_{OH} = 9.5 \text{ Vdc}) $ $ (V_{OH} = 13.5 \text{ Vdc}) $	Source	I _{OH}	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2	_ _ _ _	- 2.4 - 0.51 - 1.3 - 3.4	- 4.2 - 0.88 - 2.25 - 8.8	_ _ _ _	- 1.7 - 0.36 - 0.9 - 2.4	_ _ _ _	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	Sink	I _{OL}	5.0 10 15	0.64 1.6 4.2	_ _ _	0.51 1.3 3.4	0.88 2.25 8.8	_ _ _	0.36 0.9 2.4	_ _ _	mAdc
Input Current		I _{in}	15	_	± 0.1		±0.00001	± 0.1	_	± 1.0	μAdc
Input Capacitance (V _{in} = 0)		C _{in}	_	_	_	_	5.0	7.5	_	_	pF
Quiescent Current (Per Package)		I _{DD}	5.0 10 15	_ _ _	5.0 10 20	_ _ _	0.005 0.010 0.015	5.0 10 20	_ _ _	150 300 600	μAdc
Total Supply Current ^(5.) ^(6.) (Dynamic plus Quiescen Per Package) (C _L = 50 pF on all output buffers switching)		I _T	5.0 10 15			$I_T = (0$.42 μA/kHz) .85 μA/kHz) .43 μA/kHz)	f + I _{DD}			μAdc

^{4.} Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
5. The formulas given are for the typical characteristics only at 25°C.
6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (7.) ($C_L = 50 \text{ pF}, T_A = 25^{\circ}C$)

Characteristic	Symbol	V _{DD} Vdc	Min	Typ ^(8.)	Max	Unit
Output Rise and Fall Time $T_{TLH}, T_{THL} = (1.5 \text{ ns/pF}) \text{ C}_{L} + 25 \text{ ns}$ $T_{TLH}, T_{THL} = (0.75 \text{ ns/pF}) \text{ C}_{L} + 12.5 \text{ ns}$ $T_{TLH}, T_{THL} = (0.55 \text{ ns/pF}) \text{ C}_{L} + 9.5 \text{ ns}$	t _{TLH} , t _{THL}	5.0 10 15	_ _ _	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q1 $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) \text{ C}_L + 315 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) \text{ C}_L + 137 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) \text{ C}_L + 95 \text{ ns}$	t _{PLH} , t _{PHL}	5.0 10 15	_ _ _	260 115 80	520 230 160	ns
Clock to Q12 t_{PHL} , $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 2415 \text{ ns}$ t_{PHL} , $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 867 \text{ ns}$ t_{PHL} , $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 475 \text{ ns}$		5.0 10 15	_ _ _	1625 720 500	3250 1440 1000	ns
Propagation Delay Time Reset to Q_n $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 485 \text{ ns}$ $t_{PHL} = (0.86 \text{ ns/pF}) C_L + 182 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 145 \text{ ns}$	[†] PHL	5.0 10 15	_ _ _	370 155 115	740 310 230	ns
Clock Pulse Width	t _{WH}	5.0 10 15	385 150 115	140 55 38	_ _ _	ns
Clock Pulse Frequency	f _{cl}	5.0 10 15	_ _ _	2.1 7.0 10.0	1.5 3.5 4.5	MHz
Clock Rise and Fall Time	t _{TLH} , t _{THL}	5.0 10 15		No Limit		ns
Reset Pulse Width	twн	5.0 10 15	960 360 270	320 120 80	_ _ _	ns
Reset Removal Time	t _{rem}	5.0 10 15	130 50 30	65 25 15	_ _ _	ns

- The formulas given are for the typical characteristics only at 25°C.
 Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

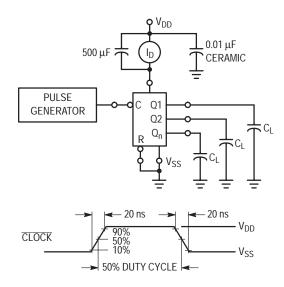


Figure 1. Power Dissipation Test Circuit and Waveform

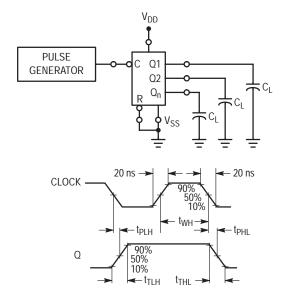


Figure 2. Switching Time Test Circuit and Waveforms

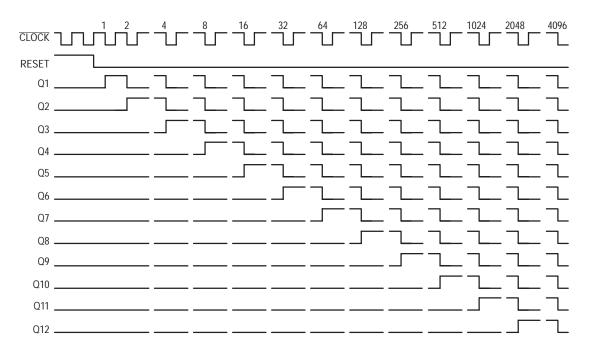


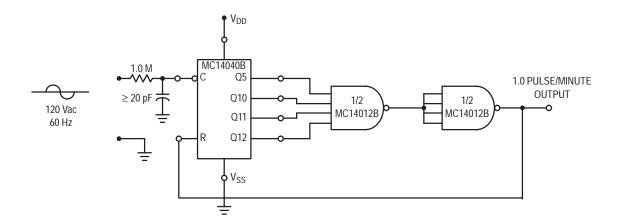
Figure 3. Timing Diagram

APPLICATIONS INFORMATION

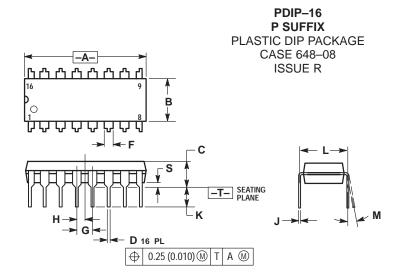
TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040B. By selecting

outputs Q5, Q10, Q11, and Q12 division by 3600 is accomplished. The MC14012B decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



PACKAGE DIMENSIONS



NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: INCH.

 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

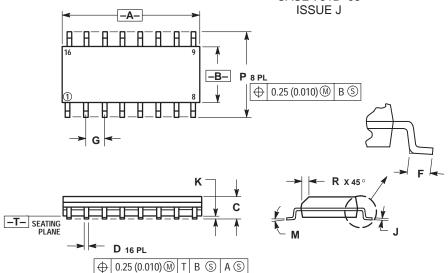
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

 5. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.740	0.770	18.80	19.55
В	0.250	0.270	6.35	6.85
С	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100	BSC	2.54	BSC
Н	0.050	BSC	1.27	BSC
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10 °
S	0.020	0.040	0.51	1.01

SOIC-16 **D SUFFIX**

PLASTIC SOIC PACKAGE CASE 751B-05



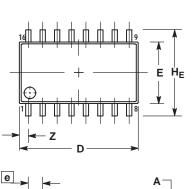
- NOTES:
 1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2 CONTROLLING DIMENSION: MILLIMETER.
 3 DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4 MAXIMUM MOLD PROTRUSION 0.15 (0.006)

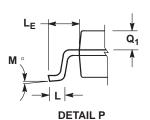
- PER SIDE.
 DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

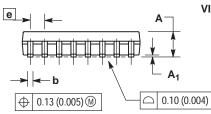
	MILLIN	METERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	9.80	10.00	0.386	0.393
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
Р	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

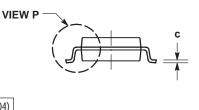
PACKAGE DIMENSIONS

SOEIAJ-16 **F SUFFIX** PLASTIC EIAJ SOIC PACKAGE CASE 966-01 **ISSUE O**









NOTES:

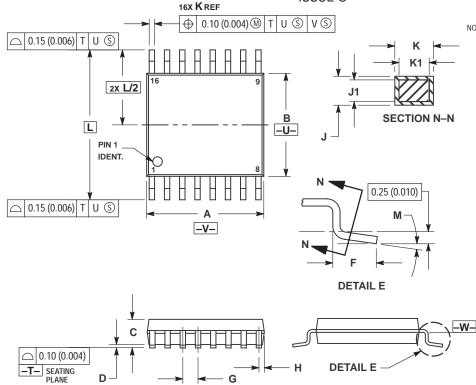
- DIMENSIONING AND TOLERANCING PER ANSI
- DIMENSIONING AND TOLERANGING PER AND Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (2014) DED SIDE.
- OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIN	METERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
С	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
е	1.27 BSC		0.050	BSC
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q ₁	0.70	0.90	0.028	0.035
Z		0.78		0.031

PACKAGE DIMENSIONS

TSSOP-16 DT SUFFIX

PLASTIC TSSOP PACKAGE CASE 948F-01 ISSUE O



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: MILLIMETER
- DIMENSION A DOES NOT INCLUDE MOLD
 FLASH. PROTRUSIONS OR GATE BURRS. MOLD
 FLASH OR GATE BURRS SHALL NOT EXCEED 0.15
 (0.006) PER SIDE.

 4. DIMENSION B DOES NOT INCLUDE INTERLEAD
- 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED

 0.25 (0.010) PER SIDE.

 5. DIMENSION K DOES NOT INCLUDE DAMBAR
- 5. DIMENSION & DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED
 AT DATUM PLANE -W-.

MILLIN	IETERS	INC	HES				
MIN	MAX	MIN	MAX				
4.90	5.10	0.193	0.200				
4.30	4.50	0.169	0.177				
	1.20		0.047				
0.05	0.15	0.002	0.006				
0.50	0.75	0.020	0.030				
0.65	0.65 BSC 0		BSC				
0.18	0.28	0.007	0.011				
0.09	0.20	0.004	0.008				
0.09	0.16	0.004	0.006				
0.19	0.30	0.007	0.012				
0.19	0.25	0.007	0.010				
6.40 BSC		0.252	BSC				
0°	8°	0°	8°				
	MIN 4.90 4.30 0.05 0.50 0.65 0.18 0.09 0.09 0.19 0.19 6.40	4.90 5.10 4.30 4.50 1.20 0.05 0.15 0.50 0.75 0.65 BSC 0.18 0.28 0.09 0.20 0.09 0.16 0.19 0.30 0.19 0.25 6.40 BSC	MIN MAX MIN 4.90 5.10 0.193 4.30 4.50 0.169 1.20 0.05 0.15 0.002 0.50 0.75 0.020 0.18 0.28 0.007 0.09 0.20 0.004 0.09 0.16 0.004 0.19 0.30 0.007 0.19 0.25 0.007 6.40 BSC 0.252				

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