CD4008BMS

CMOS 4-Bit Full Adder With Parallel Carry Out

November 1994

Features

- **High-Voltage Type (20V Rating)**
- **4 Sum Outputs Plus Parallel Look-ahead Carry-Output**
- **High-Speed Operation - Sum In-To-Sum Out, 160ns Typ; Carry In-To-Carry Out, 5ns Typ. At VDD = 10V, CL=50pF**
- **Standardized Symmetrical Output Characteristics**
- **100% Tested For Quiescent Current At 20V**
- **Maximum Input Current of 1 a at 18V Over Full Package-Temperature Range;**
  - **100nA at 18V and 25°C**
- **Noise Margin (Over Full Package Temperature Range):**
  - **1V at VDD = 5V**
  - **2V at VDD = 10V**
  - **2.5V at VDD = 15V**
- **5V, 10V and 15V Parametric Ratings**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications

- **Binary Addition/Arithmetic Units**

Description

CD4008BMS types consist of four full adder stages with fast look ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" but to permit high-speed operation in arithmetic sections using several CD4008BMS's.

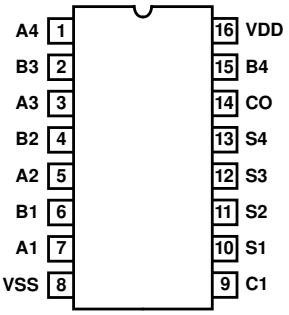
CD4008BMS inputs include the four sets of bits to be added, A1 to A4 and B1 to B4, in addition to the "Carry In" bit from a previous section. CD4008BMS outputs include the four sum bits, S1 to S4. In addition to the high speed "parallel-carry-out" which may be utilized at a succeeding CD4008BMS section.

The CD4008BMS is supplied in these 16-lead outline packages:

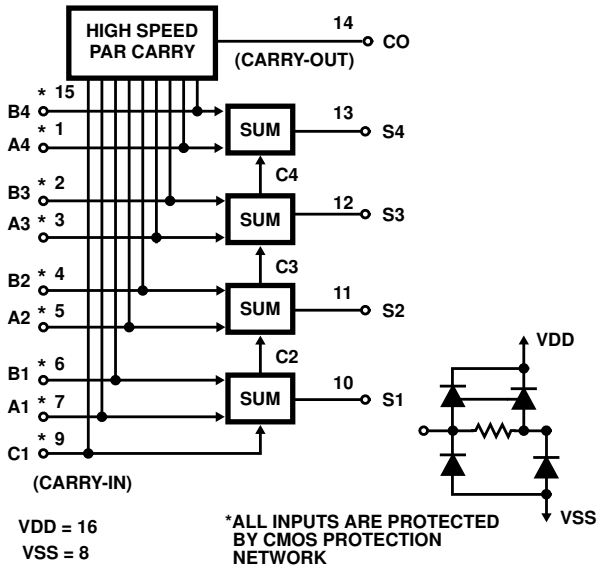
Braze Seal DIP	H4T
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout

CD4008BMS
TOP VIEW



Logic Diagram



TRUTH TABLE

A_i	B_i	C_i	C_O	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

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