FAIRCHILD SEMICONDUCTOR™

October 1987
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CD4514BC• CD4515BC
4-Bit Latched/4-to-16 Line Decoders

General Description

The CD4514BC and CD4515BC are 4-to-16 line decoders with latched inputs implemented with complementary MOS (CMOS) circuits constructed with N- and P-channel enhancement mode transistors. These circuits are primarily used in decoding applications where low power dissipation and/or high noise immunity is required.

The CD4514BC (output active high option) presents a logical "1" at the selected output, whereas the CD4515BC presents a logical "0" at the selected output. The input latches are R–S type flip-flops, which hold the last input data presented prior to the strobe transition from "1" to "0". This input data is decoded and the corresponding output is activated. An output inhibit line is also available.

Features

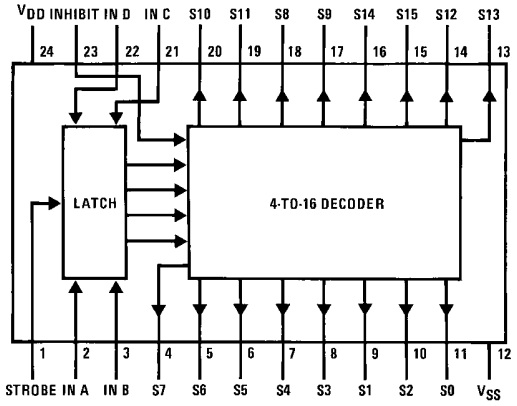
- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL: fan out of 2
  compatibility: driving 74L
- Low quiescent power dissipation:
  0.025 W/package @ 5.0 V_{DC}
- Single supply operation
- Input impedance = $10^{12}\Omega$ typically
- Plug-in replacement for MC14514, MC14515

Ordering Code:

Order Number	Package Number	Package Diagram
CD4514BCWM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
CD4514BCN	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.600 Wide
CD4515BCWM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
CD4515BCN	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.600 Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Top View

Truth Table

Decode Truth Table (Strobe = 1)

Inhibit	Data Inputs				Selected Output CD4514 = Logic "1" CD4515 = Logic "0"
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514 All Outputs = 1, CD4515

X = Don't Care

Logic Diagram