Page lookup

Process is executing on the CPU, and it issues a read to an address
The read goes to the TLB in the MMU

1. TLB does a lookup using the page number of the address
2. Common case is that the page number matches, returning a page table entry (PTE) for the mapping for this address
3. TLB validates that the PTE protection allows reads (in this example)
4. PTE specifies which physical frame holds the page
5. MMU combines the physical frame and offset into a physical address
6. MMU then reads from that physical address, returns value to CPU

➡ This is all done by the hardware

TLB misses

- TLB does not have a PTE mapping this virtual address
- or PTE in TLB, but memory access violates PTE protection bits