Verilog assignment report

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1 Introduction

The assignment requires to implement a Verilog module that can multiply two matrices together.

For semplicity sake, the two matrices are a fixed 2x2 and they coontain 16 bits numbers, where the 8 most significant bits are used to represent the integer part and the remaining 8 are used for the decimal part.

2 Verilog

Instead of creating a single, big Verilog module, two modules were created, one that implements the multiplication of two numbers, and another called ‘matrixMultiplication.v‘ that actually does the matrix multiplication. This was done to ease development.

For the same reason, the control and datapath FSM in each module have been separated.

3 FSMs

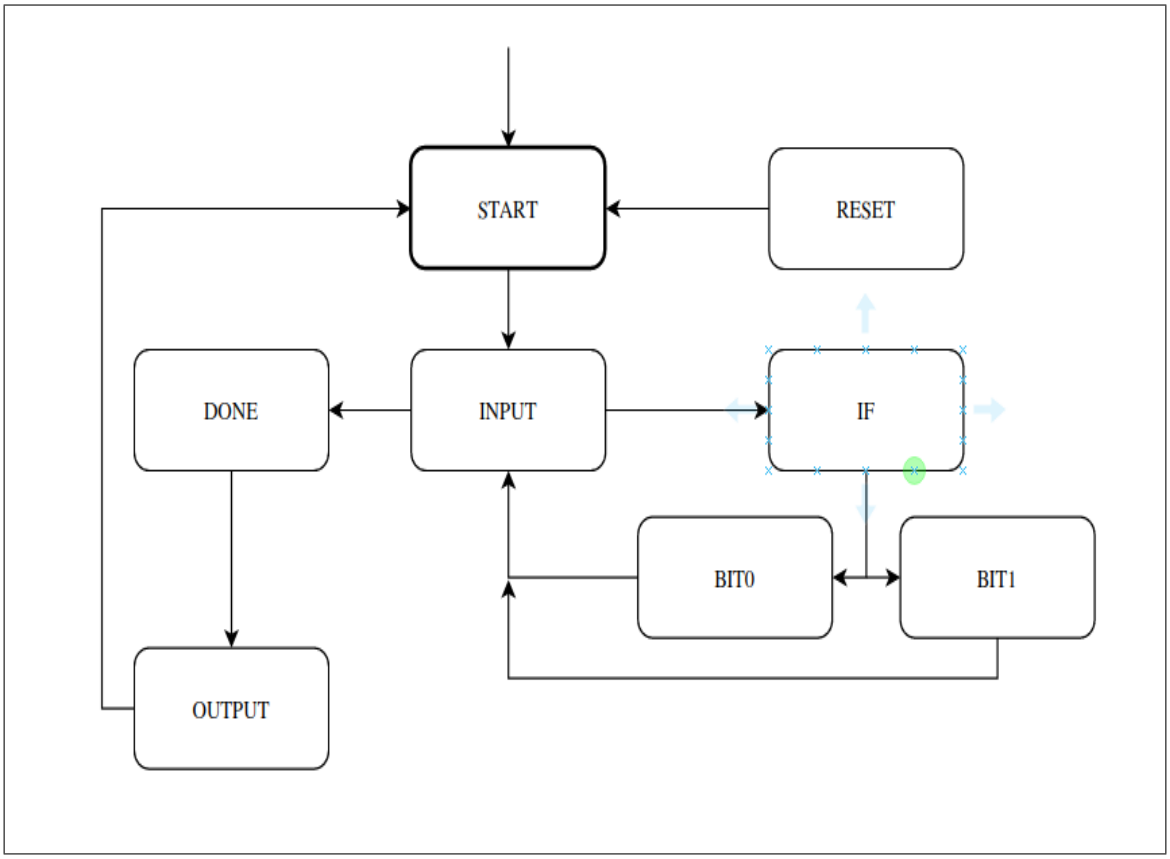

Figure 1: FSM for the binary multiplier module

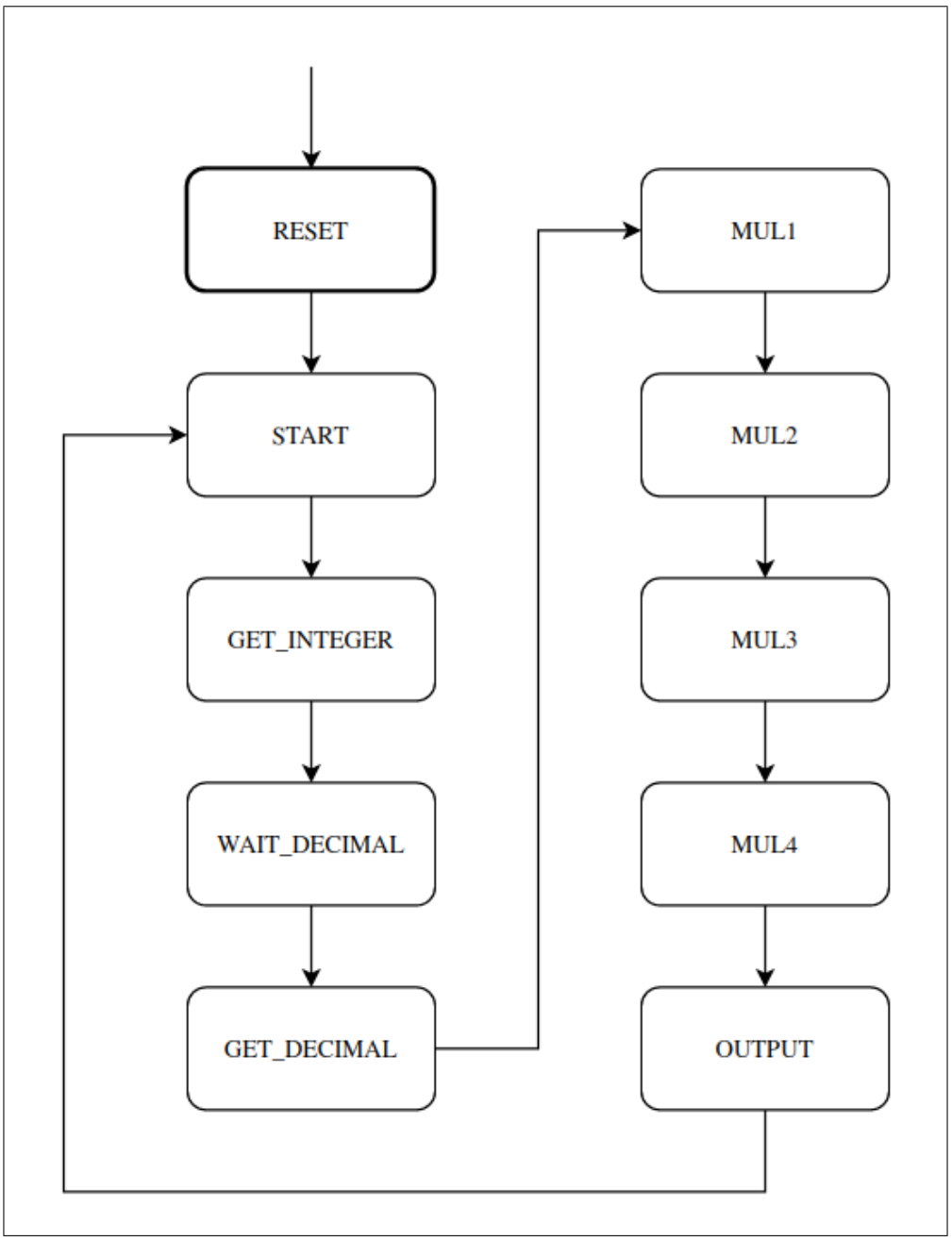

Figure 2: FSM for the matrix multiplier module

Please refer to the code for both EFSM's, they were not included for size issues.

4 FPGA Synthesis

The Verilog module, once synthesized on the FPGA gives the following result: