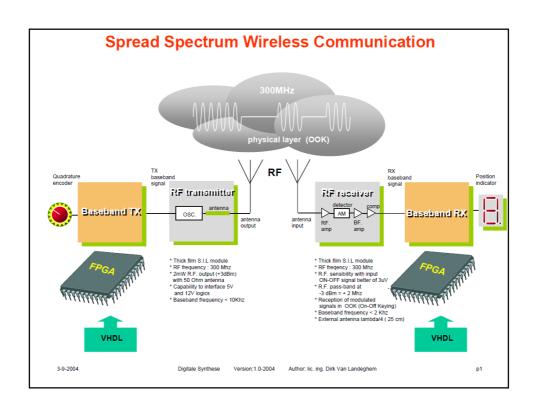
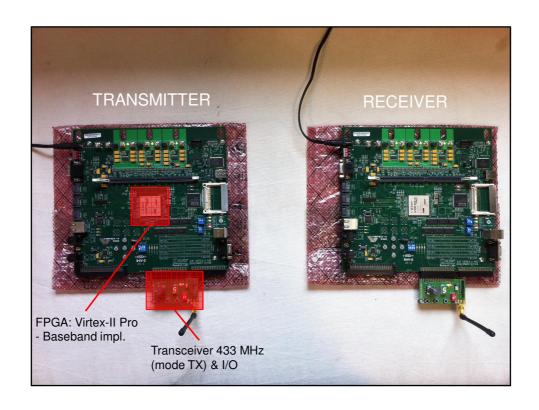


Lab Digital Synthesis

- 9 lab sessions, 1.5 hours
- · Permanent evaluation, last lab session evaluation
- What?
 - Digital Electronics: VHDL → FPGA
 - Wireless transmit-receive system
 - Direct Sequence Spread Spectrum (DSSS) technology



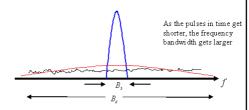


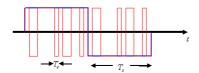
Assignment

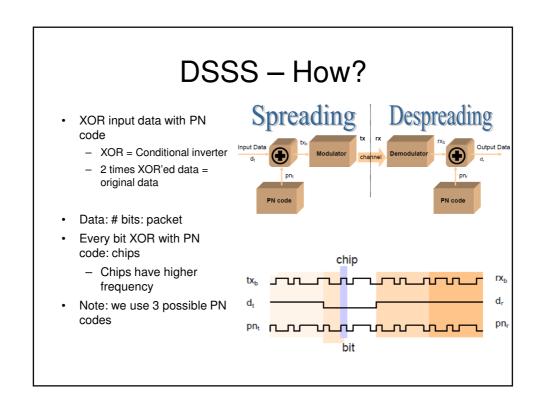
- · Prepare demo!
 - Send 4 bit binary word using DSSS technology
 - Input on TX with up/down pushbutton (or rotary encoder), readout on 7-seg
 - Output on RX using 7-seg
- · DSSS: Direct Sequence Spread Spectrum
 - Originally developed for military purposes
 - GPS systems
 - GSM

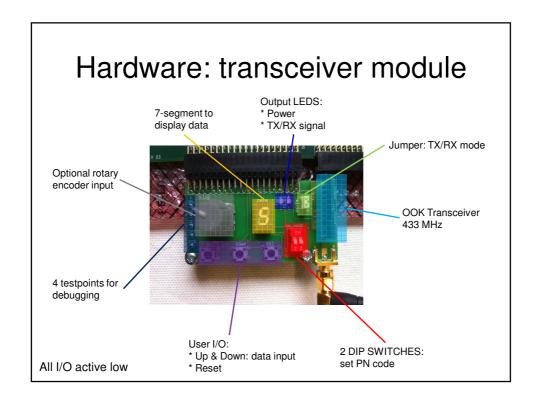
DSSS - What?

- Traditional RF: send on 1 frequency
 - disadvantages:
 - Easily traceable
 - Jamming
- DSSS = spread frequency spectrum
 - · More difficult to trace
 - · Jamming difficult
 - More users per channel (different PN code)
 - · Possibly under noise floor









Workflow

- Write VHDL code
 Simulation of VHDL code

 Modelsim
- Synthesize VHDL code \(\rightarrow \text{Xilinx ISE} \)
- Bit-file download

 Xilinx Impact

Attention!

- · Make use of two process method
 - See PDF (fsm.pdf): http://telescript.denayer.wenk.be/~kvb/Labo_Digitale_Synthese/
- · Work modular: testbench for each block
- Add comments (will be quoted)!
- Take backups (own responsibility)
- Simulations run from USB stick are slower
- Walkthrough with counter (telescript)

