Fwd: verilog 8 bit adder code

1 message

Moorthi K <moorthi.ece@sairam.edu.in> Mon, 19 Aug, 2024 at 1:38 pm
To: sec22ec142@sairamtap.edu.in <sec22ec142@sairamtap.edu.in>

---------- Forwarded message ---------
From: **Srinivasan K** <srinivasan.ece@sairam.edu.in>
Date: Sat, Aug 17, 2024, 14:33
Subject: Fwd: verilog 8 bit adder code
To: Moorthi K <moorthi.ece@sairam.edu.in>

---------- Forwarded message ---------
From: **Srinivasan K** <srinivasan.ece@sairam.edu.in>
Date: Fri, Aug 16, 2024 at 2:28 PM
Subject: verilog 8 bit adder code
To: sec22ec081@sairamtap.edu.in <sec22ec081@sairamtap.edu.in>

8 BIT RIPPLE CARRY ADDER

```
module ripplemod(a, b, cin, sum, cout);

input [07:0] a;

input [07:0] b;

input cin;

output [7:0]sum;

output cout;

wire[6:0] c;

fulladd a1(a[0],b[0],cin,sum[0],c[0]);

fulladd a2(a[1],b[1],c[0],sum[1],c[1]);

fulladd a3(a[2],b[2],c[1],sum[2],c[2]);

fulladd a4(a[3],b[3],c[2],sum[3],c[3]);

fulladd a5(a[4],b[4],c[3],sum[4],c[4]);

fulladd a6(a[5],b[5],c[4],sum[5],c[5]);

fulladd a7(a[6],b[6],c[5],sum[6],c[6]);

fulladd a8(a[7],b[7],c[6],sum[7],cout);

endmodule
```

```
module fulladd(a, b, cin, sum, cout);

input a;

input b;

input cin;

output sum;

output cout;

assign sum=(a^b^cin);

assign cout=((a&b)|(b&cin)|(a&cin));

endmodule
```

TEST BENCH

```
module rippleadder_b;

reg [7:0] a;

reg [7:0] b;

reg cin;

wire [7:0] sum;

wire cout;

ripplemod uut (.a(a),.b(b),.cin(cin),.sum(sum),.cout(cout) );

initial begin

#10 a=8'b00000001;b=8'b00000001;cin=1'b0;

#10 a=8'b00000001;b=8'b00000001;cin=1'b1;

#10 a=8'b00000010;b=8'b00000011;cin=1'b0;

#10 a=8'b10000001;b=8'b10000001;cin=1'b0;

#10 a=8'b00011001;b=8'b00110001;cin=1'b0;

#10 a=8'b00000011;b=8'b00000011;cin=1'b1;
```

#10 a=8'b11111111;b=8'b00000001;cin=1'b0;

#10 a=8'b11111111;b=8'b00000000;cin=1'b1;

#10 a=8'b11111111;b=8'b11111111;cin=1'b0;

#10 $stop;

end

endmodule

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