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सत्यमेव जयते
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सं.संख्या/Ref.No /आवेदन संख्या/Application No/ 202341006829 दिनांक/Date of Dispatch/Email: 15-01-2025

सेवा मे,/To
Pranav Bhat,
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विषय: एकस्व अधिनियम, 1970 की धारा 12 व 13 तथा एकस्व नियम, 2003 के अधीन परीक्षण रिपोर्ट
Subject: Examination report under sections 12 & 13 of the Patents Act, 1970 and the Patents Rules, 2003.

1. उपर्युक्त आवेदन के संदर्भ मे परीक्षण रिपोर्ट (अर्थात, एकस्व नियम, 2003 (यथा संशोधित) के नियम 24-ख(3) में विनिर्दिष्ट आपत्तियों का प्रथम कथन) इसके साथ संलग्न है। यह रिपोर्ट परीक्षण हेतु अनुरोध दिनांक 01-07-2024 के उत्तर मे जारी की गयी है। परीक्षण रिपोर्ट का उत्तर दाखिल करने की अंतिम तिथि (अर्थात, इस रिपोर्ट में लगाई गयी सभी आवश्यकताओं के अनुपालन की अवधि) आवेदक को आपत्तियों का प्रथम कथन जारी होने की तिथि से छः माह है।
   Please find enclosed herewith an Examination Report (i.e. a first statement of objections as specified in Rule 24-B(3) of The Patents Rules, 2003 (as amended)) in respect of above-mentioned application. This report is issued with reference to a request for examination dated 01-07-2024.The last date for filing a response to the Examination Report (i.e. a period to comply with all the requirements raised in this examination report) is six months from the date on which the first statement of objections is issued to the Applicant.

2. यदि रिपोर्ट के अंतर्गत लगाई गयी आवश्यकताओं का अनुपालन एकस्व नियम, 2003 (यथा संशोधित) के नियम 24 ख(5) में विनिर्दिष्ट अवधि के भीतर अंदर अनुपालन नहीं किया गया तो एकस्व अधिनियम 1970 की धारा 21(1) के अधीन वर्तमान आवेदन को परित्यक्त माना जाएगा।
   The instant application shall be deemed to have been abandoned under Section 21(1) of The Patents Act, 1970, unless all the requirements raised in this report are complied with in the period as specified in Rule 24-B (5) of The Patents Rules, 2003 (as amended).

3. आपका ध्यान एकस्व नियम, 2003 के नियम 24 ख(6) के प्रावधानों की ओर भी आमंत्रित किया जाता है।
   Your attention is also invited to the provisions of Rule 24-B (6) of the Patents Rules 2003.

4. आपको सलाह दी जाती है कि शीघ्र निपटान हेतु अपना उत्तर शीघ्र प्रस्तुत करें।
   You are advised to file the reply at the earliest for early disposal.

Ajay Kumar Yadav
नियंत्रक पेटेंट/ Controller of Patents

संलग्न/Enclosed: अपरोक्त अनुसार/As above

टिप्पणी: यह इलेक्ट्रोनिक रूप से उत्पन्न रिपोर्ट है।
NOTE: This is an electronically generated report.

सभी पत्राचार नियंत्रक एकस्व को उपरोल्लिखित पते पर भेजा जाये।
All communications should be sent to the Controller of Patents at the above mentioned address.

THE PATENT OFFICE

परीक्षण रिपोर्ट /Examination Report

आवेदन संख्या /Application Number	202341006829
दाखिल करने की तिथि /Date of Filing	02-08-2023
पूर्विक्ता दिनांक /Date of Priority	--
पीसीटी अंतर्राष्ट्रीय आवेदन की संख्या व दिनांक / PCT International Application No. & Date	--
आवेदक /Applicant	Lightspeed photonics Pvt. Ltd.
परीक्षण हेतु अनुरोध की संख्या व दिनांक /Request for Examination No. & Date	E2024403767001-07-2024
प्रकाशन की तिथि /Date of Publication	05-07-2024

इस परीक्षण रिपोर्ट के चार भाग हैं, अर्थात रिपोर्ट का सारांश, विस्तृत तकनीकी रिपोर्ट, औपचारिक आवश्यकताएँ तथा रिकॉर्ड मे दस्तावेज़ /
This examination report consists of four parts, namely summary of the report, detailed technical report, formal requirements and documents on record.

भाग -1: रिपोर्ट का सारांश
PART-I: SUMMARY OF THE REPORT

क्र. सं. /Sl. No.	अधिनियम के तहत आवश्यकताओं पर विस्तृत टिप्पणियां /Requirements under the Act		दावों की संख्या /Claim Numbers	टिप्पणी /Remarks
1.	धारा 2(1)(ज) के तहत आविष्कार /Invention u/s 2(1)(j)	नवीनता /Novelty	दावे /Claims: 1-10	हाँ /Yes
			दावे /Claims:	नहीं /No
		आविष्कारी कदम / Inventive step	दावे /Claims:	हाँ /Yes
			दावे /Claims: 1-10	नहीं /No
		औद्योगिक उपयोगिता /Industrial Applicability	दावे /Claims: 1-10	हाँ /Yes
			दावे /Claims:	नहीं /No
2.	धारा 3 के अधीन पेटेंट-अयोग्यता (यदि हाँ, खंड 3(क-त) /Non-patentability u/s 3 (if yes, specify section3(a-p))		दावे /Claims: 1-10	हाँ /Yes 3(f), 3(o)
			दावे /Claims:	नहीं /No
3.	[धारा 10(5) व 10(4) (ग)] के अधीन दावे /Claims [u/s 10(5) & 10(4) (c)]	स्पष्टता/ संक्षिप्तता /Clarity / Conciseness	दावे /Claims:	हाँ /Yes
			दावे /Claims: 1-10	नहीं /No
		परिभाषिकता /Definitive	दावे /Claims:	हाँ /Yes
			दावे /Claims: 1-10	नहीं /No

भाग –II विस्तृत तकनीकी रिपोर्ट
PART-II: DETAILED TECHNICAL REPORT

क. उद्धरित दस्तावेजों की सूची /A.List of documents cited:

(क) पेटेंट साहित्य / (a). Patent Literature :

क्र. सं. / Sl.no	दस्तावेज़ों का विवरण /Details of documents	प्रकाशन तिथि(दिन/माह/वर्ष) / Publication date	उद्धरित दस्तावेज़ का प्रासंगिक विवरण (पृष्ठ व अनुच्छेद संख्या) / Relevant description (page and paragraph no.) of cited document	उद्धरित दस्तावेज़ के प्रासंगिक दावे / Relevant claims of cited document	अभिकथित आविष्कार के दावे /Claims of alleged invention
1	D1: US6690845B1	10/02/2004	whole document		1-10

2	D2: US20230176304A1	08/06/2023	whole document		1-10

(ख) गैर-पेटेंट साहित्य /(b).Non-patent literature

कोई दस्तावेज़ उद्धृत नहीं है /No Document Cited

ख. अधिनियम के तहत आवश्यकताओं पर विस्तृत टिप्पणियां /B. Detailed observations on the requirements under the Act:

(1).आविष्कारी कदम / INVENTIVE STEP:

(I) ऊपर उद्धरित दस्तावेज़(जों) के संदर्भ मे स्पष्ट अध्यापन(नों) को ध्यान मे रखते हुए, निम्नलिखित कारणों से दावा(वों) (1-10) मे आविष्कारी कदम की कमी है
Claim(s) (1-10) lack(s) inventive step, being obvious in view of teaching (s) of cited document(s) above under reference for the following reasons:

D1: US6690845B1 Pub Date: 10/02/2004

D2: US20230176304A1 Pub Date: 08/06/2023

The subject matter of claims 1-10 does not involve an inventive step given the disclosures of D1 and D2, having regards to common general knowledge in the art:

Independent claim 1:

D1 discloses (the references in parentheses applying to this document) a 3 layer opto-electronic engine (See claim 1: “opto-electronic module”), comprising:

a first layer (See abstract: “Three-dimensional opto-electronic modules having a plurality of opto-electronic (O/E) layers”) that includes: a plurality of processors (See IC Chips in fig. _1; See column 39, lines 36-40: “chips (including driver/amplifier chips and or processor/ memory chips) and OE-devices (such as VCSEL, photodetectors, and others) can co-exist in the same layer in FIGS. 33-37 and 110 and 111”), and a plurality of optoelectronic connectors (See fig._1: connectors ‘2’);

a second layer that is connected to the first layer (See abstract: “Three-dimensional opto-electronic modules having a plurality of opto-electronic (O/E) layers”; See fig._111) ,

wherein the second layer includes: a first surface that faces the first layer, and a second surface that is opposite to the first surface the first surface includes: a plurality of first memories, and a plurality of first electronic components, and the second surface includes: a plurality of second memories that is different from the plurality of first memories, and a plurality of second electronic components that is different from the plurality of first electronic components (See column 39, lines 32-38: “The driver/amplifier chip described above may comprise circuits Such as driver circuits, amplifier circuits, bias circuits, temperature Stabi lizing circuits, (clock) skew compensation circuits, timing circuits, and other applicable circuits. It is also possible that chips (including driver/amplifier chips and or processor/ memory chips)”); and

a third layer connected to at least one of the first layer or the second layer (See abstract: “Three-dimensional opto-electronic modules having a plurality of opto-electronic (O/E) layers”; See fig._111),

wherein the third layer includes: a first surface that faces the second layer, and a second surface that is opposite to the first face of the third layer, the first surface of the third layer includes a plurality of third electronic components that is different from the plurality of first electronic components and the plurality of second electronic components, and the second surface of the third layer includes a plurality of fourth electronic components that is different from the plurality of first electronic components, the plurality of second electronic components, and the plurality of third electronic components (See column 39, lines 32-38: “The driver/amplifier chip described above

may comprise circuits Such as driver circuits, amplifier circuits, bias circuits, temperature Stabi lizing circuits, (clock) skew compensation circuits, timing circuits, and other applicable circuits. It is also possible that chips (including driver/amplifier chips and or processor/ memory chips)");

the first layer, the second layer, and the third layer are vertically stacked using an optimized pin configuration (See fig._111).

D1 does not disclose the following features of claim 1:

"the plurality of optoelectronic connectors are arranged to surround the plurality of processors, wherein the plurality of optoelectronic connectors and the plurality of processors are coupled using a set of connections such that route length between the plurality of processors is optimal in an intra- 3 layer opto-electronic engine communication and inter-3 layer opto-electronic engine communication is optimal and loss less to maintain signal integrity".

However coupling of processors with optoelectronic connectors is well known design option for a person skilled in the art. Same can be inferred from D2. See abstract of D2: "A system includes a substrate on which a data processor and a connector block are mounted. The connector block has a first array of electrical connectors on a first surface, and a second array of electrical conducts on a second surface that is oriented at an angle between 45° to 135° relative to a main surface of the substrate. At least a portion of the first array of electrical connectors are electrically coupled to the data processor, and the second array of electrical contacts are electrically connected to the electrical contacts of a pluggable module."

Therefore, starting only from the teachings of D1, it would be obvious to a person skilled in the art to combine the teachings of D2 with D1 to arrive at the subject matter of the independent Claim 1. Hence, the said claim lacks inventive step.

Dependent claims 2-10 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of inventive step in view of the disclosures of D1 and D2, having regards to common general knowledge in the art.

(2).पेटेंट अयोग्यता /NON PATENTABILITY:

(I) निम्नलिखित कारणों से धारा 3 के खंड (3(f), 3(o))के प्रावधान के तहत दावा(वे) (1-10) सांविधिक रूप से पेटेंट योग्य नहीं हैं / Claim(s) (1-10) are statutorily non-patentable under the provision of clause (3(f), 3(o)) of Section 3 for the following reasons:

Claimed invention, which describes a 3-layer opto-electronic engine comprising a plurality of processors, memories, optoelectronic connectors and different electronic components arranged in vertically stacked layers with an "optimized pin configuration", appears to fall under section 3(f) of the Patents Act, 1970. The invention described an arrangement of known components i.e. processors, memories, optoelectronic connectors, electronic components. Moreover the concept of vertically stacking layers with specific components is well-known in the field of electronics and optoelectronics. Claims includes an "optimized pin configuration" and also "optimal" & "lossless" communication, however it is not clear what makes the pin configuration "optimized" and what is making "optimal" and "lossless" communication.

Further it appears that no inherent coupling/interaction among the components is clear from the statement of the Claim. Different electronic components are merely placed on three vertically stacked layers that are functioning independently of one-another with no combinational function of them comes out clearly from the statement of the Claim. Such disclosure of sub-systems is a mere-arrangement or re-arrangement and thus is not allowable u/s 3(f) of the Patent Act 1970, as amended.

- The subject matter of the claimed invention in claims 1- 10 relates to the topography of integrated circuits (i.e first layer further includes a plurality of trapezium shaped interposers...../... third layer corresponds to a hexagonal shape.). Hence the subject matter of the claims are not allowable under section 3(o) of the Patents Act.

(3).प्रकटन की दक्षता /SUFFICIENCY OF DISCLOSURE:

(I) सार /Abstract:

Necessary figure and the reference numerals aren't indicated in the abstract. The 'abstract' should be prepared in accordance with the instructions contained in Rule 13{7} of the Patent Rules, 2003(as amended).

(4).स्पष्टता एवं संक्षिप्तता /CLARITY AND CONCISENESS:

(I) दावा(वे) 1-10 के संबंध मे स्पष्ट रूप से परीभाषित नहीं हैं.
Claim(s) 1-10 are not clearly worded in respect of:

1. Reference numerals in the claims shall be placed in parenthesis.

2. Claim 1 states “the plurality of optoelectronic connectors (111,113,115,117,119,121) and the plurality of processors 104 are coupled using a set of connections 102 such that route length between the plurality of processors 104 is optimal in an intra- 3 layer opto-electronic engine 100 communication and inter-3 layer opto-electronic engine 100 communication is optimal and loss less to maintain signal integrity”. However, the claim merely states the objectives of "optimal" and "lossless" communication without specifying the means or methodology by which these objectives are achieved. Specifically, the claim lacks any description of the steps, processes, or mechanisms that ensure the optimization of routing paths, as well as the maintenance of signal integrity and lossless transmission. Redraft claim 1 accordingly.

3. Claim 1 states “the first layer 101, the second layer 103, and the third layer 105 are vertically stacked using an optimized pin configuration”. The claim does not provide sufficient detail on what constitutes an "optimized pin configuration" or how the stacking is optimized, making it unclear and broad. Claim shall be drafted in such a way that it should define what makes the pin configuration “optimized”.

(5).परिभाषिकता /DEFINITIVENESS:

(I) दावा(वे)1-10 निम्नलिखित कारणों से आविष्कार को पर्याप्त रूप से परीभाषित नहीं करता(ते) हैं
Claim(s) 1-10 do not sufficiently define the invention for the reasons as follows:

- In the absence of characterizing novel/ inventive features in principal claim, the subject matter of claim does not seem to be clear u/s 10(5), and also scope is not defined u/s 10(4c) of The Patent Act. Hence comply with this requirement but within the well-defined boundary and scope of the specification disclosed.
- Principal claim should be such that it discloses fully and clearly the solution to the problem associated with the invention (as per section 10 of the act).
- The phrase " includes/ further comprising” mentioned in the claim 7 is vague, hence should be amended.
- The phrase "of claim" mentioned in the claims are not clear and definitive; it should be replaced with “as claimed in” in the claim.

(6).अन्य आवश्यकताएँ /OTHERS REQUIREMENTS:

(I)

1. In case applicant wishes to amend claims, indicate the reasons /technical significance thereof over the cited

documents in your reply. Also please provide an additional copy of marked up amendments (highlighting the amendments) wherever applicable.

2. The independent claims should be cast in the two- part form where appropriate, with those features known in combination from the prior art being placed in the preamble and the remaining features being included in the characterizing part.

भाग – III: औपचारिक आवश्यकताएँ /PART-III: FORMAL REQUIREMENTS

आपत्तियां /Objections	टिप्पणी /Remarks
Form 13	• In the Form 13 of dated 17.07.2024, the date of filing of instant application number is not correctly mentioned, Applicant is required to submit the again correctly.
Power of Attorney (Whether GPA, SPA, Stamped, requisite fee etc.)	• Stamp duty should be paid in respect of Power of Attorney for the instant application. • The signature in Power of Attorney i.e. 'Y. Rohin Kumar', is appears to be same as of inventor 'Rohin Kumar Yeluripati' as mentioned in Form 1. Kindly clear the anomaly. Applicant is required to produce 'Authorised certificate' in respect of the signatory of power of attorney. • Further, in Power of attorney, it is not mentioned under what capacity the signatory signed the same. • Applicant name should be mentioned alongwith the name and designation of signatory in the Power of Attorney.
Format of Specification (rule 13)	• Claims should be prefaced with the words "We Claim". Also the claims must be signed by the applicant/authorized patent agent.
Format of Drawings	• In drawings of dated 02.06.2024, the name of applicant is 'Lightspeed photonics Pte Ltd.' Which is different from the name of applicant of instant application. Further, on the page number 12 and 13, the PAGE NO.: 11 is mentioned. Applicant attention is drawn to section 78(2) of the Patents Act. • In drawings sheet the 'TOTAL NO. OF PAGES: 14' is mentioned, but there are only 13 pages of drawings. Kindly clear the anomaly.
Other Deficiencies	• While filing the instant application, in Form 1 of dated 02.08.2023 (post-dated), under the serial number 3B.i.e. CATEGORY OF APPLICANT, applicant exercise the same by selecting 'Others'. which is an anomaly. Applicant attention is drawn to section 78(2) of the Patents Act. • In Form 2 of dated 02.08.2023(post-dated) it is mentioned "The following specification particularly describes the invention and the manner in which it is performed." which is not correct format of Form 2 for provisional specification. Applicant attention is drawn to section 78(2) of the Patents Act. • In Form 2 of dated 02.06.2024 it is mentioned "The following specification particularly describes the invention and the way its performed." which is not correct format of Form 2 for Complete specification. Applicant attention is drawn to section 78(2) of the Patents Act. • Applicant changes the title of the instant application From "MULTIPLE LAYER ARCHITECTURE OF 3D SYSTEM IN PACKAGE" to "ASSEMBLY OF A 3 LAYER OPTO-ELECTRONIC ENGINE". Kindly clear the anomaly. Applicant attention drawn towards section 57 i.e. Form 13 for the change of title or section

Other Deficiencies	78(2) for the correction of clerical error. • Applicant fails to comply rule 13(6) of the Patent Rules, 2003(as amended in 2006). • Form 5 of dated 02.08.2023(post-dated) was not signed by the Applicant. • While filing the complete specification, the pages of description, abstract, claims and Form 2 is 35 and in the drawings sheet it mentioned 'TOTAL NO. OF PAGES: 14'. Therefore, the pages of complete specification are 49. In view of this Applicant fails to submit the fees of balance one page of complete specification. • Applicant is required to submit Form 28 (in prescribed format) alongwith supporting document for the same. • With respect to addition of name of inventors, Applicant is required to submit the supporting document for the same. Further, the No objection certificate from each inventor is required to be submit.

भाग-IV: रिकॉर्ड मे दस्तावेज़ /PART-IV: DOCUMENTS ON RECORD

निम्नलिखित दस्तावेज़ों के आधार पर यह परीक्षण रिपोर्ट तैयार की गयी है
The examination report has been prepared based on the following documents:

कार्यसूची तिथि / Docket Date	कार्यसूची संख्या /Docket Number	प्रविष्टि संख्या विवरण /Entry Number Description
02 Feb 2023	11469	1-New Application For Patent With Provisional /Complete Specification
02 Feb 2023	11469	FORM 28
01 Feb 2024	15834	6-Application For Post Dating
01 May 2024	62350	6-Application For Post Dating
02 Jun 2024	75655	2-Complete After Provisional Specification - Form 2 Check For No. OF Pages & Claims
01 Jul 2024	87918	12-Request For Early Publication - Form 9
01 Jul 2024	87961	CONVERSION OF REQUEST FOR EXAMINATION FILED UNDER RULE 24 B FOR EXPEDITED EXAMINATION FORM 18A
12 Jul 2024	92613	11-Mention Of Inventor As Such In A Patent - Form 8
17 Jul 2024	94288	18(i)-Amendment Of Application Before Grant - Form 13

परीक्षक का नाम /Name of the Examiner: AMIT KUMAR GUPTA

परीक्षक स्थान /Examiner Location: Chennai

नियंत्रक का नाम /Name of the Controller: Ajay Kumar Yadav

Controller's Email: ajaykumaryadav.ipo@gov.in

नियंत्रक स्थान /Controller Location: Delhi

टिप्पणी: परीक्षण रिपोर्ट का उत्तर दाखिल करने की अंतिम तिथि / Note: Last date for filing response to the Examination Report: 15-07-2025