14th July 2025

To,
THE PATENT OFFICE
I.P.O BUILDING
G.S.T.Road, Guindy
Chennai- 600032

Kind Attention: Ajay Kumar Yavdav, Controller of Patents

Re: Response to FER is dated on January 15th, 2025, with respect to Patent Application **No: 202341006829** filed on **02/08/2023**

Applicant(s): Lightspeed photonics Pvt. Ltd.
Title: "MULTIPLE LAYER ARCHITECTURE OF 3D SYSTEM IN PACKAGE"

Letter No: Ref.No/Application No /202341006829 Dated: 15/01/2025

Dear Sir,

With reference to your letter No Ref/Application No /202341006829 dated 15/01/2025, our humble submissions in the FER matter are as follows for and on behalf of applicant herein:

AMENDMENTS MADE TO THE CLAIMS ARE AS FOLLOWS

We Claim:

1. A 3 layer System-in-Package enabled opto-electronic engine (100), comprising:

a first layer (101) that includes:

a plurality of processors (104), and

a plurality of optoelectronic connectors (111,113,115,117,119,121) wherein

the plurality of optoelectronic connectors (111,113,115,117,119,121) are arranged to surround the plurality of processors (104) and a set of connections (102),

wherein the plurality of optoelectronic connectors (111,113,115,117,119,121) and the plurality of processors (104) are coupled using the set of connections (102) such that route length between the plurality of processors (104) is optimal in an intra-3 layer System-in-Package enabled opto-electronic engine (100) communication and inter-3 layer System-in-Package enabled opto-electronic engine (100) communication is optimal and loss less to maintain signal integrity and reduce signal degradation;

a second layer (103) that is connected to the first layer (101), wherein

the second layer (103) includes:

a first surface (123) that faces the first layer (101), and

a second surface (125) that is opposite to the first surface (123),

the first surface (123) includes:

a plurality of first memories (709A), and

a plurality of first electronic components (124), and

the second surface (125) includes:

a plurality of second memories (709B) that is different from the plurality of first memories (709A), and

a plurality of second electronic components (126) that is different from the plurality of first electronic components (124); and

a third layer (105) connected to at least one of the first layer (101) or the second layer (103), wherein

the third layer (105) includes:

a first surface (127) that faces the second layer (103), and

a second surface (129) that is opposite to the first face (127) of the third layer (105),

the first surface (127) of the third layer (105) includes a plurality of third electronic components (128) that is different from the plurality of first electronic components (124) and the plurality of second electronic components (126), and

the second surface (129) of the third layer (105) includes a plurality of fourth electronic components (130) that is different from the plurality of first electronic components (124), the plurality of second electronic components (126), and the plurality of third electronic components (128);

the first layer (101), the second layer (103), and the third layer (105) are vertically stacked using an optimized pin configuration for efficient power and data transmission.

2. The 3-layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, wherein the plurality of first electronic components (124) includes two or more of a plurality of temperature sensors (201), a series NOR flash (203), a first clock buffer (205), a crystal oscillator (207), a first power MOSFET transistor (209), a connector header mount (211), a micro low-profile header strip (219), or a combination thereof.

3. The 3 layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, wherein the plurality of second electronic components (126) includes two or more of a plurality of position connectors (303), a plurality of low power clocks (307), a plurality of shunt voltage reference ICs (309), a PCIe packet switch (311), a second clock buffer (205), a first voltage level translator (315), an 8-channel I2C switch (317), a flash memory IC (319), a linear regulator (321), a plurality of high-speed ground plane socket strips (323), or a combination thereof.

4. The 3-layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, wherein the plurality of third electronic components (128) includes two or more of a plurality of N-MOSFET transistor (401), a plurality of surface mount Silicon Schottky diodes (401B), a plurality of LEDs (403), a plurality of ultra-micro power terminals (405), a plurality of board-to-board connectors (411), a plurality of diode controllers (415), a microcontroller (419), a low profile SMD sub-miniature slide switch (421), a first low voltage ideal diode controller, a second low voltage ideal diode controller (423), a second voltage level translator (315B), a first voltage regulator (327), a second voltage regulator (329), a plurality of voltage controllers (433), or a combination thereof.

5. The 3-layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, wherein the plurality of fourth electronic components (130) includes two or more of a plurality of non-isolated DC/DC converters (501), a mezzanine connector (503), a plurality of step-down DC/DC µModule regulators (505), a power supply controller (507), a plurality of DC/DC controllers (509), a plurality of switching regulator chips (511), a plurality of DIP switches (513), a plurality of filters (515), a plurality of N-MOSFET transistors (401), a plurality of tact switches (523), a wire wound inductor (525), a power terminal header (527), a plurality of DC/DC POL converters (529), or a combination thereof.

6. The 3-layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, wherein

the first layer further includes a plurality of trapezium shaped interposers (101), and

each trapezium shaped interposer of the plurality of trapezium shaped interposers includes:

at least one processor (104) of the plurality of processors, and

a set of optoelectronic connectors (717) of the plurality of optoelectronic connectors.

7. The 3-layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, further comprises a mother board (20) that is connected to the third layer (105).

8. The 3-layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, wherein

the first layer (101) is connected to the second layer (103) via solder bumps (107), and the second layer (103) is connected to the third layer (105) via a plurality of edge connectors (109) an optimized pin configuration.

9. The 3-layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, wherein the optimized pin configuration includes a total of 3,500 pins that is about 240 pins between the first layer (101) and the second layer (103), about 2430 pins between the second layer (103) and the third layer (105), and about 600 pins between the third layer (105) and the mother board (20).

10. The 3-layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, wherein the shape of each of the first layer (101), the second layer (103), and the third layer (105) corresponds to a hexagonal shape.

SUBMISSION TO OBJECTION 1

INVENTIVE STEP:

Claim(s) (1-10) lack(s) inventive step, being obvious in view of teaching(s) of cited document(s) above under reference for the following reasons:

D1: US6690845B1 Pub Date: 10/02/2004

D2: US20230176304A1 Pub Date: 08/06/2023

The subject matter of claims 1-10 does not involve an inventive step given the disclosures of D1 and D2, having regards to common general knowledge in the art:

Independent claim 1:

D1 discloses (the references in parentheses applying to this document) a 3-layer opto-electronic engine (See claim 1: “opto-electronic module”), comprising:

a first layer (See abstract: “Three-dimensional opto-electronic modules having a plurality of opto-electronic (O/E) layers”) that includes: a plurality of processors (See IC Chips in fig. _1; See column 39, lines 36-40: “chips (including driver/amplifier chips and or processor/memory chips) and OE-devices (such as VCSEL, photodetectors, and others) can co-exist in the same layer in FIGS. 33-37 and 110 and 111”), and a

plurality of optoelectronic connectors (See fig._1: connectors ‘2’);

a second layer that is connected to the first layer (See abstract: “Three-dimensional opto-electronic modules having a plurality of opto-electronic (O/E) layers”; See fig._111),

wherein the second layer includes: a first surface that faces the first layer, and a second surface that is opposite to the first surface, the first surface includes: a plurality of first memories, and a plurality of first electronic components, and the second surface includes: a plurality of second memories that is different from the plurality of first memories, and a plurality of second electronic components that is different from the plurality of first electronic components (See column 39, lines 32-38: “The driver/amplifier chip described above may comprise circuits such as driver circuits, amplifier circuits, bias circuits, temperature stabilizing circuits, (clock) skew compensation circuits, timing circuits, and other applicable circuits. It is also possible that chips (including driver/amplifier chips and or processor/memory chips)”); and

a third layer connected to at least one of the first layer or the second layer (See abstract: “Three-dimensional opto-electronic modules having a plurality of opto-electronic (O/E) layers”; See fig._111),

wherein the third layer includes: a first surface that faces the second layer, and a second surface that is opposite to the first face of the third layer, the first surface of the third layer includes a plurality of third electronic components that is different from the plurality of first electronic components and the plurality of second electronic components, and the second surface of the third layer includes a plurality of fourth electronic components that is different from the plurality of first electronic components, the plurality of second electronic components, and the plurality of third electronic components (See column 39, lines 32-38: “The driver/amplifier chip described above may comprise circuits such as driver circuits, amplifier circuits, bias circuits, temperature stabilizing circuits, (clock) skew compensation circuits, timing circuits, and other applicable circuits. It is also possible that chips (including driver/amplifier chips and or processor/memory chips)”);

the first layer, the second layer, and the third layer are vertically stacked using an optimized pin configuration (See fig._111).

D1 does not disclose the following features of claim 1:

“the plurality of optoelectronic connectors are arranged to surround the plurality of processors, wherein the plurality of optoelectronic connectors and the plurality of processors are coupled using a set of connections such that route length between the plurality of processors is optimal in an intra-3 layer opto-electronic engine communication and inter-3 layer opto-electronic engine communication is optimal and lossless to maintain signal integrity”.

However, coupling of processors with optoelectronic connectors is a well-known design option for a person skilled in the art. Same can be inferred from D2. See abstract of D2: “A system includes a substrate on which a data processor and a connector block are mounted. The connector block has a first array of electrical connectors on a first surface, and a second array of electrical contacts on a second surface that is oriented at an angle between 45° to 135° relative to a main surface of the substrate. At least a portion of the first array of electrical connectors are electrically coupled to the data processor, and the second array of electrical contacts are electrically connected to the electrical contacts of a pluggable module.”

Therefore, starting only from the teachings of D1, it would be obvious to a person skilled in the art to combine the teachings of D2 with D1 to arrive at the subject matter of the independent Claim 1. Hence, the said claim lacks inventive step.

Dependent claims 2-10 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of inventive step in view of the disclosures of D1 and D2, having regards to common general knowledge in the art.

OUR REPLY:

Technical problem:

With the Processor performance becoming extremely power hungry, designers are looking at integrating multiple chiplets in a package to manage the heat dissipation. Vertical interconnects provide the shortest link between chips in a package. Heterogeneous integration uses packaging technology to integrate different chips or components from different foundries with different wafer sizes and feature sizes on different substrates. Modern data centers have pluggable optical transceivers

at card edge for external I/O. As next generation computation and storage require infrastructures which are closer to the processor to increase data bandwidth and reduce power consumption. However, there is a need for a heterogeneous integration with a co-package of optics with processor and memory. This set of components reduce number of connections and assembly cost for construction with increase in throughput.

Distributed computing systems and dynamic routing often have issues of their own. Traversing wires over long stretches, electrical signals are typically affected by noise and attenuation. There is a need for invention which solves the problem or reduce the effects of noise and attenuation by using different transmission method that existing techniques.

Technical solution:

The problem of low-speed interconnections in distributed computing, low signal integrity and limited processing capacity is solved by using a heterogeneous integration of various components along with high-speed transceivers and processors that are coupled with memory in modular multi layered stack. The components are distributed amongst three layers. The first layer comprises multiple processors and multiple high-speed interconnects distributed in the first layer. The second layer is a digital layer comprising clock ICs, buffer clock, MUX, JTAG, USB etc., that support the processors. The third layer is an analog layer comprising power ICs that feed power to the first two layers and external I/O interface:

A 3 layer System-in-Package enabled opto-electronic engine (100), comprising:

a first layer (101) that includes:

a plurality of processors (104), and

a plurality of optoelectronic connectors (111,113,115,117,119,121)

wherein

the plurality of optoelectronic connectors (111,113,115,117,119,121) are arranged to surround the plurality of processors (104) and a set of connections (102),

wherein the plurality of optoelectronic connectors (111,113,115,117,119,121) and the plurality of processors (104) are coupled using the set of connections (102) such that route length between the plurality of processors (104) is optimal in an intra-3 layer System-in-Package enabled opto-electronic engine (100) communication and inter-3 layer System-in-

Package enabled opto-electronic engine (100) communication is optimal and loss less to maintain signal integrity and reduce signal degradation;

a second layer (103) that is connected to the first layer (101), wherein

the second layer (103) includes:

a first surface (123) that faces the first layer (101), and

a second surface (125) that is opposite to the first surface (123),

the first surface (123) includes:

a plurality of first memories (709A), and

a plurality of first electronic components (124), and

the second surface (125) includes:

a plurality of second memories (709B) that is different from the plurality of first memories (709A), and

a plurality of second electronic components (126) that is different from the plurality of first electronic components (124); and

a third layer (105) connected to at least one of the first layer (101) or the second layer (103), wherein

the third layer (105) includes:

a first surface (127) that faces the second layer (103), and

a second surface (129) that is opposite to the first face (127) of the third layer (105),

the first surface (127) of the third layer (105) includes a plurality of third electronic components (128) that is different from the plurality of first electronic components (124) and the plurality of second electronic components (126), and

the second surface (129) of the third layer (105) includes a plurality of fourth electronic components (130) that is different from the plurality of first electronic components (124), the plurality of second electronic components (126), and the plurality of third electronic components (128);

the first layer (101), the second layer (103), and the third layer (105) are vertically stacked using an optimized pin configuration for efficient power and data transmission.

Regarding Claim 1:

The claim 1 is amended to more clearly articulate the subject matter and also to overcome the objections raised in the first examination report. The

amendments are fully supported in the specification on record.

It is well settled that in determining the differences between the prior art and the claims, the question under is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. To this end, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention.

[Emphasis Added] To establish a prima facie case of obviousness, three basic criteria must be met: (1) there must be some suggestion or motivation to modify the reference or to combine reference teachings; (2) there must be reasonable expectation of success; and (3) the prior art reference must teach or suggest all the claim limitations. Thus, Applicant respectfully traverses the rejection because the approach disclosed in D1-D2 and approach claimed in the instant application is not only different, but portions of D1-D2 upon which the Controller relied do not render the claimed invention render obvious.

Claim 1 has been amended to recite:

A 3 layer System-in-Package enabled opto-electronic engine (100), comprising:

a first layer (101) that includes:

a plurality of processors (104), and

a plurality of optoelectronic connectors (111,113,115,117,119,121) wherein

the plurality of optoelectronic connectors (111,113,115,117,119,121) are arranged to surround the plurality of processors (104) and a set of connections (102),

wherein the plurality of optoelectronic connectors (111,113,115,117,119,121) and the plurality of processors (104) are coupled using the set of connections (102) such that route length between the plurality of processors (104) is optimal in an intra-3 layer System-in-Package enabled opto-electronic engine (100) communication and inter-3 layer System-in-Package enabled opto-electronic engine (100) communication is optimal and loss less to maintain signal integrity and reduce signal degradation;

a second layer (103) that is connected to the first layer (101), wherein

the second layer (103) includes:

a first surface (123) that faces the first layer (101), and

a second surface (125) that is opposite to the first surface (123),

the first surface (123) includes:

a plurality of first memories (709A), and

a plurality of first electronic components (124), and

the second surface (125) includes:

a plurality of second memories (709B) that is different from the plurality of first memories (709A), and

a plurality of second electronic components (126) that is different from the plurality of first electronic components (124); and

a third layer (105) connected to at least one of the first layer (101) or the second layer (103), wherein

the third layer (105) includes:

a first surface (127) that faces the second layer (103), and

a second surface (129) that is opposite to the first face (127) of the third layer (105),

the first surface (127) of the third layer (105) includes a plurality of third electronic components (128) that is different from the plurality of first electronic components (124) and the plurality of second electronic components (126), and

the second surface (129) of the third layer (105) includes a plurality of fourth electronic components (130) that is different from the plurality of first electronic components (124), the plurality of second electronic components (126), and the plurality of third electronic components (128);

the first layer (101), the second layer (103), and the third layer (105) are vertically stacked using an optimized pin configuration for efficient power and data transmission.

Applicant respectfully submits that the document **D1** discloses a three-dimensional opto-electronic modules having a plurality of opto-electronic (O/E) layers, with optical signals being routed between O/E layers within one or more three dimensional volumes, are disclosed. In preferred embodiments, the O/E layers are

disposed over and above one another with at least one of their edges aligned to one another. At least two of the O/E layers have waveguides with ends near the aligned edges. A plurality of Z-connector arrays are disposed between the O/E layers and within the three-dimensional Volumes to provide a plurality of Z-direction waveguides. A first vertical optical coupler couples light from one waveguide in one O/E layer to a Z-direction waveguide, and a Second vertical optical coupler couples the light from the Z-direction waveguide to a Second waveguide in a second O/E layer. In further preferred embodiments, Segments of the Z-connector arrays are held by a holding unit.

However, the applicant humbly submits that teachings of **D1** are limited to general 3D opto-electronic module concepts and do not disclose or suggest a vertically stacked engine wherein optoelectronic connectors are arranged around processors to optimize intra-layer and inter-layer communication. While **D1** mentions co-location of processors, memory, and optoelectronic devices, it lacks architectural framework for signal routing optimization based on component placement. Specifically**, D1** does not describe a configuration where symmetrical connector placement reduces lateral signal travel, minimizes latency, and ensures signal integrity through shortest-path routing. Furthermore, **D1** does not disclose any optimized pin configuration that is functionally aligned with signal domains, thermal zones, or inter-layer communication needs. The claimed invention introduces a spatially and electrically optimized structure with dedicated interconnect paths, enabling high-speed, low-loss communication. Therefore, the applicant respectfully submits that **D1** neither anticipates nor suggests the spatial integration and communication-focused architecture described in the present invention.

Applicant respectfully submits that the document **D2** discloses a system includes a substrate on which a data processor and a connector block are mounted. The connector block has a first array of electrical connectors on a first surface, and a second array of electrical conducts on a second surface that is oriented at an angle between 45° to 135° relative to a main surface of the substrate. At least a portion of the first array of electrical connectors are electrically coupled to the data processor, and the second array of electrical contacts are electrically connected to the electrical contacts of a pluggable module. The pluggable module includes an optical module, at least one first optical connector, a first fiber optic cable optically coupled between

the optical module and the first optical connector, and a fiber guide positioned between the optical module and the first optical connector and provides mechanical support for the optical module and the first optical connector.

However, the applicant humbly submits that teachings of **D2** are limited to substrate-mounted architectures and do not disclose or suggest a vertically stacked opto-electronic engine with multi-layer inter-communication capabilities. **D2** discusses an angled connector system intended for pluggable modules, but it does not involve any stacking methodology where optoelectronic connectors surround processors to optimize routing efficiency or signal transmission. Furthermore, **D2** lacks any disclosure of layered memory and component distribution designed to support modularity, electromagnetic isolation, and high-performance signal processing. The invention described herein integrates a specialized pin configuration across stacked layers, specifically aligned with processor and memory positioning to support high-density, loss-minimized communication. **D2** does not present any configuration wherein vertical integration enables signal path optimization through physical component placement. Therefore, the applicant respectfully submits that **D2** neither anticipates nor renders obvious the synergistic structural and functional features of the present invention.

Applicant respectfully submits that when considering the combined teachings of **D1 and D2**, the instant invention demonstrates significant differences that render it non-obvious. Neither **D1** nor **D2** discloses or suggests a vertically stacked opto-electronic engine wherein optoelectronic connectors are symmetrically arranged around processors to minimize signal routing distance and enhance inter-layer communication. Additionally, the prior art lacks a specialized, functionally aligned pin configuration designed to optimize signal integrity, reduce thermal hotspots, and support high-density optical interconnects. The claimed invention introduces a synergistic architecture involving spatially optimized processor-memory distribution, impedance-matched interconnects, and co-packaged optics, which collectively achieve performance improvements not taught or suggested by the cited documents.

[Emphasis Added] D1-D2 discloses a completely different solution and does not set motivation to combine **D1** and **D2** to arrive at the Applicant claimed

invention. Even the problem statement, and the solution of **D1-D2** and Applicant claimed invention is different and hence the solutions. The problem statement is clearly evident from background of **D1-D2** and Applicant claimed invention. It is to be noted that **D1-D2** discloses completely different method and does not disclose the following features of the applicant claimed invention:

Instant invention	**D1- D2** disclosed features
A 3 layer System-in-Package enabled opto-electronic engine (100), comprising: a first layer (101) that includes: a plurality of processors (104), and a plurality of optoelectronic connectors (111,113,115,117,119,121) wherein the plurality of optoelectronic connectors (111,113,115,117,119,121) are arranged to surround the plurality of processors (104) and a set of connections (102), wherein the plurality of optoelectronic connectors (111,113,115,117,119,121) and the plurality of processors (104) are coupled using the set of connections (102) such that route length between the plurality of processors (104) is optimal in an intra-3 layer	**D1** talks about "a three-dimensional opto-electronic modules having a plurality of opto-electronic (O/E) layers, with optical signals being routed between O/E layers within one or more three dimensional volumes, are disclosed. In preferred embodiments, the O/E layers are disposed over and above one another with at least one of their edges aligned to one another. At least two of the O/E layers have waveguides with ends near the aligned edges. A plurality of Z-connector arrays are disposed between the O/E layers and within the three dimensional Volumes to provide a plurality of Z-direction waveguides. A first vertical optical coupler couples light from one waveguide in one O/E layer to a Z-direction waveguide, and a Second vertical optical coupler couples the light from the Z-direction waveguide to a Second waveguide in a second O/E layer. In further preferred embodiments, Segments of the Z-connector arrays are held by a holding unit." **D2** talks about "a system that includes a substrate on which a data processor and a

System-in-Package enabled opto-electronic engine (100) communication and inter-3 layer System-in-Package enabled opto-electronic engine (100) communication is optimal and loss less to maintain signal integrity and reduce signal degradation; a second layer (103) that is connected to the first layer (101), wherein the second layer (103) includes: a first surface (123) that faces the first layer (101), and a second surface (125) that is opposite to the first surface (123), the first surface (123) includes: a plurality of first memories (709A), and a plurality of first electronic components (124), and the second surface (125) includes: a plurality of second memories (709B) that is different from the plurality of	connector block are mounted. The connector block has a first array of electrical connectors on a first surface, and a second array of electrical conducts on a second surface that is oriented at an angle between 45° to 135° relative to a main surface of the substrate. At least a portion of the first array of electrical connectors are electrically coupled to the data processor, and the second array of electrical contacts are electrically connected to the electrical contacts of a pluggable module. The pluggable module includes an optical module, at least one first optical connector, a first fiber optic cable optically coupled between the optical module and the first optical connector, and a fiber guide positioned between the optical module and the first optical connector and provides mechanical support for the optical module and the first optical connector.” Hence, **D1-D2** fails to disclose “A 3 layer System-in-Package enabled opto-electronic engine (100), comprising: a first layer (101) that includes: a plurality of processors (104), and a plurality of optoelectronic connectors (111,113,115,117,119,121) wherein the plurality of optoelectronic connectors (111,113,115,117,119,121) are arranged to surround the plurality of processors (104) and a set of connections

first memories (709A), and

a plurality of second electronic components (126) that is different from the plurality of first electronic components (124); and

a third layer (105) connected to at least one of the first layer (101) or the second layer (103), wherein

the third layer (105) includes:

a first surface (127) that faces the second layer (103), and

a second surface (129) that is opposite to the first face (127) of the third layer (105),

the first surface (127) of the third layer (105) includes a plurality of third electronic components (128) that is different from the plurality of first electronic components (124) and the plurality of second electronic components (126), and

the second surface (129) of the third layer (105) includes a plurality of fourth electronic components (130) that is different from the plurality of first

(102),

wherein the plurality of optoelectronic connectors (111,113,115,117,119,121) and the plurality of processors (104) are coupled using the set of connections (102) such that route length between the plurality of processors (104) is optimal in an intra-3 layer System-in-Package enabled opto-electronic engine (100) communication and inter-3 layer System-in-Package enabled opto-electronic engine (100) communication is optimal and loss less to maintain signal integrity and reduce signal degradation;

a second layer (103) that is connected to the first layer (101), wherein

the second layer (103) includes:

a first surface (123) that faces the first layer (101), and

a second surface (125) that is opposite to the first surface (123),

the first surface (123) includes:

a plurality of first memories (709A), and

a plurality of first electronic components (124), and

the second surface (125) includes:

a plurality of second memories (709B) that is different from the plurality of first memories (709A), and

electronic components (124), the plurality of second electronic components (126), and the plurality of third electronic components (128); the first layer (101), the second layer (103), and the third layer (105) are vertically stacked using an optimized pin configuration for efficient power and data transmission.	a plurality of second electronic components (126) that is different from the plurality of first electronic components (124); and a third layer (105) connected to at least one of the first layer (101) or the second layer (103), wherein the third layer (105) includes: a first surface (127) that faces the second layer (103), and a second surface (129) that is opposite to the first face (127) of the third layer (105), the first surface (127) of the third layer (105) includes a plurality of third electronic components (128) that is different from the plurality of first electronic components (124) and the plurality of second electronic components (126), and the second surface (129) of the third layer (105) includes a plurality of fourth electronic components (130) that is different from the plurality of first electronic components (124), the plurality of second electronic components (126), and the plurality of third electronic components (128); the first layer (101), the second layer (103), and the third layer (105) are vertically stacked using an

	optimized pin configuration for efficient power and data transmission." A person with combining skills cannot combine the teachings provided in the prior arts (**D1-D2**). Hence, **D1-D2** fails to disclose the features present in the invention. The interpretation asserted by the examiner is not supported by the cited portions of the **D1-D2**. Thus, reconsideration is respectfully requested.

[Emphasis added] It is important to consider the functions and underlying essence of the invention as described in all steps mentioned in the claims. Therefore, it is respectfully submitted that the interpretation asserted by the Examiner is not supported by the disclosure of **D1-D2**. Further, Applicant believe the interpretation asserted by the Examiner regarding the claimed steps is not supported by the disclosure of **D1-D2**. Nowhere in the cited portions and the whole document does **D1-D2** describe or reasonably suggest the above indicated features claimed in the amended independent claim 1. Therefore, the steps of **D1-D2** are different from that of Applicant's claimed subject matter. Additionally, a prima facie obviousness has not been established. Merely recitation of portions from prior art does not sustain the rejection of obviousness unless the prior art reasonably teaches and provides articulated reasoning with rational underpinning to support the legal conclusion of obviousness. Thus, based on the above, to the extent **D1-D2** does not disclose, reasonably teach or suggest the features of the amended independent claim 1, and hence it is respectfully submitted that independent claim 1 is patentable over the cited prior art. Nor does **D1-D2** motivate one of ordinary skill in the art to combine **D1-D2** with another reference to arrive at the claimed invention. Reconsideration is respectfully requested.

Regarding Claim 2:

The 3-layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, wherein the plurality of first electronic components (124) includes two or more of a plurality of temperature sensors (201), a series NOR flash (203), a first clock buffer (205), a crystal oscillator (207), a first power MOSFET transistor (209), a connector header mount (211), a micro low-profile header strip (219), or a combination thereof.

Apart from the above, Applicant believes that dependent claim 2 is allowable not only by virtue of their dependency from patentable independent claim 1, respectively, but also by virtue of the additional features of the invention they define. The dependent claims describe various embodiments of the invention that can be combined to form the invention. The subject matter described in the instant application are different from D1-D2 so as the features described in dependent claim 2.

Regarding Claim 3:

The 3 layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, wherein the plurality of second electronic components (126) includes two or more of a plurality of position connectors (303), a plurality of low power clocks (307), a plurality of shunt voltage reference ICs (309), a PCIe packet switch (311), a second clock buffer (205), a first voltage level translator (315), an 8-channel I2C switch (317), a flash memory IC (319), a linear regulator (321), a plurality of high-speed ground plane socket strips (323), or a combination thereof.

Apart from the above, Applicant believes that dependent claim 3 is allowable not only by virtue of their dependency from patentable independent claim 1, respectively, but also by virtue of the additional features of the invention they define. The dependent claims describe various embodiments of the invention that can be combined to form the invention. The subject matter described in the instant application are different from D1-D2 so as the features described in dependent claim 3.

Regarding Claim 4:

The 3-layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, wherein the plurality of third electronic components (128) includes

two or more of a plurality of N-MOSFET transistor (401), a plurality of surface mount Silicon Schottky diodes (401B), a plurality of LEDs (403), a plurality of ultra-micro power terminals (405), a plurality of board-to-board connectors (411), a plurality of diode controllers (415), a microcontroller (419), a low profile SMD sub-miniature slide switch (421), a first low voltage ideal diode controller, a second low voltage ideal diode controller (423), a second voltage level translator (315B), a first voltage regulator (327), a second voltage regulator (329), a plurality of voltage controllers (433), or a combination thereof.

Apart from the above, Applicant believes that dependent claim 4 is allowable not only by virtue of their dependency from patentable independent claim 1, respectively, but also by virtue of the additional features of the invention they define. The dependent claims describe various embodiments of the invention that can be combined to form the invention. The subject matter described in the instant application are different from D1-D2 so as the features described in dependent claim 4.

Regarding Claim 5:

The 3-layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, wherein the plurality of fourth electronic components (130) includes two or more of a plurality of non-isolated DC/DC converters (501), a mezzanine connector (503), a plurality of step-down DC/DC µModule regulators (505), a power supply controller (507), a plurality of DC/DC controllers (509), a plurality of switching regulator chips (511), a plurality of DIP switches (513), a plurality of filters (515), a plurality of N-MOSFET transistors (401), a plurality of tact switches (523), a wire wound inductor (525), a power terminal header (527), a plurality of DC/DC POL converters (529), or a combination thereof.

Apart from the above, Applicant believes that dependent claim 5 is allowable not only by virtue of their dependency from patentable independent claim 1, respectively, but also by virtue of the additional features of the invention they define. The dependent claims describe various embodiments of the invention that can be combined to form the invention. The subject matter described in the instant application are different from D1-D2 so as the features described in dependent claim 5.

Regarding Claim 6:

The 3-layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, wherein

the first layer further includes a plurality of trapezium shaped interposers (101), and

each trapezium shaped interposer of the plurality of trapezium shaped interposers includes:

at least one processor (104) of the plurality of processors, and

a set of optoelectronic connectors (717) of the plurality of optoelectronic connectors.

Apart from the above, Applicant believes that dependent claim 6 is allowable not only by virtue of their dependency from patentable independent claim 1, respectively, but also by virtue of the additional features of the invention they define. The dependent claims describe various embodiments of the invention that can be combined to form the invention. The subject matter described in the instant application are different from D1-D2 so as the features described in dependent claim 6.

Regarding Claim 7:

The 3-layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, further comprises a mother board (20) that is connected to the third layer (105).

Apart from the above, Applicant believes that dependent claim 7 is allowable not only by virtue of their dependency from patentable independent claim 1, respectively, but also by virtue of the additional features of the invention they define. The dependent claims describe various embodiments of the invention that can be combined to form the invention. The subject matter described in the instant application are different from D1-D2 so as the features described in dependent claim 7.

Regarding Claim 8:

The 3-layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, wherein

the first layer (101) is connected to the second layer (103) via solder bumps (107), and the second layer (103) is connected to the third layer (105) via a plurality of edge connectors (109) an optimized pin configuration.

Apart from the above, Applicant believes that dependent claim 8 is allowable not only by virtue of their dependency from patentable independent claim 1, respectively, but also by virtue of the additional features of the invention they define. The dependent claims describe various embodiments of the invention that can be combined to form the invention. The subject matter described in the instant application are different from D1-D2 so as the features described in dependent claim 8.

Regarding Claim 9:

The 3-layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, wherein the optimized pin configuration includes a total of 3,500 pins that is about 240 pins between the first layer (101) and the second layer (103), about 2430 pins between the second layer (103) and the third layer (105), and about 600 pins between the third layer (105) and the mother board (20).

Apart from the above, Applicant believes that dependent claim 9 is allowable not only by virtue of their dependency from patentable independent claim 1, respectively, but also by virtue of the additional features of the invention they define. The dependent claims describe various embodiments of the invention that can be combined to form the invention. The subject matter described in the instant application are different from D1-D2 so as the features described in dependent claim 9.

Regarding Claim 10:

The 3-layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, wherein the shape of each of the first layer (101), the second layer (103), and the third layer (105) corresponds to a hexagonal shape.

Apart from the above, Applicant believes that dependent claim 10 is

allowable not only by virtue of their dependency from patentable independent claim 1, respectively, but also by virtue of the additional features of the invention they define. The dependent claims describe various embodiments of the invention that can be combined to form the invention. The subject matter described in the instant application are different from D1-D2 so as the features described in dependent claim 10.

SUBMISSION TO OBJECTION 2

NON PATENTABILITY:

Claim(s) (1-10) are statutorily non-patentable under the provision of clause (3(f), 3(o)) of Section 3 for the following reasons:

Claimed invention, which describes a 3-layer opto-electronic engine comprising a plurality of processors, memories, optoelectronic connectors and different electronic components arranged in vertically stacked layers with an “optimized pin configuration”, appears to fall under section 3(f) of the Patents Act, 1970. The invention described an arrangement of known components i.e. processors, memories, optoelectronic connectors, electronic components. Moreover, the concept of vertically stacking layers with specific components is well-known in the field of electronics and optoelectronics. Claims include an “optimized pin configuration” and also “optimal” & “lossless” communication, however it is not clear what makes the pin configuration “optimized” and what is making “optimal” and “lossless” communication.

Further it appears that no inherent coupling/interaction among the components is clear from the statement of the Claim. Different electronic components are merely placed on three vertically stacked layers that are functioning independently of one-another with no combinational function of them comes out clearly from the statement of the Claim. Such disclosure of sub-systems is a mere-arrangement or re-arrangement and thus is not allowable u/s 3(f) of the Patent Act 1970, as amended.

- The subject matter of the claimed invention in claims 1- 10 relates to the topography of integrated circuits (i.e first layer further includes a plurality of trapezium shaped interposers...../... third layer corresponds to a hexagonal shape.). Hence the subject matter of the claims are not allowable under section

3(o) of the Patents Act.

OUR REPLY:

The Applicant humbly submits that the claimed invention is not a mere arrangement or re-arrangement of known components, but a functionally integrated 3-layer System-in-Package enabled opto-electronic engine that introduces a novel architecture for enhanced signal integrity, reduced latency, and lossless communication. The invention incorporates a specifically optimized spatial placement of optoelectronic connectors around processors, an impedance-matched pin configuration, and a layered memory distribution scheme.

The Applicant respectfully submits that the components in the invention are not functioning independently but are structurally and functionally interrelated to achieve a synergistic effect that improves overall system performance. The inter-layer communication, thermal-aware layout, and optical coupling provide a combinational effect that goes beyond a simple aggregation of known elements and addresses real-world challenges in high-density optoelectronic systems.

With respect to the objection under Section 3(o), the Applicant respectfully clarifies that the reference to geometric shapes such as trapezium and hexagonal forms in the claims is not intended to claim circuit topography, but rather defines the functional design and spatial layout of the layers and interposers to support signal routing efficiency and thermal optimization. The invention does not relate to topography per se, and is therefore not excluded under Section 3(o).

SUBMISSION TO OBJECTION 3

SUFFICIENCY OF DISCLOSURE:

(I) Abstract:

Necessary figure and the reference numerals aren't indicated in the abstract. The 'abstract' should be prepared in accordance with the instructions contained in Rule 13{7} of the Patent Rules, 2003(as amended).

OUR REPLY:

The Applicant humbly submits that the abstract has been amended and now is in

compliance with the Rule 13{7} of the Patent Rules, 2003(as amended). Also, the Applicant humbly submits that the abstract now has necessary figure and the reference numerals.

SUBMISSION TO OBJECTION 4

CLARITY AND CONCISENESS:

Claim(s) 1-10 are not clearly worded in respect of:

1. Reference numerals in the claims shall be placed in parenthesis.

2. Claim 1 states “the plurality of optoelectronic connectors (111,113,115,117,119,121) and the plurality of processors 104 are coupled using a set of connections 102 such that route length between the plurality of processors 104 is optimal in an intra-3 layer opto-electronic engine 100 communication and inter-3 layer opto-electronic engine 100 communication is optimal and loss less to maintain signal integrity”. However, the claim merely states the objectives of "optimal" and "lossless" communication without specifying the means or methodology by which these objectives are achieved. Specifically, the claim lacks any description of the steps, processes, or mechanisms that ensure the optimization of routing paths, as well as the maintenance of signal integrity and lossless transmission. Redraft claim 1 accordingly.

3. Claim 1 states “the first layer 101, the second layer 103, and the third layer 105 are vertically stacked using an optimized pin configuration”. The claim does not provide sufficient detail on what constitutes an "optimized pin configuration" or how the stacking is optimized, making it unclear and broad. Claim shall be drafted in such a way that it should define what makes the pin configuration “optimized”.

OUR REPLY:

The applicant humbly submits that the claim amendment made is in compliance with section 59(1) & Section 10(4)(c) of the Patent Act, 1970. The applicant respectfully submits that, as claimed in claim 9, “The 3-layer System-in-Package enabled opto-electronic engine (100) as claimed in claim 1, wherein the optimized pin configuration includes a total of 3,500 pins that is about 240 pins between the first layer (101) and the second layer (103), about 2430 pins between the second layer (103) and the third layer (105), and about 600 pins between the third layer (105) and the mother board (20).”, the pin configuration with reduced number of pins make the system optimized. Also, the Applicant humbly submits that the reference numerals in the claims are now placed in parenthesis. Therefore, the Applicant humbly request the controller to withdraw the objection.

SUBMISSION TO OBJECTION 5

DEFINITIVENESS:

Claim(s) 1-10 do not sufficiently define the invention for the reasons as follows:

- In the absence of characterizing novel/inventive features in principal claim, the subject matter of claim does not seem to be clear u/s 10(5), and also scope is not defined u/s 10(4c) of The Patent Act. Hence comply with this requirement but within the well-defined boundary and scope of the specification disclosed.
- Principal claim should be such that it discloses fully and clearly the solution to the problem associated with the invention (as per section 10 of the act).
- The phrase "includes/further comprising” mentioned in the claim 7 is vague, hence should be amended.
- The phrase "of claim" mentioned in the claims are not clear and definitive; it should be replaced with “as claimed in” in the claim.

OUR REPLY:

The Applicant humbly submits that the claims have been duly amended to clearly define the scope and inventive features of the invention in compliance with Sections 10(4)(c) and 10(5) of the Patents Act, 1970. The principal claim has been revised to explicitly disclose the technical solution provided by the invention. Additionally, the phrasing “includes/further comprising” and “of claim” has been appropriately

amended throughout the claims for clarity and definitiveness.

SUBMISSION TO OBJECTION 6

OTHERS REQUIREMENTS:

1. In case applicant wishes to amend claims, indicate the reasons /technical significance thereof over the cited documents in your reply. Also please provide an additional copy of marked up amendments (highlighting the amendments) wherever applicable.

2. The independent claims should be cast in the two- part form where appropriate, with those features known in combination from the prior art being placed in the preamble and the remaining features being included in the characterizing part.

OUR REPLY:

The applicant humbly submits that all amendments to the specification and claims have been made strictly in accordance with Section 59 of the Patent Act, 1970. Also, the applicant respectfully verifies that the amendments have been made to clearly highlight the technical advancement over D1 and D2. A marked-up copy of the amended claims, along with a clean version, has been duly provided for reference and compliance.

FORMAL REQUIREMENTS:

Objections	Remarks	Our Reply
Form 13	• In the Form 13 of dated 17.07.2024, the date of filing of instant application number is not correctly mentioned, Applicant is required to submit the again correctly.	The Applicant hereby confirms that the deficiency is rectified by correcting the same.
Power of Attorney	• Stamp duty should be paid in respect of Power of Attorney for the instant application. • The signature in Power of Attorney i.e. 'Y. Rohin Kumar', is appears to be same as of inventor 'Rohin Kumar Yeluripati' as mentioned in Form 1. Kindly clear the anomaly. Applicant is required to produce 'Authorised certificate' in respect of the signatory of power of attorney. • Further, in Power of attorney, it is not mentioned under what capacity the signatory signed the same. • Applicant name should be mentioned along with the name and designation of signatory in the Power of Attorney.	The Applicant hereby confirms that the deficiency is rectified by correcting the same and a board resolution shall be provided regarding the signatory.
Format of Specification (rule 13)	• Claims should be prefaced with the words "We Claim". Also the claims must be signed by the applicant/authorized patent agent.	1. The Applicant humbly submits that the claim set has been duly updated to include the preface "We Claim" and has been signed by the authorized patent agent. Further, corrected drawing sheets have been submitted with the applicant's name updated, page numbering rectified, and the total number of drawing pages accurately reflected.

Format of Drawings	• In drawings of dated 02.06.2024, the name of applicant is 'Lightspeed photonics Pte Ltd.' Which is different from the name of applicant of instant application. Further, on the page number 12 and 13, the PAGE NO.: 11 is mentioned. Applicant attention is drawn to section 78(2) of the Patents Act. • In drawings sheet the 'TOTAL NO. OF PAGES: 14' is mentioned, but there are only 13 pages of drawings. Kindly clear the anomaly.	The Applicant hereby confirms that the error in total number of pages is corrected.
Other Deficiencies	• While filing the instant application, in Form 1 of dated 02.08.2023 (post-dated), under the serial number 3B.i.e. CATEGORY OF APPLICANT, applicant exercise the same by selecting 'Others'. which is an anomaly. Applicant attention is drawn to section 78(2) of the Patents Act. • In Form 2 of dated 02.08.2023(post-dated) it is mentioned "The following specification particularly describes the invention and the manner in which it is performed." which is not correct format of Form 2 for provisional specification. Applicant	1. The Applicant humbly submits that Form 2 dated 02.08.2023 has been revised to reflect the correct format for a provisional specification, in compliance with Section 78(2) of the Patents Act, 1970. 2. The Applicant further submits that Form 2 dated 02.06.2024 has been corrected

	attention is drawn to section 78(2) of the Patents Act. • In Form 2 of dated 02.06.2024 it is mentioned "The following specification particularly describes the invention and the way its performed." which is not correct format of Form 2 for Complete specification. Applicant attention is drawn to section 78(2) of the Patents Act. • Applicant changes the title of the instant application From "MULTIPLE LAYER ARCHITECTURE OF 3D SYSTEM IN PACKAGE" to "ASSEMBLY OF A 3 LAYER OPTO-ELECTRONIC ENGINE". Kindly clear the anomaly. Applicant attention drawn towards section 57 i.e. Form 13 for the change of title or section 78(2) for the correction of clerical error. • Applicant fails to comply rule 13(6) of the Patent Rules, 2003(as amended in 2006). • Form 5 of dated 02.08.2023(post-dated) was not signed by the Applicant. • While filing the complete specification, the pages of description, abstract, claims and Form 2 is 35 and in the drawings sheet it mentioned 'TOTAL NO. OF PAGES: 14'. Therefore, the pages of complete specification are 49. In view of this Applicant fails to submit the fees of balance one page of complete specification. • Applicant is required to submit Form 28 (in prescribed format) along with supporting document for the same. • With respect to addition of name of inventors, Applicant is required to submit the supporting document for the same. Further, the No objection certificate from each inventor is required to be submit.	to include the standard preamble for a complete specification, as required under the Patents Act. 3. All the errors in the forms is corrected by filing a Form 13. 4. The fee has been paid for 48 pages, and it was a clearical error that reflected 49 pages. It has been corrected. 5. NOC from inventors shall be provided

In the event above submissions are not found to be persuasive, a further hearing/an opportunity for clarification (through telephone, meeting or the like), preferably in view of Section 80 or Section 14 may please be granted before taking any adverse decision.

Yours faithfully,

Adv. Pranav Bhat
(Patent Agent - IN/PA 4580)

Enclosure:

1. Updated form 13
2. Updated form 5
3. Updated form 28
4. Updated Power of Attorney
5. A marked copy of claims
6. A clean copy of claims
7. A marked copy of Form-2(Provisional Specification)
8. A clean copy of Form-2(Provisional Specification)
9. A Marked Copy of Form-2(Complete Specification)
10. A Clean Copy of Form-2(Complete Specification)
11. A Marked copy of Drawings
12. A clean copy of drawings