E/16/078

CO 224 – Lab 5 – Part 5

Supported instructions - bne, sll, srl, sra

Opcodes

bne : 00001010

sll : 00001011

srl : 00001100

sra : 00001101

Changes made to the datapath + control

For bne instruction:

- Additional control signal BNOT is generated from the control signal.
- BNOT is set to high only for bne type instructions
- Negation of the ZERO signal which outputs from the ALU, and BNOT signal are connected to a two input AND gate.
- The output of the AND gate is high if ALU result not equals 0 when a bne instruction is functioning.
- The AND gate output is connected to a three input OR gate.
- Other two inputs of the OR gate are JUMP signal, output of BRANCH AND ZERO.
- The output of the OR gate is connected to selection port of MUX which outputs the next PC value.

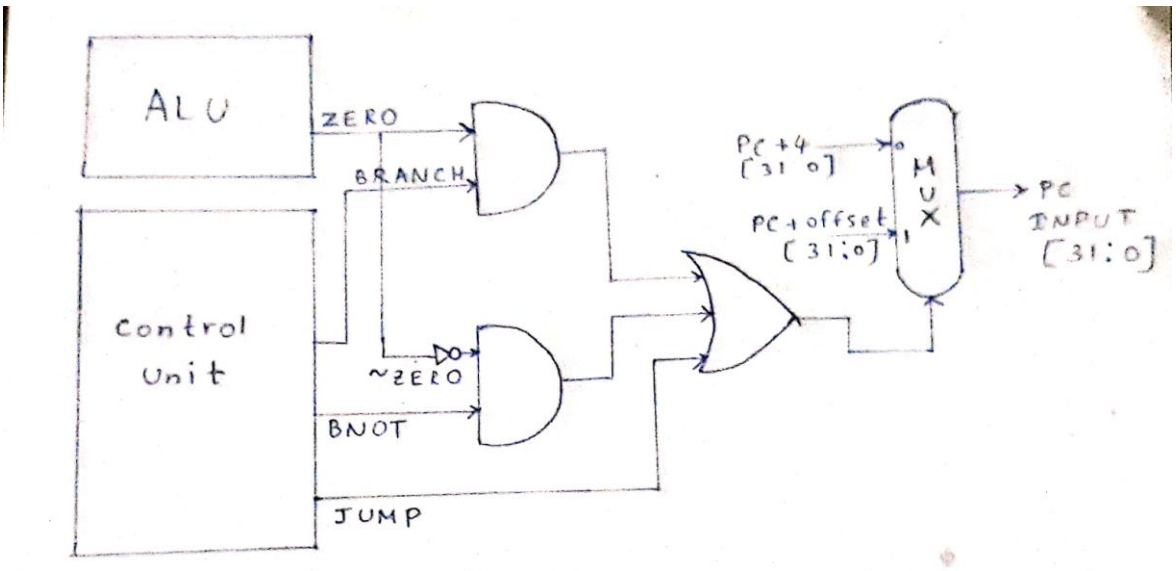

Figure 1 : Changes done to support bne

For shift instructions (sll, srl, sra):

- Additional control signals added to support shifting : SHIFT,SHIFT_ARITH,DIRECTION
  SHIFT : set high for all shift instructions ; ssl, srl, sra
  SHIFT_ARITH : set high only for arithmetic shift instrcutions ; sra
  DIRECTION : indicates the shifting direction; right=1, left=0

- A SHIFTER module is added to support shift instructions.

- Inputs of SHIFTER : VALUE, OFFSET ,SHIFT_BIT,DIRECTION

  VALUE : REGOUT1 of register file(REG_FILE) is connected to input port VALUE

  OFFSET : how many times to shift (INSTRUCTION[7:0])

  SHIFT_BIT : A module shift_bit is used to get the SHIFT_BIT

    Inputs : REGOUT1 (VALUE to be shifted), SHIFT_ARITH

    Output : SHIFT_BIT

    For arithmetic shift, module outputs the most significant bit of REGOUT1

    (If SHIFT_ARITH is 1, SHIFT_BIT = REGOUT1[7])

    For logical shift, module outputs 0 as the SHIFT_BIT

    (If SHIFT_ARITH is 0, SHIFT_BIT = 0)

  DIRECTION : the control signal generated from the control unit (right=1, left=0)

- Output of SHIFTER : SHIFTED_VALUE

- Inside SHIFTER, 4 sub modules are included to do 1 bit, 2 bit, 4 bit and 8 bit shifting.

- For each sub module, relevant bit in OFFSET is connected as SHIFT_ENABLE signal, as below.
  1 bit shifter : OFFSET[0]
  2 bit shifter : OFFSET[1]
  4 bit shifter : OFFSET[2]
  8 bit shifter : OFFSET[3]

- For 1 bit shifter, its input value is REGOUT1 as it is.
- For other sub shifters, their previous shifter module output will be send as their input, as below.
  1 bit shifter : REGOUT1
  2 bit shifter : OUT_SHIFT1 (output of 1 bit shfter)
  4 bit shifter : OUT_SHIFT2 (output of 2 bit shfter)
  8 bit shifter : OUT_SHIFT4 (output of 4 bit shfter)

- Output of the 8 bit shifter (OUT_SHIFT4) is sent as the final output of shifter; SHIFTED_VALUE
- The control signal SHIFT is used to select what is the data to be written to REG_FILE, from ALU_RESULT(output of ALU) and SHIFTED_VALUE(output of shifter)
- ALU_RESULT, SHIFTED_VALUE and SHIFT are send to a mux (MUX_REG)
- If SHIFT is high, mux send SHIFTED_VALUE to REG_FILE, or else the ALU_RESULT.

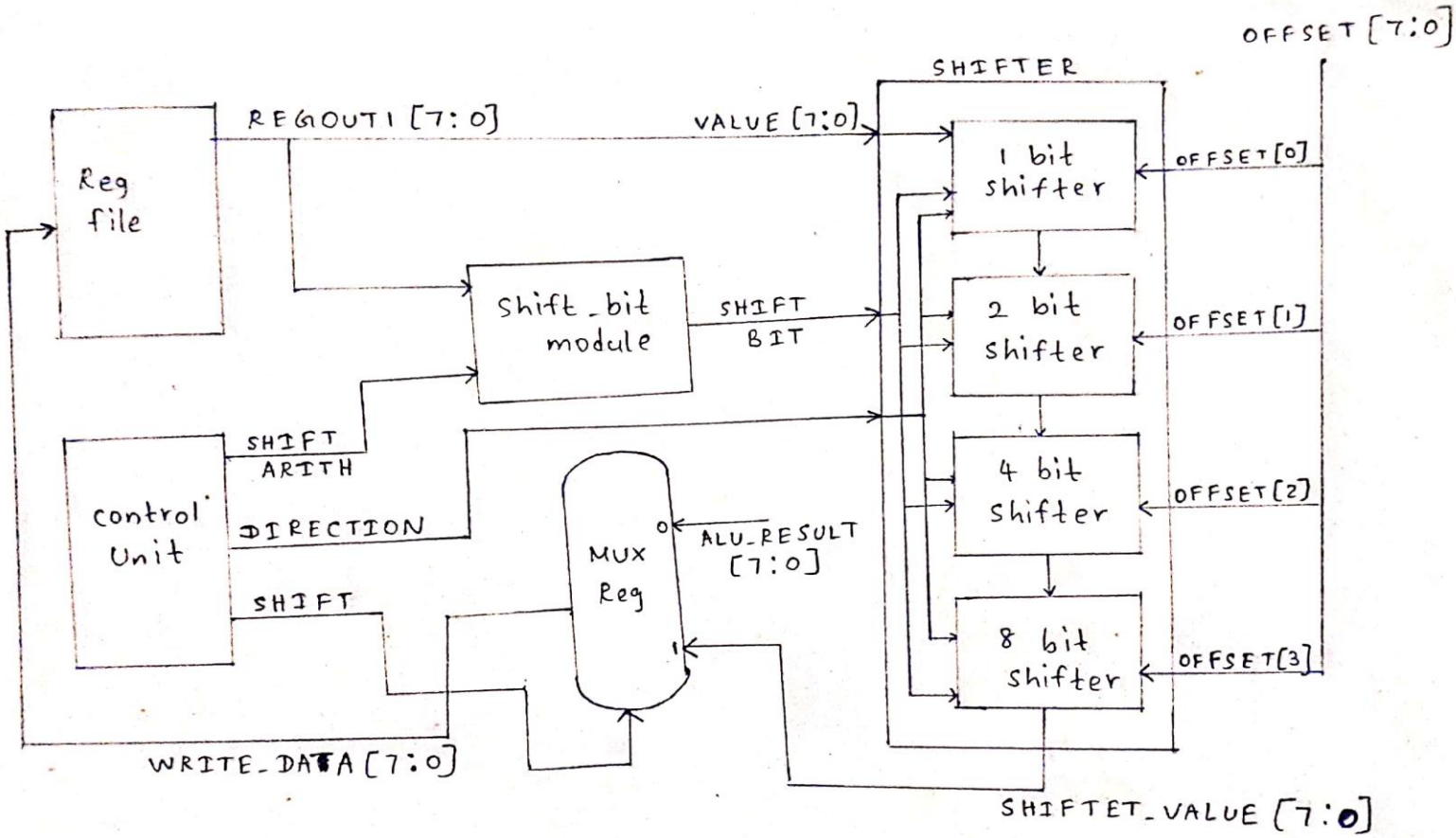

Figure 2: Changes done to support shift operations