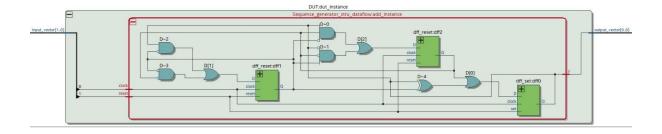
EE214 Digital Circuits Laboratory

EXP6 – Sequence Generator

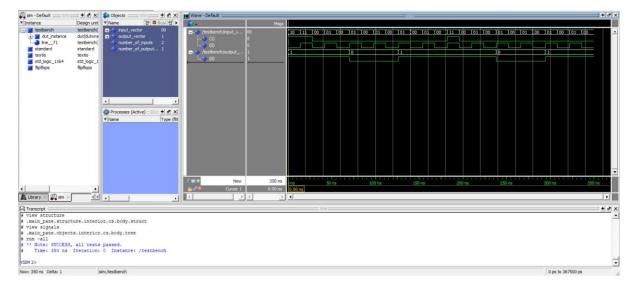
Swarup Dasharath Patil 22b3953

RTL Viewer:



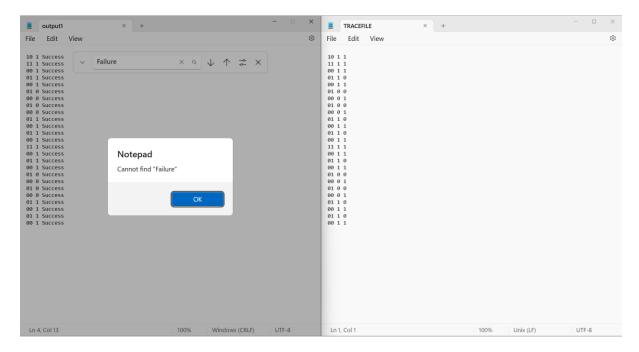
RTL Simulation:

Note: SUCCESS, all tests passed.



Scanchain based testing:

All tests were successful.



Lab Journal:

A state diagram to generate the states so that LSB of the states will generate the required sequence and from the state table with the help of K-Maps generate equations for DFF inputs in terms of present state and reset verified by the TA.

			M T W T F S S
EXPT. NO.	Weck 6: Sequence	Generala	Page No.: Date: 5/09/2023
	Priesent State	Next State	DFF, inputs
	001	011	0, 0, 70,
	011	0.00	0 1 1 0 0 0
	000	010	0 1 0
	010	101	101
	101	111	1 1 1
-	111	011	0 1 1
	100	011	0 1 1
	110	011	0 1 1
	D: 020 00 01 11 10		
	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		
			Q,)
	200		
-	01:000 01 11 10	1 0 . 0	
	0 2 1 1	$D_1 = Q_0 \overline{Q}_1 + \overline{Q}_1 \overline{Q}_2$	
	D ₂ : 0 01 11 10	0 - 000 . 5	2 2
	2.0	$D_2 = \overline{Q}_1 Q_1 Q_2 + \overline{Q}_1$	Q ₁ Q ₂
	Reset State		
	$(001) \rightarrow (011) \rightarrow (000) \rightarrow (010) \rightarrow (101)$		
	1		
		(111)	
	(Unused states:)		
	(100) (110)		Let Le
			A Depart
-	1 1		
-			
	Teacher's Signature:		