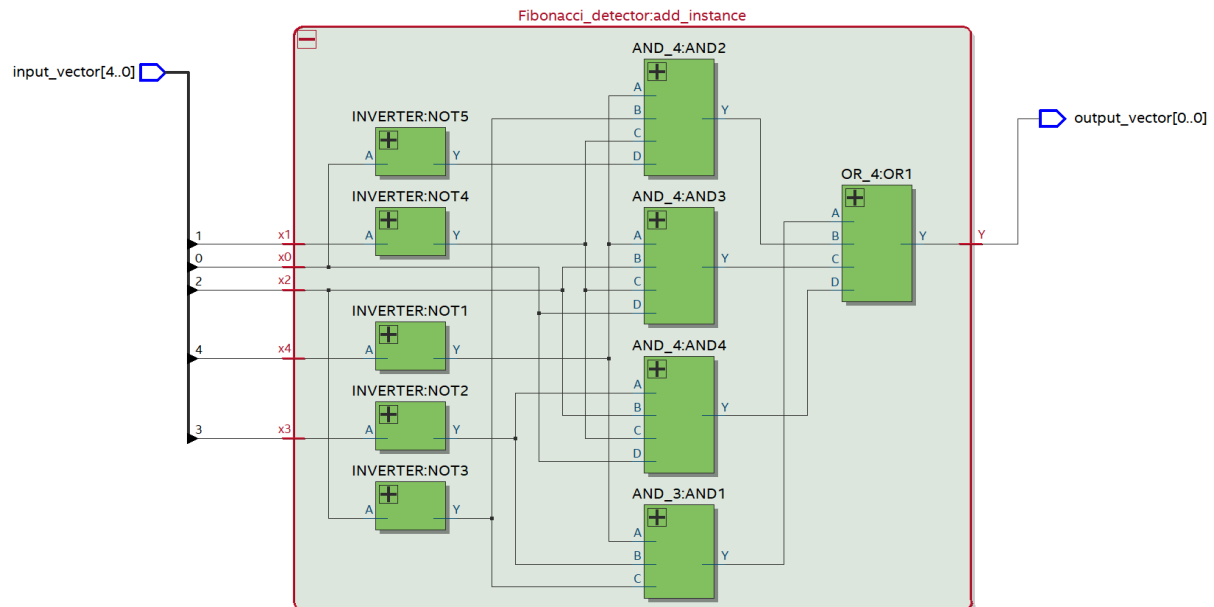


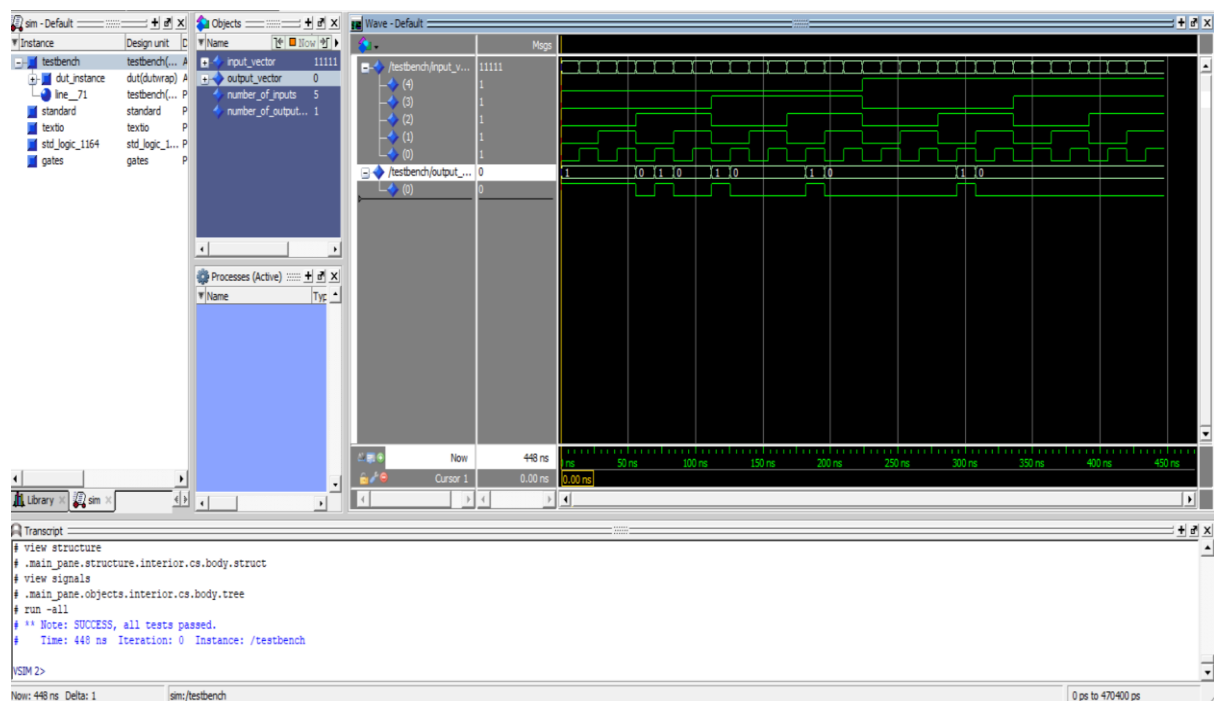
# EE214 Digital Circuits Laboratory

## EXP3 – Fibonacci Detector

### RTL Viewer:



### RTL Simulation:



## Pin Planner:

**Top View Wire Bond**

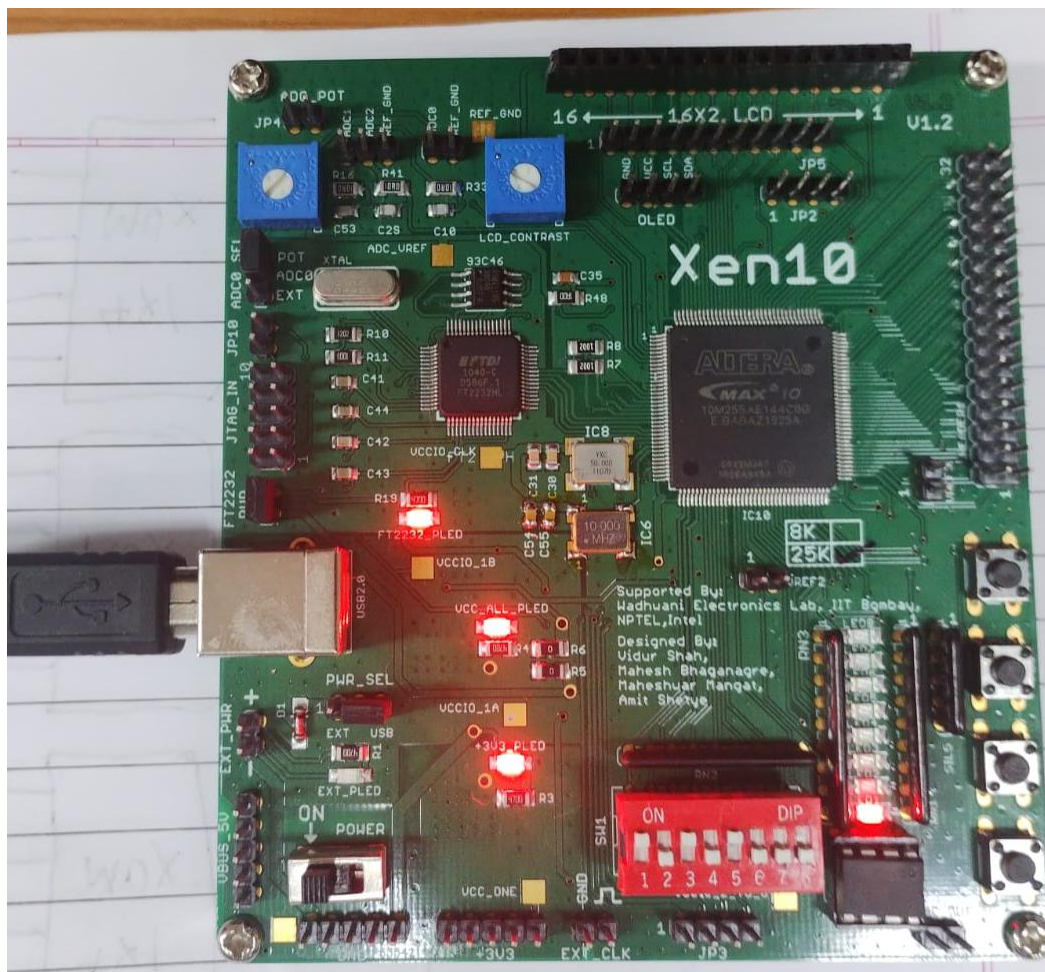
**MAX 10**  
**10M25SAE144C8G**

Node Name	Direction	Location	I/O Bank	VREF Group	Iter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	IOct Preservat
Input_vector[4]	Input	PIN_44	3	B3_NO	PIN_44	2.5 V		12mA...auto			
Input_vector[3]	Input	PIN_43	3	B3_NO	PIN_43	2.5 V		12mA...auto			
Input_vector[2]	Input	PIN_41	3	B3_NO	PIN_41	2.5 V		12mA...auto			
Input_vector[1]	Input	PIN_39	3	B3_NO	PIN_39	2.5 V		12mA...auto			
Input_vector[0]	Input	PIN_38	3	B3_NO	PIN_38	2.5 V		12mA...auto			
Output_vector[0]	Output	PIN_50	3	B3_NO	PIN_50	2.5 V		12mA...auto	2 (default)		

Filter: Pins: all

0% 00:00:00

## Manual verification using Xen-10 board:



# Lab journal:

EXPT. NO. NAME

Week 3: Fibonacci Detector

Page No.: YOUVA

Date: 25/08/2023

Number	$x_4$	$x_3$	$x_2$	$x_1$	$x_0$	y
0	0	0	0	0	0	1
1	0	0	0	0	1	1
2	0	0	0	1	0	1
3	0	0	0	1	1	1
4	0	0	1	0	0	0
5	0	0	1	0	1	1
6	0	0	1	1	0	0
7	0	0	1	1	1	0
8	0	1	0	0	0	1
9	0	1	0	0	1	0
10	0	1	0	1	0	0
11	0	1		1	1	0
12	0	1	1	0	0	0
13	0	1	1	0	1	1
21	1	0	1	1	1	1
31	1	0	1	1	1	0

Fibonacci numbers = 0, 1, 1, 2, 3, 5, 8, 13, 21, 34

$y = \bar{x}_4 \bar{x}_3 \bar{x}_2 \bar{x}_1 \bar{x}_0 + \bar{x}_4 \bar{x}_3 \bar{x}_2 \bar{x}_1 x_0$   
 $+ \bar{x}_4 \bar{x}_3 \bar{x}_2 x_1 \bar{x}_0 + x_4 x_3 x_2 x_1$

K-map

$x_4 = 0$

1	1	1	1
0	1	0	0
0	1	0	0
1	0	0	0

$x_4 = 1$

0	0	0	0
0	1	0	0
0	0	0	0
0	0	0	0

$x_4 \bar{x}_3 \bar{x}_2 \bar{x}_1 x_0$

Final:

$$y = \bar{x}_4 \bar{x}_3 \bar{x}_2 + \bar{x}_4 \bar{x}_2 \bar{x}_1 \bar{x}_0 + \bar{x}_3 x_2 \bar{x}_1 x_0 + \bar{x}_4 x_2 \bar{x}_1 x_0$$