v7.32.0.0
(Feb 1st, 2022)

IDesignSpec™ (IDS)

RTL Enhancements

1. F#16704 - Enhancement is done in case of low power coding style for the property "**rtl.write=swclear**". (More Details)
2. F#16456 - Support for "rc" and "rs" sw access with parity. (More Details)
3. F#17222 - Support of `default_nettype compiler directive in Verilog output. (More Details)
4. F#19389 - Support of repeated interface for a section in SV output. (More Details)

General Enhancements

1. F#16938 - Support for if_html with -if_html_section to generate hierarchical designs with respect to section/block/chip. (More Details)
2. F#18285 - Enhancement for the inconsistency in the struct naming hierarchy. (More Details)
3. B#1592 - Moved PER_INSTANCE_SIZE macro from top file to individual block file and renamed it based on the component name _SIZE in cheaderalt4. (More Details)
4. G#359 - Enhancement for the svgalt2 output

- Fixed box size of attributes
- Support for svgout for a single object

5. B#1593 - Support of a new property "**capi_add_name_prefix**" for appending a user given prefix in the IDS generated C APIs. (More Details).

6. F#19505 - Support for guard band in SVheader output using the new property "**headers_guard_band**".(More details)
7. F#16834 - Support for the property "**output_file_name"** in case of vheader output.

SystemRDL Enhancements

1. G#1259 - Support for dynamic assignment for ref instance. (More Details)

Bug Fixes

General

1. F#19353 - Fixed configuration file upload option in IDSCalc.
2. F#15941 - Fixed the issues of index value update in TOC according to configuration.
3. F#16948 - Fixed the generation of block-level HTML files with the switch '-if' or '-if_html' along with an appropriate warning that the switches would be ignored for block-level scenarios.
4. B#1591 - Fixed count macro to be moved to the component intermediate parent file.
5. F#12282 - Fixed STRIDE_SIZE macro to be moved to the component intermediate parent file.
6. B#1590 - Fixed the file generation issue in cheader alt4 when the same block has been referred multiple times.

1. F#18283 - Fixed the fillers when the stride is used on the chip component.

2. F#16542 - Fixed IP--XACT ports for vectors.
3. F#19555 - Fixed reset mask values in IP-XACT.
4. F#19713 - Fixed wrong address in ToC and on repeat table in htmlalt2.
5. F#16914 - Fixed reset configuration option and import configuration options have been enabled.
6. F#16403 - Fixed the description issue at signal node. The signal desc was not reflecting in ip-xact output so this issue has been fixed.
7. F#19447 - Fix for unsynthesizable FPGA clean up which was a showstopper

8. F#19528 - Error occurred in Annotation checks due to some incompatibility

RTL

1. F#17150 - Fixed the issue with the reserved fields in a reg with “rtl_hw_vector=true;” and “registered=false;” in verilog.
2. F#19405 - Fixed the issue with the "rtl.reg_enb" and "hw" access combinations in verilog.

3. F#17120 - Fixed the issue with parity_widget not getting generated with "-if" switch

4. F#19325 - Fixed the issue with property {reset_type=async} for block with APB bus
5. F#17120 - Fixed parity_error requirement for signals without read valid

6. F#17202- Fixed lint errors when using non-default reset signal.

7. F#19451 - Fixed the parity error generation issue.

UVM

1. F#17047 - Fix for inconsistency in case of hdl_path_slice on the field with hdl_path UDP in the 7.x.x.x series.

2. F#19518 - Fixes for hdl_path_gate on section with repeat.

IDS NextGen™ (IDS-NG)

Enhancements

1. G#442 - Support for copy and paste of one test case in another test case. (More Details)
2. G#675 - Support of lock feature for register and field in update param view. (More Details)

Bug Fixes

3. F#16533 - Fixed the issue of importing CSV files into IDSNG.
4. F#19394 - Fixed incorrect-sorting-of-bits-field-in-register-view in IDS-NG.
5. G#345 - Fixed the issue of Help-> Quick start takes you to a Page not found.
6. G#647 - Fixed issue of Missing File name label on Create IP has been fixed.
7. G#812 - Fixed issue of Incorrect sorting of bits in register field has been fixed.
8. G#867 - Fixed update param issue in case of yaml import or param added in the import file.
9. G#665 - Fixed csv output issue for ISS in IDS-NG.
10. G#553 - Fixed issue of sv configuration template by default - write_mirror (%a, %d, %m, %c)

SOC Enterprise™

Enhancements

1. SoC-E checks added:
   a. At different levels of hierarchy, a module output can connect to the parent's module output and not the parent's input port. (More Details)
   b. An input can be connected to only other inputs. This is true for the same or all levels of hierarchy. (More Details)
   c. Multiple drivers on a net (FAN-IN)/(FAN-OUT) Port, slice and bit wise. (More Details)