Release Notes
v7.28.0.0
(Dec 31st, 2021)

IDesignSpec™ (IDS)

RTL Enhancements

Verilog

1. F#17015 - Support for Synopsys directive "infer_multibit" for inferring multibit flops and latches. (More Details)

2. F#17120 - Support for removing the dependency of parity error calculation on '*_rd_valid'. (More Details)

3. F#16665 - Support of the **"rtl_error_enb_cntrl"** property through which a register bit or signal could enable or disable the error response in RTL. (More Details)

SystemVerilog

1. F#16943 - **Support of the** "svout_filename" **property to customize the name of the generated individual block-level file as well as the top chip file in a chip-level case.** (More Details)

UVM Enhancements

1. F#9590 - Support for setting the volatile bit to '1' in case of fields that have the property "singlepulse=true". (More Details)

2. F#17080 - Support for [#1] and [#2] in the hdl_path UDP for subblock and chip-in-chip flow. (More Details)

3. F#16821 - Support of virtual registers inside section in UVM. (More Details)

4. F#18288 - Support of "uvm.handle_name_format" property for fields. (More Details)

General Enhancements

1. F#16953 - Support for the chip inside chip for PDF-alt4 output. (More Details)

2. F#16738 - Support for the "stride" property with the chip in chip hierarchy for Headeralt4 output. (More Details)

3. F#16445 - Support for chip in chip for SVGalt2 output in IDSBatch. (More Details)

4. F#17101 - Enhancement in "cheader_add_regmap_offset" for the incorrect address calculation issue. (More Details)

1. F#16704 - **Support of custom checks through TCL for ensuring proper component names.** (More Details)

2. **B#1526 - Support of C Test for memories defined in the design using optimized header macros.** (More Details)

5. F#17096 - Support for the switch "-addr_sort_chip_block" which is to sort the blocks and chip components inside a register map. (More Details)

6. F#16206 - Support for "**verbose, log, cache_dir, queue_lic, and retry_time**" switches inside **set_config** API in TCL configuration. (More Details)

7. F#16948 - Support for the switches "-if" or " "-if_html" with "-if_html_section" which will generate multiple outputs with block elements as the top element for HTML-alt2 output. (More Details).

8. G#JAVA#385 - Support for system directory in TCL configuration in IDSWord. (More Details)

9. F#16577 - Support for the chip in chip hierarchy in IDSWord. (More Details)

10. F#16672 - Support for param in the description for documentation htmlalt2, pdf, markdown outputs. (More Details).

11. F#17217 - Support for is_rsv property for chip, block, and section component for htmlalt2 and pdfalt4. (More Details).

SystemRDL Enhancements

1. F#17016 - Support for the switch "-rdl_perl_no_verbose", which is used to remove the content of the "-verbose" data from the log file when the user will use the switch "-rdl_perl_debug". (More Details)

2. F#16476 - Support for one-time writable(RW1) register access. (More Details)

3. F#16892 - Support for w**arning addition on instantiating memories in SystemRDL without the keyword 'external' to update users on the external functionality of the instantiated memory.** (More Details)

4. F#16935 - **Support for the creation of multiple enum copies in SystemRDL output.** (More Details)

Bug Fixes

RTL

1. F#16990 - Fixes in annotation for usage of "**sv_interface=struct:bus_inf" and "sv_interface=struct:bus_struct" properties.**

2. F#16658 - Fix for **the "**single_address_data_out**" property with the module name in Verilog output.**

3. **F#15887 - Fix for extra always begin end and clock name issue in case of "**custom_sync=true**" property in Verilog output.**

4. F#16405 - Fix for the parameter duplicacy issue in case of enums when a file is referred in the top chip **in SV output**.

5. F#17209 - Fix for incorrect address calculation for block offset and register offset in case of "byte_addressing=false" **in Verilog output**.

6. F#17080 - Support of hdl_path with "registered=false" **in Verilog output**.

UVM

1. F#17047 - Fix in "hdl_path_slice" on the field for UDP "hdl_path".

2. F#16954 - Fixed issue with the backdoor path if the register is declared in 2-D array form.

General

1. F#17006 - Fixed the issue of macro redefinition when the same block is used in different chips in the case of chip in chip hierarchy in cheader output.
2. F#16953 - Fixed the link issue in PDF-alt4 output for chip inside chip hierarchy.
3. F#17066 - Fixed IP-XACT generation issue when resetsignal is used in the input.
4. F#16891 - Fix for modifying register "Description" field using TCL API in IDSWord.

ARV™

Enhancements

1. B#1578 - Support of virtual registers inside section in ARV. (More Details)

Specta-AV™

Bug Fixes

1. B#1579 - Fix for repeated registers while generating checkers for it.

SLIP-G™

Enhancements

1. **B#1234 - Addition of UART IP in the library of SLIP-G.** (More Details)

IDS NextGen™ (IDS-NG)

Enhancements

1. G#IDSNG#61 - Enhancement in the look and feel of spreadsheets along with the addition of **"insert a row above"** and **"insert column left"** options in the spreadsheet view. (More Details)

Bug Fixes

1. F#17049 - Fix for the **"Insert row below"** option in the register bit field.