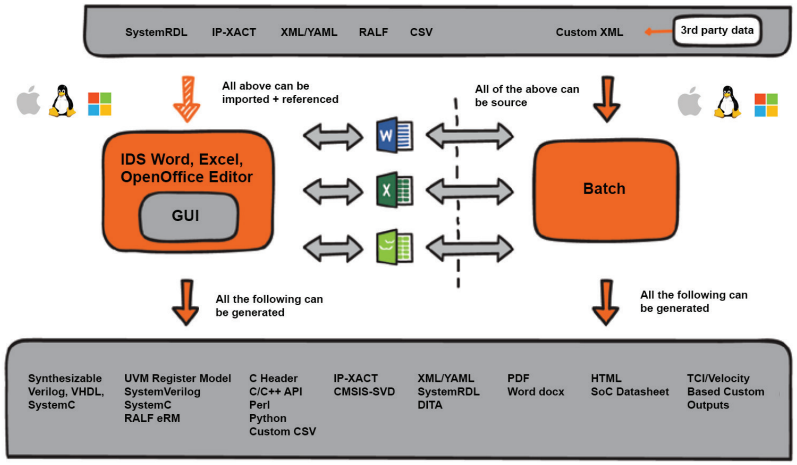
IDesignSpec™

AGNISYS
SYSTEM DEVELOPMENT WITH CERTAINTY

Centralized register design generation from golden specification



IDesignSpec helps IP/SoC design architects and engineers to address the needs of increased productivity, shorter development cycles and flexibility to create product variants by managing the hardware-software interface (HSI) specification effectively. In the complex designs of today, there is a need for interaction between system architects, software developers, hardware designers, system integrators and verification specialists. This has led to a need for developing the HSI specification at higher levels of abstraction to define the different types of registers, memory maps, which can automatically generate the desired code needed by the design teams.

Using IDesignSpec, design teams can develop the specification for the standard and special registers in MS Word, MS Excel, LibreOffice or text based industry standard formats such as SystemRDL, RALF or IP-XACT and generates synthesizable RTL, UVM model, C/C++ Headers, HTML or PDF.

Register design entry

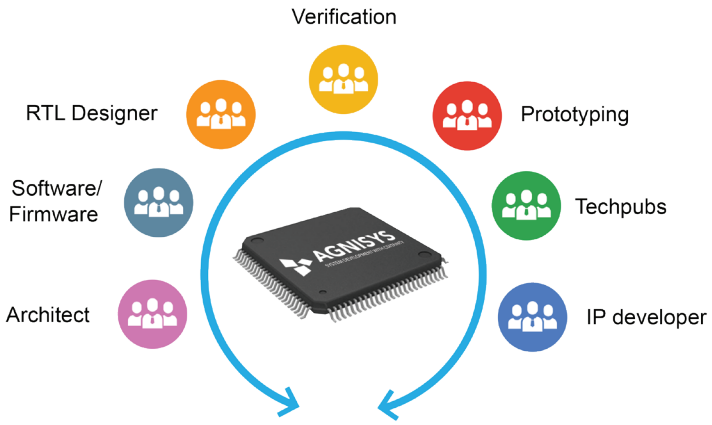
Architects and designers can quickly specify either simple or over 20 types of special registers using the user-friendly templates provided for MS Word, MS Excel, OpenOffice Calc or Adobe FrameMaker. Alternatively text based inputs such as System RDL, XML, IP-XACT can also be used. The registers can be created hierarchically as needed by the design teams.

Benefits:

- One golden specification for all teams
- Control changes to specification as they flow down to relevant design and verification elements
- Automatically generate desired models - UVM, Verilog/VHDL, coverage, software model etc.
- Correct by construction output for different teams
- Parameterized output code to maximize re-use
- Customize output code as needed; Specify properties for RTL, UVM and C code based on over 10k register behavior combinations
- Mitigate errors early in design cycle
- Shorter SoC/IP development cycles

Special registers

The UVM library includes examples of few commonly used special registers such as indirect, indexed, alias and RO/WO registers. But today's SoCs mandate more specialized register behavior to meet the various Hardware-Software interface requirements. IDesignSpec supports over 20 special registers including shadow, lock, trigger-buffer, interrupt, counter or external.



Output code generation

Based on the golden specification, the various members in the SoC team can use IDesignSpec via either the GUI or the command line to generate the desired code. The output code can be customized as needed to meet various requirements for RTL, C++ Classes, verification code and documentation by using the Velocity template and TCL API. The generated RTL Code (VHDL, Verilog, System Verilog or SystemC) for the registers is human-readable and embellished with easy-to-follow comments. The RTL also includes a bus slave and a decode logic specific to the bus protocol (AHB, APB, AXI, AXI-Lite, or proprietary), ensuring instant connection of the application logic with the register bus. The generated UVM register model includes register arrays, memories, indirect access registers, FIFO registers, coverage, constraints models and hdl_path.

Document generation

The customizable document generator can output file formats such as HTML, PDF, Custom PDF, .doc, .xls, DITA, IP-XACT, System RDL or ARM CMSIS.

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