Ver 7.2.0.0

v7.2.0.0

(October 03rd, 2020)

IDesignSpec (IDS)

RTL Enhancements:

- Read data construct has been enhanced with parameterization in verilog output. (More details)
- Bus error is now parameterized in verilog output. (More details)
- "rtl_busport_prefix" property has been supported in verilog output to prefix the names of all the bus ports with a string. (More details)
- "buffer_trig" property has been enhanced to take the value of a mask field. (More details)
- Tilelink aggregation logic has been supported in verilog output. (More details)
- "ext_signal = prot" property has been enhanced to route the protection checks written in external CSRs to the external interface through the widget's protection signal. (More details)
- "next="<fieldname>@incrsaturate/@decrsaturate/@incrthreshold/@decrthreshold"" property has been supported in verilog output. (More details)
- SECDED feature, which is Single Error Correction and Double Error Detection, is added to enhance functional safety capability of the tool. (More details)

SV Enhancements:

- "sv_interface=struct" has been enhanced with "rtl.reg_enb", "registered" and pulses properties. (More details)

General Enhancements:

- Supported **".\"** in configuration for output generated in current directory in IDS Word.
- Supported SystemRDL 2.0 outputs in IDS Word and IDS Excel.(More details)
- Supported QUESTA, XCELIUM, VIVADO, VCS in -tool command line option in IDS Batch.
- Supported node-locked license for flex licensing in IDS Batch.
- Enhancement in QUEUE implementation in flex to follow the true 'First In First Out' queue processing for queued license requests.

Bug Fixes:

RTL

- Fixed incorrect address width and formation of incorrect empty addresses when stride is used for verilog output.
- Naming convention of referred blocks is fixed when "vhdl.entity" property is used.
- "module_name" property is fixed for verilog output.
- Fixed "external_ack" property in case of external section for verilog output.
- amba3ahblte.v widget has been fixed to use hsel to qualify reads and writes.
- Hw driven interrupts are fixed when used along with "rtl.hw_enb = false" property.
- Read pulse is fixed with repeat for verilog output.

UVM

- Fixed extra "`endif" in case of coverage.per_instance.
- Fix done in case of parameter when different parameters are used in case of ref from different file.
- Fix done in interrupt with "rtl.hw_enb=false" property.
- Hdl paths are fixed in case of repeated sections inside the section.

Headers

- Fixed unexpected size of inserted filler within a container structure when the value of the address unit is taken other than its default value (i.e. 8) incase of header-alt1 output.
- Fixed filler names at board level hierarchy for header-alt1 output.
- Header-alt1 output is fixed for accepting different number formats for default values of registers/fields.
- Fixes done for indexes in case of repeat in svheader output.

General

- Fixes done in memory width (not in power of 2) while importing word (docx) file.

IDS NextGen™ (IDS-NG)

Enhancement:

- Supported SystemRDL alt1 and alt2 outputs. (More details)
- Supported inline enum declaration. (More details)

Bug Fixes:

- Fixed parsing issue in multiple reg group hierarchy template in IDSNG.

- Fixed fatal error issue while using multiple instances of IDSBatch.

SoC Enterprise (SoC-E™)

Enhancements:

- User defined base address and size have been supported for aggregation logic.
- SoC-E™ configuration setting for bus width and address unit have been supported.
- Read file has been supported through the search path in the read command.

ISequenceSpec™ (ISS)

Enhancements:

- Enums can now be passed as arguments of sequences. (More details)

SLIP-G™

Enhancements:

- Standard configuration APIs are now generated for the following IPs (More details):

  PIC, TIMER, GPIO, I2C

ASVV™

Enhancements:

ARV-METAL™

- Interrupts are now supported in bare-metal environment with SweRV (RISC-V) processor. (More details)

ARV-C™

- C-Tests have now been enhanced to handle interrupts.

Bug fixes:

ARV-Sim™

- Fix done for indirect Register by removing the redundant uvm code when UVM_NO_COVERAGE flag is high.

Specta-AV™

First version of Specta-AV is now available.

- Cross Coverage between multiple inline LUT’s are now supported. (More details)