Ver 7.4.0.0

v7.4.0.0

(November 30th, 2020)

IDesignSpec™ (IDS)

RTL Enhancements:

1. Depth of the memory or SystemRDL keyword "mementries" has been enhanced to accept parameterized values as well. (More Details)
2. Property 'counter.incr.val' or SystemRDL keyword "incrvalue", which specifies the value by which the counter is incremented, can now accept parameterized values. (More Details)

3. "rb_valid_stages" and "rb_data_stages" are now supported for AMBA3AHBLITE and APB Bus. (More Details)

4. Enhancement of "singlepulse" property for sw access "rw". (More Details)

UVM Enhancements:

1. Parameterized Constraints have been supported. (More Details)

2. UVM RAL Coverage model now works in case of registers with repeat. (More Details)

C Header Enhancements:

1. A new switch "arch_size" has been introduced to consider the software architecture size for accessing larger register definitions in an array of maximum architecture size. (More Details)

SystemRDL Enhancements:

1. Support for parameter overriding at section and register in verilog output. (More Details)

2. "%=" expression which specifies the alignment of the next address when instantiating a component has been supported at regfile/addrmap component as well. (More Details)

General Enhancements:

1. A new property "html_show_reserved_bits=true|bottom" is introduced to display the reserved bits of field in the generated HTML ALT2 output. (More Details)

2. Descriptions added on registers are now reflected in Python output.

3. "-cache_dir" has been supported to provide a path (absolute/relative) where '.ids' directory will be created. If this is not mentioned, then the '.ids' directory will be created at the default location. (More Details)

Bug Fixes:

RTL

1. Fix for incorrect offset derivation of an entity having parameterized repeat value.
2. Fix for system verilog structures (sv_interface="struct") when hardware read pulses ("rtl.hw_r1p" property) are used.
3. Fix for saturation of counters with "next" property for sw access "ro".
4. Following fixes has been done for stride in verilog output:
   a. Fix for stride at section and register to support parameters and complex expressions.
   b. Fix for stride at block level for verilog output.

UVM

1. Fix for top_property "auto_volatile=false" for volatile fields in third party output.

2. Fix for conditional statements in UVM output.

SystemRDL

1. Fix for the hang issue in the SystemRDL compiler when [i] (i.e., italic character) is used in the specification.

2. Fix for SystemRDL compiler in case a conditional statement (ternary operator) is used which contains output level parameters.

3. Change in behavior of register for a field with sw access = r and hw access = w according to SystemRDL 2.0 standard. Earlier, IDS used to create a flop but now there will be a wire/bus - hardware assignment. A warning has been added indicating the change.

4. Fix for removal of error messages from block in case of "errextbus" in SystemRDL compiler.

5. Changed the naming convention of register's class in UVM RAL output in case of definitive definition using RDL.

6. Fixed "ispresent" property issue with “doc_unused_remove” property in HTML/PDF output.

General

1. Fix issue for addresses in case of ref in IDSWord for IP-XACT input.

2. Fix for “dir_specific_out” for generated output in particular directory in HTML ALT2 output and ARV-Sim.

3. Fix for constraint in case of description property shown in HTML ALT2 output.

4. Fix for “**Data loss warning message”** issue in IDSBatch.

5. Fix for “stride” property for HTML ALT2, Verilog & C header output.

6. Fix “add_doc_above” property in HTML ALT2 output.

IDS NextGen™ (IDS-NG)

Enhancement:

- Sorting of templates is supported. (More Details)
- Japanese characters are supported in the specification. (More Details)

ASVV™

Enhancements:

ARV-Sim™

1. Deep hierarchy is supported for sections and “repeat” in ARV-Sim.

Note:

1. ‘wor’ has been removed in case of tilelink ports in verilog output.

2. ‘*prot_i’ wire has been removed from aggregation logic for AMBA buses.

3. `defines for variants will appear in the aggregation logic file.

4. Block offset will be addressed in following way so as to remove lint warning

    [addr_width-1 : 0] block_offset = {(addr_width){1'b0}};

Known Issues

- Limitations of “add_doc” and “add_doc_above” properties in HTML ALT2 output
    a. Bullet is not supported.
    b. Some special characters of MS Word are not supported (e.g., ‘ ’ “ ” – © ® ™ ≥ ≤ ±).
    c. Emf format image (MS-Word drawing image) is not supported.
- Limitations in Verilog output
    a. Addressing (select logic and invalid addresses) for MBD (Multiple Bus Domain)
    b. Repeat on block for proprietary bus
- In SystemRDL input, hierarchical parameter overriding for register and reg_file is supported for RTL but not yet supported for UVM.
- Currently working on to improve support of stride in C header files for more robust structure.
- In system verilog output, when input specification contains underscores in the component names, then use “-preserve” switch.