# Ver 7.0.0.0

## v7.0.0.0

*(September 05th, 2020)*

## IDesignSpec (IDS)

### RTL Enhancements:

- Widget property has been introduced for the generation of various bus widgets in the output. License update is required for accessing this feature. (More Details)
- Defines for synchronous and asynchronous behaviour in the widget has been replaced with parameter, based on reset_type property. (More Details)
- "Page_count" property has been parameterized for paged registers. (More Details)
- Separate page select registers for the hardware and software side have been supported. (More Details)
- AXI4LITE bus is now supported in VHDL. (More Details)
- Multiple bus domains are supported for AMBA3AHBLITE and TILELINK bus. (More Details)
- "rtl_hw_vector" property is now supported with: (More Details)

    a. All IDS supported hardware and software accesses,

    b. Properties related to pulses, and

    c. "registered = false" property.

### UVM Enhancements:

- Lock properties are now supported for repeated registers. (More Details)
- Multiple reset values of fields have been supported in case of repeated sections. (More Details)
- AXI4LITE and AXI4FULL buses are now supported for VHDL in ARV. (More Details)
- "uvm.regmodel=<string>" property is used in case of third party UVM environments. By default, the top register module name in ARV Environment is set to the top IDS generated module name. By using this property we can override it in case of third party environments. (More Details)

- Filelist has been supported in case of uvmtest in ARV.

## SV Enhancements:

- Structs are now supported for external sections. (More Details)
- "module_name" property has been enhanced in struct package generation for blocks with sv_interface. (More Details)

## SystemRDL Enhancements:

- Support for chip-inside-chip to enable deep hierarchy creation through "chip=true" property. (More Details)
- Multidimensional repeat is now supported in SystemRDL output. (More Details)
- type ="nomem" is supported in SystemRDL output. (More Details)
- Parameter overriding has been supported for output level parameters. (More Details)
- Various RTL and UVM properties have been supported at register-level in SystemRDL output. For e.g reset_type, reset_level, interrupt property etc.
- Multiple instances of reggroup present inside a block have been supported in UVM output while using SystemRDL input format.

## SVheader and Cheader Enhancements:

- 'Structure' template can now be used simultaneously at block and chip level. (More Details)
- Top_property "auto_volatile=true" has been supported for volatile fields in Cheader. (More Details)

## Multi-out ( -if ) Enhancements:

"-if" switch have been enhanced in the following scenarios and output:

- Alternate registers have been supported in UVM output. (More Details)
- "doc_unused_remove=true" being used as top property along with "is_rsv"/"is_present" property in case of multi-out (-if/-if_html) selected for HTML-ALT2 output.When the user uses the top property "doc_unused_remove=true", the component or instance on which "ispresent=false" or "is_rsv=true" has been applied, then that will be removed from the documentation. (More Details)
- Property "type=nomem" in UVM RAL has been supported". (More Details)
- Fixes done in naming convention of "uvm_mem" class for alternate registers in UVM output while using "-if" switch. (More Details)

## General Enhancements:

- "-dir_out_specific" command line switch has been enhanced for directing output in specific directories in case of ARV, VHeader and C_API output. (More Details)
- Support for FIFO based queuing in "Flex licensing" has been done. (More Details)
- Support description (doc) in Python output for reg, reggroup, block and chip.
- JSON output has been supported in IDS-BATCH. (More Details)

## Bug Fixes:

### RTL

- Fixes done for the file generation issue when the same block is referred multiple times inside a chip in VHDL output.
- Fixes done for the instance naming issue in VHDL with multi out. Now, all the files related to block (entity, architecture, package) will be named according to the name of the block. The name of the instances associated with the referred block will appear in the top chip package.
- Fixes done for the unused error signals for the memory template in VHDL output.
- Fixes done for signal inside struct when it has input signals but no input ports in System Verilog output.
- Fixes done for enums in case of repeat on field in Verilog output.
- Fixes done for variants if IDS properties are variant-dependent and top is a block in Verilog output.
- Fixes done for "ispresent/is_rsv=true/false" property when used with sw writable accesses in Verilog output.
- Fixes done for unassigned wire signals in repeated external memories with properties "addressing=regalign" and "addressing=fullalign" in Verilog output.

### UVM

- Fixes done for multiple instances of a register in different regfiles and blocks in UVM output.
- Fixes done for unique coverage name in case of repeat when block is referred from another file.

### SystemRDL

- Fixes done for SystemRDL UDP's type in SystemRDL output.
- Fixes done for SystemRDL property 'accesswidth' when register is referred from another file.

### Cheader

- Fixes done for multiple enum table generation in Cheader output.

### Documentation

- Fixes done for new-line character in register description for PDFalt2 output.
- Fixes done for absolute address in HTMLalt2 output for third party output.
- Fixes done for inconsistency issue in field table, CSS alignment, extra line break and font-style for HTMLalt2 output.

### General

- Fixes done for " 'h " for hexadecimal value in enum when generating XRSL output from IP-XACT.
- Fixes done for the issue with regfile instantiations through perl code.
- Fixes done for encoding issues and support German characters in IDSWord.
- Fixes done for variant issues with CSV input.
- JSON output has been supported in IDS-BATCH. (More Details)

## IDS NextGen™ (IDS-NG)

### Enhancement:

- Variants are now supported in IDS-NG. (More Details)
- JSON output has been supported in IDS-NG. (More Details)

## SoC Enterprise (SoC-E™)

## Enhancements:

- Support for IP-XACT output version 1.5 and 2014 in "generate" command:
  Syntax "generate -out <ipxact/ipxact1_5/ipxact2014> -dir <out-dir>
  ***Note :*** *By default, IP-XACT will be generated as "ipxact2014" version*
- Support for user defined prefixes in the names of bus interface connections:
  Syntax "connect -source/-source_inst <source-name> -dest/dest_inst <dest-name> -bus <bus-nama> -[source_prefix <source-prefix-name>] [dest_prefix <dest-prefix-name> ]
- Support for bus direction type (master/slave) for creating or adding a bus:
  Syntax "create -type <type> -name <instance-name> [-top] -bus <bus-name> -bus_type <master/slave>.
- Supported IP-XACT as an input IP.
- Supported IP-XACT design which has bus interfaces, ad-hoc connectivity and components as well.