Release Notes
v7.20.0.0
(Aug 27th, 2021)

IDesignSpec™ (IDS)

RTL Enhancements

1. B#1194 - **"cdc.clock=<clockname>:handshake"** property has been supported in VHDL output.(More Details)
2. F#16145 - **"rtl.hw_enb=false"** and **"hard_reset=false"** with **"cdc.clock"** has been supported for verilog output.(More Details)
3. B#1403 - Addition of error messages in counters when property is applied on the register.

Bug Fixes

RTL

1. F#16157 - Fix for floating rd_valid/wr_valid issue while creating double-buffered register in verilog output.
2. B#1414 - Fix for redundant "regname>_<fldname>_in_enb" port when **"rtl.hw_vector=true"** property is used while generating verilog output.
3. B#1416 - Fix for signal width calculation when page register is used in specification while generating verilog output.
4. F#15868 - Fix for the incorrect use of iterator in case of multi reset in verilog output.
5. F#15969 - Fix for unused port, "<regname>_<fldname>_in", when vectored hardware ports are used in verilog output.

UVM

1. B#1212 - Fix for HDL path of repeated blocks.

2. B#857 - Fix for repeated sample function in the same class in case of coverage on external components.

3. F#16282 - Fix for the issue in filename with parameterized addrmap when **"inst_name_cppstyle=true"** property is used.

4. F#16185 - Fix for undefined class during dynamic assignment when **"module_name"** property is applied at the block level.

5. F#15238 - Fix for naming conventions issue at block and chip level class with **"inst_name_cppstyle=true"**.

6. F#15135 - Fix for incorrect class name when multiple sections with same instance names are defined inside different sections.

7. F#15137 - Fix for HDL path of repeated sections when **"explicit_name=true"** property is used.

8. B#1415 - Fix for incorrect generation of 'foreach' loop when alias registers are defined inside sections.

Header

1. F#15888 - Fix for the incorrect value of fillers in headeralt2 output in case of stride.

2. B#1359 - Fix for enum names when block level enums are present in SVHeader output.

3. F#15249 - Fix for the naming convention of structs when **"inst_name_cppstyle"** is used in the specification to generate optimized header output.

4. F#15275 - Fix for removing the inclusion of *_address.h file from the top level header file in optimized header output.

5. F#15275 - Fix for the *_offset macros in the *_address.h file in optimized header output.

IP-XACT

1. F#16110 - Fix for width of virtual registers in UVM RAL output when IP-XACT is taken as input format.

2. F#16093 - Fix for constraints when enums are used inside the alternate registers in UVM RAL output when IP-XACT is taken as input format.

3. F#16092 - Fix for removing the alternate registers from IP-XACT when **"ipxact_rm_alt_reg=true"** UDP is used on the top component.

General

1. F#16118 - Fix for removing annotation for virtual register inside section for pdfalt2 output.

ISequenceSpec™ (ISS)

Enhancements

1. B#1386 - Read-Modify-Write has been supported in iss_firmware output. (More Details)

Bug Fixes

1. B#1411 - Fix for the assignment of iterator in while loop in iss_firmware output.

2. B#1412 - Fix for enum assignment when the same mnemonic is used in different enums in iss_firmware and iss_sv output.

3. B#1406 - Fix for non-dependency of data types in firmware api file(*_api.h) on -c_type or -c_type_std "gcc" switch.

4. B#1406 - Fix for read/write on the user defined struct in iss_firmware when the entire struct is written to a register.

5. B#1406 - Fix for the assignments of user defined struct members or the whole struct to a variable in iss_firmware.

ARV™

Bug Fixes

1. B#1212 - Fix in HDL path for memory.
2. B#1385 - Fix in external dummy memory issue with Tilelink/AXI4FULL bus.
3. B#1346 - Fix for repeat in case of external register.
4. B#1346 - Fix in the sequences for repeated registers with sw access as either ro or wo.

Specta-AV™

Enhancements

1. B#1363 - Support for constants and complex expressions in checkers. (More Details)

Bug Fixes

1. B#1363 - Fix for the naming issue in the absence of the "-preserve" option in checkers.
2. B#1369 - Fix for mismatch of "addr_width" issue in case of VHDL in top.sv file.
3. B#1403 - Fix for improved error messages in checkers when invalid input is fed to the checkers.
4. B#1191 - Fix in spectaavbatch for Specta-AV™ output generation.

ASVV™

Enhancements

1. B#1360 - Support for individual error count for each generated standard tests along with interactive error report generation on running standard/custom tests.

Bug Fixes

1. B#1408 - Fix for addresses in top wrapper aggregator when repeated blocks are taken inside chip.
2. B#1409 - Fix for custom tests, captured using ISequenceSpec™, when run in the ASVV™ environment.
3. B#1410 - Fix for naming issues in standard tests of shadow register.

IDS NextGen™ (IDS-NG)

Enhancements

1. G#IDSNG#45 - Support for **"intr.irq_per_channel"** property in event view.(More Details)
2. G#IDSNG#44 - Support for Assertions in Hierarchy view.(More Details)
3. G#IDSNG#48 - Support for Events in Hierarchy view.(More Details)
4. G#IDSNG#71 - Support for hierarchy level and property based hinting in checker view.(More Details)