Release Notes
v7.22.0.0
(Sep 29th, 2021)

IDesignSpec™ (IDS)

UVM Enhancements

1. B#1433 - The hardware events counter is supported in UVM RAL. (More Details)
2. B#1441 - Hardware monitor is now supported for interrupts in UVM. (More Details)
3. F#15680 - Enhancement has been done for the HDL path in case of **"registered=false"** and **"external"** by using the command line switch "**-hdlpath_all**". (More Details)

SystemRDL Enhancement

1. F#16205 - Enhancement has been done for UVM and C-Header output for getting user-defined names when **"inst_name"** property is used. (More Details)

HTML-alt2 Enhancement

1. F#16242 - Support of new property **"doc.rm_define=1"** to remove parameters in the generated htmlalt2 output.

Bug Fixes

RTL

1. F#16409 - Fix in chip-in-chip flow for **"hierarchical_decode"** with multicast/broadcast feature.
2. F#16409 - Fix in the **"output_file_name"** property when used along with the **"module_name"** property to generate an output file with a custom name.
3. F#16222 - Fix for null pointer issue in case of chip-in-chip scenario with Tilelink bus.
4. F#15962 - Fix in **"we"** property when the top element is a chip.

5. B#1452 - Fix in signal bits select with **"counter.hw.enb"** property for verilog output.

6. F#16104 - Fix for linting issues like, ExplicitRadix, LhsGreaterThanRhs, MultAsgnInSameScope, ReducntionOpTo1Bit, SigAsgnButNoRef, SignedUnsignedExpr and VectorParam as reported by Spyglass for verilog output.

7. F#16162 - Fix for <regname>_<fldname>_in_enb signal when register is write-only from hardware and read-only from software for Verilog2001 output.

UVM

1. F#16513 - Fix in **"uvm.reg_access"** property with multiple bus domains.

2. F#16319 - Fix for the generation issue of large values in constraint, i.e., *{constraint=value=[1:4294967295]}*.

3. F#15962- Fix for the missing lock callback classes with **"uvm_class_name_inst"**.

4. B#1436 - Fix in callback naming issue in case of **"counter.sw.wr"** and **"counter.sw.rd"** property.

5. B#1480 - Fix in individually_accessible bit of field in case of ARV™/Specta-AV™.

6. B#1455 - Fix for the callback naming issue in case of status, and enable registers.

7. F#15868 - Fix for the duplication of hdl_path code in the generated RAL when "**hdl_path_gate**" and "**hdl_path"** properties are used.

8. B#1483 - Fix for the missing end function in case of deep hierarchy of chip-in-chip scenario.

9. F#16135 - Fix for incorrect class name when multiple registers with same instance names are defined inside different sections.

SystemRDL

1. Following fixes are done when "**inst_name_cppstyle=true**" property is used in the input specification:
   a. F#16352 - Fix for naming convention of UVM generated file and its class name when string parameters are used in addrmap.
   b. F#16346 - Fix in optimized C-header output for regfile struct/union name.

c. F#16348 - Fix in optimized C-header output to generate the file with the referred file name instead of the instance block name.
d. F#16282 - Fix in optimized C-header and UVM outputs for issue in the filename with parameterized addrmap in chip level hierarchy.
e. B#1485 - Fix for removing ` from the parameter's name for UVM and optimized C-header output.
f. F#16369 - Fix for UVM and optimized C-header when special characters are used in parameters as a part of mathematical expression.

IP-XACT

1. F#16268 - Fix for overriding of the "version" node in the generated IP-XACT by using version UDP at the top component.

2. F#16403: Fix for port direction of signals in IP-XACT output.

3. F#16215: Re-ordered the position of <ipxact:enumeratedValues> and <ipxact:modifiedWriteValue> nodes for successful validation of IP-XACT file.

General

1. F#16146 - Fix in the generated Python APIs when registers with identical names are used in different sections of the registermap.

2. F#16118 - Fix in address for virtual register when referred inside a section.

3. F#16424 - Fix for naming in UVM classes and structs/unions in C-header outputs when dynamic assignment of reset is used.

4. B#1446 - Fix for Chinese and Japanese characters missing in PDF-alt4 output.

5. F#16223 - Fix in internal_toc description with multiout generation for htmlalt2 output.

6. F#15771 - Fix in property **"html_show_reserved_bits=true"** to show unused bits in fields in htmlalt2 output.

7. F#16298 - Fix in ToC addressing in word documentation output when generated with different address units.

8. F#16403 - Fix in the declaration of signal 'port type' in the generated pdfalt2 output.

ISequenceSpec™ (ISS)

Enhancements

1. B#1424 - Support for register struct inside a user-defined struct in C-header and firmware output. (More Details)
2. B#1424/B#1458 - Support for initialization of user-defined struct in firmware and UVM output. (More Details)
3. F#16355 - Support for const keyword in arguments in structs. (More Details)
4. F#16360 - Support for the inclusion of header files in firmware sequence file(.c).

Bug Fixes

1. B#1068 - Fix for non-generation of sequence outputs when the same sequence is called twice.
2. B#1079 - Fix in the graph alignment issue of flowchart output.
3. F#16154 - Fix in ISS flowchart output when generated with multiple arguments and constants in the sequence view.

ARV™

Bug Fixes

1. B#1273 - Fix for Riviera-Pro makefile for GUI mode.

Specta-AV™

Enhancements

1. B#1405 - Support for RAL value assignment in variables for checkers. (More Details)

2. B#1405 - Support for description of variables, constants, and checks. (More Details)
3. B#1273 - Support for Riviera-Pro simulator in Specta-AV™. (More Details)
4. B#1438 - Now bins range for coverage can be specified in tabular format as well as inline format. (More Details)

Bug Fixes

1. B#1273 - Fix in Makefile for Xcelium for GUI mode.
2. B#1273 - Fix in the result report of simulation in Makefile for Xcelium.
3. B#1454 - Fix in interrupt sequence with respect to hw interface.
4. B#1440 - Fix in signals assignment in tapper interface file.
5. B#1453 - Fix for the issue of tif/cif naming in checkers.

SLIP-G™

Enhancements

1. B#1287 - I2S IP is now available as a part of the standard library. (More Details)
2. B#1162 - Linked List has been supported in DMA. (More Details)

ASVV™

Enhancements

1. B#1390 - Support for an optimized header for running C-based tests in the generated environment. (More Details)

2. B#1481 - Support for removing dependency on forced offsets for design instantiation in the generated environment.

3. B#1389 - SweRV core update to the latest core version 1.9 in the generated environment.

4. B#1391 - Support for the LookUpTable based coverage. (More Details)

5. B#1443 - Support for ctests for shadow addresses in the specification. (More Details)

Bug Fixes

1. B#1443 - Fix for ctests generated for alias registers.

2. B#1482 - Fix for generating bins for all register accesses for improved coverage.

IDS NextGen™ (IDS-NG)

Enhancements

1. G#JAVA#336 **-** Support for sequence view in Specta-AV™. (More Details)

2. G#IDSNG#47 - Support for ASVV™ outline. (More Details)

3. G#IDSNG#25 - Support for the GUI option to generate ASVV™ environment files as part of 'Advance Validation' in the configuration window. (More Details)

4. G#IDSNG#331 - Support for project-based configuration. (More Details)

5. G#IDSNG#334 - Support for GUI checker configuration in the checker template. (More Details)

6. G#IDSNG#361 - Support for GUI option to Specta av output as part of 'Advance Verification' in the configuration window. (More Details)

7. G#IDSNG#442 - Support for inline enum in Reg view in the signal table.

Bug Fixes

1. G#Java#339 - Fix for incorrect block size in generated output through IDS-NG input file.
2. F#16065 - Fix for validation error in multiple sequences for IDS-NG input file.
3. F#15959 - Fix in description content in IDS-NG when excel file is imported.