Ver 6.46.0.0

v6.46.0.0

(November 30th, 2020)

IDesignSpec™ (IDS)

RTL Enhancements:

1. Paged registers have been made to work across the blocks. (More Details)

2. Following enhancements are done for "widget" property (More Details):
   a. Macros are replaced with parameters in the generated widgets.
   b. Single widget file will be generated with a customized name in the output directory for specified flavor in the widget property.

3. "cdc.clock" property has been enhanced to work with the "buffer_trig" property. (More Details)

4. "rb_valid_stages" and "rb_data_stages" are now supported for AMBA3AHBLITE and APB Bus. (More Details)

5. Enhancement of "singlepulse" property for sw access "rw". (More Details)

C Header Enhancements:

1. A new switch "arch_size" has been introduced to consider the software architecture size for accessing larger register definitions in an array of maximum architecture size. (More Details)

SystemRDL Enhancements:

1. Enhanced address sorting of IP-XACT file when referred to from a System-RDL input file.

2. Supported dynamic array assignment in C Header and HTML output. (More Details)

3. "%=" expression which specifies the alignment of the next address when instantiating a component has been supported at regfile/addrmap component as well. (More Details)

General Enhancements:

1. Descriptions added on registers are now reflected in Python output.

2. "-cache_dir" has been supported to provide a path (absolute/relative) where '.ids' directory will be created. If this is not mentioned, then the '.ids' directory will be created at the default location. (More Details)

Bug Fixes:

RTL

1. Fix for system verilog structures (sv_interface="struct") when hardware read pulses ("rtl.hw_r1p" property) are used.
2. Fix for localparam issue in dynamic array support for verilog output.
3. Fix for usage of *_write_error and *_error_wire signals which were declared but not used in verilog output.
4. Fix for the generation process of the "external_ack.v" module.
5. Fix for "rd_wait" logic in case of a flopped APB widget when "widget" property is applied on block.
6. Fix for linting issue in case of repeated registers with at least one of the fields being unregistered and "rw" sw access.
7. Fix for "sv_interface=struct" property for external regfiles.

UVM

1. Following fixes are done for hdl paths:
    a. Fix for "hdl_path_internal" property when applied on block and section simultaneously along with "-hdlpath" switch.
    b. Fix for "hdl_path" property or "-hdlpath" switch when applied on section.
    c. Fix for "hdl_path" property (on register) when "hdl_path_internal" property is applied on section/block in UVM RAL output.

2. Fix for incorrect package name when "-vertical_reuse" switch is used.

3. Fix for non-generation of structures in case of nested external regfile.

SystemRDL

1. Change in behavior of register for a field with sw access = r and hw access = w according to SystemRDL 2.0 standard. Earlier, IDS used to create a flop but now there will be a wire/bus - hardware assignment. A warning has been added indicating the change.

2. Fix for removal of error messages from block in case of "errextbus" in SystemRDL compiler.

3. Changed the naming convention of register's class in UVM RAL output in case of definitive definition using RDL.

4. Fixed "ispresent" property issue with "doc_unused_remove" property in HTML/PDF output.

General

1. Fixed issue for addresses in case of ref in IDSWord for IP-XACT input.
2. Fixed time consuming memory issues when a user has a large document/spec in IDSWord.
3. Fix for multiple IDSBatch runs simultaneously
4. Fix for '**Data loss warning message'** issue in IDSBatch.
5. Fix for embedded perl issue in case of 'ro' permission on the source directory.

IDS NextGen™ (IDS-NG)

Enhancement:

- Sorting of templates is supported. (More Details)
- Japanese characters are supported in the specification. (More Details)

Known Issues

- "resetsignal" works with hw pulses with "-fast" switch but not otherwise.
- "out_enb_stages" with "repeat" is correct with "-fast" switch.
- Read error is not being generated for 'w1' access.
- Combination of backslash and asterisk (*) when used in the description of any element (chip/block/section/register/field) in input specification for the resultant python output is not supported.