Release Notes
v7.24.0.0
(Nov 2nd, 2021)

IDesignSpec™ (IDS)

RTL Enhancements

1. F#16448 - Enhancement has been done for the command line option **"-filelist"** for System Verilog output, earlier it could be used only with **"sv_interface=struct"** property. (More Details)

2. F#16488 -**"-variant"** command line option has been enhanced for disabling the variant values, i.e., -variant !var1. (More Details)

3. F#16382 - Supported **"rsv_rd_val=true"** property for reading values of reserved fields present inside a register. (More Details)

4. F#16456 - Parity is now supported with reset, i.e., it will now depend upon the initial value of the data register and the type of parity. (More Details)

5. F#16580 - Read/write pulses are now supported for external registers. (More Details)

6. F#16608 - Parity error, in case of parity per byte, will be calculated continuously during run time, that is, dependency on "*_rd_valid" signal is removed. (More Details)

UVM Enhancements

1. B#1522 - Enhancement has been done for **"uvm.vreg_class"** and **"uvm.vreg_field_class"** properties to define custom classes for virtual registers. (More Details)

2. F#16178 - Supported **"uvm_add_regmap_offset"** property to change the offset of regmap generated with **"uvm_add_regmap"**. (More Details)

IP-XACT Enhancements

1. F#15599 - Enhancement has been done to support chip-in-chip flow in IP-XACT output. (More Details)

General Enhancements

1. F#16606 - Enhancement has been done for the support of '\n' character in the **"-copyright"** switch for the new line. (More Details)
2. F#16178 - Supported **"cheader_add_regmap_offset"** property for header-alt1 output with **"cheader_opt=true"** property to change the offset of regmap generated with **"cheader_add_regmap"**. (More Details)
3. F#15830 - **"not_generate"** property is enhanced for UVM and header-alt1 when used along with **"cheader_opt=true"** property to disable generation of chip/block components on which it is applied. (More Details)

Bug Fixes

RTL

1. F#16618 - Fix for incorrect generation of bus port (psel) name case in select logic for decode of blocks with hierarchical decode in the generated Verilog RTL.
2. B#1468 - Fix in **"undefined_rd_val=true"** property for undefined fields inside a register.
3. B#1450 - Fix in **"clock_enable=true"** with all SW accesses in Verilog output.
4. F#16213 - Fix for generation of parity logic, in Verilog, where dependency on "*in_enb" signal is removed when a field is read-only from SW and write-only from the hw side.
5. F#15787 - Fix for iterator name in case of multidimensional repeat of register inside repeated block in Verilog output.
6. B#1467 - Fix incorrect protection signal usage when "**field_prot**" property is used for the APB bus in Verilog output.
7. B#1443 - Fix in data-type mismatch on usage of lock value in read/write expression in generated Verilog RTL.

8. F#16253 - Fix in "**reset_type"** usage with widget instantiation in the RTL for AMBA-AHB bus.

9. F#15567 - Fixed bit-width mismatch lint warning in "amba_widget.sv" file.

UVM

1. B#1437 - Fix in illegal bins for w0t and w1t SW accesses.

2. F#16643 - Fix in UVM class naming when the name of the field starts with "_".

SystemRDL

F#16626 - Fix in the **"accesswidth"** UDP when IP-XACT file is referred as a block.

General

1. F#16553 - Fix done for the usage of the signal table inside a chip so that it gets reflected in both block and the chip.

2. F#16510 - Fix for reading the absolute and relative path from the "**ids_read**" command in Tcl file for the input file format.

3. F#16618 - Fix in incorrect usage of user defined data type on applying the switch "**-c_type"** in the generated C-API output.

4. F#16650 - Fix in C-API output for chip-in-chip flow to remove duplicate read and write functions.

5. F#16730 - Fix in fillers for header-alt2 in case of memory.

6. B#1521 - Fix for the incorrect filler size of block in case of deep hierarchy of chip-in-chip for header-alt1 with **"cheader_opt=true"** property.

7. F#16348 - Fix in the naming of struct when XML file is referred in an addrmap for header-alt1 with **"cheader_opt=true"** property.

8. F#16223 - Fixed the issue for language error in excel input for "**html_header**" property on linux idsbatch (excel template) for HTML-alt2 output.

9. F#16158- Fix in incorrect filler and address macro in case of stride in last container element in header-alt1 output.

10. F#16119 - Fix in optimized header and UVM output when a register or section is instantiated multiple times in different blocks.

11. F#16325 - Fix for non generation of optimized header output when stride is used along with count = 1 in input specification.

ISequenceSpec™ (ISS)

Enhancements

1. B#1460 - Support for read check in firmware and System Verilog output. (More Details)

2. B#1459 - Support for parameterization switch **-switch_intf** "INTF1=I2C,INTF2=SPI". (More Details)

ARV™

Bug Fixes

1. B#1518 - Fix in sequences for RO access register.

Specta-AV™

Enhancements

1. B#1259 - Support for annotation check messages in "assign-lib" for invalid inputs.

2. G#IDSNG#63 - Improvement in Specta-AV™ GUI structure in IDS-NG.

Bug Fixes

1. B#1517 - Fix in coverage collector for Xcelium simulator.

2. B#1519 - Fix for the task name in top.sv file in case of counters for chip level specification.

SLIP-G™

Enhancements

1. G#IDSNG#49 - Supported links for the datasheet of each individual IP.

2. G#IDSNG#41 - Supported in DMA configuration settings, drop-down menu instead of a textbox for *'MASTER_WRITE_BUS'* and '*MASTER_READ_BUS*'.

ASVV™

Enhancements

1. B#1392 - Support of interrupt-tests to validate interrupts in design. (More Details)

2. B#1395 - JTAG is supported for debugging at system level in the SweRV environment. (More Details)

Bug Fixes

1. B#1443- Fix in automatic tests for lock register in design.

2. B#1443- Fix in naming convention for alias register tests at deep hierarchy chip-in-chip level.

3. B#1523- Fix in naming inconsistency in the optimized header with **"cheader_opt=true"** property for their usage in automatically generated c-based tests at system level validation.

IDS NextGen™ (IDS-NG)

Enhancements

1. G#IDSNG#45 - Support for ChatBot in IDS-NG. (More Details)
2. G#IDSNG#57 - Support for hinting in assign value templates for sequence view.
3. G#IDSNG#53 - Support for struct template in IDS-NG. (More Details)
4. G#IDSNG#61 - Support for checker settings in configuration in IDS-NG. (More Details)
5. G#IDSNG#72 - Enhancement has been done to improve the look and feel of the IDS-NG GUI window. (More Details)

Bug Fixes

1. G#IDSNG#56 - Fixed tool crashes issue in case of not getting the closing bracket with eval keyword.
2. G#IDSNG#71 - Fixed IDS-NG file permission issue in linux OS.