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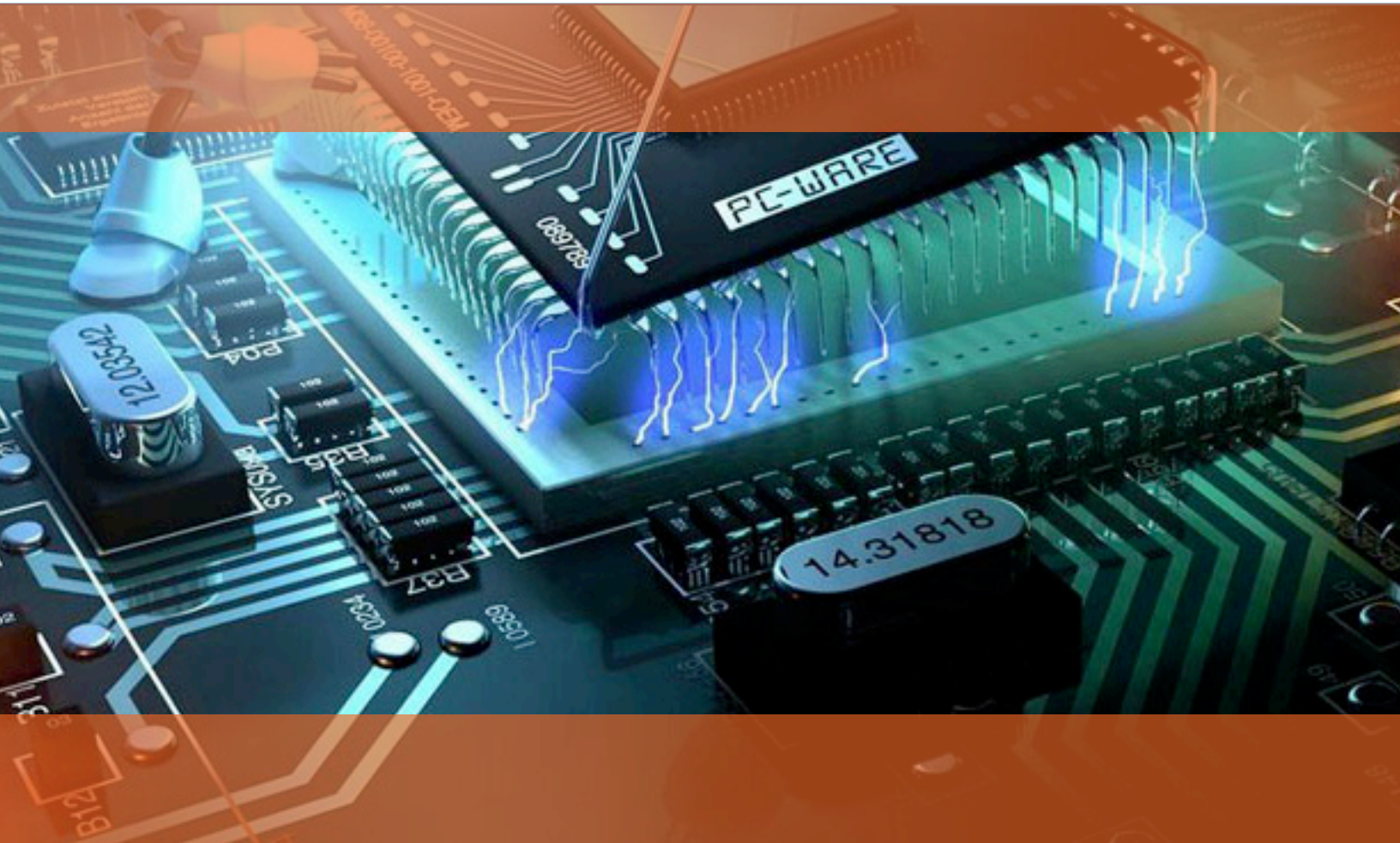
ACCELERATING DESIGN VERIFICATION

15 Benefits Of Working With Agnisys On Your Chip Design Project



The design of Semiconductors in electronic systems has become far more complex in recent years because of the increase in the number of transistors and the availability of Intellectual Property (IP) enabling design teams to implement solutions with much higher levels of integration than previously possible.

Designing these mammoth devices is only one part of the equation. These challenges amplify with each member of the product team. It is nearly impossible to keep the specification aligned with the design, ensuring that the verification of the design conforms to the specification versus real-world stimulus, that testing the device in the lab can be accomplished and finally documenting the device so customers can integrate them into their system. All of this is made much more difficult with the increase in design size and complexity.

Semiconductor engineering management and design team leaders face these challenges every single day. To reduce the risk of their chip design project, partners that provide tools, services and training for their team are highly valuable.

Semiconductor Design Challenges: Bugs are inevitable

One software study shows that during coding, designers inject approximately 1 defect for every 10 lines of code. The process of compiling, reviewing, analyzing, and testing the code reduces this rate. For typical new code that has been well tested, a remaining defect rate of six to seven defects per thousand lines of code (KLOC) is common. Consider a 50 million-gate semiconductor design. This corresponds to approximately 10 million lines of code. At .1 defects per KLOC, this means that the chip is likely to ship with 5000 defects.

Semiconductor Design Challenges: Getting the design right and verifying it

One of the biggest challenges in digital design today is achieving functional correctness. As designs become larger and more complex, the challenge of functional verification has become extremely difficult.

In particular, a number of new, sophisticated verification techniques have been added to the engineer's toolbox: constrained random testing, assertion-based testing, and formal verification. Unfortunately, these new techniques merely extend the previous trend in verification. We know that with more effort (and more sophisticated tools) we can find more bugs. But we have no useful model for how to find all of them.

Solution to Semiconductor Design Challenges:

1. Write less code by using more pre-verified IP blocks
2. Automate the connectivity (registers and memory maps) between the IP blocks, software and user designs

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3. Automate the testing with register and memory map generated UVM verification code to ensure the interfaces were implemented properly

Semiconductor Design Challenge: The learning curve for adopting UVM is steep

The current reference implementation of the UVM standard is in SystemVerilog language. SystemVerilog and UVM provide mechanisms to create company-wide consistency and reusable verification components for checking, coverage collection, and stimulus generation, and to modify the behavior of those components for specific tests. However, SystemVerilog and UVM provide more than this, so much more, in fact, that the learning curve can be discouraging for engineers.

Semiconductor Design Challenge: Sometimes you just don't have enough DV engineers to meet project deadlines

It is very common for project leads and engineering management to hire design verification engineering consultants to keep the DV portion of the project on track. The problem is finding well-trained engineers with the latest DV methodologies that most companies are using, System Verilog and UVM.

Solution to Semiconductor Design Challenges:

1. Hire a qualified training company to provide an on-site SV/UVM training class
2. Outsource parts of your DV project to a qualified service provider who has the tools, the team and the knowhow to implement high quality DV code. The typical portions of the DV projects that many companies outsource are:
    a. Development of the test bench environment
    b. Creation of the infrastructure for the test environment
    c. The tests themselves
    d. Coverage driven verification (aka metric driven verification)
    e. Integration of vendor tools to streamline verification

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In order to tame these challenges and implement these solutions, seek a trusted partner who has many years of experience in design, verification and training in semiconductor methodologies.

Agnisys Offers Product, Service and Training Solutions to Address Your Semiconductor Design Challenges

Agnisys is a focused company on the design and verification of advanced semiconductors. In order to be a full service provider we provide tools, services and training to help companies reduce the risk of their semiconductor design project while meeting their project schedule.

IDesignSpec™ is a software product that helps companies integrate IP, automate the connectivity (registers and memory maps between the IP blocks, software, and user design blocks), and automate the testing (with register and memory map generated UVM verification code to ensure the interfaces were implemented properly).

DVinsight™ is a software product that helps design verification engineers who are using System Verilog and the Universal Verification Methodology (UVM) libraries to create UVM code that is correct by construction because it checks for correctness during the code creation process. DVinsight gives the DV engineer helpful insight into their DV code and ensures compliance with industry best practices when using UVM while adhering to established UVM methods.

Agnisys Closure™ is a hardware verification service that provides turnkey semiconductor verification services or resources that augment your existing design verification team. Our unique set of techniques for managing projects ensure that there is clear visibility into the project and it will meet your semiconductor verification deadlines.

Agnisys SV/UVM Training Services is the leading provider of Design and Verification Training, offering a broad range of courses that may be customized to match the needs of your team. Our courses are available for on-site instruction. Our training services are more than just a dictated class, because our instructors are experienced design and verification engineers who strive to impart to the students the best real-world experiences they have learned during their many years of design and DV.

Agnisys works with your project lead and design management to customize offerings that help your team perform at their peak. We work with each customer to make sure our solutions; products, services and training, meet their specific needs. Our operating philosophy is to always be very easy to work with and conform to the client's needs. One example is that we offer free versions of our products that any engineer can request and receive without any level of bureaucracy.

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We follow these six operating principles:

1. All customers must be absolutely happy and we will not rest until they are
2. Users should not have to jump through any hoops in order to gain access to our products
3. We must always listen to customers to understand their needs
4. Keep our products and services as simple as possible like Einstein said, “everything should be made simple but not simpler” after all these are complicated semiconductor designs
5. Easy things should be simple and difficult things should be possible
6. All products should be very flexible and extensible to enable productive integration into any semiconductor design environment

If you would like to Reduce Bugs in your semiconductor project, verify that your design is correct, decrease the learning curve of your DV team, or increase your team’s bandwidth to ensure your project is done on time then reach out to Agnisys for help.

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1. One company that offers tools, training and services for design and verification of advanced semiconductors
2. IDesignSpec enables seamless integration of IP with direct reading of each IP's IP-XACT XML code
3. IDesignSpec automatically generates register and memory map code for your design team from a single source specification – as specification changes occur, new code is automatically regenerated
4. IDesignSpec automatically generates System Verilog UVM code to verify the registers and memory maps for the design and automatically generating tests to ensure the registers were implemented properly
5. IDesignSpec automatically generates the C-Header files for the software and firmware engineers to ensure their understanding of the interfaces is aligned with design and DV teams and consistency is maintained during and after specification changes occur
6. IDesignSpec automatically generates user documentation of the registers and memory maps in the design ensuring your customers have the right information to work with when integrating your chip into their system
7. DVinsight provides Design Verification engineers with a way to verify that they have not made any errors in their System Verilog UVM code – especially the type that are not caught by compilers
8. DVinsight is a light-weight and easy to use editor for your UVM code generation that benefits those engineers who are new to UVM or to catch errors for the expert significantly minimizing the coding defects per KLOC
9. Agnisys Closure can provide turn-key verification services for your design or serve as an overflow resource to your team
10. Agnisys SV/UVM Training Services can decrease the learning curve for engineers who are new to System Verilog or UVM
11. Agnisys SV/UVM Training Services team provides unique insights that are available only from designers with years of experience designing and verifying semiconductors.
12. Agnisys SV/UVM Training Services has delivered services to companies like Intel, Microsemi, Vitesse Semiconductor, Xilinx and more.
13. Agnisys provides free versions of all of its software products so that any engineer can try them, thus eliminating any semblance of bureaucracy.
14. Agnisys is eager to be the preferred partner for IP, SoC, ASIC or FPGA design teams.
15. Agnisys wants to make sure you are extremely happy with our products and services and we will not rest until you are.

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