Release Notes
v7.26.0.0
(Nov 30th, 2021)

IDesignSpec™ (IDS)

RTL Enhancements

1. F#15957 - "RO" access is now supported in the case of status registers and "r/w1c" or "w1c" for pending registers. (More Details)
2. F#16741 - Support for "**rtl_no_access_error=true"** property to remove register access-related errors from verilog output. (More Details)
3. B#1529 - Support for parameterization of AMBA3AHBlite bus widget. (More Details)
4. B#1529 - Support for parameterization of axi4full_dar bus widget. (More Details)

UVM Enhancements

1. F#15957 - Support for interrupts with repeat in UVM RAL. (More Details)

General Enhancements

1. G#JAVA#378: Support for multi-out (-if switch) for pdfalt4 output.
2. G#JAVA#376: Support for Python-API for custom generator of IDS.
3. G#JAVA#375: Support for SystemRDL alt1 and alt2 output in IDSExcel.
4. G#JAVA#262: Supported VHDL output in IDSBatch.
5. G#JAVA#370: Supported Svgalt2 output in IDSBatch. (More Details)

Bug Fixes

RTL

1. F#16767 - Fix in rtl.sw_write=clear in case of repeat.
2. B#805 - Fixes in the usage of property “registered=false” for cases where regwidth is greater than the used bus-width.
3. F#16704 Fixes in error reporting on the usage of unidentified lock value when lock property is applied on a register.
4. F#16781: Widget property has been updated with the latest flopped APB widget.
5. F#16658 - Fix for Verilog output when "single_address_data_out" property is used with 7x series.
6. F#16834 - Fix for vheader output for Vheader not getting generated in chip_in_chip flow when the topmost addrmap is defined as a chip by chip=true property.
7. F#16788 - Fix has been done for verilog output when rtl.hw_set is used with hw=na access.
8. F#16785 - Fix has been done for verilog output when parity=even property is used.

UVM

1. B#1549 - Fix for the issue with cg_addr when a block is referred multiple times in the same chip.
2. B#1549 - Fix the issue with cg_addr in case of the subblock.

General

1. F#16178 - Fix for implementing “uvm_add_regmap_offset” property for UVM and “cheader_add_regmap_offset” for headeralt4 to change the offset of regmap generated with “uvm_add_regmap” and “cheader_add_regmap” properties.
2. F#15830 - Fix for supporting “not_generate” for UVM and headeralt4 to disable generation of chip/block components on which it is applied.

3. F#16811: Fixed generation issue of cheader alt4 (cheader_opt=true) when the same chip is referred to in a chip multiple times in chip-in-chip hierarchy.

4. F#16844: Fix for wrong base address generation in the top address file in cheader alt4 output when the IPXACT file is referred to in the RDL file.

5. F#16948 - Fix for warning message addition on the usage of multi-out option at block level scenario for HTML outputs.

6. F#16450 - Fix for warning message addition when regfile instance is used inside the top chip.

7. F#16902 - Fix done in the python API when the object of a reg class is created.

8. F#16834 - Fix done in annotation for error messaging when error messaging didn't point out that field was missing when IDSExcel input case is used.

9. F#16682: Fixed empty "Property:'' banner even if using "-hide_pdf_prop all" in pdfalt4 output.

ARV™

Enhancements

1. B#1547 - Interrupt sequences are now supported with "repeat" in ARV. (More Details)

Bug Fixes

1. B#1548 - Repeat on register issue with RW and RO sequence.

2. B#1548 - Fix in Interrupt Sequence when the interrupt is present on a register.

3. F#16741 - Fix in the "uvm.handle_name_format" property when "%p" is present.

SLIP-G™

Enhancements

1. G#IDSNG#76: Support for UART IP in SLIP-G. (More Details)

Bug Fixes

1. B#1019 - Fix in verilog output for DMA slip-g for the issues in case of interrupt when using intr.enable and intr.status together.
2. F#16787: Fixed for Eval function in register properties.

iSpec.ai™

Enhancements

1. B#1527 - Improved AI engine for complex identification of System Verilog Assertions to English and vice-versa.

IDS NextGen™ (IDS-NG)

Enhancements

2. G#IDSNG#74: Support for ability to lock multiple fields in param view in IDSNG.
3. G#IDSNG#58: Support for changing the theme in IDS-NG GUI is now available. (More Details)

Bug Fixes

1. G#JAVA#374: Fixed issue of importing CSV file into IDSNG.