Release Notes
v7.14.0.0
(June 4th, 2021)
IDesignSpec™ (IDS)

RTL Enhancements
Verilog

1. "-reg_port_case" switch has been introduced for changing port and signal names to upper/lower case. (More Details)

2. Parity has been enhanced with "ecc_sniffer" to enable checking and generation of parity error periodically.

3. Read and write protection is supported for AMBA-AHB, AMBA-3AHBLite and APB bus. (More Details)

4. "counter.hw.enb" property has been supported with signal value.

5. "sv_interface=struct" has been enhanced for overriding block size using parameters. (More Details)

UVM Enhancements

1. "uvm_contxt" property has been introduced to override the values to be programmed to the field through the UVM factory using override by instance instead of override by type. (More Details)

2. "uvm.resetsignal=true" property has been introduced for generation of separate interface file for signal applied on reset value. (More Details)

C header Enhancements

1. "-c_type_std" switch has been introduced to change the data types as defined in the argument of the switch. (More Details)

SystemRDL

1. "ispresent" property has been enhanced to induce holes, i.e., empty spaces. (More Details)

Note:

a. Earlier, ispresent property was considered as a reserved component.

b. “doc_unused_remove” property has been deprecated in case of “ispresent= false”.

General Enhancements

1. Checker template is enhanced for addition of ‘assign’ table in IDSExcel.

2. Markdown output is enhanced with the following:(More Details)

    a. Definition of top level components (like system, board, chip, block & reg) can be displayed in text format using heading style.

    b. Description of components will be defined in a text format using heading style.

    c. Anchor links will be added in TOC. This link will redirect to its original definition.

3. Register group/Section is supported in CMSIS-SV output.

4. ‘eval()’ keyword has been enhanced for evaluation of a string at run time in the description of a field/register/section component in a register map. (More Details)

5. Alias registers can have lesser fields as compared to the primary registers while generating verilog and UVM output. (More Details)

6. Support for “ipxact_comp=board" and “ipxact_compact=true” IDS UDP at block level in IPXACT. (More Details)

Bug Fixes

RTL (Verilog)

1. Fix in “rtl_hw_vector” when used with “registered=false”.

2. Fix for sw write logic when “rtl.byte_enable=false” is used along with “hard_reset=false”.

3. Fix for syntactically incorrect instantiation of handshake widget when CDC is used from the software side.

4. Fix for missing conditional statement when parity inject error feature is used.

5. Fix for changing the localparam from unpacked type to packed type in case of dynamic array assignment.

6. Fix for naming of iterators in dynamic arrayed reset assignment.

7. Fix for XSLT failure issue in case of shadow register.

8. Fix for concatenation of comment line and normal line in case of "-no_lint_warn" switch along with unaligned offsets for external registers.
9. Fix for aligned and unaligned address calculation for external registers.
10. Fix for reset value of double buffer in case of "buffer_trig_reg" IDS UDP.
11. Fix for reducing the generation time when using "buffer_trig_reg" IDS UDP.

UVM

1. Fix for "lock" property callback in case of repeated section.
2. Fix for "alias" callback classes in case of "-vertical_reuse" switch.
3. Fix for parameter overriding when components are referred.
4. Fix in cross coverage without "-preserve" switch.
5. Fix in naming convention in case of multiple instances of the same block for chip-in-chip flow.

SystemRDL

1. Fix for compiler freeze on erroneous RDLFormatCode in SystemRDL input.
2. Fix for usage of parameters with external components.
3. Fix in dynamic reset assignment with following properties:

1. "tmr_error =true"
2. hdl_path

C Header

1. Fix in '<component_name>_size' macro when empty addresses are present at the end.
2. Fix for "cheadar.name_format" property when sections are used in the register map.

3. Fix for "warnings" issue in case of variant.
4. Fix for the underscore "_" in case of "cheader.name_format" property.
5. Fix for reset value in dynamic arrayed reset assignment.
6. Fix for wrong offset generation in case of "-addr_sort" switch.

General

1. Following fixes are done for HTML-alt2 output:
    a. Fix for different fonts in description.
    b. Fix for bold text issue in excel input file.
    c. Fix for support of internal table of content for block, section, and register template.
2. Following fixes are done for CMSIS-SVD output:
    a. Fix for incorrect values of "resetValue" and "resetMask" nodes.
    b. Fix in case of repeated registers.
3. Fix in "-log" switch for generating the right exit code.

ISequenceSpec™ (ISS)

Enhancements

1. Following enhancements have been made for UVM and firmware output :

    i) "for" loop has been supported in python input format. (More detail)
    ii) "foreach" loop has been supported. (More detail)
    iii) "break" and "continue" statements have been supported in python input format only. (More detail)

2. "return_type" property has been supported for firmware output. (More detail)

ARV™

Enhancements

1. "output_file_name" property has been supported.

Specta-AV™

Enhancements

1. Support for VIP integration in automatic verification. (More detail)
2. "add_vip" property has been introduced for the VIP integration to the slave interface which requires the name of VIP and vendor name separated by ":" as its value and this property is applicable only for the signals, e.g., {add_vip=AHB:Questa} (More detail)
3. "read_vip_xml" switch has been introduced to read the VIP XML format data file. (More detail)

Bug Fixes

1. Fix in coverage collector (Specta-AV) when signal table is used in the specification.
2. Fix in LUT for defining values with range in inline format.

ASVV™

Enhancements

1. Volatile hardware registers have been supported, i.e., now users can write through hardware using either interfaces or HDL paths. (More Details)

IDS NextGen™ (IDS-NG)

Enhancements:

1. Git integration has been improved with diffs and merges. (More Details)
2. Enum, define, param has been supported in sequence view.(More Details)
3. IDSNextGen is supported for macOS.

4. “assign” table is supported in the sequence view template.