4.3 Agnisys generated format Vs required format

The IP headers are generated using Agnisys tool. The following section shows the Agnisys generated structures and bit masks, and the format required by Innophase. Uart peripheral header is taken as an example in the Table 1.

Agnisys generated	Innophase requirement	Description
File name		
uart_apbw.2.2.9.h	inp_uart_ip.h	inp_<peripheral_name>_ip.h
Main Structure		
typedef struct { uartapbw_RBRTHR RBRTHR; hwint8 filler1[0x3]; uartapbw_IER IER; .... … } uartapbw_s;	typedef struct { __IOM uart_rbrthr_t RBRTHR; uint8_t filler1[0x3]; __IOM uart_ier_t IER; .... ….. } inp_uart_base_t;	Structure name: inp_<peripheral_name_in_small>_base_t Replace hwint8 with uint8_t
Register inside the main structure		
uartapbw_RBRTHR RBRTHR;	__IOM uart_rbrthr_t RBRTHR;	Here, #define __IOM volatile Structure name: <peripheral_name_in_small>_<register_name_in_small>_t <register_name_in_caps>;
Individual Register bit definitions		

typedef union {
struct {
hwint RBRTHR : 8;
} bf;
hwint b;
}uartapbw RBRTHR;
	typedef union {
	struct {
	uint32_t RBRTHR : 8;
	} bf;
	uint32_t b;
	}uart_rbrthr_t;
		Structure name in small.
		Bit fields in caps.
		Replace hwint with uint32_t
		Remove new lines in between

Macros		

#define uartapbw_RBRTHR_READMASK 0xFF	#define INP_UART_RBRTHR_READMASK (0xFF)	#define INP_<peripheral_name_in_caps>_<register_name_in_caps>_<macro_name_in_caps> (<value in hex>UL)
#define UART_APBW_REGISTERS_IER_ENRCVRLSI_OFFSET 2	#define INP_UART_REGISTERS_IER_ENRCVRLSI_Pos (0UL)	#define INP_<peripheral_name_in_caps>_REGISTERS_<register_name_in_caps>_<bitfield_name_in_caps>_Pos (<number_in_decimal>UL)
#define UART_APBW_REGISTERS_IER_ENRCVRLSI_MASK 0x4	#define INP_UART_REGISTERS_IER_ENRCVRLSI_Msk (0x4UL)	#define INP_<peripheral_name_in_caps>_REGISTERS_<register_name_in_caps>_<bitfield_name_in_caps>_Msk (<number_in_hex>UL)
define uartapbw_s_ADDRESS 0x00	#define INP_UART_ADDRESS (0x00UL)	All other macros in caps, prepend by INP_<peripheral_name_in_caps>_<macro_name_in_caps> (<value in hex>UL)
Comments		
No option for comments	Require comments explaining the register's purpose	Should be also to add comments to the main peripheral structure.
Has Agnisys header template	Option to add a proprietary copyright to file.	

Table 1: Agnisys Vs Required Format Comparison Table

The IP header file must have the following masks for bit manipulations. Except for these two macros, all the other macros should be in all CAPS.

#define INP_UART_REGISTERS_IER_ENRCVRLSI_Pos (0UL)

#define INP_UART_REGISTERS_IER_ENRCVRLSI_Msk (0xFUL)

The above two macros are used with **_VAL2FLD** and **_FLD2VAL** , which requires that format.

4.4 Doxygen style comments

If the Agnisys generated header file does not provide any option to add comments to registers, then the header file will not have any comments.