dwc_mipi_cdphy2_rx_2l2t_ns

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1.1.1.232	reg : CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE1_OVR_10	0x0000	0x120A	86
1.1.1.234	reg : CORE_DIG_IOCTRL_R_DPHY_PPI_LANE1_OVR_0	0x0000	0x1210	87
1.1.1.235	reg : CORE_DIG_IOCTRL_R_DPHY_PPI_LANE1_OVR_1	0x0000	0x1211	87
1.1.1.236	reg : CORE_DIG_IOCTRL_R_DPHY_PPI_LANE1_OVR_2	0x0000	0x1212	87

1.1.1.237	reg : CORE_DIG_IOCTRL_R_DPHY_PPI_LANE1_OVR_3	0x0000	0x1213	87
1.1.1.238	reg : CORE_DIG_IOCTRL_R_DPHY_PPI_LANE1_OVR_4	0x0000	0x1214	88
1.1.1.239	reg : CORE_DIG_IOCTRL_R_DPHY_PPI_LANE1_OVR_5	0x0000	0x1215	88
1.1.1.240	reg : CORE_DIG_IOCTRL_R_DPHY_PPI_LANE1_OVR_6	0x0000	0x1216	89
1.1.1.242	reg : CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_0	0x0000	0x1220	89
1.1.1.243	reg : CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_1	0x0000	0x1221	90
1.1.1.244	reg : CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_2	0x0000	0x1222	90
1.1.1.245	reg : CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_3	0x0000	0x1223	90
1.1.1.246	reg : CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_4	0x0000	0x1224	91
1.1.1.247	reg : CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_5	0x0000	0x1225	91
1.1.1.248	reg : CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_6	0x0000	0x1226	91
1.1.1.249	reg : CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_7	0x0000	0x1227	91
1.1.1.250	reg : CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_8	0x0000	0x1228	91
1.1.1.251	reg : CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_9	0x0000	0x1229	92
1.1.1.252	reg : CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_10	0x0000	0x122A	92
1.1.1.253	reg : CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_11	0x0000	0x122B	93
1.1.1.254	reg : CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_12	0x0000	0x122C	93
1.1.1.255	reg : CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_13	0x0000	0x122D	94
1.1.1.256	reg : CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_14	0x0000	0x122E	94
1.1.1.257	reg : CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_15	0x0000	0x122F	95
1.1.1.258	reg : CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_0	0x0000	0x1230	95
1.1.1.259	reg : CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_1	0x0000	0x1231	95
1.1.1.260	reg : CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_2	0x0000	0x1232	95

1.1.1.261	reg : CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_3	0x0000	0x1233	96
1.1.1.262	reg : CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_4	0x0000	0x1234	96
1.1.1.263	reg : CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_5	0x0000	0x1235	96
1.1.1.264	reg : CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_6	0x0000	0x1236	96
1.1.1.265	reg : CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_7	0x0000	0x1237	97
1.1.1.266	reg : CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_8	0x0000	0x1238	97
1.1.1.267	reg : CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_9	0x0000	0x1239	97
1.1.1.268	reg : CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_10	0x0000	0x123A	98
1.1.1.269	reg : CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_11	0x0000	0x123B	98
1.1.1.270	reg : CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_12	0x0000	0x123C	99
1.1.1.271	reg : CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_13	0x0000	0x123D	99
1.1.1.272	reg : CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_14	0x0000	0x123E	99
1.1.1.273	reg : CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_15	0x0000	0x123F	100
1.1.1.274	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_0	0x0000	0x1240	100
1.1.1.275	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_1	0x0000	0x1241	100
1.1.1.276	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_2	0x0000	0x1242	100
1.1.1.277	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_3	0x0110	0x1243	101
1.1.1.278	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_4	0x0000	0x1244	101
1.1.1.279	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_5	0x0000	0x1245	102
1.1.1.280	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_6	0x0000	0x1246	102
1.1.1.281	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_7	0x8000	0x1247	102
1.1.1.282	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_8	0x1C00	0x1248	102
1.1.1.283	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_9	0x1000	0x1249	103

1.1.1.284	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_10	0x02B8	0x124A	103
1.1.1.285	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_11	0x0000	0x124B	104
1.1.1.286	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_12	0x0000	0x124C	104
1.1.1.287	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_13	0x1000	0x124D	105
1.1.1.288	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_14	0x0000	0x124E	106
1.1.1.289	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_15	0x0000	0x124F	106
1.1.1.290	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_16	0x0004	0x1250	107
1.1.1.291	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_17	0x0000	0x1251	107
1.1.1.292	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_18	0x0000	0x1252	107
1.1.1.293	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_19	0x0000	0x1253	107
1.1.1.294	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_20	0x0000	0x1254	108
1.1.1.295	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_21	0x0000	0x1255	108
1.1.1.296	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_22	0x0000	0x1256	108
1.1.1.297	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_23	0x0000	0x1257	108
1.1.1.298	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_24	0x0000	0x1258	108
1.1.1.299	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_25	0x0000	0x1259	109
1.1.1.300	reg : CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_26	0x0000	0x125A	109
1.1.1.302	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_0	0x0000	0x1260	110
1.1.1.303	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_1	0x0000	0x1261	111
1.1.1.304	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_2	0x0000	0x1262	111
1.1.1.305	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_3	0x0000	0x1263	111
1.1.1.306	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_4	0x0000	0x1264	111
1.1.1.307	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_5	0x0000	0x1265	112

1.1.1.308	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_6	0x0000	0x1266	112
1.1.1.309	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_7	0x0000	0x1267	113
1.1.1.310	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_8	0x0000	0x1268	113
1.1.1.311	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_9	0x0000	0x1269	113
1.1.1.312	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_10	0x0000	0x126A	114
1.1.1.313	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_11	0x0000	0x126B	114
1.1.1.314	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_12	0x0000	0x126C	114
1.1.1.315	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_13	0x0000	0x126D	114
1.1.1.316	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_14	0x0000	0x126E	114
1.1.1.317	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_15	0x0000	0x126F	114
1.1.1.318	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_16	0x0000	0x1270	115
1.1.1.319	reg : CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_17	0x0000	0x1271	115
1.1.1.321	reg : CORE_DIG_RW_TRIO1_0	0x044A	0x1280	116
1.1.1.322	reg : CORE_DIG_RW_TRIO1_1	0x000A	0x1281	116
1.1.1.323	reg : CORE_DIG_RW_TRIO1_2	0x000A	0x1282	116
1.1.1.325	reg : CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_0	0x0000	0x1440	116
1.1.1.326	reg : CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_1	0x0000	0x1441	116
1.1.1.327	reg : CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_2	0x0000	0x1442	117
1.1.1.328	reg : CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_3	0x0110	0x1443	117
1.1.1.329	reg : CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_4	0x0000	0x1444	118
1.1.1.330	reg : CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_5	0x0000	0x1445	118
1.1.1.331	reg : CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_6	0x0000	0x1446	118
1.1.1.332	reg : CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_7	0x8000	0x1447	119
1.1.1.333	reg : CORE_DIG_IOCTRL_RW_AFE	0x1C00	0x1448	119

	_LANE2_CTRL_8			
1.1.1.334	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_9	0x1000	0x1449	119
1.1.1.335	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_10	0x02B8	0x144A	120
1.1.1.336	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_11	0x0000	0x144B	120
1.1.1.337	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_12	0x0000	0x144C	121
1.1.1.338	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_13	0x1000	0x144D	122
1.1.1.339	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_14	0x0000	0x144E	122
1.1.1.340	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_15	0x0000	0x144F	123
1.1.1.341	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_16	0x0004	0x1450	123
1.1.1.342	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_17	0x0000	0x1451	123
1.1.1.343	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_18	0x0000	0x1452	124
1.1.1.344	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_19	0x0000	0x1453	124
1.1.1.345	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_20	0x0000	0x1454	124
1.1.1.346	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_21	0x0000	0x1455	124
1.1.1.347	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_22	0x0000	0x1456	124
1.1.1.348	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_23	0x0000	0x1457	125
1.1.1.349	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_24	0x0000	0x1458	125
1.1.1.350	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_25	0x0000	0x1459	125
1.1.1.351	reg : CORE_DIG_IOCTRL_RW_AFE _LANE2_CTRL_26	0x0000	0x145A	126
1.1.1.353	reg : CORE_DIG_IOCTRL_R_AFE_ LANE2_CTRL_0	0x0000	0x1460	126
1.1.1.354	reg : CORE_DIG_IOCTRL_R_AFE_ LANE2_CTRL_1	0x0000	0x1461	127
1.1.1.355	reg : CORE_DIG_IOCTRL_R_AFE_ LANE2_CTRL_2	0x0000	0x1462	127
1.1.1.356	reg : CORE_DIG_IOCTRL_R_AFE_ LANE2_CTRL_3	0x0000	0x1463	127
1.1.1.357	reg : CORE_DIG_IOCTRL_R_AFE_	0x0000	0x1464	128

	LANE2_CTRL_4			
1.1.1.358	reg : CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_5	0x0000	0x1465	128
1.1.1.359	reg : CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_6	0x0000	0x1466	129
1.1.1.360	reg : CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_7	0x0000	0x1467	129
1.1.1.361	reg : CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_8	0x0000	0x1468	130
1.1.1.362	reg : CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_9	0x0000	0x1469	130
1.1.1.363	reg : CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_10	0x0000	0x146A	130
1.1.1.364	reg : CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_11	0x0000	0x146B	130
1.1.1.365	reg : CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_12	0x0000	0x146C	130
1.1.1.366	reg : CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_13	0x0000	0x146D	131
1.1.1.367	reg : CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_14	0x0000	0x146E	131
1.1.1.368	reg : CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_15	0x0000	0x146F	131
1.1.1.369	reg : CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_16	0x0000	0x1470	131
1.1.1.370	reg : CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_17	0x0000	0x1471	132
1.1.1.372	reg : CORE_DIG_IOCTRL_RW_DPHY_PPI_CLK_OVR_0	0x0000	0x1A00	132
1.1.1.373	reg : CORE_DIG_IOCTRL_RW_DPHY_PPI_CLK_OVR_1	0x0000	0x1A01	133
1.1.1.374	reg : CORE_DIG_IOCTRL_RW_DPHY_PPI_CLK_OVR_2	0x0000	0x1A02	133
1.1.1.375	reg : CORE_DIG_IOCTRL_R_DPHY_PPI_CLK_OVR_0	0x0000	0x1A03	133
1.1.1.376	reg : CORE_DIG_IOCTRL_R_DPHY_PPI_CLK_OVR_1	0x0000	0x1A04	134
1.1.1.378	reg : CORE_DIG_IOCTRL_RW_COMMON_PPI_OVR_0	0x0000	0x1C00	134
1.1.1.379	reg : CORE_DIG_IOCTRL_RW_COMMON_PPI_OVR_1	0x0000	0x1C01	135
1.1.1.380	reg : CORE_DIG_IOCTRL_RW_COMMON_PPI_OVR_2	0x0000	0x1C02	135
1.1.1.381	reg : CORE_DIG_IOCTRL_RW_COMMON_PPI_OVR_3	0x0000	0x1C03	135
1.1.1.382	reg : CORE_DIG_IOCTRL_RW_COM	0x0000	0x1C04	136

	MON_PPI_OVR_4			
1.1.1.383	reg : CORE_DIG_IOCTRL_RW_CON MON_PPI_OVR_5	0x0000	0x1C05	136
1.1.1.384	reg : CORE_DIG_IOCTRL_RW_CON MON_PPI_OVR_6	0x0000	0x1C06	136
1.1.1.385	reg : CORE_DIG_IOCTRL_RW_CON MON_PPI_OVR_7	0x0000	0x1C07	136
1.1.1.386	reg : CORE_DIG_IOCTRL_RW_CON MON_PPI_OVR_8	0x0000	0x1C08	136
1.1.1.387	reg : CORE_DIG_IOCTRL_RW_CON MON_PPI_OVR_9	0x0000	0x1C09	136
1.1.1.388	reg : CORE_DIG_IOCTRL_RW_CON MON_PPI_OVR_10	0x0000	0x1C0A	136
1.1.1.389	reg : CORE_DIG_IOCTRL_RW_CON MON_PPI_OVR_11	0x0000	0x1C0B	137
1.1.1.391	reg : CORE_DIG_IOCTRL_R_COMM ON_PPI_OVR_0	0x0000	0x1C10	137
1.1.1.392	reg : CORE_DIG_IOCTRL_R_COMM ON_PPI_OVR_1	0x0000	0x1C11	137
1.1.1.393	reg : CORE_DIG_IOCTRL_R_COMM ON_PPI_OVR_2	0x0000	0x1C12	137
1.1.1.394	reg : CORE_DIG_IOCTRL_R_COMM ON_PPI_OVR_3	0x0000	0x1C13	138
1.1.1.395	reg : CORE_DIG_IOCTRL_R_COMM ON_PPI_OVR_4	0x0000	0x1C14	138
1.1.1.396	reg : CORE_DIG_IOCTRL_R_COMM ON_PPI_OVR_5	0x0000	0x1C15	138
1.1.1.397	reg : CORE_DIG_IOCTRL_R_COMM ON_PPI_OVR_6	0x0000	0x1C16	138
1.1.1.398	reg : CORE_DIG_IOCTRL_R_COMM ON_PPI_OVR_7	0x0000	0x1C17	138
1.1.1.399	reg : CORE_DIG_IOCTRL_R_COMM ON_PPI_OVR_8	0x0000	0x1C18	138
1.1.1.400	reg : CORE_DIG_IOCTRL_R_COMM ON_PPI_OVR_9	0x0000	0x1C19	139
1.1.1.401	reg : CORE_DIG_IOCTRL_R_COMM ON_PPI_OVR_10	0x0000	0x1C1A	139
1.1.1.403	reg : CORE_DIG_IOCTRL_RW_AFE _CB_CTRL_0	0x0000	0x1C20	139
1.1.1.404	reg : CORE_DIG_IOCTRL_RW_AFE _CB_CTRL_1	0x0000	0x1C21	140
1.1.1.405	reg : CORE_DIG_IOCTRL_RW_AFE _CB_CTRL_2	0x0000	0x1C22	140
1.1.1.406	reg : CORE_DIG_IOCTRL_RW_AFE _CB_CTRL_3	0x40F6	0x1C23	141
1.1.1.407	reg : CORE_DIG_IOCTRL_RW_AFE	0x2292	0x1C24	141

	_CB_CTRL_4			
1.1.1.408	reg : CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_5	0x4100	0x1C25	141
1.1.1.409	reg : CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_6	0x0000	0x1C26	142
1.1.1.410	reg : CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_7	0x0000	0x1C27	142
1.1.1.411	reg : CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_8	0x0000	0x1C28	143
1.1.1.412	reg : CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_9	0x0000	0x1C29	143
1.1.1.413	reg : CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_10	0x0000	0x1C2A	143
1.1.1.414	reg : CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_11	0x0004	0x1C2B	144
1.1.1.416	reg : CORE_DIG_IOCTRL_R_AFE_CB_CTRL_0	0x0000	0x1C30	144
1.1.1.417	reg : CORE_DIG_IOCTRL_R_AFE_CB_CTRL_1	0x0000	0x1C31	145
1.1.1.418	reg : CORE_DIG_IOCTRL_R_AFE_CB_CTRL_2	0x0000	0x1C32	145
1.1.1.419	reg : CORE_DIG_IOCTRL_R_AFE_CB_CTRL_3	0x0000	0x1C33	145
1.1.1.420	reg : CORE_DIG_IOCTRL_R_AFE_CB_CTRL_4	0x0000	0x1C34	146
1.1.1.422	reg : CORE_DIG_RW_COMMON_0	0x0000	0x1C40	146
1.1.1.423	reg : CORE_DIG_RW_COMMON_1	0x0000	0x1C41	146
1.1.1.424	reg : CORE_DIG_RW_COMMON_2	0x0000	0x1C42	147
1.1.1.425	reg : CORE_DIG_RW_COMMON_3	0x0000	0x1C43	147
1.1.1.426	reg : CORE_DIG_RW_COMMON_4	0x0000	0x1C44	147
1.1.1.427	reg : CORE_DIG_RW_COMMON_5	0x0000	0x1C45	147
1.1.1.428	reg : CORE_DIG_RW_COMMON_6	0x0089	0x1C46	147
1.1.1.429	reg : CORE_DIG_RW_COMMON_7	0x0015	0x1C47	148
1.1.1.430	reg : CORE_DIG_RW_COMMON_8	0x0000	0x1C48	148
1.1.1.431	reg : CORE_DIG_RW_COMMON_9	0x00CC	0x1C49	148
1.1.1.432	reg : CORE_DIG_RW_COMMON_10	0x000F	0x1C4A	149
1.1.1.433	reg : CORE_DIG_RW_COMMON_11	0x0000	0x1C4B	149
1.1.1.434	reg : CORE_DIG_RW_COMMON_12	0x0015	0x1C4C	149
1.1.1.435	reg : CORE_DIG_RW_COMMON_13	0x0000	0x1C4D	149
1.1.1.436	reg : CORE_DIG_RW_COMMON_14	0x003F	0x1C4E	150

1.1.1.437	reg : CORE_DIG_RW_COMMON_15	0x0000	0x1C4F	150
1.1.1.439	reg : CORE_DIG_ANACTRL_RW_C MMON_ANACTRL_0	0x1B6D	0x1CF0	150
1.1.1.440	reg : CORE_DIG_ANACTRL_RW_C MMON_ANACTRL_1	0x009B	0x1CF1	151
1.1.1.441	reg : CORE_DIG_ANACTRL_RW_C MMON_ANACTRL_2	0x0444	0x1CF2	151
1.1.1.442	reg : CORE_DIG_ANACTRL_RW_C MMON_ANACTRL_3	0x0404	0x1CF3	151
1.1.1.444	reg : CORE_DIG_COMMON_RW_D KEW_FINE_MEM	0x0000	0x1FF0	151
1.1.1.445	reg : CORE_DIG_COMMON_R_DES EW_FINE_MEM	0x0000	0x1FF1	152
1.1.1.447	reg : PPI_RW_DPHY_LANE0_LBER T_0	0x0000	0x2000	152
1.1.1.448	reg : PPI_RW_DPHY_LANE0_LBER T_1	0x0000	0x2001	153
1.1.1.449	reg : PPI_R_DPHY_LANE0_LBERT _0	0x0001	0x2002	153
1.1.1.450	reg : PPI_R_DPHY_LANE0_LBERT _1	0x0000	0x2003	153
1.1.1.451	reg : PPI_RW_DPHY_LANE0_SPAR E	0x0000	0x2004	153
1.1.1.453	reg : PPI_RW_DPHY_LANE1_LBER T_0	0x0000	0x2200	153
1.1.1.454	reg : PPI_RW_DPHY_LANE1_LBER T_1	0x0000	0x2201	154
1.1.1.455	reg : PPI_R_DPHY_LANE1_LBERT _0	0x0001	0x2202	154
1.1.1.456	reg : PPI_R_DPHY_LANE1_LBERT _1	0x0000	0x2203	154
1.1.1.457	reg : PPI_RW_DPHY_LANE1_SPAR E	0x0000	0x2204	155
1.1.1.459	reg : CORE_DIG_DLANE_0_RW_CF G_0	0x0000	0x3000	155
1.1.1.460	reg : CORE_DIG_DLANE_0_RW_CF G_1	0x0000	0x3001	155
1.1.1.461	reg : CORE_DIG_DLANE_0_RW_CF G_2	0x0000	0x3002	155
1.1.1.463	reg : CORE_DIG_DLANE_0_RW_LF _0	0x463C	0x3040	155
1.1.1.464	reg : CORE_DIG_DLANE_0_RW_LF _1	0x8010	0x3041	156
1.1.1.465	reg : CORE_DIG_DLANE_0_RW_LF _2	0x0001	0x3042	156

1.1.1.467	reg : CORE_DIG_DLANE_0_R_LP_0	0x0000	0x3050	156
1.1.1.468	reg : CORE_DIG_DLANE_0_R_LP_1	0x0000	0x3051	156
1.1.1.470	reg : CORE_DIG_DLANE_0_R_HS_TX_0	0x0000	0x3070	157
1.1.1.472	reg : CORE_DIG_DLANE_0_RW_HS_RX_0	0x091D	0x3080	157
1.1.1.473	reg : CORE_DIG_DLANE_0_RW_HS_RX_1	0x4010	0x3081	157
1.1.1.474	reg : CORE_DIG_DLANE_0_RW_HS_RX_2	0x169B	0x3082	157
1.1.1.475	reg : CORE_DIG_DLANE_0_RW_HS_RX_3	0x2412	0x3083	158
1.1.1.476	reg : CORE_DIG_DLANE_0_RW_HS_RX_4	0x0096	0x3084	158
1.1.1.477	reg : CORE_DIG_DLANE_0_RW_HS_RX_5	0x0000	0x3085	158
1.1.1.478	reg : CORE_DIG_DLANE_0_RW_HS_RX_6	0x002D	0x3086	158
1.1.1.479	reg : CORE_DIG_DLANE_0_RW_HS_RX_7	0x3B06	0x3087	158
1.1.1.480	reg : CORE_DIG_DLANE_0_RW_HS_RX_8	0x0000	0x3088	159
1.1.1.481	reg : CORE_DIG_DLANE_0_RW_HS_RX_9	0x00FF	0x3089	159
1.1.1.482	reg : CORE_DIG_DLANE_0_RW_HS_RX_10	0x0001	0x308A	159
1.1.1.483	reg : CORE_DIG_DLANE_0_RW_HS_RX_11	0x0002	0x308B	160
1.1.1.484	reg : CORE_DIG_DLANE_0_RW_HS_RX_12	0x0003	0x308C	160
1.1.1.486	reg : CORE_DIG_DLANE_0_R_HS_RX_0	0x0000	0x3090	160
1.1.1.487	reg : CORE_DIG_DLANE_0_R_HS_RX_1	0x0000	0x3091	160
1.1.1.488	reg : CORE_DIG_DLANE_0_R_HS_RX_2	0x00A0	0x3092	160
1.1.1.489	reg : CORE_DIG_DLANE_0_R_HS_RX_3	0x0000	0x3093	161
1.1.1.490	reg : CORE_DIG_DLANE_0_R_HS_RX_4	0x0000	0x3094	161
1.1.1.492	reg : CORE_DIG_DLANE_0_RW_HS_TX_0	0x0009	0x3100	161
1.1.1.493	reg : CORE_DIG_DLANE_0_RW_HS_TX_1	0x0020	0x3101	161

1.1.1.494	reg : CORE_DIG_DLANE_0_RW_HS_TX_2	0x0003	0x3102	161
1.1.1.495	reg : CORE_DIG_DLANE_0_RW_HS_TX_3	0x0006	0x3103	161
1.1.1.496	reg : CORE_DIG_DLANE_0_RW_HS_TX_4	0x0007	0x3104	162
1.1.1.497	reg : CORE_DIG_DLANE_0_RW_HS_TX_5	0x0007	0x3105	162
1.1.1.498	reg : CORE_DIG_DLANE_0_RW_HS_TX_6	0x000A	0x3106	162
1.1.1.499	reg : CORE_DIG_DLANE_0_RW_HS_TX_7	0x00FF	0x3107	162
1.1.1.500	reg : CORE_DIG_DLANE_0_RW_HS_TX_8	0x001C	0x3108	162
1.1.1.501	reg : CORE_DIG_DLANE_0_RW_HS_TX_9	0x000A	0x3109	163
1.1.1.502	reg : CORE_DIG_DLANE_0_RW_HS_TX_10	0x000A	0x310A	163
1.1.1.503	reg : CORE_DIG_DLANE_0_RW_HS_TX_11	0x0007	0x310B	163
1.1.1.504	reg : CORE_DIG_DLANE_0_RW_HS_TX_12	0x0014	0x310C	163
1.1.1.506	reg : CORE_DIG_DLANE_1_RW_CFG_0	0x0000	0x3200	163
1.1.1.507	reg : CORE_DIG_DLANE_1_RW_CFG_1	0x0000	0x3201	163
1.1.1.508	reg : CORE_DIG_DLANE_1_RW_CFG_2	0x0000	0x3202	164
1.1.1.510	reg : CORE_DIG_DLANE_1_RW_LP_0	0x463C	0x3240	164
1.1.1.511	reg : CORE_DIG_DLANE_1_RW_LP_1	0x8010	0x3241	164
1.1.1.512	reg : CORE_DIG_DLANE_1_RW_LP_2	0x0001	0x3242	164
1.1.1.514	reg : CORE_DIG_DLANE_1_R_LP_0	0x0000	0x3250	165
1.1.1.515	reg : CORE_DIG_DLANE_1_R_LP_1	0x0000	0x3251	165
1.1.1.517	reg : CORE_DIG_DLANE_1_R_HS_TX_0	0x0000	0x3270	165
1.1.1.519	reg : CORE_DIG_DLANE_1_RW_HS_RX_0	0x091D	0x3280	165
1.1.1.520	reg : CORE_DIG_DLANE_1_RW_HS_RX_1	0x4010	0x3281	165
1.1.1.521	reg : CORE_DIG_DLANE_1_RW_HS_RX_2	0x169B	0x3282	166

1.1.1.522	reg : CORE_DIG_DLANE_1_RW_HS_RX_3	0x2412	0x3283	166
1.1.1.523	reg : CORE_DIG_DLANE_1_RW_HS_RX_4	0x0096	0x3284	166
1.1.1.524	reg : CORE_DIG_DLANE_1_RW_HS_RX_5	0x0000	0x3285	166
1.1.1.525	reg : CORE_DIG_DLANE_1_RW_HS_RX_6	0x002D	0x3286	167
1.1.1.526	reg : CORE_DIG_DLANE_1_RW_HS_RX_7	0x3B06	0x3287	167
1.1.1.527	reg : CORE_DIG_DLANE_1_RW_HS_RX_8	0x0000	0x3288	167
1.1.1.528	reg : CORE_DIG_DLANE_1_RW_HS_RX_9	0x00FF	0x3289	168
1.1.1.529	reg : CORE_DIG_DLANE_1_RW_HS_RX_10	0x0001	0x328A	168
1.1.1.530	reg : CORE_DIG_DLANE_1_RW_HS_RX_11	0x0002	0x328B	168
1.1.1.531	reg : CORE_DIG_DLANE_1_RW_HS_RX_12	0x0003	0x328C	168
1.1.1.533	reg : CORE_DIG_DLANE_1_R_HS_RX_0	0x0000	0x3290	168
1.1.1.534	reg : CORE_DIG_DLANE_1_R_HS_RX_1	0x0000	0x3291	169
1.1.1.535	reg : CORE_DIG_DLANE_1_R_HS_RX_2	0x00A0	0x3292	169
1.1.1.536	reg : CORE_DIG_DLANE_1_R_HS_RX_3	0x0000	0x3293	169
1.1.1.537	reg : CORE_DIG_DLANE_1_R_HS_RX_4	0x0000	0x3294	169
1.1.1.539	reg : CORE_DIG_DLANE_1_RW_HS_TX_0	0x0009	0x3300	170
1.1.1.540	reg : CORE_DIG_DLANE_1_RW_HS_TX_1	0x0020	0x3301	170
1.1.1.541	reg : CORE_DIG_DLANE_1_RW_HS_TX_2	0x0003	0x3302	170
1.1.1.542	reg : CORE_DIG_DLANE_1_RW_HS_TX_3	0x0006	0x3303	170
1.1.1.543	reg : CORE_DIG_DLANE_1_RW_HS_TX_4	0x0007	0x3304	170
1.1.1.544	reg : CORE_DIG_DLANE_1_RW_HS_TX_5	0x0007	0x3305	170
1.1.1.545	reg : CORE_DIG_DLANE_1_RW_HS_TX_6	0x000A	0x3306	171
1.1.1.546	reg : CORE_DIG_DLANE_1_RW_HS_TX_7	0x00FF	0x3307	171

1.1.1.547	reg : CORE_DIG_DLANE_1_RW_HS_TX_8	0x001C	0x3308	171
1.1.1.548	reg : CORE_DIG_DLANE_1_RW_HS_TX_9	0x000A	0x3309	171
1.1.1.549	reg : CORE_DIG_DLANE_1_RW_HS_TX_10	0x000A	0x330A	171
1.1.1.550	reg : CORE_DIG_DLANE_1_RW_HS_TX_11	0x0007	0x330B	171
1.1.1.551	reg : CORE_DIG_DLANE_1_RW_HS_TX_12	0x0014	0x330C	172
1.1.1.553	reg : CORE_DIG_DLANE_CLK_RW_CFG_0	0x0000	0x3800	172
1.1.1.554	reg : CORE_DIG_DLANE_CLK_RW_CFG_1	0x0000	0x3801	172
1.1.1.555	reg : CORE_DIG_DLANE_CLK_RW_CFG_2	0x0000	0x3802	172
1.1.1.557	reg : CORE_DIG_DLANE_CLK_RW_LP_0	0x463C	0x3840	172
1.1.1.558	reg : CORE_DIG_DLANE_CLK_RW_LP_1	0x8010	0x3841	173
1.1.1.559	reg : CORE_DIG_DLANE_CLK_RW_LP_2	0x0001	0x3842	173
1.1.1.561	reg : CORE_DIG_DLANE_CLK_R_LP_0	0x0000	0x3850	173
1.1.1.562	reg : CORE_DIG_DLANE_CLK_R_LP_1	0x0000	0x3851	173
1.1.1.564	reg : CORE_DIG_DLANE_CLK_R_HS_TX_0	0x0000	0x3870	174
1.1.1.566	reg : CORE_DIG_DLANE_CLK_RW_HS_RX_0	0x091D	0x3880	174
1.1.1.567	reg : CORE_DIG_DLANE_CLK_RW_HS_RX_1	0x4010	0x3881	174
1.1.1.568	reg : CORE_DIG_DLANE_CLK_RW_HS_RX_2	0x169B	0x3882	174
1.1.1.569	reg : CORE_DIG_DLANE_CLK_RW_HS_RX_3	0x2412	0x3883	175
1.1.1.570	reg : CORE_DIG_DLANE_CLK_RW_HS_RX_4	0x0096	0x3884	175
1.1.1.571	reg : CORE_DIG_DLANE_CLK_RW_HS_RX_5	0x0000	0x3885	175
1.1.1.572	reg : CORE_DIG_DLANE_CLK_RW_HS_RX_6	0x002D	0x3886	175
1.1.1.573	reg : CORE_DIG_DLANE_CLK_RW_HS_RX_7	0x3B06	0x3887	175
1.1.1.574	reg : CORE_DIG_DLANE_CLK_RW_HS_RX_8	0x0000	0x3888	176

1.1.1.575	reg : CORE_DIG_DLANE_CLK_RW_HS_RX_9	0x00FF	0x3889	176
1.1.1.576	reg : CORE_DIG_DLANE_CLK_RW_HS_RX_10	0x0001	0x388A	176
1.1.1.577	reg : CORE_DIG_DLANE_CLK_RW_HS_RX_11	0x0002	0x388B	177
1.1.1.578	reg : CORE_DIG_DLANE_CLK_RW_HS_RX_12	0x0003	0x388C	177
1.1.1.580	reg : CORE_DIG_DLANE_CLK_R_HS_RX_0	0x0000	0x3890	177
1.1.1.581	reg : CORE_DIG_DLANE_CLK_R_HS_RX_1	0x0000	0x3891	177
1.1.1.582	reg : CORE_DIG_DLANE_CLK_R_HS_RX_2	0x00A0	0x3892	177
1.1.1.583	reg : CORE_DIG_DLANE_CLK_R_HS_RX_3	0x0000	0x3893	178
1.1.1.584	reg : CORE_DIG_DLANE_CLK_R_HS_RX_4	0x0000	0x3894	178
1.1.1.586	reg : CORE_DIG_DLANE_CLK_RW_HS_TX_0	0x0009	0x3900	178
1.1.1.587	reg : CORE_DIG_DLANE_CLK_RW_HS_TX_1	0x0020	0x3901	178
1.1.1.588	reg : CORE_DIG_DLANE_CLK_RW_HS_TX_2	0x0003	0x3902	178
1.1.1.589	reg : CORE_DIG_DLANE_CLK_RW_HS_TX_3	0x0006	0x3903	178
1.1.1.590	reg : CORE_DIG_DLANE_CLK_RW_HS_TX_4	0x0007	0x3904	179
1.1.1.591	reg : CORE_DIG_DLANE_CLK_RW_HS_TX_5	0x0007	0x3905	179
1.1.1.592	reg : CORE_DIG_DLANE_CLK_RW_HS_TX_6	0x000A	0x3906	179
1.1.1.593	reg : CORE_DIG_DLANE_CLK_RW_HS_TX_7	0x00FF	0x3907	179
1.1.1.594	reg : CORE_DIG_DLANE_CLK_RW_HS_TX_8	0x001C	0x3908	179
1.1.1.595	reg : CORE_DIG_DLANE_CLK_RW_HS_TX_9	0x000A	0x3909	180
1.1.1.596	reg : CORE_DIG_DLANE_CLK_RW_HS_TX_10	0x000A	0x390A	180
1.1.1.597	reg : CORE_DIG_DLANE_CLK_RW_HS_TX_11	0x0007	0x390B	180
1.1.1.598	reg : CORE_DIG_DLANE_CLK_RW_HS_TX_12	0x0014	0x390C	180
1.1.1.600	reg : PPI_RW_CPHY_TRIO0_LBERT_0	0x0000	0x4000	180

1.1.1.601	reg : PPI_RW_CPHY_TRIO0_LBERT_1	0x0000	0x4001	181
1.1.1.602	reg : PPI_R_CPHY_TRIO0_LBERT_0	0x0001	0x4002	181
1.1.1.603	reg : PPI_R_CPHY_TRIO0_LBERT_1	0x0000	0x4003	181
1.1.1.604	reg : PPI_RW_CPHY_TRIO0_SPARE	0x0000	0x4004	181
1.1.1.606	reg : PPI_RW_CPHY_TRIO1_LBERT_0	0x0000	0x4200	182
1.1.1.607	reg : PPI_RW_CPHY_TRIO1_LBERT_1	0x0000	0x4201	182
1.1.1.608	reg : PPI_R_CPHY_TRIO1_LBERT_0	0x0001	0x4202	183
1.1.1.609	reg : PPI_R_CPHY_TRIO1_LBERT_1	0x0000	0x4203	183
1.1.1.610	reg : PPI_RW_CPHY_TRIO1_SPARE	0x0000	0x4204	183
1.1.1.612	reg : CORE_DIG_CLANE_0_RW_CFG_0	0x00F0	0x5000	183
1.1.1.614	reg : CORE_DIG_CLANE_0_RW_CFG_2	0x0000	0x5002	184
1.1.1.616	reg : CORE_DIG_CLANE_0_RW_LP_0	0x463C	0x5040	184
1.1.1.617	reg : CORE_DIG_CLANE_0_RW_LP_1	0x8010	0x5041	184
1.1.1.618	reg : CORE_DIG_CLANE_0_RW_LP_2	0x0001	0x5042	184
1.1.1.620	reg : CORE_DIG_CLANE_0_R_LP_0	0x0000	0x5050	184
1.1.1.621	reg : CORE_DIG_CLANE_0_R_LP_1	0x0000	0x5051	185
1.1.1.623	reg : CORE_DIG_CLANE_0_RW_HS_RX_0	0x0065	0x5080	185
1.1.1.624	reg : CORE_DIG_CLANE_0_RW_HS_RX_1	0x007E	0x5081	185
1.1.1.626	reg : CORE_DIG_CLANE_0_R_TX_0	0x0000	0x5091	185
1.1.1.628	reg : CORE_DIG_CLANE_0_RW_HS_TX_0	0x0014	0x5100	185
1.1.1.629	reg : CORE_DIG_CLANE_0_RW_HS_TX_1	0x0003	0x5101	186
1.1.1.630	reg : CORE_DIG_CLANE_0_RW_HS_TX_2	0x0003	0x5102	186
1.1.1.631	reg : CORE_DIG_CLANE_0_RW_HS_TX_3	0x0000	0x5103	186

1.1.1.632	reg : CORE_DIG_CLANE_0_RW_HS_TX_4	0x0000	0x5104	186
1.1.1.633	reg : CORE_DIG_CLANE_0_RW_HS_TX_5	0x0000	0x5105	186
1.1.1.634	reg : CORE_DIG_CLANE_0_RW_HS_TX_6	0x0000	0x5106	187
1.1.1.635	reg : CORE_DIG_CLANE_0_RW_HS_TX_7	0x000D	0x5107	187
1.1.1.636	reg : CORE_DIG_CLANE_0_RW_HS_TX_8	0x000A	0x5108	187
1.1.1.637	reg : CORE_DIG_CLANE_0_RW_HS_TX_9	0x0006	0x5109	187
1.1.1.638	reg : CORE_DIG_CLANE_0_RW_HS_TX_10	0x0002	0x510A	188
1.1.1.639	reg : CORE_DIG_CLANE_0_RW_HS_TX_11	0x000A	0x510B	188
1.1.1.640	reg : CORE_DIG_CLANE_0_RW_HS_TX_12	0x000A	0x510C	188
1.1.1.641	reg : CORE_DIG_CLANE_0_RW_HS_TX_13	0x0006	0x510D	188
1.1.1.643	reg : CORE_DIG_CLANE_1_RW_CFG_0	0x00F0	0x5200	188
1.1.1.645	reg : CORE_DIG_CLANE_1_RW_CFG_2	0x0000	0x5202	189
1.1.1.647	reg : CORE_DIG_CLANE_1_RW_LP_0	0x463C	0x5240	189
1.1.1.648	reg : CORE_DIG_CLANE_1_RW_LP_1	0x8010	0x5241	189
1.1.1.649	reg : CORE_DIG_CLANE_1_RW_LP_2	0x0001	0x5242	189
1.1.1.651	reg : CORE_DIG_CLANE_1_R_LP_0	0x0000	0x5250	190
1.1.1.652	reg : CORE_DIG_CLANE_1_R_LP_1	0x0000	0x5251	190
1.1.1.654	reg : CORE_DIG_CLANE_1_RW_HS_RX_0	0x0065	0x5280	190
1.1.1.655	reg : CORE_DIG_CLANE_1_RW_HS_RX_1	0x007E	0x5281	190
1.1.1.657	reg : CORE_DIG_CLANE_1_R_TX_0	0x0000	0x5291	190
1.1.1.659	reg : CORE_DIG_CLANE_1_RW_HS_TX_0	0x0014	0x5300	191
1.1.1.660	reg : CORE_DIG_CLANE_1_RW_HS_TX_1	0x0003	0x5301	191
1.1.1.661	reg : CORE_DIG_CLANE_1_RW_HS_TX_2	0x0003	0x5302	191

1.1.1.662	reg : CORE_DIG_CLANE_1_RW_HS _TX_3	0x0000	0x5303	191
1.1.1.663	reg : CORE_DIG_CLANE_1_RW_HS _TX_4	0x0000	0x5304	191
1.1.1.664	reg : CORE_DIG_CLANE_1_RW_HS _TX_5	0x0000	0x5305	192
1.1.1.665	reg : CORE_DIG_CLANE_1_RW_HS _TX_6	0x0000	0x5306	192
1.1.1.666	reg : CORE_DIG_CLANE_1_RW_HS _TX_7	0x000D	0x5307	192
1.1.1.667	reg : CORE_DIG_CLANE_1_RW_HS _TX_8	0x000A	0x5308	192
1.1.1.668	reg : CORE_DIG_CLANE_1_RW_HS _TX_9	0x0006	0x5309	193
1.1.1.669	reg : CORE_DIG_CLANE_1_RW_HS _TX_10	0x0002	0x530A	193
1.1.1.670	reg : CORE_DIG_CLANE_1_RW_HS _TX_11	0x000A	0x530B	193
1.1.1.671	reg : CORE_DIG_CLANE_1_RW_HS _TX_12	0x000A	0x530C	193
1.1.1.672	reg : CORE_DIG_CLANE_1_RW_HS _TX_13	0x0006	0x530D	193

1 dwc_mipi_cdphy2_rx_2l2t_ns

Block | 0x0000 - 0xFFFE

vendor : Synopsys
library : DesignWareCores
version : 1.0
reset_type : async

1.1 cdphy

RegGrp | 0x0000 - 0xFFFE

1.1.1 cdphy_mem_map

RegGrp | 0x0000 - 0xFFFE

Describes all the registers in this IP.
range : 65535

1.1.1.2 PPI_STARTUP_RW_COMMON_DPHY_0

Reg. | 0x0C00

PWR_DWN state address configuration
access : read-write

bits	name	s/w	h/w	default	description
7:0	PWR_DWN_addr	rw	ro	0x0	Configures behavior of PWR_DWN state. This field is quasi-static. - [7] stuck: if 1'b1, FSM will stop in this state. - [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck. - [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate.

					- [4:0] next_state: defines the next state. Please check the table for state codes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.3 PPI_STARTUP_RW_COMMON_DPHY_1

Reg. 0x0C01

BG_ON state address configuration
access : read-write

bits	name	s/w	h/w	default	description
7:0	BG_ON_addr	rw	ro	0x22	Configures behavior of BG_ON state. This field is quasi-static. - [7] stuck: if 1'b1, FSM will stop in this state. - [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck. - [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate. - [4:0] next_state: defines the next state. Please check the table for state codes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.4 PPI_STARTUP_RW_COMMON_DPHY_2

Reg. 0x0C02

RCAL state address configuration
access : read-write

bits	name	s/w	h/w	default	description
7:0	RCAL_addr	rw	ro	0x4	Configures behavior of RCAL state. This field is quasi-static. - [7] stuck: if 1'b1, FSM will stop in this state. - [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck. - [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate. - [4:0] next_state: defines the next state. Please check the table for state codes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.5 PPI_STARTUP_RW_COMMON_DPHY_3

Reg. 0x0C03

PLL_START state address configuration
access : read-write

bits	name	s/w	h/w	default	description
7:0	PLL_START_addr	rw	ro	0x45	Configures behavior of PLL_START state. This field is quasi-static. - [7] stuck: if 1'b1, FSM will stop in this state. - [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck. - [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate. - [4:0] next_state: defines the next state. Please check the table for state codes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.6 PPI_STARTUP_RW_COMMON_DPHY_4

Reg. 0x0C04

HS_DCO_CAL state address configuration
access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_DCO_CAL_addr	rw	ro	0x5	Configures behavior of HS_DCO_CAL state. This field is quasi-static. - [7] stuck: if 1'b1, FSM will stop in this state. - [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck.

					- [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate. - [4:0] next_state: defines the next state. Please check the table for state codes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.7 PPI_STARTUP_RW_COMMON_DPHY_5

Reg. 0x0C05

OFFSET_CAL state address configuration
access : read-write

bits	name	s/w	h/w	default	description
7:0	OFFSET_CAL_addr	rw	ro	0x6	Configures behavior of OFFSET_CAL state. This field is quasi-static. - [7] stuck: if 1'b1, FSM will stop in this state. - [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck. - [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate. - [4:0] next_state: defines the next state. Please check the table for state codes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.8 PPI_STARTUP_RW_COMMON_DPHY_6

Reg. 0x0C06

LP_DCO_CAL state address configuration
access : read-write

bits	name	s/w	h/w	default	description
7:0	LP_DCO_CAL_addr	rw	ro	0x7	Configures behavior of LP_DCO_CAL state. This field is quasi-static. - [7] stuck: if 1'b1, FSM will stop in this state. - [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck. - [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate. - [4:0] next_state: defines the next state. Please check the table for state codes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.9 PPI_STARTUP_RW_COMMON_DPHY_7

Reg. 0x0C07

DPHY_DDL_CAL state address configuration
access : read-write

bits	name	s/w	h/w	default	description
7:0	DPHY_DDL_CAL_addr	rw	ro	0x30	Configures behavior of DPHY_DDL_CAL state. This field is quasi-static. - [7] stuck: if 1'b1, FSM will stop in this state. - [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck. - [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate. - [4:0] next_state: defines the next state. Please check the table for state codes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.10 PPI_STARTUP_RW_COMMON_DPHY_8

Reg. 0x0C08

CPHY_DDL_CAL state address configuration
access : read-write

bits	name	s/w	h/w	default	description
7:0	CPHY_DDL_CAL_addr	rw	ro	0x10	Configures behavior of CPHY_DDL_CAL state. This field is quasi-static.

					- [7] stuck: if 1'b1, FSM will stop in this state. - [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck. - [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate. - [4:0] next_state: defines the next state. Please check the table for state codes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.11 PPI_STARTUP_RW_COMMON_DPHY_9

Reg. 0x0C09

DESKEW_1P1 state address configuration
access : read-write

bits	name	s/w	h/w	default	description
7:0	DESKEW_1P1_addr	rw	ro	0x50	Configures behavior of DESKEW_1P1 state. This field is quasi-static. - [7] stuck: if 1'b1, FSM will stop in this state. - [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck. - [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate. - [4:0] next_state: defines the next state. Please check the table for state codes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.12 PPI_STARTUP_RW_COMMON_DPHY_A

Reg. 0x0C0A

HIBERNATE state address configuration
access : read-write

bits	name	s/w	h/w	default	description
7:0	HIBERNATE_addr	rw	ro	0x21	Configures behavior of HIBERNATE state. This field is quasi-static. - [7] stuck: if 1'b1, FSM will stop in this state. - [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck. - [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate. - [4:0] next_state: defines the next state. Please check the table for state codes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.14 PPI_STARTUP_RW_COMMON_DPHY_10

Reg. 0x0C10

PHY_READY state address configuration
access : read-write

bits	name	s/w	h/w	default	description
7:0	PHY_READY_addr	rw	ro	0x2F	Configures behavior of PHY_READY state. This field is quasi-static. - [7] stuck: if 1'b1, FSM will stop in this state. - [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck. - [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate. - [4:0] next_state: defines the next state. Please check the table for state codes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.15 PPI_STARTUP_RW_COMMON_STARTUP_1_1

Reg. 0x0C11

PHY startup FSM configuration
access : read-write

bits	name	s/w	h/w	default	description
11:0	PHY_READY_DLY	rw	ro	0x96	Delay of phy_ready signal from the hard macro to top. Measured in cfg_clk cycles. This field is quasi-static.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.16 PPI_STARTUP_RW_COMMON_STARTUP_1_2

Reg. 0x0C12

PHY startup FSM configuration
access : read-write

bits	name	s/w	h/w	default	description
11:0	TXCLKESC_SWAP_DLY	rw	ro	0x78	Delay of txclkesc_swap signal from the hard macro to top. Measured in cfg_clk cycles. This field is quasi-static.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.18 PPI_CALIBCTRL_RW_COMMON_CALIBCTRL_2_0

Reg. 0x0C20

Power on lane calibration configuration
access : read-write

bits	name	s/w	h/w	default	description
4:0	LANE_CALIB_OFFSETCAL_LAST	rw	ro	0x4	Indicator of last lane to calibrate (lane4 down to lane0) This field is quasi-static.
9:5	LANE_CALIB_OFFSETCAL_EN	rw	ro	0x7	Calibration enable for all lanes (lane4 down to lane0) This field is quasi-static.
10	OFFSETCAL_RECALIBRATION_EN	rw	ro	0x0	Enable to manually allow offset recalibration. Active high.
11	TERMCAL_RECALIBRATION_EN	rw	ro	0x0	Enable to manually allow terminal recalibration. Active high.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.19 PPI_CALIBCTRL_R_COMMON_CALIBCTRL_2_1

Reg. 0x0C21

DDL calibration observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	DDL_COUNTER_TARGET_OBS_LSBs	ro	ro	0x0	16 LSBs of the counter target calculated during DDL calibration

1.1.1.20 PPI_CALIBCTRL_R_COMMON_CALIBCTRL_2_2

Reg. 0x0C22

DDL calibration observability
access : read-only

bits	name	s/w	h/w	default	description
7:0	DDL_COUNTER_TARGET_OBS_MSBs	ro	ro	0x0	8 MSBs of the counter target calculated during DDL calibration
15:8	DDL_COUNTER_MULT_OBS_LSBs	ro	ro	0x0	8 LSBs of the multiplication calculated during DDL calibration

1.1.1.21 PPI_CALIBCTRL_R_COMMON_CALIBCTRL_2_3

Reg. 0x0C23

DDL calibration observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	DDL_COUNTER_MULT_OBS_MSBs	ro	ro	0x0	16 MSBs of the multiplication calculated during DDL calibration

1.1.1.22 PPI_CALIBCTRL_R_COMMON_CALIBCTRL_2_4

Reg. 0x0C24

DDL calibration observability

access : read-only

bits	name	s/w	h/w	default	description
12:0	DDL_COUNTER_SUM_OBS	ro	ro	0x0	Result of the sum calculated during DDL calibration
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.23 PPI_CALIBCTRL_R_COMMON_CALIBCTRL_2_5

Reg. 0x0C25

DDL calibration observability
access : read-only

bits	name	s/w	h/w	default	description
3:0	DDL_CAL_STATUS0	ro	ro	0x0	Status of Lane 0's DDL calibration - Bit 0 : Signals that the calibration has finished, regardless of the result - Bit 1 : Indicates an error in the calibration (Full bias range was swept with no convergence) - Bit 2 : Indicates an error in the calibration (osc_clk was detected to be stuck) - Bit 3 : Final result is outside of the set acceptable range.
7:4	DDL_CAL_STATUS1	ro	ro	0x0	Status of Lane 1's DDL calibration - Bit 0 : Signals that the calibration has finished, regardless of the result - Bit 1 : Indicates an error in the calibration (Full bias range was swept with no convergence) - Bit 2 : Indicates an error in the calibration (osc_clk was detected to be stuck) - Bit 3 : Final result is outside of the set acceptable range.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.24 PPI_CALIBCTRL_RW_COMMON_BG_0

Reg. 0x0C26

Bandgap configuration
access : read-write

bits	name	s/w	h/w	default	description
8:0	BG_MAX_COUNTER	rw	ro	0x8F	Configures waiting time since the beginning of bandgap state until the jump to the next state. Measured in config clock cycles. This field is quasi-static.
15:9	RESERVED_15_9	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.25 PPI_CALIBCTRL_RW_COMMON_CALIBCTRL_2_7

Reg. 0x0C27

Power on lane calibration configuration
access : read-write

bits	name	s/w	h/w	default	description
4:0	STATE_DONE_TIMER_THRES	rw	ro	0x8	Sets the time to move to the next FSM state to allow all blocks to synchronize their flags appropriately. Measured in config clock cycles. This field is quasi-static.
15:5	RESERVED_15_5	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.26 PPI_CALIBCTRL_RW_ADC_CFG_0

Reg. 0x0C28

ADC configuration register 0
access : read-write

bits	name	s/w	h/w	default	description
0	ADC_ENB	rw	ro	0x0	ADC enable (active high, edge triggered)
15:1	RESERVED_15_1	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.27 PPI_CALIBCTRL_RW_ADC_CFG_1

Reg. 0x0C29

ADC configuration register 1
access : read-write

bits	name	s/w	h/w	default	description
7:0	ADC_WAIT_THRESH_T1	rw	ro	0x0	ADC wait threshold timer 1
15:8	ADC_WAIT_THRESH_T2	rw	ro	0x0	ADC wait threshold timer 2

1.1.1.28 PPI_CALIBCTRL_R_ADC_DEBUG

Reg. 0x0C2A

ADC outputs observability
access : read-only

bits	name	s/w	h/w	default	description
9:0	CB_ATB_SEL_DAC	ro	ro	0x0	ADC output word calculated using SAR algorithm
10	ADC_DONE	ro	ro	0x0	ADC done flag. This flag is asserted at the end of ADC SAR operation and de-asserted with the rising edge of the adc enable.
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.29 PPI_CALIBCTRL_RW_COMMON_CALIBCTRL_2_1

Reg. 0x0C2B

RX Equalization configurations
access : read-write

bits	name	s/w	h/w	default	description
10:0	RXEQ_WAIT_TIME	rw	ro	0x2	Time to wait after applying RX EQ Setting. (In cfg_clk cycles). This field is quasi-static.
11	RXEQ_ENABLE_REG	rw	ro	0x1	Enable RX equalization algorithm. This field is quasi-static.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.30 PPI_CALIBCTRL_R_COMMON_CALIBCTRL_2_6

Reg. 0x0C2C

RX Equalization calibration observability
access : read-only

bits	name	s/w	h/w	default	description
1:0	RXEQ_STATUS	ro	ro	0x0	Status of RX equalization calibration - Bit 0 : Signals the calibration has finished - Bit 1 : Indicates an error in the calibration
15:2	RESERVED_15_2	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.31 PPI_CALIBCTRL_RW_COMMON_CALIBCTRL_2_2

Reg. 0x0C2D

DDL calibration configurations
access : read-write

bits	name	s/w	h/w	default	description
2:0	DDL_CALS_DONE_DLY	rw	ro	0x4	Delay of ddl_cals_done flag to ensure stability of phy_calib[4:2] before entering phy_ready. (In cfg_clk cycles). This field is quasi-static.
15:3	RESERVED_15_3	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.32 PPI_CALIBCTRL_RW_COMMON_CALIBCTRL_2_3

Reg. 0x0C2E

DDL VT Drift configurations
access : read-write

bits	name	s/w	h/w	default	description
3:0	DDL_VT_MIN_EQUAL_READINGS	rw	ro	0x8	Minimum equal readings to make a decision in the algorithm (In cfg_clk cycles). This field is quasi-static.
4	DDL_VT_CAL_EN	rw	ro	0x1	Enable DDL VT drift calibration. This field is quasi static.
15:5	RESERVED_15_5	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.33 PPI_CALIBCTRL_R_COMMON_CALIBCTRL_2_7

Reg. 0x0C2F

DDL VT drift calibration observability
access : read-only

bits	name	s/w	h/w	default	description
3:0	DDL_VT_DRIFT_CAL_STATUS	ro	ro	0x0	Status of DDL VT drift calibration - Bit 0 : Lane 0 has successfully run the calibration - Bit 1 : Lane 1 has successfully run the calibration - Bit 2 : Lane 2 has successfully run the calibration - Bit 3 : Lane 3 has successfully run the calibration
15:4	RESERVED_15_4	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.34 PPI_CALIBCTRL_RW_HS_RX_0

Reg. 0x0C30

CPHY HS RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
0	HS_CDR_UPDATE_SETTINGS_REG	rw	ro	0x1	Signal used to update the CDR calibration machine's settings (Active high)
1	HS_CDR_FEEDBACK_ENABLED_REG	rw	ro	0x1	Signal which indicates whether the feedback loop is enabled. (Active high)
15:2	RESERVED_15_2	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.35 PPI_CALIBCTRL_RW_HS_RX_1

Reg. 0x0C31

CPHY HS RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_CDR_TIMEBASE_TARGET_REG	rw	ro	0x14	Timebase for the oscillation clock's tick count (cfg_clk cycles)

1.1.1.36 PPI_CALIBCTRL_RW_HS_RX_2

Reg. 0x0C32

CPHY HS RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_CDR_COARSE_TARGET_REG	rw	ro	0x14	Target for the oscillation clock's tick count (osc_clk cycles)

1.1.1.37 PPI_CALIBCTRL_RW_HS_RX_3

Reg. 0x0C33

CPHY HS RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_CDR_STUCK_THRESH_REG	rw	ro	0x0	Minimum tick count not to flag a stuck condition (Osc_clk cycles). Quasi static.

1.1.1.38 PPI_CALIBCTRL_RW_HS_RX_4

Reg. 0x0C34

CPHY HS RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
4:0	HS_CDR_COARSE_OBS_SEL_REG	rw	ro	0x0	Selector to define setting for which to read CDR cycle count results
9:5	HS_CDR_COARSE_INIT_REG	rw	ro	0x0	Define initial coarse value setting

14:10	HS_CDR_COARSE_END_REG	rw	ro	0x1F	Define final coarse value setting
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.39 PPI_CALIBCTRL_RW_HS_RX_5

Reg. 0x0C35

CPHY HS RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_CDR_INIT_WAIT_TARGET_REG	rw	ro	0x0	Counter target for initial CDR delay. (Cfg_clk cycles). Quasi static.

1.1.1.41 PPI_CALIBCTRL_R_COMMON_CALIBCTRL_4_0

Reg. 0x0C40

CDR calibration observability
access : read-only

bits	name	s/w	h/w	default	description
0	CDR_CAL_STATUS0	ro	ro	0x0	Status of Trio 0's CDR calibration
1	O_CDR_CALDONE0	ro	ro	0x0	Signal of Trio 0 that flags the completion of a CDR calibration (Active high)
2	CDR_CAL_STATUS1	ro	ro	0x0	Status of Trio 1's CDR calibration
3	O_CDR_CALDONE1	ro	ro	0x0	Signal of Trio 1 that flags the completion of a CDR calibration (Active high)
15:4	RESERVED_15_4	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.42 PPI_CALIBCTRL_R_COMMON_CALIBCTRL_4_1

Reg. 0x0C41

CDR calibration observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	COARSE_DIF_TARGET_0	ro	ro	0xFFFF	Difference between the oscillation clock's tick count towards the selected target

1.1.1.43 PPI_CALIBCTRL_R_COMMON_CALIBCTRL_4_2

Reg. 0x0C42

CDR calibration observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	CR_COARSE_VALUE_OBS_0	ro	ro	0x0	- CDR clock cycles measured for setting defined in cdr_coarse_obs_sel_reg

1.1.1.44 PPI_CALIBCTRL_R_COMMON_CALIBCTRL_4_3

Reg. 0x0C43

CDR calibration observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	COARSE_DIF_TARGET_1	ro	ro	0xFFFF	Difference between the oscillation clock's tick count towards the selected target

1.1.1.45 PPI_CALIBCTRL_R_COMMON_CALIBCTRL_4_4

Reg. 0x0C44

CDR calibration observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	CR_COARSE_VALUE_OBS_1	ro	ro	0x0	- CDR clock cycles measured for setting defined in cdr_coarse_obs_sel_reg

1.1.1.47 PPI_CALIBCTRL_RW_COMMON_ARBT_0

Reg. 0x0C50

PHY calib Arbitrator parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	ARBT_CAL_PRIOTITY	rw	ro	0x0	Signal which indicates the priority of each PHY ready calibrations. This field is quasi-static.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.48 PPI_CALIBCTRL_RW_COMMON_ARBT_1

Reg. 0x0C51

PHY calib Arbitrator parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	ARBT_CAL_LOCK	rw	ro	0x0	Signal which indicates lock property of each PHY ready calibrations (Active high).
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.49 PPI_CALIBCTRL_RW_COMMON_ARBT_2

Reg. 0x0C52

PHY calib Arbitrator parameters control
access : read-write

bits	name	s/w	h/w	default	description
3:0	ARBT_CALIB_READ_DELTA	rw	ro	0x2	Length of phy calib read pulse in the arbitrator (In cfg_clk cycles). This field is quasi-static.
7:4	ARBT_CALIB_WRITE_DELTA	rw	ro	0x2	Length of phy calib write pulse in the arbitrator (In cfg_clk cycles). This field is quasi-static.
15:8	ARBT_CALIB_OP_DELTA	rw	ro	0x8	Time between calib operations in the arbitrator (In cfg_clk cycles). This field is quasi-static.

1.1.1.51 PPI_RW_LPDCOCAL_TOP_OVERRIDE

Reg. 0x0E00

LP-DCO calibration control
access : read-write

bits	name	s/w	h/w	default	description
0	LPCDCOCAL_I_MAN_LPDCO_CLKEN	rw	ro	0x0	o_lpdco_clk_en override value. Used for debug purposes.
1	LPCDCOCAL_I_MAN_LPDCO_CLKEN_EN	rw	ro	0x0	o_lpdco_clk_en override enable. Active high. Used for debug purposes.
2	LPCDCOCAL_I_MAN_LPDCOEN	rw	ro	0x0	o_lpdco_en override value. Used for debug purposes.
3	LPCDCOCAL_I_MAN_LPDCOEN_EN	rw	ro	0x0	o_lpdco_en override enable. Active high. Used for debug purposes.
4	LPCDCOCAL_I_MAN_LPDCO_PON	rw	ro	0x0	o_lpdco_pon override value. Used for debug purposes.
5	LPCDCOCAL_I_MAN_LPDCO_PON_EN	rw	ro	0x0	o_lpdco_pon override enable. Active high. Used for debug purposes.
6	LPCDCOCAL_I_MAN_FWORD_LATCH	rw	ro	0x0	o_fword_latch override value. Used for debug purposes.
13:7	LPCDCOCAL_I_MAN_FWORD	rw	ro	0x0	o_fword override value. Used for debug purposes.
14	LPCDCOCAL_I_MAN_CAL_EN	rw	ro	0x0	o_fword and o_fword_latch override enable. Active high. Used for debug purposes.
15	LPCDCOCAL_I_MAN_TRIGGER	rw	ro	0x0	Enable for triggering new LPDCO calibration. Active on rising edge.

1.1.1.52 PPI_RW_LPDCOCAL_TIMEBASE

Reg. 0x0E01

LP-DCO calibration control
access : read-write

bits	name	s/w	h/w	default	description
9:0	LPCDCOCAL_TIMEBASE	rw	ro	0x0	Timebase configuration required to measure LPDCO clock. Defined in cfg_clk cycles.
15:10	RESERVED_15_10	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.53 PPI_RW_LPDCOCAL_NREF

Reg. 0x0E02

LP-DCO calibration control
access : read-write

bits	name	s/w	h/w	default	description
10:0	LPCDCOCAL_NREF	rw	ro	0x0	Sets LPDCO calibration target: number of expected LPDCO clock ticks observed within measurement window.
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.54 PPI_RW_LPDCOCAL_NREF_RANGE

Reg. 0x0E03

LP-DCO calibration control
access : read-write

bits	name	s/w	h/w	default	description
4:0	LPCDCOCAL_NREF_RANGE	rw	ro	0x0	Range around LPCDCOCAL_NREF where calibration is considered successful.
15:5	RESERVED_15_5	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.55 PPI_RW_LPDCOCAL_NREF_TRIGGER_MAN

Reg. 0x0E04

LP-DCO calibration control
access : read-write

bits	name	s/w	h/w	default	description
0	LPDCOCAL_CMU_REF_TRIGGER_OVR_VAL	rw	ro	0x0	LP-DCO clock measurement unit trigger override value. Used for debug purposes.
1	LPDCOCAL_CMU_REF_TRIGGER_OVR_EN	rw	ro	0x0	LP-DCO clock measurement unit trigger override enable. Active high. Used for debug purposes.
15:2	RESERVED_15_2	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.56 PPI_RW_LPDCOCAL_TWAIT_CONFIG

Reg. 0x0E05

LP-DCO calibration control
access : read-write

bits	name	s/w	h/w	default	description
8:0	LPCDCOCAL_TWAIT_COARSE	rw	ro	0xC8	Counter (in cfg_clk cycles) which controls the settling time after changing the coarse setting before performing the next measurement. This field is quasi-static.
15:9	LPCDCOCAL_TWAIT_PON	rw	ro	0x0	Counter (in cfg_clk cycles) which controls the settling time between enabling the analog circuitry and starting the calibration. This field is quasi-static.

1.1.1.57 PPI_RW_LPDCOCAL_VT_CONFIG

Reg. 0x0E06

LP-DCO calibration control
access : read-write

bits	name	s/w	h/w	default	description
0	LPCDCOCAL_VT_TRACKING_EN	rw	ro	0x0	Enables VT tracking mode where calibration machine will keep monitoring LP-DCO's frequency and adjusting to variations. Active high. This field is quasi-static.

1	LPCDCOCAL_USE_IDEAL_NREF	rw	ro	0x1	Selects which reference target to use in VT tracking mode. This field is quasi-static. - 1'b0: VT tracking mode uses LPCDCOCAL_NREF as reference target. - 1'b1: VT tracking mode uses the result from the power on calibration as reference target.
6:2	LPCDCOCAL_VT_NREF_RANGE	rw	ro	0x0	Defines the tolerance which VT tracking mode still considers to be good. Setting will only be updated if measured LP-DCO frequency deviates from interval [NREF - LPCDCOCAL_VT_NREF_RANGE; NREF + LPCDCOCAL_VT_NREF_RANGE]. This field is quasi-static.
15:7	LPCDCOCAL_TWAIT_FINE	rw	ro	0xC8	Counter (in cfg_clk cycles) which controls the settling time after changing the fine setting before performing the next measurement. This field is quasi-static.

1.1.1.58 PPI_R_LPDCOCAL_DEBUG_RB

Reg. 0x0E07

LP-DCO calibration observability
access : read-only

bits	name	s/w	h/w	default	description
10:0	LPDCOCAL_N_MEAS	ro	ro	0x0	dco_clk counter result of last measurement.
12:11	LPDCOCAL_ERROR_RB	ro	ro	0x0	Power-on calibration error. - Bit 1 asserts - None of the coarse curves can be selected (hard error). - Bit 0 asserts - None of the coarse curves can be selected within target range (soft error).
13	LPDCOCAL_CAL_DONE	ro	ro	0x0	Power-on calibration has successfully finished. Active high.
14	LPDCOCAL_N_MEAS_DONE	ro	ro	0x0	LPDCO machine CMU indication that measurement is ready
15	LPDCOCAL_ERROR_VT_RB	ro	ro	0x0	VT drift calibration error. Occurs when correction reached max/min nfine control word.

1.1.1.59 PPI_RW_LPDCOCAL_COARSE_CFG

Reg. 0x0E08

LP-DCO calibration control
access : read-write

bits	name	s/w	h/w	default	description
1:0	NCOARSE_START	rw	ro	0x1	Selects the first coarse curve to be used in the sweep. This field is quasi-static.
3:2	NCOARSE_DIAG	rw	ro	0x1	Selects which coarse curve data is to be observed after LPDCO calibration is completed. Used for debug.
8:4	SCALE_REF	rw	ro	0x10	Sets the reference point to be used to find the best match from the coarse curves This field is quasi-static.
15:9	RESERVED_15_9	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.60 PPI_R_LPDCOCAL_DEBUG_COARSE_RB

Reg. 0x0E09

LP-DCO calibration observability
access : read-only

bits	name	s/w	h/w	default	description
1:0	LPDCOCAL_CAL_BOUND_STATUS	ro	ro	0x0	Indication of the quality of the calibration result relatively to the target
5:2	LPDCOCAL_CAL_COARSE_HIT	ro	ro	0x0	Indicates in which coarse curves calibration hit the target
9:6	LPDCOCAL_PON_STATE	ro	ro	0x0	State of LPDCO pon machine
15:10	RESERVED_15_10	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.61 PPI_R_LPDCOCAL_DEBUG_COARSE_MEAS_0_RB

Reg. 0x0E0A

LP-DCO calibration observability
access : read-only

bits	name	s/w	h/w	default	description
10:0	LPDCOCAL_STORED_MEAS_0	ro	ro	0x0	Indicates the last measurement of the selected coarse curve
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.62 PPI_R_LPDCOCAL_DEBUG_COARSE_MEAS_1_RB

Reg. 0x0E0B

LP-DCO calibration observability
access : read-only

bits	name	s/w	h/w	default	description
10:0	LPDCOCAL_STORED_MEAS_1	ro	ro	0x0	Indicates the N-1 measurement of the selected coarse curve
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.63 PPI_R_LPDCOCAL_DEBUG_COARSE_FWORD_RB

Reg. 0x0E0C

LP-DCO calibration observability
access : read-only

bits	name	s/w	h/w	default	description
7:0	LPDCOCAL_STORED_FWORD_0	ro	ro	0x0	Flag indication of the last point (N) of calibration for the selected coarse curve
15:8	LPDCOCAL_STORED_FWORD_1	ro	ro	0x0	Flag indication of the last point (N-1) of calibration for the selected coarse curve

1.1.1.64 PPI_R_LPDCOCAL_DEBUG_MEASURE_CURR_ERROR

Reg. 0x0E0D

LP-DCO calibration observability
access : read-only

bits	name	s/w	h/w	default	description
11:0	LPDCOCAL_MEAS_CURR_ERROR	ro	ro	0x0	Error value observed along the consecutive measurements
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.65 PPI_R_LPDCOCAL_DEBUG_MEASURE_LAST_ERROR

Reg. 0x0E0E

LP-DCO calibration observability
access : read-only

bits	name	s/w	h/w	default	description
11:0	LPDCOCAL_LAST_MEAS_ERROR	ro	ro	0x800	Saved error value observed along the consecutive measurements
14:12	LPDCOCAL_VT_STATE	ro	ro	0x0	State of VT drift machine
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.66 PPI_R_LPDCOCAL_DEBUG_VT

Reg. 0x0E0F

LP-DCO calibration observability
access : read-only

bits	name	s/w	h/w	default	description
0	LPDCOCAL_N_WITHIN_RANGE_VT	ro	ro	0x0	VTdrift machine indicating that we are within defined range

1	LPDCOCAL_N_BELOW_RANGE_VT	ro	ro	0x0	VTdrift machine indicating that we are below defined range
2	LPDCOCAL_N_ABOVE_RANGE_VT	ro	ro	0x0	VTdrift machine indicating that we are above defined range
13:3	LPDCOCAL_MEAS_ADJ_P0_VT	ro	ro	0x0	Measured DCO values during VT drift adjustment
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.67 PPI_RW_LB_TIMEBASE_CONFIG

Reg. 0x0E10

High speed loopback timebase configuration
access : read-write

bits	name	s/w	h/w	default	description
15:0	LOOPBACK_TIMEBASE	rw	ro	0x180	Timebase configuration required to measure HS loopback clock. Defined in cfg_clk cycles.

1.1.1.68 PPI_RW_LB_STARTCMU_CONFIG

Reg. 0x0E11

High speed loopack measurement trigger
access : read-write

bits	name	s/w	h/w	default	description
0	LB_START_CMU	rw	ro	0x0	Trigger to start high speed loopback clock measurement. Active high.
15:1	RESERVED_15_1	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.69 PPI_R_LBPULSE_COUNTER_RB

Reg. 0x0E12

High speed loopback measurement results
access : read-only

bits	name	s/w	h/w	default	description
15:0	LB_PULSE_COUNTER	ro	ro	0x0	Measured ticks of high speed loopback clock observed within timebase window.

1.1.1.70 PPI_R_LB_START_CMU_RB

Reg. 0x0E13

High speed loopback measurement flag
access : read-only

bits	name	s/w	h/w	default	description
0	LB_STOP_CMU	ro	ro	0x0	High speed loopback flag indicating that measurement is completed. Active high.
15:1	RESERVED_15_1	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.71 PPI_RW_LB_DPHY_BURST_START

Reg. 0x0E14

DPHY loopback burst control
access : read-write

bits	name	s/w	h/w	default	description
0	LBERT_DPHY_TXREQUESTHS_CLK	rw	ro	0x0	Initiates the HS-TX entry on the clock lane. Used for loopback purposes. Must be set to zero in mission mode. Active high.
1	LBERT_DPHY_TXREQUESTHS_DATA	rw	ro	0x0	Initiates the HS-TX entry on the data lane. All lanes enter HS at the same time. Used for loopback purposes. Must be set to zero in mission mode. Active high.
2	LBERT_DPHY_TXDATATRANSFERENHS_DATA	rw	ro	0x0	Initiates the HS-TX payload packing. Triggered on all lanes at the same time. Used for loopback purposes. Must be set to zero in mission mode. Active high.
3	LBERT_DPHY_TXSKEWCALHS_DATA	rw	ro	0x0	Initiates the HS-TX deskew training sequence. All lanes enter HS at the same time. Used for loopback purposes. Must be set to zero in mission mode. Active high.

4	LBERT_DPHY_TXALTERNATECALHS_DATA	rw	ro	0x0	Initiates the HS-TX alternate calibration training sequence. All lanes enter HS at the same time. Used for loopback purposes. Must be set to zero in mission mode. Active high.
15:5	RESERVED_15_5	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.72 PPI_RW_LB_CPHY_BURST_START

Reg. 0x0E15

CPHY loopback burst control
access : read-write

bits	name	s/w	h/w	default	description
0	LBERT_CPHY_TXREQUESTHS_DATA	rw	ro	0x0	Initiates the HS-TX entry on the data lane. All lanes enter HS at the same time. Used for loopback purposes. Must be set to zero in mission mode. Active high.
1	LBERT_CPHY_TXDATATRANSFERENHS_DATA	rw	ro	0x0	Initiates the HS-TX payload packing. Triggered on all lanes at the same time. Used for loopback purposes. Must be set to zero in mission mode. Active high.
15:2	RESERVED_15_2	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.74 PPI_RW_DDLCAL_CFG_0

Reg. 0x0E20

DDL calibration configurations
access : read-write

bits	name	s/w	h/w	default	description
9:0	DDLCAL_TIMEBASE_TARGET	rw	ro	0x14	Timebase for oscillation clock measurement (cfg_clk cycles). Quasi static.
15:10	RESERVED_15_10	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.75 PPI_RW_DDLCAL_CFG_1

Reg. 0x0E21

DDL calibration configurations
access : read-write

bits	name	s/w	h/w	default	description
10:0	DDLCAL_MAX_PHASE	rw	ro	0x40	Maximum phase setting for DDL calibration. Quasi static.
14:11	DDLCAL_INC_PHASE_VALUE	rw	ro	0x6	DDL calibration phase setting increment value. Quasi static.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.76 PPI_RW_DDLCAL_CFG_2

Reg. 0x0E22

DDL calibration configurations
access : read-write

bits	name	s/w	h/w	default	description
7:0	DDLCAL_ENABLE_WAIT	rw	ro	0x14	Time to wait before counting the oscillation clock's ticks after applying a phase setting (cfg_clk cycles). Quasi static.
8	DDLCAL_DDL_DLL	rw	ro	0x1	Select DDL or DLL calibration.
9	DDLCAL_UPDATE_SETTINGS	rw	ro	0x1	Flag to update the machine's settings.
11:10	DDLCAL_TUNE_MODE	rw	ro	0x2	Select phase setting to use during DDL calibration.
15:12	DDLCAL_WAIT	rw	ro	0x4	Wait time between DDL calibrations (in cfg_clk cycles) Quasi static.

1.1.1.77 PPI_RW_DDLCAL_CFG_3

Reg. 0x0E23

DDL calibration configurations
access : read-write

bits	name	s/w	h/w	default	description

11:0	DDLCAL_COUNTER_REF	rw	ro	0x47	Target number of ticks for the oscillation clock (cfg_clk cycles). Quasi static.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.78 PPI_RW_DDLCAL_CFG_4

Reg. 0x0E24

DDL calibration configurations
access : read-write

bits	name	s/w	h/w	default	description
11:0	DDLCAL_STUCK_THRESH	rw	ro	0x2	Minimum number of oscillation clock ticks not to flag stuck condition (cfg_clk cycles). Quasi static.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.79 PPI_RW_DDLCAL_CFG_5

Reg. 0x0E25

DDL calibration configurations
access : read-write

bits	name	s/w	h/w	default	description
3:0	DDLCAL_DDL_COARSE_BANK	rw	ro	0x0	Number of used coarse delay cells. Quasi static.
10:4	DDLCAL_DLL_FBK	rw	ro	0x7	Coarse delay output used as output of DLL. Quasi static.
11	HSRX_CDPHY_SEL_FAST	rw	ro	0x0	Coarse delay value switch. Quasi static. - 1'b0 : Bigger delay - 1'b1 : Smaller delay
12	DDLCAL_DDL_MANUAL_CAL	rw	ro	0x0	Override for the automatic DDL calibration settings (ddl_coarse_bank, dll_fbk). Quasi static.
14:13	DDLCAL_BIAS_CRITERIA	rw	ro	0x0	Bias selection criteria. Quasi static. - 2'b00 : Closest value to DDLCAL_TARGET_BIAS - 2'b01 : Maximum bias setting value - 2'b01 : Minimum bias setting value
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.80 PPI_RW_DDLCAL_CFG_6

Reg. 0x0E26

DDL calibration configurations
access : read-write

bits	name	s/w	h/w	default	description
11:0	DDLCAL_MAX_DIFF	rw	ro	0x64	Maximum difference towards target not to flag an error. Quasi static.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.81 PPI_RW_DDLCAL_CFG_7

Reg. 0x0E27

DDL calibration configurations
access : read-write

bits	name	s/w	h/w	default	description
6:0	DDLCAL_START_DELAY	rw	ro	0x32	Counter threshold for initial delay before DDL calibration start. (cfg_clk cycles). Quasi static
12:7	DDLCAL_DECR_WAIT	rw	ro	0xA	Counter threshold for ddl_en deassertion (cfg_clk cycles). Quasi static.
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.82 PPI_RW_DDLCAL_CFG_8

Reg. 0x0E28

DDL calibration configurations
access : read-write

bits	name	s/w	h/w	default	description
7:0	DDLCAL_DISABLE_TIME	rw	ro	0x0	Time the DDL is disabled after applying a phase setting (cfg_clk cycles). Quasi static.

13:8	DDLCAL_CLEAR_COUNT_THRESH	rw	ro	0x20	Counter threshold for the reset of the oscillation counter of the DDL calibration. (cfg_clk cycles). Quasi static.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.83 PPI_RW_DDLCAL_CFG_9

Reg. 0x0E29

DDL calibration configurations
access : read-write

bits	name	s/w	h/w	default	description
10:0	DDLCAL_INIT_PHASE	rw	ro	0x3F	Initial phase setting for DDL calibration. Quasi static.
15:11	DDLCAL_TARGET_BIAS	rw	ro	0x10	Target bias setting for DDL calibration. Quasi static.

1.1.1.84 PPI_R_DDLCAL_DEBUG_0

Reg. 0x0E2A

DDL calibration observability
access : read-only

bits	name	s/w	h/w	default	description
11:0	DDLCAL_COUNTER0	ro	ro	0x0	Value of the tick count for phase = 0. For observability purposes.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.85 PPI_R_DDLCAL_DEBUG_1

Reg. 0x0E2B

DDL calibration observability
access : read-only

bits	name	s/w	h/w	default	description
11:0	DDLCAL_COUNTERX	ro	ro	0x0	Value of the tick count for phase = X. For observability purposes.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.86 PPI_RW_CDRCAL_CFG_0

Reg. 0x0E2C

DDL calibration configurations
access : read-write

bits	name	s/w	h/w	default	description
6:0	CDRCAL_START_DELAY	rw	ro	0x32	Counter threshold for initial delay before CDR calibration start. (cfg_clk cycles). Quasi static
10:7	CDRCAL_WAIT	rw	ro	0x4	Wait time between CDR calibrations (in cfg_clk cycles) Quasi static.
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.87 PPI_RW_RXEQ_CFG_0

Reg. 0x0E2D

RX Equalization configurations
access : read-write

bits	name	s/w	h/w	default	description
2:0	RXEQ_INIT_LANE	rw	ro	0x0	Selects which lane to calibrate RX Equalization. Quasi static
15:3	RESERVED_15_3	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.89 PPI_RW_PARITY_TEST

Reg. 0x0E30

Parity test set and clear control
access : read-write

bits	name	s/w	h/w	default	description

0	CR_PARITY_TESTCLEAR	rw	ro	0x0	Parity error clear. Active high. In the presence of a parity error, output asserts and remains asserted until CR_PARITY_TESTCLEAR is asserted.
1	CR_PARITY_TESTSET	rw	ro	0x0	Parity error set. Active high. Set to force parity error to assert.
15:2	RESERVED_15_2	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.90 PPI_RW_STARTUP_OVR_0

Reg. 0x0E31

Override control for state in startup FSM
access : read-write

bits	name	s/w	h/w	default	description
4:0	STARTUP_STATE_OVR_VAL	rw	ro	0x0	Startup FMS state override value
15:5	RESERVED_15_5	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.91 PPI_RW_STARTUP_STATE_OVR_1

Reg. 0x0E32

Override control for state in startup FSM
access : read-write

bits	name	s/w	h/w	default	description
0	STARTUP_STATE_OVR_EN	rw	ro	0x0	Startup FMS state override enable
2:1	TXCLKESC_DRV_CFG	rw	ro	0x0	Escape clock driver configuration - 2'b00: Swap from cfg_clk_div to txclkesc during startup - 2'b01: Permanently driven with cfg_clk_div - 2'b10: Permanently driven with txclkesc - 2'b11: Reserved
15:3	RESERVED_15_3	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.92 PPI_RW_DTB_SELECTOR

Reg. 0x0E33

Selector control for DTB
access : read-write

bits	name	s/w	h/w	default	description
7:0	DTB_SELECT_ADDR	rw	ro	0x0	DTB selector address for soft macro signals
8	DTB_SOURCE_SELECT	rw	ro	0x0	DTB source selector : soft or hard macro
15:9	RESERVED_15_9	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.94 PPI_RW_DPHY_CLK_SPARE

Reg. 0x0E35

DPHY spare registers
access : read-write

bits	name	s/w	h/w	default	description
15:0	DPHY_CLK_LANE_SPARE	rw	ro	0x0	Spare registers for future use

1.1.1.95 PPI_RW_COMMON_CFG

Reg. 0x0E36

Common system configurations
access : read-write

bits	name	s/w	h/w	default	description
1:0	CFG_CLK_DIV_FACTOR	rw	ro	0x2	Selects cfg_clk division factor for txclkesc assignment. Quasi-static. - 2'b00 : No division - 2'b01 : Factor of 2 - 2'b10 : Factor of 4 - 2'b10 : Factor of 8

2	DPHY_HS_IDLE_EN	rw	ro	0x0	Enables support of DPHY HS-idle. Active high. Quasi-static.
3	GEN2_SEL	rw	ro	0x0	Controls the A2D interface width. Used to support higher data rates, up to DPHY 6.5Gbps and CPHY 6.5Gsps. Please check "Startup Sequence". Quasi static.
15:4	RESERVED_15_4	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.97 PPI_RW_TERMCAL_CFG_0

Reg. 0x0E40

Termination calibration configurations
access : read-write

bits	name	s/w	h/w	default	description
6:0	TERMCAL_TIMER	rw	ro	0x13	Period of atb_clk measured in cfg_clk cycles.
15:7	RESERVED_15_7	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.98 PPI_R_TERMCAL_DEBUG_0

Reg. 0x0E41

Termination calibration observability
access : read-only

bits	name	s/w	h/w	default	description
0	TERMCAL_COMP_UNCHANGED	ro	ro	0x0	Termination calibration error. Active high.
1	TERMCAL_CAL_ERROR	ro	ro	0x0	Termination calibration multi-toggle detection. Active high.
2	TERMCAL_CALDONE	ro	ro	0x0	Termination calibration done flag. Active high.
15:3	RESERVED_15_3	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.99 PPI_RW_TERMCAL_CTRL_0

Reg. 0x0E42

Termination calibration controllability
access : read-write

bits	name	s/w	h/w	default	description
0	TERMCAL_CALDONE_PULSE_OVR_VAL	rw	ro	0x0	termcal_caldone_pulse override value. Used for debug purposes.
1	TERMCAL_CALDONE_PULSE_OVR_EN	rw	ro	0x0	termcal_caldone_pulse override enable. Active high. Used for debug purposes.
2	TERMCAL_CALDONE_OVR_VAL	rw	ro	0x0	termcal_caldone override value. Used for debug purposes.
3	TERMCAL_CALDONE_OVR_EN	rw	ro	0x0	termcal_caldone override enable. Active high. Used for debug purposes.
15:4	RESERVED_15_4	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.101 PPI_RW_OFFSETCAL_CFG_0

Reg. 0x0E50

Offset calibration configurations
access : read-write

bits	name	s/w	h/w	default	description
4:0	OFFSETCAL_WAIT_THRESH	rw	ro	0x4	Wait threshold of 200ns from the time that the offsetcal setting is changed to the time that the DAC output is sampled. Configured in cfg_clk cycles.
5	OFFSETCAL_CALIB_MODE	rw	ro	0x0	Defines the offset calibration mode. - 1'b0 : Outputs default setting when no transition is detected on pre-amplifier. - 1'b1 : Outputs max or min setting depending on the inital state of the pre-amplifier if no transition is detected.
15:6	RESERVED_15_6	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.102 PPI_R_OFFSETCAL_DEBUG_LANE0

Reg. 0x0E51

Offset calibration observability

access : read-only

bits	name	s/w	h/w	default	description
3:0	OFFSETCAL_ERRCAL_RIGHT	ro	ro	0x0	Offset calibration error output from dclk lane rigth. Active high. - 4'b1xxx : Calibration error - An error has been detected - 4'b1001 : Calibration error - Lines did not toggle - 4'b1010 : Calibration error - One off the lines didn't toggle - 4'b1011 : Calibration error - Lines toggle during ramp up/down but not during ramp down/up - 4'b0000 : Calibration ok - Lines have toggled for different calibration words - 4'b0001 : Calibration ok - Lines have toggled for the same calibration word
7:4	OFFSETCAL_ERRCAL_LEFT	ro	ro	0x0	Offset calibration error output from dclk lane left. Active high. - 4'b1xxx : Calibration error - An error has been detected - 4'b1001 : Calibration error - Lines did not toggle - 4'b1010 : Calibration error - One off the lines didn't toggle - 4'b1011 : Calibration error - Lines toggle during ramp up/down but not during ramp down/up - 4'b0000 : Calibration ok - Lines have toggled for different calibration words - 4'b0001 : Calibration ok - Lines have toggled for the same calibration word
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.103 PPI_R_OFFSETCAL_DEBUG_LANE1

Reg. 0x0E52

Offset calibration observability
access : read-only

bits	name	s/w	h/w	default	description
3:0	OFFSETCAL_ERRCAL_RIGHT	ro	ro	0x0	Offset calibration error output from dclk lane rigth. Active high. - 4'b1xxx : Calibration error - An error has been detected - 4'b1001 : Calibration error - Lines did not toggle - 4'b1010 : Calibration error - One off the lines didn't toggle - 4'b1011 : Calibration error - Lines toggle during ramp up/down but not during ramp down/up - 4'b0000 : Calibration ok - Lines have toggled for different calibration words - 4'b0001 : Calibration ok - Lines have toggled for the same calibration word
7:4	OFFSETCAL_ERRCAL_LEFT	ro	ro	0x0	Offset calibration error output from dclk lane left. Active high. - 4'b1xxx : Calibration error - An error has been detected - 4'b1001 : Calibration error - Lines did not toggle - 4'b1010 : Calibration error - One off the lines didn't toggle - 4'b1011 : Calibration error - Lines toggle during ramp up/down but not during ramp down/up - 4'b0000 : Calibration ok - Lines have toggled for different calibration words - 4'b0001 : Calibration ok - Lines have toggled for the same calibration word
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.104 PPI_R_OFFSETCAL_DEBUG_LANE2

Reg. 0x0E53

Offset calibration observability
access : read-only

bits	name	s/w	h/w	default	description
3:0	OFFSETCAL_ERRCAL_RIGHT	ro	ro	0x0	Offset calibration error output from dclk lane rigth. Active high. - 4'b1xxx : Calibration error - An error has been detected - 4'b1001 : Calibration error - Lines did not toggle - 4'b1010 : Calibration error - One off the lines didn't toggle

					- 4'b1011 : Calibration error - Lines toggle during ramp up/ down but not during ramp down/up - 4'b0000 : Calibration ok - Lines have toggled for different calibration words - 4'b0001 : Calibration ok - Lines have toggled for the same calibration word
7:4	OFFSETCAL_ERRCAL_LEFT	ro	ro	0x0	Offset calibration error output from dclk lane left. Active high. - 4'b1xxx : Calibration error - An error has been detected - 4'b1001 : Calibration error - Lines did not toggle - 4'b1010 : Calibration error - One off the lines didn't toggle - 4'b1011 : Calibration error - Lines toggle during ramp up/ down but not during ramp down/up - 4'b0000 : Calibration ok - Lines have toggled for different calibration words - 4'b0001 : Calibration ok - Lines have toggled for the same calibration word
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.106 PPI_RW_OFFSETCAL_CFG_1

Reg. 0x0E56

Offset calibration configurations
access : read-write

bits	name	s/w	h/w	default	description
7:0	OFFSETCAL_WRD_2	rw	ro	0x0	Defines the offset calibration word when no transition is detected on input and comparator output bit[1]=0.
15:8	OFFSETCAL_WRD_1	rw	ro	0xFF	Defines the offset calibration word when no transition is detected on input and comparator output bit[1]=1.

1.1.1.108 PPI_RW_HSDCOCAL_CFG_O

Reg. 0x0E80

HS-DCO calibration control
access : read-write

bits	name	s/w	h/w	default	description
9:0	HSDCOCAL_SELDAC_INIT_POINT	rw	ro	0x100	Configure sel_dac initial point value. This field is quasi-static.
10	HSDCOCAL_UPDATE_SETTINGS	rw	ro	0x0	Flag to update the machine's settings. Active high.
11	HSDCOCAL_BYPASS_FWORD	rw	ro	0x0	Flag to bypass f_word calibration. Active high.
12	HSDCOCAL_ENABLE_OVR_VAL	rw	ro	0x0	calibctrl o_hsdcocal_cal_en override value.
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.109 PPI_RW_HSDCOCAL_CFG_1

Reg. 0x0E81

HS-DCO calibration control
access : read-write

bits	name	s/w	h/w	default	description
7:0	HSDCOCAL_WAIT_SELDAC	rw	ro	0x1	Counter (in cfg_clk cycles) which controls the settling time between changing sel_dac configuration and trigger new DCO clock measure. This field is quasi-static.
15:8	HSDCOCAL_WAIT_PON	rw	ro	0x1	Counter (in cfg_clk cycles) which controls the settling time between powering on the analog circuitry (pon) and starting the calibration (enable). This field is quasi-static.

1.1.1.110 PPI_RW_HSDCOCAL_CFG_2

Reg. 0x0E82

HS-DCO calibration control
access : read-write

bits	name	s/w	h/w	default	description

7:0	HSDCOCAL_ENABLE_DLY	rw	ro	0x1	Counter (in cfg_clk cycles) which controls the settling time between tune_clkdig_en deassertion and AFE enable de-assertion. This field is quasi-static.
15:8	HSDCOCAL_TUNE_CLKDIG_ENABLE_DLY	rw	ro	0xC7	Counter (in cfg_clk cycles) which controls the settling time between AFE enable and tune_clkdig_en. This field is quasi-static.

1.1.1.111 PPI_RW_HSDCOCAL_CFG_3

Reg. 0x0E83

HS-DCO calibration control
access : read-write

bits	name	s/w	h/w	default	description
7:0	HSDCOCAL_FWORD_DISABLE_TIME	rw	ro	0x1	Counter (in cfg_clk cycles) which controls the settling time between enable deassertion and changing f_word configuration. This field is quasi-static.
15:8	HSDCOCAL_FWORD_ENABLE_TIME	rw	ro	0x1	Counter (in cfg_clk cycles) which controls the settling time between changing f_word configuration and enable assertion. This field is quasi-static.

1.1.1.112 PPI_RW_HSDCOCAL_CFG_4

Reg. 0x0E84

HS-DCO calibration control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HSDCOCAL_N_REF	rw	ro	0x0	Sets HSDCO calibration target: number of expected HSDCO clock ticks observed within measurement window. This field is quasi-static.

1.1.1.113 PPI_RW_HSDCOCAL_CFG_5

Reg. 0x0E85

HS-DCO calibration control
access : read-write

bits	name	s/w	h/w	default	description
0	HSDCOCAL_ENABLE_OVR_EN	rw	ro	0x0	calibctrl o_hsdcocal_cal_en override enable. Active high.
8:1	HSDCOCAL_TIMEBASE_TARGET	rw	ro	0x13	Timebase for oscillation clock measurement (cfg_clk cycles). This field is quasi-static.
15:9	RESERVED_15_9	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.114 PPI_RW_HSDCOCAL_CFG_6

Reg. 0x0E86

HS-DCO calibration control
access : read-write

bits	name	s/w	h/w	default	description
9:0	HSDCOCAL_SELDAC_UP_LIMIT	rw	ro	0x1FF	Configure sel_dac upper limit value. This field is quasi-static.
15:10	RESERVED_15_10	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.115 PPI_RW_HSDCOCAL_CFG_7

Reg. 0x0E87

HS-DCO calibration control
access : read-write

bits	name	s/w	h/w	default	description
9:0	HSDCOCAL_SELDAC_DOWN_LIMIT	rw	ro	0x0	Configure sel_dac lower limit value. This field is quasi-static.
15:10	RESERVED_15_10	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.116 PPI_RW_HSDCOCAL_CFG_8

Reg. 0x0E88

HS-DCO calibration control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HSDCOCAL_N_REF_RANGE	rw	ro	0x0	Sets HSDCO calibration target frequency range. This field is quasi-static.

1.1.1.117 PPI_R_HSDCOCAL_DEBUG_RB

Reg. 0x0E89

HS-DCO calibration observability
access : read-only

bits	name	s/w	h/w	default	description
3:0	HSDCOCAL_STATE	ro	ro	0x0	Power-on FSM current state.
6:4	HSDCOCAL_ERROR	ro	ro	0x0	Power-on calibration error. Target frequency not reached.
7	HSDCOCAL_DONE	ro	ro	0x0	Power-on calibration has successfully finished. Active high.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.119 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE0_OVR_0

Reg. 0x1000

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXACTIVEHS_D0_OVR_VAL	rw	ro	0x0	o_rxactivehs_d0_ override value. Used for debug purposes.
1	O_RXSYNCHS_D0_OVR_VAL	rw	ro	0x0	o_rxsynchs_d0_ override value. Used for debug purposes.
3:2	O_RXVALIDHS_D0_OVR_VAL	rw	ro	0x0	o_rxvalidhs_d0_ override value. Used for debug purposes.
4	O_RXSKEWCALHS_D0_OVR_VAL	rw	ro	0x0	o_rxskewcalhs_d0_ override value. Used for debug purposes.
5	O_RXWORDCLKHS_D0_OVR_VAL	rw	ro	0x0	o_rxwordclkhs_d0_ override value. Used for debug purposes.
6	O_RXALTERNATECALHS_D0_OVR_VAL	rw	ro	0x0	o_rxalternatecalhs_d0 override value. Used for debug purposes.
15:7	RESERVED_15_7	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.120 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE0_OVR_1

Reg. 0x1001

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_D0_OVR_VAL	rw	ro	0x0	o_rxdatahs_d0 override value. Used for debug purposes.

1.1.1.121 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE0_OVR_2

Reg. 0x1002

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXACTIVEHS_D0_OVR_EN	rw	ro	0x0	o_rxactivehs_d0 override enable. Active high. Used for debug purposes.
1	O_RXSYNCHS_D0_OVR_EN	rw	ro	0x0	o_rxsynchs_d0 override enable. Active high. Used for debug purposes.
2	O_RXVALIDHS_D0_OVR_EN	rw	ro	0x0	o_rxvalidhs_d0 override enable. Active high. Used for debug purposes.
3	O_RXSKEWCALHS_D0_OVR_EN	rw	ro	0x0	o_rxskewcalhs_d0 override enable. Active high. Used for debug purposes.

4	O_RXWORDCLKHS_D0_OVR_EN	rw	ro	0x0	o_rxwordclkhs_d0 override enable. Active high. Used for debug purposes.
5	O_RXDATAHS_D0_OVR_EN	rw	ro	0x0	o_rxdatahs_d0 override enable. Active high. Used for debug purposes.
6	I_TXREQUESTHS_D0_OVR_EN	rw	ro	0x0	i_txrequesths_d0 override enable. Active high. Used for debug purposes.
7	I_TXDATATRANSFERENHS_D0_OVR_EN	rw	ro	0x0	i_txdatatransferenhs_d0 override enable. Active high. Used for debug purposes.
8	O_TXREADYHS_D0_OVR_EN	rw	ro	0x0	o_txreadyhs_d0 override enable. Active high. Used for debug purposes.
9	O_TXWORDCLKHS_D0_OVR_EN	rw	ro	0x0	o_txwordclkhs_d0 override enable. Active high. Used for debug purposes.
10	I_TXDATAHS_D0_OVR_EN	rw	ro	0x0	i_txdatahs_d0 override enable. Active high. Used for debug purposes.
11	O_RXALTERNATECALHS_D0_OVR_EN	rw	ro	0x0	o_rxalternatecalhs_d0 override enable. Active high. Used for debug purposes.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.122 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE0_OVR_3

Reg. 0x1003

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXCLKESC_D0_OVR_VAL	rw	ro	0x0	o_rxclkesc_d0 override value. Used for debug purposes.
1	O_RXLPDTESC_D0_OVR_VAL	rw	ro	0x0	o_rxlpdtesc_d0 override value. Used for debug purposes.
2	O_RXULPSESC_D0_OVR_VAL	rw	ro	0x0	o_rxulpsesc_d0 override value. Used for debug purposes.
3	O_RXVALIDESC_D0_OVR_VAL	rw	ro	0x0	o_rxvalidesc_d0 override value. Used for debug purposes.
7:4	O_RXTRIGGERESC_D0_OVR_VAL	rw	ro	0x0	o_rxtriggeresc_d0 override value. Used for debug purposes.
15:8	O_RXDATAESC_D0_OVR_VAL	rw	ro	0x0	o_rxdataesc_d0 override value. Used for debug purposes.

1.1.1.123 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE0_OVR_4

Reg. 0x1004

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXCLKESC_D0_OVR_EN	rw	ro	0x0	o_rxclkesc_d0 override enable. Active high. Used for debug purposes.
1	O_RXLPDTESC_D0_OVR_EN	rw	ro	0x0	o_rxlpdtesc_d0 override enable. Active high. Used for debug purposes.
2	O_RXULPSESC_D0_OVR_EN	rw	ro	0x0	o_rxulpsesc_d0 override enable. Active high. Used for debug purposes.
3	O_RXVALIDESC_D0_OVR_EN	rw	ro	0x0	o_rxvalidesc_d0 override enable. Active high. Used for debug purposes.
4	O_RXTRIGGERESC_D0_OVR_EN	rw	ro	0x0	o_rxtriggeresc_d0 override enable. Active high. Used for debug purposes.
5	O_RXDATAESC_D0_OVR_EN	rw	ro	0x0	o_rxdataesc_d0 override enable. Active high. Used for debug purposes.
15:6	RESERVED_15_6	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.124 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE0_OVR_5

Reg. 0x1005

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description

15:0	I_TXDATAHS_D0_OVR_VAL	rw	ro	0x0	i_txdatahs_d0 override value. Used for debug purposes.

1.1.1.125 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE0_OVR_6

Reg. 0x1006

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_TXREQUESTHS_D0_OVR_VAL	rw	ro	0x0	i_txrequesths_d0 override value. Used for debug purposes.
1	I_TXDATATRANSFERENHS_D0_OVR_VAL	rw	ro	0x0	i_txdatatransferenhs_d0 override value. Used for debug purposes.
2	O_TXREADYHS_D0_OVR_VAL	rw	ro	0x0	o_txreadyhs_d0 override value. Used for debug purposes.
3	O_TXWORDCLKHS_D0_OVR_VAL	rw	ro	0x0	o_txwordclkhs_d0 override value. Used for debug purposes.
4	I_TXSKEWCALHS_D0_OVR_VAL	rw	ro	0x0	i_txskewcalhs_d0 override value. Used for debug purposes.
15:5	RESERVED_15_5	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.126 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE0_OVR_7

Reg. 0x1007

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_TXREQUESTESC_D0_OVR_VAL	rw	ro	0x0	i_txrequestesc_d0 override value. Used for debug purposes.
1	I_TXLPDTESC_D0_OVR_VAL	rw	ro	0x0	i_txlpdtesc_d0 override value. Used for debug purposes.
2	I_TXULPSEXIT_D0_OVR_VAL	rw	ro	0x0	i_txulpsexit_d0 override value. Used for debug purposes.
3	I_TXULPSESC_D0_OVR_VAL	rw	ro	0x0	i_txulpsesc_d0 override value. Used for debug purposes.
4	I_TXVALIDESC_D0_OVR_VAL	rw	ro	0x0	i_txvalidesc_d0 override value. Used for debug purposes.
5	O_TXREADYESC_D0_OVR_VAL	rw	ro	0x0	o_txreadyesc_d0 override value. Used for debug purposes.
9:6	I_TXTRIGGERESC_D0_OVR_VAL	rw	ro	0x0	i_txtriggeresc_d0 override value. Used for debug purposes.
10	I_TXDATAESC_D0_OVR_EN	rw	ro	0x0	i_txdataesc_d0 override enable. Active high. Used for debug purposes.
11	I_TXALTERNATECALHS_D0_OVR_EN	rw	ro	0x0	i_txalternatecalhs_d0 override enable. Active high. Used for debug purposes.
12	I_TXSKEWCALHS_D0_OVR_EN	rw	ro	0x0	i_txskewcalhs_d0 override enable. Active high. Used for debug purposes.
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.127 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE0_OVR_8

Reg. 0x1008

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_TXREQUESTESC_D0_OVR_EN	rw	ro	0x0	i_txrequestesc_d0 override enable. Active high. Used for debug purposes.
1	I_TXLPDTESC_D0_OVR_EN	rw	ro	0x0	i_txlpdtesc_d0 override enable. Active high. Used for debug purposes.
2	I_TXULPSEXIT_D0_OVR_EN	rw	ro	0x0	i_txulpsexit_d0override enable. Active high. Used for debug purposes.

3	I_TXULPSESC_D0_OVR_EN	rw	ro	0x0	i_txulpsesc_d0override enable. Active high. Used for debug purposes.
4	I_TXVALIDESC_D0_OVR_EN	rw	ro	0x0	i_txvalidesc_d0 override enable. Active high. Used for debug purposes.
5	O_TXREADYESC_D0_OVR_EN	rw	ro	0x0	o_txreadyesc_d0override enable. Active high. Used for debug purposes.
6	I_TXTRIGGERESC_D0_OVR_EN	rw	ro	0x0	i_txtriggeresc_d0override enable. Active high. Used for debug purposes.
14:7	I_TXDATAESC_D0_OVR_VAL	rw	ro	0x0	i_txdataesc_d0 override value. Used for debug purposes.
15	I_TXALTERNATECALHS_D0_OVR_VAL	rw	ro	0x0	i_txalternatecalhs_d0 override value. Used for debug purposes.

1.1.1.128 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE0_OVR_9

Reg. 0x1009

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_ENABLE_D0_OVR_VAL	rw	ro	0x0	i_enable_d0 override value. Used for debug purposes.
1	O_STOPSTATE_D0_OVR_VAL	rw	ro	0x0	o_stopstate_d0 override value. Used for debug purposes.
2	O_ULPSACTIVENOT_D0_OVR_VAL	rw	ro	0x0	o_ulpsactivenot_d0 override value. Used for debug purposes.
3	I_TURNREQUEST_D0_OVR_VAL	rw	ro	0x0	i_turnrequest_d0 override value. Used for debug purposes.
4	I_TURNDISABLE_D0_OVR_VAL	rw	ro	0x0	i_turndisable_d0 override value. Used for debug purposes.
5	O_DIRECTION_D0_OVR_VAL	rw	ro	0x0	o_direction_d0 override value. Used for debug purposes.
6	I_FORCERXMODE_D0_OVR_VAL	rw	ro	0x0	i_forcerxmode_d0 override value. Used for debug purposes.
7	I_FORCETXSTOPMODE_D0_OVR_VAL	rw	ro	0x0	i_forcetxstopmode_d0 override value. Used for debug purposes.
8	O_ERRESC_D0_OVR_VAL	rw	ro	0x0	o_erresc_d0 override value. Used for debug purposes.
9	O_ERRSYNCESC_D0_OVR_VAL	rw	ro	0x0	o_errsyncesc_d0 override value. Used for debug purposes.
10	O_ERRCONTROL_D0_OVR_VAL	rw	ro	0x0	o_errcontrol_d0 override value. Used for debug purposes.
11	O_ERRCONTENTIONLP0_D0_OVR_VAL	rw	ro	0x0	o_errcontentionlp0_d0 override value. Used for debug purposes.
12	O_ERRCONTENTIONLP1_D0_OVR_VAL	rw	ro	0x0	o_errcontentionlp1_d0 override value. Used for debug purposes.
13	O_ERRSOTHS_D0_OVR_VAL	rw	ro	0x0	o_errsoths_d0 override value. Used for debug purposes.
14	O_ERRSOTSYNCHS_D0_OVR_VAL	rw	ro	0x0	o_errsotsynchs_d0 override value. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.129 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE0_OVR_10

Reg. 0x100A

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_ENABLE_D0_OVR_EN	rw	ro	0x0	i_enable_d0 override enable. Active high. Used for debug purposes.
1	O_STOPSTATE_D0_OVR_EN	rw	ro	0x0	o_stopstate_d0 override enable. Active high. Used for debug purposes.
2	O_ULPSACTIVENOT_D0_OVR_EN	rw	ro	0x0	o_ulpsactivenot_d0 override enable. Active high. Used for debug purposes.

3	I_TURNREQUEST_D0_OVR_EN	rw	ro	0x0	i_turnrequest_d0 override enable. Active high. Used for debug purposes.
4	I_TURNDISABLE_D0_OVR_EN	rw	ro	0x0	i_turndisable_d0 override enable. Active high. Used for debug purposes.
5	O_DIRECTION_D0_OVR_EN	rw	ro	0x0	o_direction_d0 override enable. Active high. Used for debug purposes.
6	I_FORCERXMODE_D0_OVR_EN	rw	ro	0x0	i_forcerxmode_d0 override enable. Active high. Used for debug purposes.
7	I_FORCETXSTOPMODE_D0_OVR_EN	rw	ro	0x0	i_forcetxstopmode_d0 override enable. Active high. Used for debug purposes.
8	O_ERRESC_D0_OVR_EN	rw	ro	0x0	o_erresc_d0 override enable. Active high. Used for debug purposes.
9	O_ERRSYNCESC_D0_OVR_EN	rw	ro	0x0	o_errsyncesc_d0 override enable. Active high. Used for debug purposes.
10	O_ERRCONTROL_D0_OVR_EN	rw	ro	0x0	o_errcontrol_d0 override enable. Active high. Used for debug purposes.
11	O_ERRCONTENTIONLP0_D0_OVR_EN	rw	ro	0x0	o_errcontentionlp0_d0 override enable. Active high. Used for debug purposes.
12	O_ERRCONTENTIONLP1_D0_OVR_EN	rw	ro	0x0	o_errcontentionlp1_d0 override enable. Active high. Used for debug purposes.
13	O_ERRSOTHS_D0_OVR_EN	rw	ro	0x0	o_errsoths_d0 override enable. Active high. Used for debug purposes.
14	O_ERRSOTSYNCHS_D0_OVR_EN	rw	ro	0x0	o_errsotsynchs_d0 override enable. Active high. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.131 CORE_DIG_IOCTRL_R_DPHY_PPI_LANE0_OVR_0

Reg. 0x1010

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
0	O_RXACTIVEHS_D0	ro	rw	0x0	o_rxactivehs_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	O_RXSYNCHS_D0	ro	rw	0x0	o_rxsynchs_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
3:2	O_RXVALIDHS_D0	ro	rw	0x0	o_rxvalidhs_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
4	O_RXSKEWCALHS_D0	ro	rw	0x0	o_rxskewcalhs_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
5	O_RXWORDCLKHS_D0	ro	rw	0x0	o_rxwordclkhs_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
6	O_RXALTERNATECALHS_D0	ro	rw	0x0	o_rxalternatecalhs_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:7	RESERVED_15_7	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.132 CORE_DIG_IOCTRL_R_DPHY_PPI_LANE0_OVR_1

Reg. 0x1011

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_D0	ro	rw	0x0	o_rxdatahs_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.133 CORE_DIG_IOCTRL_R_DPHY_PPI_LANE0_OVR_2

Reg. 0x1012

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	I_TXDATAHS_D0_INT	ro	rw	0x0	i_txdatahs_d0_int override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.134 CORE_DIG_IOCTRL_R_DPHY_PPI_LANE0_OVR_3

Reg. 0x1013

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
0	I_TXREQUESTESC_D0_INT	ro	rw	0x0	i_txrequestesc_d0_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	I_TXLPDTESC_D0_INT	ro	rw	0x0	i_txlpdtesc_d0_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
2	I_TXULPSEXIT_D0_INT	ro	rw	0x0	i_txulpsexit_d0_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
3	I_TXULPSESC_D0_INT	ro	rw	0x0	i_txulpsesc_d0_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
4	I_TXVALIDESC_D0_INT	ro	rw	0x0	i_txvalidesc_d0_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
5	O_TXREADYESC_D0	ro	rw	0x0	o_txreadyesc_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
9:6	I_TXTRIGGERESC_D0_INT	ro	rw	0x0	i_txtriggeresc_d0_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
10	I_TXALTERNATECALHS_D0_INT	ro	rw	0x0	i_txalternatecalhs_d0_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
11	I_TXSKEWCALHS_D0_INT	ro	rw	0x0	i_txskewcalhs_d0_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
12	I_TXREQUESTHS_D0_INT	ro	rw	0x0	i_txrequesths_d0_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
13	I_TXDATATRANSFERENHS_D0_INT	ro	rw	0x0	i_txdatatransferenhs_d0_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
14	O_TXREADYHS_D0	ro	rw	0x0	o_txreadyhs_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15	O_TXWORDCLKHS_D0	ro	rw	0x0	o_txwordclkhs_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.135 CORE_DIG_IOCTRL_R_DPHY_PPI_LANE0_OVR_4

Reg. 0x1014

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
7:0	I_TXDATAESC_D0_INT	ro	rw	0x0	i_txdataesc_d0_int override multiplexer output. Used for debug purposes. (volatile) volatile : true

15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.136 CORE_DIG_IOCTRL_R_DPHY_PPI_LANE0_OVR_5

Reg. 0x1015

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
0	O_RXCLKESC_D0	ro	rw	0x0	o_rxclkesc_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	O_RXLPDTESC_D0	ro	rw	0x0	o_rxlpdtesc_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
2	O_RXULPSESC_D0	ro	rw	0x0	o_rxulpsesc_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
3	O_RXVALIDESC_D0	ro	rw	0x0	o_rxvalidesc_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
7:4	O_RXTRIGGERESC_D0	ro	rw	0x0	o_rxtriggeresc_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:8	O_RXDATAESC_D0	ro	rw	0x0	o_rxdataesc_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.137 CORE_DIG_IOCTRL_R_DPHY_PPI_LANE0_OVR_6

Reg. 0x1016

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
0	I_ENABLE_D0_INT	ro	rw	0x0	i_enable_d0_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	O_STOPSTATE_D0	ro	rw	0x0	o_stopstate_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
2	O_ULPSACTIVENOT_D0	ro	rw	0x0	o_ulpsactivenot_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
3	I_TURNREQUEST_D0_INT	ro	rw	0x0	i_turnrequest_d0_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
4	I_TURNDISABLE_D0_INT	ro	rw	0x0	i_turndisable_d0_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
5	O_DIRECTION_D0	ro	rw	0x0	o_direction_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
6	I_FORCERXMODE_D0_INT	ro	rw	0x0	i_forcerxmode_d0_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
7	I_FORCETXSTOPMODE_D0_INT	ro	rw	0x0	i_forcetxstopmode_d0_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
8	O_ERRESC_D0	ro	rw	0x0	o_erresc_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
9	O_ERRSYNCESC_D0	ro	rw	0x0	o_errsyncesc_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
10	O_ERRCONTROL_D0	ro	rw	0x0	o_errcontrol_d0 override multiplexer output. Used for debug purposes. (volatile)

					volatile : true
11	O_ERRCONTENTIONLP0_D0	ro	rw	0x0	o_errcontentionlp0_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
12	O_ERRCONTENTIONLP1_D0	ro	rw	0x0	o_errcontentionlp1_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
13	O_ERRSOTHS_D0	ro	rw	0x0	o_errsoths_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
14	O_ERRSOTSYNCHS_D0	ro	rw	0x0	o_errsotsynchs_d0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.139 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE0_OVR_0

Reg. 0x1020

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_C0_OVR_VAL	rw	ro	0x0	o_rxdatahs_c0 override value. Used for debug purposes.

1.1.1.140 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE0_OVR_1

Reg. 0x1021

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_C0_OVR_VAL	rw	ro	0x0	o_rxdatahs_c0 override value. Used for debug purposes.

1.1.1.141 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE0_OVR_2

Reg. 0x1022

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXACTIVEHS_C0_OVR_VAL	rw	ro	0x0	o_rxactivehs_c0 override value. Used for debug purposes.
2:1	O_RXSYNCHS_C0_OVR_VAL	rw	ro	0x0	o_rxsynchs_c0 override value. Used for debug purposes.
4:3	O_RXVALIDHS_C0_OVR_VAL	rw	ro	0x0	o_rxvalidhs_c0 override value. Used for debug purposes.
6:5	O_RXINVALIDCODEHS_C0_OVR_VAL	rw	ro	0x0	o_rxinvalidcodehs_c0 override value. Used for debug purposes.
7	O_RXWORDCLKHS_C0_OVR_VAL	rw	ro	0x0	o_rxwordclkhs_c0 override value. Used for debug purposes.
10:8	O_RXSYNCTYPEHS0_C0_OVR_VAL	rw	ro	0x0	o_rxsynctypehs0_c0 override value. Used for debug purposes.
13:11	O_RXSYNCTYPEHS1_C0_OVR_VAL	rw	ro	0x0	o_rxsynctypehs1_c0 override value. Used for debug purposes.
15:14	O_RXALPVALIDHS_C0_OVR_VAL	rw	ro	0x0	o_rxalpvalidhs_c0 override value. Used for debug purposes.

1.1.1.142 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE0_OVR_3

Reg. 0x1023

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXALPVALIDHS_C0_OVR_EN	rw	ro	0x0	o_rxalpvalidhs_c0 override enable. Active high. Used for debug purposes.
4:1	O_RXALPCODE0_C0_OVR_VAL	rw	ro	0x0	o_rxalpcode0_c0 override value. Used for debug purposes.
8:5	O_RXALPCODE1_C0_OVR_VAL	rw	ro	0x0	o_rxalpcode1_c0 override value. Used for debug purposes.
9	O_RXALPNIBBLE0_C0_OVR_EN	rw	ro	0x0	o_rxalpnibble0_c0 override enable. Active high. Used for debug purposes.
10	O_RXALPNIBBLE1_C0_OVR_EN	rw	ro	0x0	o_rxalpnibble1_c0 override enable. Active high. Used for debug purposes.
11	O_RXACTIVEHS_C0_OVR_EN	rw	ro	0x0	o_rxactivehs_c0 override enable. Active high. Used for debug purposes.
12	O_RXSYNCHS_C0_OVR_EN	rw	ro	0x0	o_rxsynchs_c0 override enable. Active high. Used for debug purposes.
13	O_RXVALIDHS_C0_OVR_EN	rw	ro	0x0	o_rxvalidhs_c0 override enable. Active high. Used for debug purposes.
14	O_RXINVALIDCODEHS_C0_OVR_EN	rw	ro	0x0	o_rxinvalidcodehs_c0 override enable. Active high. Used for debug purposes.
15	O_RXWORDCLKHS_C0_OVR_EN	rw	ro	0x0	o_rxwordclkhs_c0 override enable. Active high. Used for debug purposes.

1.1.1.143 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE0_OVR_4

Reg. 0x1024

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXSYNCTYPEHS0_C0_OVR_EN	rw	ro	0x0	o_rxsynctypehs0_c0 override enable. Active high. Used for debug purposes.
1	O_RXSYNCTYPEHS1_C0_OVR_EN	rw	ro	0x0	o_rxsynctypehs1_c0 override enable. Active high. Used for debug purposes.
2	O_RXDATAHS_C0_OVR_EN	rw	ro	0x0	o_rxdatahs_c0 override enable. Active high. Used for debug purposes.
6:3	O_RXALPNIBBLE0_C0_OVR_VAL	rw	ro	0x0	o_rxalpnibble0_c0 override value. Used for debug purposes.
10:7	O_RXALPNIBBLE1_C0_OVR_VAL	rw	ro	0x0	o_rxalpnibble1_c0 override value. Used for debug purposes.
11	O_RXALPCODE0_C0_OVR_EN	rw	ro	0x0	o_rxalpcode0_c0 override enable. Active high. Used for debug purposes.
12	O_RXALPCODE1_C0_OVR_EN	rw	ro	0x0	o_rxalpcode1_c0 override enable. Active high. Used for debug purposes.
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.144 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE0_OVR_5

Reg. 0x1025

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
2:0	I_TXSYNCTYPEHS0_C0_OVR_VAL	rw	ro	0x0	i_txsynctypehs0_c0 override value. Used for debug purposes.
5:3	I_TXSYNCTYPEHS1_C0_OVR_VAL	rw	ro	0x0	i_txsynctypehs1_c0 override value. Used for debug purposes.
7:6	I_TXSENDSYNCHS_C0_OVR_VAL	rw	ro	0x0	i_txsendsynchs_c0 override value. Used for debug purposes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.145 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE0_OVR_6

Reg. 0x1026

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	I_TXDATAHS_C0_OVR_VAL	rw	ro	0x0	i_txdatahs_c0 override value. Used for debug purposes.

1.1.1.146 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE0_OVR_7

Reg. 0x1027

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	I_TXDATAHS_C0_OVR_VAL	rw	ro	0x0	i_txdatahs_c0 override value. Used for debug purposes.

1.1.1.147 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE0_OVR_8

Reg. 0x1028

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_TXREQUESTESC_C0_OVR_VAL	rw	ro	0x0	i_txrequestesc_c0 override value. Used for debug purposes.
1	I_TXLPDTESC_C0_OVR_VAL	rw	ro	0x0	i_txlpdtesc_c0 override value. Used for debug purposes.
2	I_TXULPSEXIT_C0_OVR_VAL	rw	ro	0x0	i_txulpsexit_c0 override value. Used for debug purposes.
3	I_TXULPSESC_C0_OVR_VAL	rw	ro	0x0	i_txulpsesc_c0 override value. Used for debug purposes.
4	I_TXVALIDESC_C0_OVR_VAL	rw	ro	0x0	i_txvalidesc_c0 override value. Used for debug purposes.
5	O_TXREADYESC_C0_OVR_VAL	rw	ro	0x0	o_txreadyesc_c0 override value. Used for debug purposes.
9:6	I_TXTRIGGERESC_C0_OVR_VAL	rw	ro	0x0	i_txtriggeresc_c0 override value. Used for debug purposes.
10	I_TXDATAESC_C0_OVR_EN	rw	ro	0x0	i_txdataesc_c0 override enable. Active high. Used for debug purposes.
11	I_TXREQUESTHS_C0_OVR_VAL	rw	ro	0x0	i_txrequesths_c0 override value. Used for debug purposes.
12	I_TXDATATRANSFERENHS_C0_OVR_VAL	rw	ro	0x0	i_txdatatransferenhs_c0 override value. Used for debug purposes.
13	O_TXREADYHS_C0_OVR_VAL	rw	ro	0x0	o_txreadyhs_c0 override value. Used for debug purposes.
14	O_TXWORDCLKHS_C0_OVR_VAL	rw	ro	0x0	o_txwordclkhs_c0 override value. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.148 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE0_OVR_9

Reg. 0x1029

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_TXREQUESTESC_C0_OVR_EN	rw	ro	0x0	i_txrequestesc_c0 override enable. Active high. Used for debug purposes.
1	I_TXLPDTESC_C0_OVR_EN	rw	ro	0x0	i_txlpdtesc_c0 override enable. Active high. Used for debug purposes.
2	I_TXULPSEXIT_C0_OVR_EN	rw	ro	0x0	i_txulpsexit_c0 override enable. Active high. Used for debug purposes.
3	I_TXULPSESC_C0_OVR_EN	rw	ro	0x0	i_txulpsesc_c0 override enable. Active high. Used for debug purposes.
4	I_TXVALIDESC_C0_OVR_EN	rw	ro	0x0	i_txvalidesc_c0 override enable. Active high. Used for debug purposes.

5	O_TXREADYESC_C0_OVR_EN	rw	ro	0x0	o_txreadyesc_c0 override enable. Active high. Used for debug purposes.
6	I_TXTRIGGERESC_C0_OVR_EN	rw	ro	0x0	i_txtriggeresc_c0 override enable. Active high. Used for debug purposes.
14:7	I_TXDATAESC_C0_OVR_VAL	rw	ro	0x0	i_txdataesc_c0 override value. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.149 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE0_OVR_10

Reg. 0x102A

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXCLKESC_C0_OVR_VAL	rw	ro	0x0	o_rxclkesc_c0 override value. Used for debug purposes.
1	O_RXLPDTESC_C0_OVR_VAL	rw	ro	0x0	o_rxlpdtesc_c0 override value. Used for debug purposes.
2	O_RXULPSESC_C0_OVR_VAL	rw	ro	0x0	o_rxulpsesc_c0 override value. Used for debug purposes.
3	O_RXVALIDESC_C0_OVR_VAL	rw	ro	0x0	o_rxvalidesc_c0 override value. Used for debug purposes.
7:4	O_RXTRIGGERESC_C0_OVR_VAL	rw	ro	0x0	o_rxtriggeresc_c0 override value. Used for debug purposes.
15:8	O_RXDATAESC_C0_OVR_VAL	rw	ro	0x0	o_rxdataesc_c0 override value. Used for debug purposes.

1.1.1.150 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE0_OVR_11

Reg. 0x102B

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXCLKESC_C0_OVR_EN	rw	ro	0x0	o_rxclkesc_c0 override enable. Active high. Used for debug purposes.
1	O_RXLPDTESC_C0_OVR_EN	rw	ro	0x0	o_rxlpdtesc_c0 override enable. Active high. Used for debug purposes.
2	O_RXULPSESC_C0_OVR_EN	rw	ro	0x0	o_rxulpsesc_c0 override enable. Active high. Used for debug purposes.
3	O_RXVALIDESC_C0_OVR_EN	rw	ro	0x0	o_rxvalidesc_c0 override enable. Active high. Used for debug purposes.
4	O_RXTRIGGERESC_C0_OVR_EN	rw	ro	0x0	o_rxtriggeresc_c0 override enable. Active high. Used for debug purposes.
5	O_RXDATAESC_C0_OVR_EN	rw	ro	0x0	o_rxdataesc_c0 override enable. Active high. Used for debug purposes.
6	I_TXREQUESTHS_C0_OVR_EN	rw	ro	0x0	i_txrequesths_c0 override enable. Active high. Used for debug purposes.
7	I_TXDATATRANSFERENHS_C0_OVR_EN	rw	ro	0x0	i_txdatatransferenhs_c0 override enable. Active high. Used for debug purposes.
8	O_TXREADYHS_C0_OVR_EN	rw	ro	0x0	o_txreadyhs_c0 override enable. Active high. Used for debug purposes.
9	O_TXWORDCLKHS_C0_OVR_EN	rw	ro	0x0	o_txwordclkhs_c0 override enable. Active high. Used for debug purposes.
10	I_TXDATAHS_C0_OVR_EN	rw	ro	0x0	i_txdatahs_c0 override enable. Active high. Used for debug purposes.
11	I_TXSENDSYNCHS_C0_OVR_EN	rw	ro	0x0	i_txsendsynchs_c0 override enable. Active high. Used for debug purposes.
12	I_TXSYNCTYPEHS0_C0_OVR_EN	rw	ro	0x0	i_txsynctypehs0_c0 override enable. Active high. Used for debug purposes.
13	I_TXSYNCTYPEHS1_C0_OVR_EN	rw	ro	0x0	i_txsynctypehs1_c0 override enable. Active high. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.151 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE0_OVR_12

Reg. 0x102C

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_ENABLE_C0_OVR_VAL	rw	ro	0x0	i_enable_c0 override value. Used for debug purposes.
1	O_STOPSTATE_C0_OVR_VAL	rw	ro	0x0	o_stopstate_c0 override value. Used for debug purposes.
2	O_ULPSACTIVENOT_C0_OVR_VAL	rw	ro	0x0	o_ulpsactivenot_c0 override value. Used for debug purposes.
3	I_TURNREQUEST_C0_OVR_VAL	rw	ro	0x0	i_turnrequest_c0 override value. Used for debug purposes.
4	I_TURNDISABLE_C0_OVR_VAL	rw	ro	0x0	i_turndisable_c0 override value. Used for debug purposes.
5	O_DIRECTION_C0_OVR_VAL	rw	ro	0x0	o_direction_c0 override value. Used for debug purposes.
6	I_FORCERXMODE_C0_OVR_VAL	rw	ro	0x0	i_forcerxmode_c0 override value. Used for debug purposes.
7	I_FORCETXSTOPMODE_C0_OVR_VAL	rw	ro	0x0	i_forcetxstopmode_c0 override value. Used for debug purposes.
8	O_ERRESC_C0_OVR_VAL	rw	ro	0x0	o_erresc_c0 override value. Used for debug purposes.
9	O_ERRSYNCESC_C0_OVR_VAL	rw	ro	0x0	o_errsyncesc_c0 override value. Used for debug purposes.
10	O_ERRCONTROL_C0_OVR_VAL	rw	ro	0x0	o_errcontrol_c0 override value. Used for debug purposes.
11	O_ERRCONTENTIONLP0_C0_OVR_VAL	rw	ro	0x0	o_errcontentionlp0_c0 override value. Used for debug purposes.
12	O_ERRCONTENTIONLP1_C0_OVR_VAL	rw	ro	0x0	o_errcontentionlp1_c0 override value. Used for debug purposes.
13	O_ERRSOTHS_C0_OVR_VAL	rw	ro	0x0	o_errsoths_c0 override value. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.152 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE0_OVR_13

Reg. 0x102D

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_ENABLE_C0_OVR_EN	rw	ro	0x0	i_enable_c0 override enable. Active high. Used for debug purposes.
1	O_STOPSTATE_C0_OVR_EN	rw	ro	0x0	o_stopstate_c0 override enable. Active high. Used for debug purposes.
2	O_ULPSACTIVENOT_C0_OVR_EN	rw	ro	0x0	o_ulpsactivenot_c0 override enable. Active high. Used for debug purposes.
3	I_TURNREQUEST_C0_OVR_EN	rw	ro	0x0	i_turnrequest_c0 override enable. Active high. Used for debug purposes.
4	I_TURNDISABLE_C0_OVR_EN	rw	ro	0x0	i_turndisable_c0 override enable. Active high. Used for debug purposes.
5	O_DIRECTION_C0_OVR_EN	rw	ro	0x0	o_direction_c0 override enable. Active high. Used for debug purposes.
6	I_FORCERXMODE_C0_OVR_EN	rw	ro	0x0	i_forcerxmode_c0 override enable. Active high. Used for debug purposes.
7	I_FORCETXSTOPMODE_C0_OVR_EN	rw	ro	0x0	i_forcetxstopmode_c0 override enable. Active high. Used for debug purposes.
8	O_ERRESC_C0_OVR_EN	rw	ro	0x0	o_erresc_c0 override enable. Active high. Used for debug purposes.
9	O_ERRSYNCESC_C0_OVR_EN	rw	ro	0x0	o_errsyncesc_c0 override enable. Active high. Used for debug purposes.
10	O_ERRCONTROL_C0_OVR_EN	rw	ro	0x0	o_errcontrol_c0 override enable. Active high. Used for debug purposes.
11	O_ERRCONTENTIONLP0_C0_OVR_EN	rw	ro	0x0	o_errcontentionlp0_c0 override enable. Active high. Used for debug purposes.

12	O_ERRCONTENTIONLP1_C0_OVR_EN	rw	ro	0x0	o_errcontentionlp1_c0 override enable. Active high. Used for debug purposes.
13	O_ERRSOTHS_C0_OVR_EN	rw	ro	0x0	o_errsoths_c0 override enable. Active high. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.153 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE0_OVR_14

Reg. 0x102E

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_TXALPCODE0_C0_OVR_EN	rw	ro	0x0	i_txalpcode0_c0 override enable. Active high. Used for debug purposes.
1	I_TXALPCODE1_C0_OVR_EN	rw	ro	0x0	i_txalpcode1_c0 override enable. Active high. Used for debug purposes.
3:2	I_TXSENDALPHS_C0_OVR_VAL	rw	ro	0x0	i_txsendalphs_c0 override value. Used for debug purposes.
7:4	I_TXALPNIBBLE0_C0_OVR_VAL	rw	ro	0x0	i_txalpnibble0_c0 override value. Used for debug purposes.
11:8	I_TXALPNIBBLE1_C0_OVR_VAL	rw	ro	0x0	i_txalpnibble1_c0 override value. Used for debug purposes.
14:12	I_ALPWAKESTATE_C0_OVR_VAL	rw	ro	0x0	i_alpwakestate_c0 override value. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.154 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE0_OVR_15

Reg. 0x102F

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_TXSENDALPHS_C0_OVR_EN	rw	ro	0x0	i_txsendalphs_c0 override enable. Active high. Used for debug purposes.
1	I_TXALPNIBBLE0_C0_OVR_EN	rw	ro	0x0	i_txalpnibble0_c0 override enable. Active high. Used for debug purposes.
2	I_TXALPNIBBLE1_C0_OVR_EN	rw	ro	0x0	i_txalpnibble1_c0 override enable. Active high. Used for debug purposes.
3	I_ALPWAKESTATE_C0_OVR_EN	rw	ro	0x0	i_alpwakestate_c0 override enable. Active high. Used for debug purposes.
7:4	I_TXALPCODE0_C0_OVR_VAL	rw	ro	0x0	i_txalpcode0_c0 override value. Used for debug purposes.
11:8	I_TXALPCODE1_C0_OVR_VAL	rw	ro	0x0	i_txalpcode1_c0 override value. Used for debug purposes.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.155 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE0_OVR_0

Reg. 0x1030

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_C0	ro	rw	0x0	o_rxdatahs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.156 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE0_OVR_1

Reg. 0x1031

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_C0	ro	rw	0x0	o_rxdatahs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.157 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE0_OVR_2

Reg. 0x1032

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_C0	ro	rw	0x0	o_rxdatahs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.158 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE0_OVR_3

Reg. 0x1033

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
0	O_RXACTIVEHS_C0	ro	rw	0x0	o_rxactivehs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
2:1	O_RXSYNCHS_C0	ro	rw	0x0	o_rxsynchs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
4:3	O_RXVALIDHS_C0	ro	rw	0x0	o_rxvalidhs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
6:5	O_RXINVALIDCODEHS_C0	ro	rw	0x0	o_rxinvalidcodehs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
7	O_RXWORDCLKHS_C0	ro	rw	0x0	o_rxwordclkhs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
10:8	O_RXSYNCTYPEHS0_C0	ro	rw	0x0	o_rxsynctypehs0_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
13:11	O_RXSYNCTYPEHS1_C0	ro	rw	0x0	o_rxsynctypehs1_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.159 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE0_OVR_4

Reg. 0x1034

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
3:0	O_RXALPCODE0_C0	ro	rw	0x0	o_rxalpcode0_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
7:4	O_RXALPCODE1_C0	ro	rw	0x0	o_rxalpcode1_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.160 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE0_OVR_5

Reg. 0x1035

Digital hard macro interface observability

access : read-only

bits	name	s/w	h/w	default	description
2:0	I_TXSYNCTYPEHS0_C0_INT	ro	rw	0x0	i_txsynctypehs0_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
5:3	I_TXSYNCTYPEHS1_C0_INT	ro	rw	0x0	i_txsynctypehs1_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
13:6	I_TXDATAESC_C0_INT	ro	rw	0x0	i_txdataesc_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.161 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE0_OVR_6

Reg. 0x1036

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
1:0	O_RXALPVALIDHS_C0	ro	rw	0x0	o_rxalpvalidhs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
5:2	O_RXALPNIBBLE0_C0	ro	rw	0x0	o_rxalpnibble0_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
9:6	O_RXALPNIBBLE1_C0	ro	rw	0x0	o_rxalpnibble1_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
11:10	I_TXSENDSYNCHS_C0_INT	ro	rw	0x0	i_txsendsynchs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.162 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE0_OVR_7

Reg. 0x1037

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	I_TXDATAHS_C0_INT	ro	rw	0x0	i_txdatahs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.163 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE0_OVR_8

Reg. 0x1038

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	I_TXDATAHS_C0_INT	ro	rw	0x0	i_txdatahs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.164 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE0_OVR_9

Reg. 0x1039

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
0	I_TXREQUESTESC_C0_INT	ro	rw	0x0	i_txrequestesc_c0 override multiplexer output. Used for debug purposes. (volatile)

					volatile : true
1	I_TXLPDTESC_C0_INT	ro	rw	0x0	i_txlpdtesc_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
2	I_TXULPSEXIT_C0_INT	ro	rw	0x0	i_txulpsexit_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
3	I_TXULPSESC_C0_INT	ro	rw	0x0	i_txulpsesc_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
4	I_TXVALIDESC_C0_INT	ro	rw	0x0	i_txvalidesc_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
5	O_TXREADYESC_C0	ro	rw	0x0	o_txreadyesc_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
9:6	I_TXTRIGGERESC_C0_INT	ro	rw	0x0	i_txtriggeresc_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
10	I_TXREQUESTHS_C0_INT	ro	rw	0x0	i_txrequesths_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
11	I_TXDATATRANSFERENHS_C0_INT	ro	rw	0x0	i_txdatatransferenhs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
12	O_TXREADYHS_C0	ro	rw	0x0	o_txreadyhs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
13	O_TXWORDCLKHS_C0	ro	rw	0x0	o_txwordclkhs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.165 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE0_OVR_10

Reg. | 0x103A

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
0	O_RXCLKESC_C0	ro	rw	0x0	o_rxclkesc_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	O_RXLPDTESC_C0	ro	rw	0x0	o_rxlpdtesc_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
2	O_RXULPSESC_C0	ro	rw	0x0	o_rxulpsesc_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
3	O_RXVALIDESC_C0	ro	rw	0x0	o_rxvalidesc_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
7:4	O_RXTRIGGERESC_C0	ro	rw	0x0	o_rxtriggeresc_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:8	O_RXDATAESC_C0	ro	rw	0x0	o_rxdataesc_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.166 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE0_OVR_11

Reg. | 0x103B

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description

0	I_ENABLE_C0_INT	ro	rw	0x0	i_enable_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	O_STOPSTATE_C0	ro	rw	0x0	o_stopstate_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
2	O_ULPSACTIVENOT_C0	ro	rw	0x0	o_ulpsactivenot_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
3	I_TURNREQUEST_C0_INT	ro	rw	0x0	i_turnrequest_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
4	I_TURNDISABLE_C0_INT	ro	rw	0x0	i_turndisable_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
5	O_DIRECTION_C0	ro	rw	0x0	o_direction_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
6	I_FORCERXMODE_C0_INT	ro	rw	0x0	i_forcerxmode_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
7	I_FORCETXSTOPMODE_C0_INT	ro	rw	0x0	i_forcetxstopmode_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
8	O_ERRESC_C0	ro	rw	0x0	o_erresc_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
9	O_ERRSYNCESC_C0	ro	rw	0x0	o_errsyncesc_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
10	O_ERRCONTROL_C0	ro	rw	0x0	o_errcontrol_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
11	O_ERRCONTENTIONLP0_C0	ro	rw	0x0	o_errcontentionlp0_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
12	O_ERRCONTENTIONLP1_C0	ro	rw	0x0	o_errcontentionlp1_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
13	O_ERRSOTHS_C0	ro	rw	0x0	o_errsoths_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.167 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE0_OVR_12

Reg. 0x103C

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_C0	ro	rw	0x0	o_rxdatahs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.168 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE0_OVR_13

Reg. 0x103D

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_C0	ro	rw	0x0	o_rxdatahs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.169 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE0_OVR_14

Reg. 0x103E

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
1:0	I_TXSENDALPHS_C0_INT	ro	rw	0x0	i_txsendalphs_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
5:2	I_TXALPCODE0_C0_INT	ro	rw	0x0	i_txalpcode0_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
9:6	I_TXALPCODE1_C0_INT	ro	rw	0x0	i_txalpcode1_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
12:10	I_ALPWAKESTATE_C0_INT	ro	rw	0x0	i_alpwakestate_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.170 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE0_OVR_15

Reg. 0x103F

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
3:0	I_TXALPNIBBLE0_C0_INT	ro	rw	0x0	i_txalpnibble0_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
7:4	I_TXALPNIBBLE1_C0_INT	ro	rw	0x0	i_txalpnibble1_c0 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.171 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_0

Reg. 0x1040

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
10:0	OA_LANE0_SPARE_IN	rw	ro	0x0	Lane 0 input spare bus (bits[10:9] independent current programmability 0-100% 1-75% 2-150% 3-125%; bit[8] vt drift compensation bypass; bit[7] dcc programmability 0-filter bandwidth 100% 1-filter bandwidth 200%; bits[6:0] spare bus) This signal is quasi-static.
11	OA_LANE0_SHORT_LB_EN	rw	ro	0x0	oa_lane0_short_lb_en bit configuration.This signal is quasi-static. Please check table for more details.
12	OA_LANE0_HSTX_LOWCAP_EN_OVR_EN	rw	ro	0x0	oa_lane0_hstx_lowcap_en override enable. Active high. Used for debug purposes.
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.172 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_1

Reg. 0x1041

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
4:0	OA_LANE0_HSRX_DPHY_DDL_BIAS_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_bias override value. Used for debug purposes.
11:5	OA_LANE0_HSRX_DPHY_DLL_FBK_OVR	rw	ro	0x0	oa_lane0_hsrx_dphy_dll_fbk override value. Used for debug purposes.

	_VAL				
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.173 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_2

Reg. 0x1042

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_LANE0_SEL_LANE_CFG	rw	ro	0x0	Lane 0 D-PHY/C-PHY configuration. 1'b0: D-PHY data lane (when phy_mode is 1'b0); C-PHY slave lane (when phy_mode is 1'b1). 1'b1: D-PHY clock lane (when phy_mode is 1'b0); C-PHY master lane (when phy_mode is 1'b1). This signal is quasi-static. Please check table for more details.
1	OA_LANE0_HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_cphy_cdr_fbk_fast_lock_en override enable. Active high. Used for debug purposes.
2	OA_LANE0_HSRX_TERM_EN200OHMS	rw	ro	0x0	Lane 0 HS-RX termination value. Please check table for more details.
3	OA_LANE0_HSRX_DPHY_DDL_PON_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_pon override value. Used for debug purposes.
5:4	OA_LANE0_HSTX_LOWCAP_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hstx_lowcap_en override value. Used for debug purposes.
6	OA_LANE0_HSTX_DIV_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hstx_div_en override value. Used for debug purposes.
7	OA_LANE0_HSTX_DATA_BC_OVR_EN	rw	ro	0x0	oa_lane0_hstx_data_ca override enable. Active high. Used for debug purposes.
8	OA_LANE0_HSTX_DATA_CA_OVR_EN	rw	ro	0x0	oa_lane0_hstx_data_ca override enable. Active high. Used for debug purposes.
10:9	OA_LANE0_HSTX_TERM_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hstx_term_en override value. Used for debug purposes.
11	OA_LANE0_HSRX_DPHY_DDL_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_en override enable. Active high. Used for debug purposes.
12	OA_LANE0_HSRX_CDPHY_SEL_FAST_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_cdphy_sel_fast override enable. Active high. Used for debug purposes.
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.174 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_3

Reg. 0x1043

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
1:0	OA_LANE0_HSTX_PON_OVR_VAL	rw	ro	0x0	oa_lane0_hstx_pon override value. Used for debug purposes.
3:2	OA_LANE0_HSTX_BOOST_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hstx_boost_en override value. Used for debug purposes.
4	OA_LANE0_HSTX_SEL_PHASE0	rw	ro	0x1	Lane 0 HS-TX clock phase selection. 1'b0: 90 (for D-PHY clock lane configuration). 1'b1: 0 (for both C-PHY and D-PHY data lane configurations). This signal is quasi-static. Please check table for more details.
7:5	OA_LANE0_HSTX_EQA	rw	ro	0x0	Lane 0 HS-TX de-emphasis word (upper-half). This signal is quasi-static. Please check table for more details.
8	OA_LANE0_HSTX_SEL_CLKLB	rw	ro	0x1	Lane 0 HS-TX clock source. 1'b0: External PLL clock. 1'b1: Common block internal DCO clock. This signal is quasi-static.
9	OA_LANE0_LPTX_DIN_DN_OVR_VAL	rw	ro	0x0	oa_lane0_lptx_din_dn override value. Used for debug purposes.
10	OA_LANE0_LPTX_DIN_DP_OVR_VAL	rw	ro	0x0	oa_lane0_lptx_din_dp override value. Used for debug purposes.

11	OA_LANE0_HSRX_DPHY_DDL_DCC_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_dcc_en override value. Used for debug purposes.
12	OA_LANE0_HSRX_DPHY_DDL_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_en override value. Used for debug purposes.
13	OA_LANE0_HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_cphy_cdr_fbk_fast_lock_en override value. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.175 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_4

Reg. 0x1044

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_LANE0_HSTX_PON_OVR_EN	rw	ro	0x0	oa_lane0_hstx_pon override enable. Active high. Used for debug purposes.
1	OA_LANE0_HSTX_BOOST_EN_OVR_EN	rw	ro	0x0	oa_lane0_hstx_boost_en override enable. Active high. Used for debug purposes.
4:2	OA_LANE0_HSTX_EQB	rw	ro	0x0	Lane 0 HS-TX de-emphasis word (lower-half). This signal is quasi-static. Please check table for more details.
5	OA_LANE0_HSTX_CLK_OBS_EN	rw	ro	0x0	Lane 0 HS clock pattern driven in the lines (debug feature). Active high. This signal is quasi-static.
6	OA_LANE0_LPTX_DIN_DN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes.
7	OA_LANE0_LPTX_DIN_DP_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes.
9:8	OA_LANE0_LPTX_SR_BYPASS_EN	rw	ro	0x0	oa_lane0_lptx_sr_bypass_en override enable. Active high. Used for debug purposes.
10	OA_LANE0_HSTX_TERM_EN_OVR_EN	rw	ro	0x0	oa_lane0_hstx_term_en override enable. Active high. Used for debug purposes.
11	OA_LANE0_HSRX_DPHY_DDL_DCC_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.176 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_5

Reg. 0x1045

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
15:0	OA_LANE0_HSTX_DATA_AB_DPHY_OVR_VAL	rw	ro	0x0	oa_lane0_hstx_data_ab_dphy override value. Used for debug purposes.

1.1.1.177 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_6

Reg. 0x1046

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
13:0	OA_LANE0_HSTX_DATA_BC_OVR_VAL	rw	ro	0x0	oa_lane0_hstx_data_bc override value. Used for debug purposes.
14	OA_LANE0_HSTX_DATA_AB_DPHY_OVR_EN	rw	ro	0x0	oa_lane0_hstx_data_ab_dphy override enable. Active high. Used for debug purposes.
15	OA_LANE0_HSRX_DPHY_DDL_PON_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_pon override enable. Active high. Used for debug purposes.

1.1.1.178 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_7

Reg. 0x1047

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
13:0	OA_LANE0_HSTX_DATA_CA_OVR_VAL	rw	ro	0x0	oa_lane0_hstx_data_ca override value. Used for debug purposes.
15:14	OA_LANE0_HSRX_GMODE	rw	ro	0x2	Lane 0 HS-RX preamplifier bandwidth configuration. This signal is quasi-static. Please check table for more details.

1.1.1.179 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_8

Reg. 0x1048

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
1:0	OA_LANE0_LPTX_EN_OVR_VAL	rw	ro	0x0	oa_lane0_lptx_en override value. Used for debug purposes.
3:2	OA_LANE0_LPTX_PON_OVR_VAL	rw	ro	0x0	oa_lane0_lptx_pon override value. Used for debug purposes.
5:4	OA_LANE0_LPTX_PULLDWN_EN_OVR_VAL	rw	ro	0x0	oa_lane0_lptx_pulldwn_en override value. Used for debug purposes.
6	OA_LANE0_LPRX_LP_PON_OVR_EN	rw	ro	0x0	oa_lane0_lprx_lp_pon override enable. Active high. Used for debug purposes.
7	OA_LANE0_LPRX_CD_PON_OVR_EN	rw	ro	0x0	oa_lane0_lprx_cd_pon override enable. Active high. Used for debug purposes.
8	OA_LANE0_LPRX_ULP_PON_OVR_EN	rw	ro	0x0	oa_lane0_lprx_ulp_pon override enable. Active high. Used for debug purposes.
9	OA_LANE0_HSRX_CPHY_CDR_FBK_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_cphy_cdr_fbk_en override value. Used for debug purposes.
13:10	OA_LANE0_HSRX_CPHY_CDR_FBK_CAP_PROG	rw	ro	0x7	Lane 0 C-PHY low-pass filter bandwidth (symbol rate dependent). This signal is quasi-static. Please check table for more details.
14	OA_LANE0_HSRX_VCM_DET_SYNC_BYPASS	rw	ro	0x0	Enable vcm detector filter bypass which controls CDR input propagation. This signal is quasi-static. Please check table for more details.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.180 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_9

Reg. 0x1049

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
1:0	OA_LANE0_LPRX_LP_PON_OVR_VAL	rw	ro	0x0	oa_lane0_lprx_lp_pon override value. Used for debug purposes.
3:2	OA_LANE0_LPRX_CD_PON_OVR_VAL	rw	ro	0x0	oa_lane0_lprx_cd_pon override value. Used for debug purposes.
5:4	OA_LANE0_LPRX_ULP_PON_OVR_VAL	rw	ro	0x0	oa_lane0_lprx_ulp_pon override value. Used for debug purposes.
6	OA_LANE0_LPTX_EN_OVR_EN	rw	ro	0x0	oa_lane0_lptx_en override enable. Active high. Used for debug purposes.
7	OA_LANE0_LPTX_PON_OVR_EN	rw	ro	0x0	oa_lane0_lptx_pon override enable. Active high. Used for debug purposes.
8	OA_LANE0_LPTX_PULLDWN_EN_OVR_EN	rw	ro	0x0	oa_lane0_lptx_pulldwn_en override enable. Active high. Used for debug purposes.
9	OA_LANE0_HSRX_CPHY_CDR_FBK_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_cphy_cdr_fbk_en override enable. Active high. Used for debug purposes.
10	OA_LANE0_HSRX_CPHY_MASK_CHANGE_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_cphy_mask_change override value. Used for debug purposes.

11	OA_LANE0_HSRX_CPHY_DELAY_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_cphy_delay override enable. Active high. Used for debug purposes.
12	OA_LANE0_HSRX_CDPHY_SEL_FAST_OVR_VAL	rw	ro	0x1	oa_lane0_hsrx_cdphy_sel_fast override value. Please check table for more details.
14:13	OA_LANE0_HSRX_CDPHY_SEL_TYPE	rw	ro	0x0	oa_lane0_hsrx_cdphy_sel_type override value. Active high. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.181 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_10

Reg. 0x104A

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
2:0	OA_LANE0_HSRX_EQUALIZER_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_equalizer override value. Used for debug purposes.
5:3	OA_LANE0_HSRX_HS_CLK_DIV	rw	ro	0x7	Lane 0 D-PHY DDR clock lane divider (data rate dependent). This signal is quasi-static. Please check table for more details.
6	OA_LANE0_HSRX_SEL_GATED_POLARITY	rw	ro	0x0	Lane <0> deserializer output polarity (D-PHY related). Active high. This signal is quasi-static. Please check table for more details.
9:7	OA_LANE0_HSRX_CPHY_CDR_DIV	rw	ro	0x5	Lane 0 C-PHY oscillation clock divider (for calibration). This signal is quasi-static. Please check table for more details.
14:10	OA_LANE0_HSRX_CPHY_DELAY_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_cphy_delay override value. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.182 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_11

Reg. 0x104B

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_LANE0_HSRX_TERM_RIGHT_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_term_right_en override value. Used for debug purposes.
1	OA_LANE0_HSRX_TERM_LEFT_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_term_left_en override value. Used for debug purposes.
2	OA_LANE0_HSRX_DPHY_CLK_CHANNEL_PULL_EN	rw	ro	0x0	Lane 0 D-PHY clock channel pull-up/pull-down enable. Active high. This signal is quasi-static. Please check table for more details.
3	OA_LANE0_HSRX_HS_CLK_DIV_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_hs_clk_div_en override value. Used for debug purposes.
4	OA_LANE0_HSRX_DESERIALIZER_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_deserializer_en override value. Used for debug purposes.
5	OA_LANE0_HSRX_DESERIALIZER_DATA_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_deserializer_data_en override value. Used for debug purposes.
6	OA_LANE0_HSRX_DESERIALIZER_DIV_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_deserializer_div_en override value. Used for debug purposes.
7	OA_LANE0_HSRX_OFFCAL_OBS_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_offcal_obs_en override value. Used for debug purposes.
8	OA_LANE0_HSRX_VCM_DET_PON_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_vcm_det_pon override value. Used for debug purposes.
9	OA_LANE0_HSRX_VCM_DET_OUT_EN_O	rw	ro	0x0	oa_lane0_hsrx_vcm_det_out_en override value. Used for debug purposes.

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10	OA_LANE0_HSRX_CPHY_ALP_DET_RIGHT_PON_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_cphy_alp_det_right_pon override value. Used for debug purposes.
11	OA_LANE0_HSRX_CPHY_ALP_DET_LEFT_PON_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_cphy_alp_det_left_pon override value. Used for debug purposes.
12	OA_LANE0_HSRX_CPHY_MASK_CHANGE_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_cphy_mask_change override enable. Active high. Used for debug purposes.
13	OA_LANE0_HSRX_PON_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_pon override enable. Active high. Used for debug purposes.
14	OA_LANE0_HSRX_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_en override enable. Active high. Used for debug purposes.
15	OA_LANE0_HSTX_DIV_EN_OVR_EN	rw	ro	0x0	oa_lane0_hstx_div_en override enable. Active high. Used for debug purposes.

1.1.1.183 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_12

Reg. 0x104C

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_LANE0_HSRX_TERM_RIGHT_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_term_right_en override enable. Active high. Used for debug purposes.
1	OA_LANE0_HSRX_TERM_LEFT_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_term_left_en override enable. Active high. Used for debug purposes.
2	OA_LANE0_HSRX_HS_CLK_DIV_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_hs_clk_div_en override enable. Active high. Used for debug purposes.
3	OA_LANE0_HSRX_DESERIALIZER_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_deserializer_en override enable. Active high. Used for debug purposes.
4	OA_LANE0_HSRX_DESERIALIZER_DATA_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_deserializer_data_en override enable. Active high. Used for debug purposes.
5	OA_LANE0_HSRX_DESERIALIZER_DIV_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_deserializer_div_en override enable. Active high. Used for debug purposes.
6	OA_LANE0_HSRX_OFFCAL_OBS_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_offcal_obs_en override enable. Active high. Used for debug purposes.
7	OA_LANE0_HSRX_VCM_DET_PON_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_vcm_det_pon override enable. Active high. Used for debug purposes.
8	OA_LANE0_HSRX_VCM_DET_OUT_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_vcm_det_out_en override enable. Active high. Used for debug purposes.
9	OA_LANE0_HSRX_CPHY_ALP_DET_RIGHT_PON_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_cphy_alp_det_right_pon override enable. Active high. Used for debug purposes.
10	OA_LANE0_HSRX_CPHY_ALP_DET_LEFT_PON_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_cphy_alp_det_left_pon override enable. Active high. Used for debug purposes.
12:11	OA_LANE0_HSRX_PON_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_pon override value. Used for debug purposes.
14:13	OA_LANE0_HSRX_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_en override value. Used for debug purposes.
15	OA_LANE0_HSRX_CPHY_SR_BYPASS_Z	rw	ro	0x0	Enable for the slew rate control latch bypass inside CDR. This signal is quasi-static. Please check table for more details.

1.1.1.184 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_13

Reg. 0x104D

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_LANE0_HSRX_DPHY_DDL_BIAS_BYPASS_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_bias_bypass_en override value. Used for debug purposes.
1	OA_LANE0_HSRX_DPHY_DDL_BYPASS_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_bypass_en override value. Used for debug purposes.
2	OA_LANE0_HSRX_DPHY_DDL_PHASE_CHANGE_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_phase_change override value. Used for debug purposes.
3	OA_LANE0_HSRX_DPHY_DLL_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_dphy_dll_en override value. Used for debug purposes.
4	OA_LANE0_HSRX_DPHY_PREAMBLE_CAL_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_dphy_preamble_cal_en override value. Used for debug purposes.
9:5	OA_LANE0_HSRX_DPHY_DDL_VT_COMP_BIAS_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_vt_comp_bias override value. Used for debug purposes.
10	OA_LANE0_HSRX_DPHY_DATA_DELAY_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_data_delay override enable. Active high. Used for debug purposes.
13:11	OA_LANE0_HSRX_DPHY_DDL_DIV	rw	ro	0x2	Lane 0 HS-RX DDL oscillation clock divider. This signal is quasi-static. Please check table for more details.
15:14	OA_LANE0_HSRX_CPHY_FINE_RANGE	rw	ro	0x0	Delay line fine delay cell setting for DDL. This signal is quasi-static. Please check table for more details.

1.1.1.185 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_14

Reg.

0x104E

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_LANE0_HSRX_DPHY_DDL_BIAS_BYPASS_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_bias_bypass_en override enable. Active high. Used for debug purposes.
1	OA_LANE0_HSRX_DPHY_DDL_BYPASS_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_bypass_en override enable. Active high. Used for debug purposes.
2	OA_LANE0_HSRX_DPHY_DDL_PHASE_CHANGE_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_phase_change override enable. Active high. Used for debug purposes.
3	OA_LANE0_HSRX_DPHY_DLL_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_dll_en override enable. Active high. Used for debug purposes.
4	OA_LANE0_HSRX_DPHY_PREAMBLE_CAL_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_preamble_cal_en override enable. Active high. Used for debug purposes.
5	OA_LANE0_HSRX_DPHY_DDL_VT_COMP_EN_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_vt_comp_en override enable. Used for debug purposes.
9:6	OA_LANE0_HSRX_DPHY_DATA_DELAY_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_dphy_data_delay override value. Used for debug purposes.
10	OA_LANE0_HSRX_DPHY_DDL_BIAS_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_bias override enable. Active high. Used for debug purposes.
11	OA_LANE0_HSRX_DPHY_DDL_COARSE_BANK_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_coarse_bank override enable. Active high. Used for debug purposes.
12	OA_LANE0_HSRX_DPHY_DDL_TUNE_MODE_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_tune_mode override enable. Active high. Used for debug purposes.
13	OA_LANE0_HSRX_DPHY_DLL_FBK_OVR	rw	ro	0x0	oa_lane0_hsrx_dphy_dll_fbk override enable. Active high. Used for debug purposes.

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14	OA_LANE0_HSRX_EQUALIZER_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_equalizer override enable. Active high. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.186 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_15 Reg. 0x104F

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
3:0	OA_LANE0_HSRX_DPHY_DDL_COARSE_BANK_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_coarse_bank override value. Used for debug purposes.
5:4	OA_LANE0_HSRX_DPHY_DDL_TUNE_MODE_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_tune_mode override value. Used for debug purposes.
6	OA_LANE0_HSRX_DPHY_DDL_VT_COMP_EN_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_vt_comp_en override value. Used for debug purposes.
7	OA_LANE0_HSRX_DPHY_DDL_VT_COMP_BIAS_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_vt_comp_bias override enable. Used for debug purposes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.187 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_16 Reg. 0x1050

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
2:0	OA_LANE0_HSRX_DPHY_DLL_CP_PROG	rw	ro	0x4	Lane 0 D-PHY HS-RX DDL charge pump gain configuration. This signal is quasi-static. Please check table for more details.
4:3	OA_LANE0_HSRX_DPHY_CLK_CHANNEL	rw	ro	0x0	Lane 0 D-PHY HS-RX clock channel selection. This signal is quasi-static. Please check table for more details.
5	OA_LANE0_HSRX_OFFCAL_RIGHT_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_offcal_right override enable. Active high. Used for debug purposes.
6	OA_LANE0_HSRX_OFFCAL_LEFT_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_offcal_left override enable. Active high. Used for debug purposes.
7	OA_LANE0_HSRX_DPHY_DDL_PHASE_RIGHT_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_phase_right override enable. Active high. Used for debug purposes.
8	OA_LANE0_HSRX_DPHY_DDL_PHASE_MID_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_phase_mid override enable. Active high. Used for debug purposes.
9	OA_LANE0_HSRX_DPHY_DDL_PHASE_LEFT_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_phase_left override enable. Active high. Used for debug purposes.
10	OA_LANE0_HSRX_MODE_OVR_EN	rw	ro	0x0	oa_lane0_hsrx_mode override enable. Active high. Used for debug purposes.
15:11	OA_LANE0_ATB_SW	rw	ro	0x0	Lane 0 analog test bus signal selection. This signal is quasi-static. Please check table for more details.

1.1.1.188 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_17 Reg. 0x1051

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
7:0	OA_LANE0_HSRX_OFFCAL_RIGHT_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_offcal_right override value. Used for debug purposes.

15:8	OA_LANE0_HSRX_OFFCAL_LEFT_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_offcal_left override value. Used for debug purposes.

1.1.1.189 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_18

Reg. 0x1052

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
10:0	OA_LANE0_HSRX_DPHY_DDL_PHASE_RIGHT_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_phase_right override value. Used for debug purposes.
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.190 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_19

Reg. 0x1053

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
10:0	OA_LANE0_HSRX_DPHY_DDL_PHASE_MID_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_phase_mid override value. Used for debug purposes.
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.191 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_20

Reg. 0x1054

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
10:0	OA_LANE0_HSRX_DPHY_DDL_PHASE_LEFT_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_dphy_ddl_phase_left override value. Used for debug purposes.
13:11	OA_LANE0_HSRX_MODE_OVR_VAL	rw	ro	0x0	oa_lane0_hsrx_mode override value. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.192 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_21

Reg. 0x1055

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
15:0	IA_LANE0_HSRX_DATA_AB_LEFT_OVR_VAL	rw	ro	0x0	ia_lane0_hsrx_data_ab_left override value. Used for debug purposes.

1.1.1.193 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_22

Reg. 0x1056

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
15:0	IA_LANE0_HSRX_DATA_BC_MID_OVR_VAL	rw	ro	0x0	ia_lane0_hsrx_data_bc_left override value. Used for debug purposes.

1.1.1.194 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_23

Reg. 0x1057

Analog macro lane 0 control

access : read-write

bits	name	s/w	h/w	default	description
15:0	IA_LANE0_HSRX_DATA_CA_RIGHT_OVR_VAL	rw	ro	0x0	ia_lane0_hsrx_data_ca_right override value. Used for debug purposes.

1.1.1.195 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_24

Reg. 0x1058

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
0	IA_LANE0_HSRX_DATA_AB_LEFT_OVR_EN	rw	ro	0x0	ia_lane0_hsrx_data_ab_left override enable. Active high. Used for debug purposes.
1	IA_LANE0_HSRX_DATA_BC_MID_OVR_EN	rw	ro	0x0	ia_lane0_hsrx_data_bc_mid override enable. Active high. Used for debug purposes.
2	IA_LANE0_HSRX_DATA_CA_RIGHT_OVR_EN	rw	ro	0x0	ia_lane0_hsrx_data_ca_right override enable. Active high. Used for debug purposes.
3	IA_LANE0_HSRX_WORD_CLK_OVR_EN	rw	ro	0x0	ia_lane0_hsrx_word_clk override enable. Active high. Used for debug purposes.
4	IA_LANE0_HSRX_HS_CLK_DIV_OUT_OVR_EN	rw	ro	0x0	ia_lane0_hsrx_hs_clk_div_out override enable. Active high. Used for debug purposes.
5	IA_LANE0_HSTX_WORD_CLK_OVR_EN	rw	ro	0x0	ia_lane0_hstx_word_clk override enable. Active high. Used for debug purposes.
6	IA_LANE0_HSRX_VCM_DET_OUT_OVR_EN	rw	ro	0x0	ia_lane0_hsrx_vcm_det_out override enable. Active high. Used for debug purposes.
7	IA_LANE0_HSRX_OUT_CAL_LEFT_N_OVR_EN	rw	ro	0x0	ia_lane0_hsrx_out_cal_left_n override enable. Active high. Used for debug purposes.
8	IA_LANE0_HSRX_OUT_CAL_LEFT_P_OVR_EN	rw	ro	0x0	ia_lane0_hsrx_out_cal_left_p override enable. Active high. Used for debug purposes.
9	IA_LANE0_HSRX_OUT_CAL_RIGHT_N_OVR_EN	rw	ro	0x0	ia_lane0_hsrx_out_cal_right_n override enable. Active high. Used for debug purposes.
10	IA_LANE0_HSRX_OUT_CAL_RIGHT_P_OVR_EN	rw	ro	0x0	ia_lane0_hsrx_out_cal_right_p override enable. Active high. Used for debug purposes.
11	IA_LANE0_HSRX_DPHY_DDL_OSC_CLK_OVR_EN	rw	ro	0x0	ia_lane0_hsrx_dphy_ddl_osc_clk override enable. Active high. Used for debug purposes.
12	IA_LANE0_HSRX_CPHY_ALP_DET_LEFT_OUT_OVR_EN	rw	ro	0x0	ia_lane0_hsrx_cphy_alp_det_left_out override enable. Active high. Used for debug purposes.
13	IA_LANE0_HSRX_CPHY_ALP_DET_RIGHT_OUT_OVR_EN	rw	ro	0x0	ia_lane0_hsrx_cphy_alp_det_right_out override enable. Active high. Used for debug purposes.
14	IA_LANE0_HSRX_CPHY_CDR_OSC_CLK_OVR_EN	rw	ro	0x0	ia_lane0_hsrx_cphy_cdr_osc_clk override enable. Active high. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.196 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_25

Reg. 0x1059

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
0	IA_LANE0_HSRX_DPHY_DDL_OSC_CLK_OVR_VAL	rw	ro	0x0	ia_lane0_hsrx_dphy_ddl_osc_clk override value. Used for debug purposes.

1	IA_LANE0_HSRX_CPHY_ALP_DET_LEFT_OUT_OVR_VAL	rw	ro	0x0	ia_lane0_hsrx_cphy_alp_det_left_out override value. Used for debug purposes.
2	IA_LANE0_HSRX_CPHY_ALP_DET_RIGHT_OUT_OVR_VAL	rw	ro	0x0	ia_lane0_hsrx_cphy_alp_det_right_out override value. Used for debug purposes.
3	IA_LANE0_HSRX_CPHY_CDR_OSC_CLK_OVR_VAL	rw	ro	0x0	ia_lane0_hsrx_cphy_cdr_osc_clk override value. Used for debug purposes.
5:4	IA_LANE0_LPRX_DOUTCD_OVR_VAL	rw	ro	0x0	ia_lane0_lprx_doutcd override value. Used for debug purposes.
7:6	IA_LANE0_LPRX_DOUTLP_OVR_VAL	rw	ro	0x0	ia_lane0_lprx_doutlp override value. Used for debug purposes.
9:8	IA_LANE0_LPRX_DOUTULP_OVR_VAL	rw	ro	0x0	ia_lane0_lprx_doutulp override value. Used for debug purposes.
13:10	IA_LANE0_SPARE_OUT_OVR_VAL	rw	ro	0x0	ia_lane0_spare_out override value. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.197 CORE_DIG_IOCTRL_RW_AFE_LANE0_CTRL_26

Reg. 0x105A

Analog macro lane 0 control
access : read-write

bits	name	s/w	h/w	default	description
0	IA_LANE0_LPRX_DOUTCD_OVR_EN	rw	ro	0x0	ia_lane0_lprx_doutcd override enable. Active high. Used for debug purposes.
1	IA_LANE0_LPRX_DOUTLP_OVR_EN	rw	ro	0x0	ia_lane0_lprx_doutlp override enable. Active high. Used for debug purposes.
2	IA_LANE0_LPRX_DOUTULP_OVR_EN	rw	ro	0x0	ia_lane0_lprx_doutulp override enable. Active high. Used for debug purposes.
3	IA_LANE0_SPARE_OUT_OVR_EN	rw	ro	0x0	ia_lane0_spare_out override enable. Active high. Used for debug purposes.
4	IA_LANE0_HSRX_WORD_CLK_OVR_VAL	rw	ro	0x0	ia_lane0_hsrx_word_clk override value. Used for debug purposes.
5	IA_LANE0_HSRX_HS_CLK_DIV_OUT_OVR_VAL	rw	ro	0x0	ia_lane0_hsrx_hs_clk_div_out override value. Used for debug purposes.
6	IA_LANE0_HSTX_WORD_CLK_OVR_VAL	rw	ro	0x0	ia_lane0_hstx_word_clk override value. Used for debug purposes.
7	IA_LANE0_HSRX_VCM_DET_OUT_OVR_VAL	rw	ro	0x0	ia_lane0_hsrx_vcm_det_out override value. Used for debug purposes.
8	IA_LANE0_HSRX_OUT_CAL_LEFT_N_OVR_VAL	rw	ro	0x0	ia_lane0_hsrx_out_cal_left_n override value. Used for debug purposes.
9	IA_LANE0_HSRX_OUT_CAL_LEFT_P_OVR_VAL	rw	ro	0x0	ia_lane0_hsrx_out_cal_left_p override value. Used for debug purposes.
10	IA_LANE0_HSRX_OUT_CAL_RIGHT_N_OVR_VAL	rw	ro	0x0	ia_lane0_hsrx_out_cal_right_n override value. Used for debug purposes.
11	IA_LANE0_HSRX_OUT_CAL_RIGHT_P_OVR_VAL	rw	ro	0x0	ia_lane0_hsrx_out_cal_right_p override value. Used for debug purposes.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.199 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_0

Reg. 0x1060

Analog macro lane 0 observability
access : read-only

bits	name	s/w	h/w	default	description
1:0	OA_LANE0_HSTX_PON	ro	rw	0x0	oa_lane0_hstx_pon multiplexer output. Used for debug purposes. (volatile) volatile : true

3:2	OA_LANE0_HSTX_BOOST_EN	ro	rw	0x0	oa_lane0_hstx_boost_en multiplexer output. Used for debug purposes. (volatile) volatile : true
4	OA_LANE0_HSRX_DPHY_DDL_PON	ro	rw	0x0	oa_lane0_hsrx_dphy_ddl_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
6:5	OA_LANE0_HSTX_LOWCAP_EN	ro	rw	0x0	oa_lane0_hstx_lowcap_en multiplexer output. Used for debug purposes. (volatile) volatile : true
7	OA_LANE0_LPTX_DIN_DN	ro	rw	0x0	oa_lane0_lptx_din_dn multiplexer output. Used for debug purposes. (volatile) volatile : true
8	OA_LANE0_LPTX_DIN_DP	ro	rw	0x0	oa_lane0_lptx_din_dp multiplexer output. Used for debug purposes. (volatile) volatile : true
9	OA_LANE0_HSRX_DPHY_DDL_DCC_EN	ro	rw	0x0	oa_lane0_hsrx_dphy_ddl_dcc_en multiplexer output. Used for debug purposes. (volatile) volatile : true
10	OA_LANE0_HSRX_DPHY_DDL_EN	ro	rw	0x0	oa_lane0_hsrx_dphy_ddl_en multiplexer output. Used for debug purposes. (volatile) volatile : true
11	OA_LANE0_HSRX_CPHY_CDR_FBK_FAST_LOCK_EN	ro	rw	0x0	oa_lane0_hsrx_cphy_cdr_fbk_fast_lock_en multiplexer output. Used for debug purposes. (volatile) volatile : true
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.200 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_1

Reg. 0x1061

Analog macro lane 0 observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	OA_LANE0_HSTX_DATA_AB_DPHY	ro	rw	0x0	oa_lane0_hstx_data_ab_dphy multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.201 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_2

Reg. 0x1062

Analog macro lane 0 observability
access : read-only

bits	name	s/w	h/w	default	description
13:0	OA_LANE0_HSTX_DATA_BC	ro	rw	0x0	oa_lane0_hstx_data_bc multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	OA_LANE0_HSTX_TERM_EN	ro	rw	0x0	oa_lane0_hstx_term_en multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.202 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_3

Reg. 0x1063

Analog macro lane 0 observability
access : read-only

bits	name	s/w	h/w	default	description
13:0	OA_LANE0_HSTX_DATA_CA	ro	rw	0x0	oa_lane0_hstx_data_ca[multiplexer output. Used for debug purposes. (volatile) volatile : true
14	OA_LANE0_HSTX_DIV_EN	ro	rw	0x0	oa_lane0_hstx_div_en multiplexer output. Used for debug purposes. (volatile) volatile : true
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.203 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_4

Reg. 0x1064

Analog macro lane 0 observability
access : read-only

bits	name	s/w	h/w	default	description
1:0	OA_LANE0_LPTX_EN	ro	rw	0x0	oa_lane0_lptx_en multiplexer output. Used for debug purposes. (volatile) volatile : true
3:2	OA_LANE0_LPTX_PON	ro	rw	0x0	oa_lane0_lptx_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
5:4	OA_LANE0_LPTX_PULLDWN_EN	ro	rw	0x0	oa_lane0_lptx_pulldwn_en multiplexer output. Used for debug purposes. (volatile) volatile : true
7:6	OA_LANE0_LPRX_LP_PON	ro	rw	0x0	oa_lane0_lprx_lp_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
9:8	OA_LANE0_LPRX_CD_PON	ro	rw	0x0	oa_lane0_lprx_cd_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
11:10	OA_LANE0_LPRX_ULP_PON	ro	rw	0x0	oa_lane0_lprx_ulp_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
12	OA_LANE0_HSRX_CPHY_CDR_FBK_EN	ro	rw	0x0	oa_lane0_hsrx_cphy_cdr_fbk_en multiplexer output. Used for debug purposes. (volatile) volatile : true
13	OA_LANE0_HSRX_CPHY_MASK_CHANGE	ro	rw	0x0	oa_lane0_hsrx_cphy_mask_change multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.204 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_5

Reg.

0x1065

Analog macro lane 0 observability
access : read-only

bits	name	s/w	h/w	default	description
0	OA_LANE0_HSRX_TERM_RIGHT_EN	ro	rw	0x0	oa_lane0_hsrx_term_right_en multiplexer output. Used for debug purposes. (volatile) volatile : true
1	OA_LANE0_HSRX_TERM_LEFT_EN	ro	rw	0x0	oa_lane0_hsrx_term_left_en multiplexer output. Used for debug purposes. (volatile) volatile : true
2	OA_LANE0_HSRX_HS_CLK_DIV_EN	ro	rw	0x0	oa_lane0_hsrx_hs_clk_div_en multiplexer output. Used for debug purposes. (volatile) volatile : true
3	OA_LANE0_HSRX_DESERIALIZER_EN	ro	rw	0x0	oa_lane0_hsrx_deserializer_en multiplexer output. Used for debug purposes. (volatile) volatile : true
4	OA_LANE0_HSRX_DESERIALIZER_DATA_EN	ro	rw	0x0	oa_lane0_hsrx_deserializer_data_en multiplexer output. Used for debug purposes. (volatile) volatile : true
5	OA_LANE0_HSRX_DESERIALIZER_DIV_EN	ro	rw	0x0	oa_lane0_hsrx_deserializer_div_en multiplexer output. Used for debug purposes. (volatile) volatile : true
6	OA_LANE0_HSRX_OFFCAL_OBS_EN	ro	rw	0x0	oa_lane0_hsrx_offcal_obs_en multiplexer output. Used for debug purposes. (volatile) volatile : true
7	OA_LANE0_HSRX_VCM_DET_PON	ro	rw	0x0	oa_lane0_hsrx_vcm_det_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
8	OA_LANE0_HSRX_VCM_DET_OUT_EN	ro	rw	0x0	oa_lane0_hsrx_vcm_det_out_en multiplexer output. Used for debug purposes. (volatile) volatile : true
9	OA_LANE0_HSRX_CPHY_ALP_DET_RIGHT_PON	ro	rw	0x0	oa_lane0_hsrx_cphy_alp_det_right_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
10	OA_LANE0_HSRX_CPHY_ALP_DET_LEF	ro	rw	0x0	oa_lane0_hsrx_cphy_alp_det_left_pon multiplexer output. Used for debug purposes. (volatile)

	T_PON				volatile : true
12:11	OA_LANE0_HSRX_PON	ro	rw	0x0	oa_lane0_hsrx_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
14:13	OA_LANE0_HSRX_EN	ro	rw	0x0	oa_lane0_hsrx_en multiplexer output. Used for debug purposes. (volatile) volatile : true
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.205 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_6

Reg. 0x1066

Analog macro lane 0 observability
access : read-only

bits	name	s/w	h/w	default	description
0	OA_LANE0_HSRX_DPHY_DDL_BIAS_BYPASS_EN	ro	rw	0x0	oa_lane0_hsrx_dphy_ddl_bias_bypass_en multiplexer output. Used for debug purposes. (volatile) volatile : true
1	OA_LANE0_HSRX_DPHY_DDL_BYPASS_EN	ro	rw	0x0	oa_lane0_hsrx_dphy_ddl_bypass_en multiplexer output. Used for debug purposes. (volatile) volatile : true
2	OA_LANE0_HSRX_DPHY_DDL_PHASE_CHANGE	ro	rw	0x0	oa_lane0_hsrx_dphy_ddl_phase_change multiplexer output. Used for debug purposes. (volatile) volatile : true
3	OA_LANE0_HSRX_DPHY_DLL_EN	ro	rw	0x0	oa_lane0_hsrx_dphy_dll_en multiplexer output. Used for debug purposes. (volatile) volatile : true
4	OA_LANE0_HSRX_DPHY_PREAMBLE_CAL_EN	ro	rw	0x0	oa_lane0_hsrx_dphy_preamble_cal_en multiplexer output. Used for debug purposes. (volatile) volatile : true
8:5	OA_LANE0_HSRX_DPHY_DATA_DELAY	ro	rw	0x0	oa_lane0_hsrx_dphy_data_delay multiplexer output. Used for debug purposes. (volatile) volatile : true
9	OA_LANE0_HSRX_DPHY_DDL_VT_COMP_EN	ro	rw	0x0	oa_lane0_hsrx_dphy_ddl_vt_comp_en multiplexer output. Used for debug purposes. (volatile) volatile : true
14:10	OA_LANE0_HSRX_DPHY_DDL_VT_COMP_BIAS	ro	rw	0x0	oa_lane0_hsrx_dphy_ddl_vt_comp_bias multiplexer output. Used for debug purposes. (volatile) volatile : true
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.206 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_7

Reg. 0x1067

Analog macro lane 0 observability
access : read-only

bits	name	s/w	h/w	default	description
4:0	OA_LANE0_HSRX_DPHY_DDL_BIAS	ro	rw	0x0	oa_lane0_hsrx_dphy_ddl_bias multiplexer output. Used for debug purposes. (volatile) volatile : true
8:5	OA_LANE0_HSRX_DPHY_DDL_COARSE_BANK	ro	rw	0x0	oa_lane0_hsrx_dphy_ddl_coarse_bank multiplexer output. Used for debug purposes. (volatile) volatile : true
10:9	OA_LANE0_HSRX_DPHY_DDL_TUNE_MODE	ro	rw	0x0	oa_lane0_hsrx_dphy_ddl_tune_mode multiplexer output. Used for debug purposes. (volatile) volatile : true
15:11	OA_LANE0_HSRX_CPHY_DELAY	ro	rw	0x0	oa_lane0_hsrx_cphy_delay multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.207 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_8

Reg. 0x1068

Analog macro lane 0 observability
access : read-only

bits	name	s/w	h/w	default	description

6:0	OA_LANE0_HSRX_DPHY_DLL_FBK	ro	rw	0x0	oa_lane0_hsrx_dphy_dll_fbk multiplexer output. Used for debug purposes. (volatile) volatile : true
9:7	OA_LANE0_HSRX_EQUALIZER	ro	rw	0x0	oa_lane0_hsrx_equalizer multiplexer output. Used for debug purposes. (volatile) volatile : true
10	OA_LANE0_HSRX_CDPHY_SEL_FAST	ro	rw	0x0	oa_lane0_hsrx_cdphy_sel_fast multiplexer output. Used for debug purposes. (volatile) volatile : true
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.208 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_9

Reg. 0x1069

Analog macro lane 0 observability
access : read-only

bits	name	s/w	h/w	default	description
7:0	OA_LANE0_HSRX_OFFCAL_RIGHT	ro	rw	0x0	oa_lane0_hsrx_offcal_right multiplexer output. Used for debug purposes. (volatile) volatile : true
15:8	OA_LANE0_HSRX_OFFCAL_LEFT	ro	rw	0x0	oa_lane0_hsrx_offcal_left multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.209 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_10

Reg. 0x106A

Analog macro lane 0 observability
access : read-only

bits	name	s/w	h/w	default	description
10:0	OA_LANE0_HSRX_DPHY_DDL_PHASE_RIGHT	ro	rw	0x0	oa_lane0_hsrx_dphy_ddl_phase_right multiplexer output. Used for debug purposes. (volatile) volatile : true
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.210 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_11

Reg. 0x106B

Analog macro lane 0 observability
access : read-only

bits	name	s/w	h/w	default	description
10:0	OA_LANE0_HSRX_DPHY_DDL_PHASE_MID	ro	rw	0x0	oa_lane0_hsrx_dphy_ddl_phase_mid multiplexer output. Used for debug purposes. (volatile) volatile : true
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.211 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_12

Reg. 0x106C

Analog macro lane 0 observability
access : read-only

bits	name	s/w	h/w	default	description
10:0	OA_LANE0_HSRX_DPHY_DDL_PHASE_LEFT	ro	rw	0x0	oa_lane0_hsrx_dphy_ddl_phase_left multiplexer output. Used for debug purposes. (volatile) volatile : true
13:11	OA_LANE0_HSRX_MODE	ro	rw	0x0	oa_lane0_hsrx_mode multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.212 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_13

Reg. 0x106D

Analog macro lane 0 observability

access : read-only

bits	name	s/w	h/w	default	description
15:0	IA_LANE0_HSRX_DATA_AB_LEFT_INT	ro	rw	0x0	ia_lane0_hsrx_data_ab_left multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.213 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_14

Reg. 0x106E

Analog macro lane 0 observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	IA_LANE0_HSRX_DATA_BC_MID_INT	ro	rw	0x0	ia_lane0_hsrx_data_bc_mid_ multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.214 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_15

Reg. 0x106F

Analog macro lane 0 observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	IA_LANE0_HSRX_DATA_CA_RIGHT_INT	ro	rw	0x0	ia_lane0_hsrx_data_ca_right multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.215 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_16

Reg. 0x1070

Analog macro lane 0 observability
access : read-only

bits	name	s/w	h/w	default	description
0	IA_LANE0_HSRX_WORD_CLK_INT	ro	rw	0x0	ia_lane0_hsrx_word_clk multiplexer output. (volatile) volatile : true
1	IA_LANE0_HSRX_HS_CLK_DIV_OUT_INT	ro	rw	0x0	ia_lane0_hsrx_hs_clk_div_out multiplexer output. Used for debug purposes. (volatile) volatile : true
2	IA_LANE0_HSTX_WORD_CLK_INT	ro	rw	0x0	ia_lane0_hstx_word_clk multiplexer output. Used for debug purposes. (volatile) volatile : true
3	IA_LANE0_HSRX_VCM_DET_OUT_INT	ro	rw	0x0	ia_lane0_hsrx_vcm_det_out multiplexer output. Used for debug purposes. (volatile) volatile : true
4	IA_LANE0_HSRX_OUT_CAL_LEFT_N_INT	ro	rw	0x0	ia_lane0_hsrx_out_cal_left_n multiplexer output. Used for debug purposes. (volatile) volatile : true
5	IA_LANE0_HSRX_OUT_CAL_LEFT_P_INT	ro	rw	0x0	ia_lane0_hsrx_out_cal_left_p multiplexer output. Used for debug purposes. (volatile) volatile : true
6	IA_LANE0_HSRX_OUT_CAL_RIGHT_N_INT	ro	rw	0x0	ia_lane0_hsrx_out_cal_right_n multiplexer output. Used for debug purposes. (volatile) volatile : true
7	IA_LANE0_HSRX_OUT_CAL_RIGHT_P_INT	ro	rw	0x0	ia_lane0_hsrx_out_cal_right_p multiplexer output. Used for debug purposes. (volatile) volatile : true
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.216 CORE_DIG_IOCTRL_R_AFE_LANE0_CTRL_17

Reg. 0x1071

Analog macro lane 0 observability
access : read-only

bits	name	s/w	h/w	default	description
0	IA_LANE0_HSRX_DPHY_DDL_OSC_CLK	ro	rw	0x0	ia_lane0_hsrx_dphy_ddl_osc_clk multiplexer output. Used for debug purposes. (volatile)

	_INT				volatile : true
1	IA_LANE0_HSRX_CPHY_ALP_DET_LEFT_OUT_INT	ro	rw	0x0	ia_lane0_hsrx_cphy_alp_det_left_out multiplexer output. Used for debug purposes. (volatile) volatile : true
2	IA_LANE0_HSRX_CPHY_ALP_DET_RIGHT_OUT_INT	ro	rw	0x0	ia_lane0_hsrx_cphy_alp_det_right_out multiplexer output. Used for debug purposes. (volatile) volatile : true
3	IA_LANE0_HSRX_CPHY_CDR_OSC_CLK_INT	ro	rw	0x0	ia_lane0_hsrx_cphy_cdr_osc_clk multiplexer output. Used for debug purposes. (volatile) volatile : true
5:4	IA_LANE0_LPRX_DOUTCD_INT	ro	rw	0x0	ia_lane0_lprx_doutcd multiplexer output. Used for debug purposes. (volatile) volatile : true
7:6	IA_LANE0_LPRX_DOUTLP_INT	ro	rw	0x0	ia_lane0_lprx_doutlp multiplexer output. Used for debug purposes. (volatile) volatile : true
9:8	IA_LANE0_LPRX_DOUTULP_INT	ro	rw	0x0	ia_lane0_lprx_doutulp multiplexer output. Used for debug purposes. (volatile) volatile : true
13:10	IA_LANE0_SPARE_OUT_INT	ro	rw	0x0	ia_lane0_spare_out multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.218 CORE_DIG_RW_TRIO0_0

Reg. 0x1080

Configurations for Trio 0
access : read-write

bits	name	s/w	h/w	default	description
2:0	DESERIALIZER_DATA_EN_DELAY_THRESH	rw	ro	0x2	Counter for deserializer_data_en delay. Quasi static. 0 is a forbidden value.
5:3	DESERIALIZER_DIV_EN_DELAY_THRESH	rw	ro	0x1	Counter for deserializer_div_en delay. In dco_clk cycles. Quasi static. 0 is a forbidden value.
8:6	DESERIALIZER_DIV_EN_DELAY_DEASS_THRESH	rw	ro	0x1	Counter for deassertion of deserializer_div_en after deassertion of deserializer_data_en. In dco_clk cycles, for higher datarates in word_clk cycles. Quasi Static. 0 is a forbidden value.
15:9	POST_RECEIVED_RESET_THRESH	rw	ro	0x2	Counter for resetting the post detected flag. In word_clk cycles. Quasi static.

1.1.1.219 CORE_DIG_RW_TRIO0_1

Reg. 0x1081

Configurations for Trio 0
access : read-write

bits	name	s/w	h/w	default	description
15:0	POST_DET_DELAY_THRESH	rw	ro	0xA	Counter for deassertion of deserializer_data_en after Post2 reception. In dco_clk cycles. Quasi static.

1.1.1.220 CORE_DIG_RW_TRIO0_2

Reg. 0x1082

Configurations for Trio 0
access : read-write

bits	name	s/w	h/w	default	description
7:0	DESERIALIZER_EN_DELAY_DEASS_THRESH	rw	ro	0xA	Counter for deassertion of deserializer_en after deassertion of deserializer_data_en. In dco_clk cycles. Quasi Static. 0 is a forbidden value.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.222 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE1_OVR_0

Reg. 0x1200

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXACTIVEHS_D1_OVR_VAL	rw	ro	0x0	o_rxactivehs_d1_ override value. Used for debug purposes.
1	O_RXSYNCHS_D1_OVR_VAL	rw	ro	0x0	o_rxsynchs_d1_ override value. Used for debug purposes.
3:2	O_RXVALIDHS_D1_OVR_VAL	rw	ro	0x0	o_rxvalidhs_d1_ override value. Used for debug purposes.
4	O_RXSKEWCALHS_D1_OVR_VAL	rw	ro	0x0	o_rxskewcalhs_d1_ override value. Used for debug purposes.
5	O_RXWORDCLKHS_D1_OVR_VAL	rw	ro	0x0	o_rxwordclkhs_d1_ override value. Used for debug purposes.
6	O_RXALTERNATECALHS_D1_OVR_VAL	rw	ro	0x0	o_rxalternatecalhs_d1 override value. Used for debug purposes.
15:7	RESERVED_15_7	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.223 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE1_OVR_1

Reg. 0x1201

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_D1_OVR_VAL	rw	ro	0x0	o_rxdatahs_d1 override value. Used for debug purposes.

1.1.1.224 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE1_OVR_2

Reg. 0x1202

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXACTIVEHS_D1_OVR_EN	rw	ro	0x0	o_rxactivehs_d1 override enable. Active high. Used for debug purposes.
1	O_RXSYNCHS_D1_OVR_EN	rw	ro	0x0	o_rxsynchs_d1 override enable. Active high. Used for debug purposes.
2	O_RXVALIDHS_D1_OVR_EN	rw	ro	0x0	o_rxvalidhs_d1 override enable. Active high. Used for debug purposes.
3	O_RXSKEWCALHS_D1_OVR_EN	rw	ro	0x0	o_rxskewcalhs_d1 override enable. Active high. Used for debug purposes.
4	O_RXWORDCLKHS_D1_OVR_EN	rw	ro	0x0	o_rxwordclkhs_d1 override enable. Active high. Used for debug purposes.
5	O_RXDATAHS_D1_OVR_EN	rw	ro	0x0	o_rxdatahs_d1 override enable. Active high. Used for debug purposes.
6	I_TXREQUESTHS_D1_OVR_EN	rw	ro	0x0	i_txrequesths_d1 override enable. Active high. Used for debug purposes.
7	I_TXDATATRANSFERENHS_D1_OVR_EN	rw	ro	0x0	i_txdatatransferenhs_d1 override enable. Active high. Used for debug purposes.
8	O_TXREADYHS_D1_OVR_EN	rw	ro	0x0	o_txreadyhs_d1 override enable. Active high. Used for debug purposes.
9	O_TXWORDCLKHS_D1_OVR_EN	rw	ro	0x0	o_txwordclkhs_d1 override enable. Active high. Used for debug purposes.
10	I_TXDATAHS_D1_OVR_EN	rw	ro	0x0	i_txdatahs_d1 override enable. Active high. Used for debug purposes.
11	O_RXALTERNATECALHS_D1_OVR_EN	rw	ro	0x0	o_rxalternatecalhs_d1 override enable. Active high. Used for debug purposes.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.225 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE1_OVR_3

Reg. 0x1203

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXCLKESC_D1_OVR_VAL	rw	ro	0x0	o_rxclkesc_d1 override value. Used for debug purposes.
1	O_RXLPDTESC_D1_OVR_VAL	rw	ro	0x0	o_rxlpdtesc_d1 override value. Used for debug purposes.
2	O_RXULPSESC_D1_OVR_VAL	rw	ro	0x0	o_rxulpsesc_d1 override value. Used for debug purposes.
3	O_RXVALIDESC_D1_OVR_VAL	rw	ro	0x0	o_rxvalidesc_d1 override value. Used for debug purposes.
7:4	O_RXTRIGGERESC_D1_OVR_VAL	rw	ro	0x0	o_rxtriggeresc_d1 override value. Used for debug purposes.
15:8	O_RXDATAESC_D1_OVR_VAL	rw	ro	0x0	o_rxdataesc_d1 override value. Used for debug purposes.

1.1.1.226 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE1_OVR_4

Reg. 0x1204

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXCLKESC_D1_OVR_EN	rw	ro	0x0	o_rxclkesc_d1 override enable. Active high. Used for debug purposes.
1	O_RXLPDTESC_D1_OVR_EN	rw	ro	0x0	o_rxlpdtesc_d1 override enable. Active high. Used for debug purposes.
2	O_RXULPSESC_D1_OVR_EN	rw	ro	0x0	o_rxulpsesc_d1 override enable. Active high. Used for debug purposes.
3	O_RXVALIDESC_D1_OVR_EN	rw	ro	0x0	o_rxvalidesc_d1 override enable. Active high. Used for debug purposes.
4	O_RXTRIGGERESC_D1_OVR_EN	rw	ro	0x0	o_rxtriggeresc_d1 override enable. Active high. Used for debug purposes.
5	O_RXDATAESC_D1_OVR_EN	rw	ro	0x0	o_rxdataesc_d1 override enable. Active high. Used for debug purposes.
15:6	RESERVED_15_6	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.227 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE1_OVR_5

Reg. 0x1205

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	I_TXDATAHS_D1_OVR_VAL	rw	ro	0x0	i_txdatahs_d1 override value. Used for debug purposes.

1.1.1.228 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE1_OVR_6

Reg. 0x1206

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_TXREQUESTHS_D1_OVR_VAL	rw	ro	0x0	i_txrequesths_d1 override value. Used for debug purposes.
1	I_TXDATATRANSFERENHS_D1_OVR_VAL	rw	ro	0x0	i_txdatatransferenhs_d1 override value. Used for debug purposes.
2	O_TXREADYHS_D1_OVR_VAL	rw	ro	0x0	o_txreadyhs_d1 override value. Used for debug purposes.
3	O_TXWORDCLKHS_D1_OVR_VAL	rw	ro	0x0	o_txwordclkhs_d1 override value. Used for debug purposes.

4	I_TXSKEWCALHS_D1_OVR_VAL	rw	ro	0x0	i_txskewcalhs_d1 override value. Used for debug purposes.
15:5	RESERVED_15_5	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.229 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE1_OVR_7

Reg. 0x1207

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_TXREQUESTESC_D1_OVR_VAL	rw	ro	0x0	i_txrequestesc_d1 override value. Used for debug purposes.
1	I_TXLPDTESC_D1_OVR_VAL	rw	ro	0x0	i_txlpdtesc_d1 override value. Used for debug purposes.
2	I_TXULPSEXIT_D1_OVR_VAL	rw	ro	0x0	i_txulpsexit_d1 override value. Used for debug purposes.
3	I_TXULPSESC_D1_OVR_VAL	rw	ro	0x0	i_txulpsesc_d1 override value. Used for debug purposes.
4	I_TXVALIDESC_D1_OVR_VAL	rw	ro	0x0	i_txvalidesc_d1 override value. Used for debug purposes.
5	O_TXREADYESC_D1_OVR_VAL	rw	ro	0x0	o_txreadyesc_d1 override value. Used for debug purposes.
9:6	I_TXTRIGGERESC_D1_OVR_VAL	rw	ro	0x0	i_txtriggeresc_d1 override value. Used for debug purposes.
10	I_TXDATAESC_D1_OVR_EN	rw	ro	0x0	i_txdataesc_d1 override enable. Active high. Used for debug purposes.
11	I_TXALTERNATECALHS_D1_OVR_EN	rw	ro	0x0	i_txalternatecalhs_d1 override enable. Active high. Used for debug purposes.
12	I_TXSKEWCALHS_D1_OVR_EN	rw	ro	0x0	i_txskewcalhs_d1 override enable. Active high. Used for debug purposes.
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.230 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE1_OVR_8

Reg. 0x1208

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_TXREQUESTESC_D1_OVR_EN	rw	ro	0x0	i_txrequestesc_d1 override enable. Active high. Used for debug purposes.
1	I_TXLPDTESC_D1_OVR_EN	rw	ro	0x0	i_txlpdtesc_d1 override enable. Active high. Used for debug purposes.
2	I_TXULPSEXIT_D1_OVR_EN	rw	ro	0x0	i_txulpsexit_d1override enable. Active high. Used for debug purposes.
3	I_TXULPSESC_D1_OVR_EN	rw	ro	0x0	i_txulpsesc_d1override enable. Active high. Used for debug purposes.
4	I_TXVALIDESC_D1_OVR_EN	rw	ro	0x0	i_txvalidesc_d1 override enable. Active high. Used for debug purposes.
5	O_TXREADYESC_D1_OVR_EN	rw	ro	0x0	o_txreadyesc_d1override enable. Active high. Used for debug purposes.
6	I_TXTRIGGERESC_D1_OVR_EN	rw	ro	0x0	i_txtriggeresc_d1override enable. Active high. Used for debug purposes.
14:7	I_TXDATAESC_D1_OVR_VAL	rw	ro	0x0	i_txdataesc_d1 override value. Used for debug purposes.
15	I_TXALTERNATECALHS_D1_OVR_VAL	rw	ro	0x0	i_txalternatecalhs_d1 override value. Used for debug purposes.

1.1.1.231 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE1_OVR_9

Reg. 0x1209

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description

0	I_ENABLE_D1_OVR_VAL	rw	ro	0x0	i_enable_d1 override value. Used for debug purposes.
1	O_STOPSTATE_D1_OVR_VAL	rw	ro	0x0	o_stopstate_d1 override value. Used for debug purposes.
2	O_ULPSACTIVENOT_D1_OVR_VAL	rw	ro	0x0	o_ulpsactivenot_d1 override value. Used for debug purposes.
3	I_TURNREQUEST_D1_OVR_VAL	rw	ro	0x0	i_turnrequest_d1 override value. Used for debug purposes.
4	I_TURNDISABLE_D1_OVR_VAL	rw	ro	0x0	i_turndisable_d1 override value. Used for debug purposes.
5	O_DIRECTION_D1_OVR_VAL	rw	ro	0x0	o_direction_d1 override value. Used for debug purposes.
6	I_FORCERXMODE_D1_OVR_VAL	rw	ro	0x0	i_forcerxmode_d1 override value. Used for debug purposes.
7	I_FORCETXSTOPMODE_D1_OVR_VAL	rw	ro	0x0	i_forcetxstopmode_d1 override value. Used for debug purposes.
8	O_ERRESC_D1_OVR_VAL	rw	ro	0x0	o_erresc_d1 override value. Used for debug purposes.
9	O_ERRSYNCESC_D1_OVR_VAL	rw	ro	0x0	o_errsyncesc_d1 override value. Used for debug purposes.
10	O_ERRCONTROL_D1_OVR_VAL	rw	ro	0x0	o_errcontrol_d1 override value. Used for debug purposes.
11	O_ERRCONTENTIONLP0_D1_OVR_VAL	rw	ro	0x0	o_errcontentionlp0_d1 override value. Used for debug purposes.
12	O_ERRCONTENTIONLP1_D1_OVR_VAL	rw	ro	0x0	o_errcontentionlp1_d1 override value. Used for debug purposes.
13	O_ERRSOTHS_D1_OVR_VAL	rw	ro	0x0	o_errsoths_d1 override value. Used for debug purposes.
14	O_ERRSOTSYNCHS_D1_OVR_VAL	rw	ro	0x0	o_errsotsynchs_d1 override value. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.232 CORE_DIG_IOCTRL_RW_DPHY_PPI_LANE1_OVR_10

Reg. 0x120A

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_ENABLE_D1_OVR_EN	rw	ro	0x0	i_enable_d1 override enable. Active high. Used for debug purposes.
1	O_STOPSTATE_D1_OVR_EN	rw	ro	0x0	o_stopstate_d1 override enable. Active high. Used for debug purposes.
2	O_ULPSACTIVENOT_D1_OVR_EN	rw	ro	0x0	o_ulpsactivenot_d1 override enable. Active high. Used for debug purposes.
3	I_TURNREQUEST_D1_OVR_EN	rw	ro	0x0	i_turnrequest_d1 override enable. Active high. Used for debug purposes.
4	I_TURNDISABLE_D1_OVR_EN	rw	ro	0x0	i_turndisable_d1 override enable. Active high. Used for debug purposes.
5	O_DIRECTION_D1_OVR_EN	rw	ro	0x0	o_direction_d1 override enable. Active high. Used for debug purposes.
6	I_FORCERXMODE_D1_OVR_EN	rw	ro	0x0	i_forcerxmode_d1 override enable. Active high. Used for debug purposes.
7	I_FORCETXSTOPMODE_D1_OVR_EN	rw	ro	0x0	i_forcetxstopmode_d1 override enable. Active high. Used for debug purposes.
8	O_ERRESC_D1_OVR_EN	rw	ro	0x0	o_erresc_d1 override enable. Active high. Used for debug purposes.
9	O_ERRSYNCESC_D1_OVR_EN	rw	ro	0x0	o_errsyncesc_d1 override enable. Active high. Used for debug purposes.
10	O_ERRCONTROL_D1_OVR_EN	rw	ro	0x0	o_errcontrol_d1 override enable. Active high. Used for debug purposes.
11	O_ERRCONTENTIONLP0_D1_OVR_EN	rw	ro	0x0	o_errcontentionlp0_d1 override enable. Active high. Used for debug purposes.
12	O_ERRCONTENTIONLP1_D1_OVR_EN	rw	ro	0x0	o_errcontentionlp1_d1 override enable. Active high. Used for debug purposes.
13	O_ERRSOTHS_D1_OVR_EN	rw	ro	0x0	o_errsoths_d1 override enable. Active high. Used for debug purposes.

14	O_ERRSOTSYNCHS_D1_OVR_EN	rw	ro	0x0	o_errsotsynchs_d1 override enable. Active high. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.234 CORE_DIG_IOCTRL_R_DPHY_PPI_LANE1_OVR_0

Reg. 0x1210

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
0	O_RXACTIVEHS_D1	ro	rw	0x0	o_rxactivehs_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	O_RXSYNCHS_D1	ro	rw	0x0	o_rxsynchs_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
3:2	O_RXVALIDHS_D1	ro	rw	0x0	o_rxvalidhs_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
4	O_RXSKEWCALHS_D1	ro	rw	0x0	o_rxskewcalhs_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
5	O_RXWORDCLKHS_D1	ro	rw	0x0	o_rxwordclkhs_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
6	O_RXALTERNATECALHS_D1	ro	rw	0x0	o_rxalternatecalhs_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:7	RESERVED_15_7	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.235 CORE_DIG_IOCTRL_R_DPHY_PPI_LANE1_OVR_1

Reg. 0x1211

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_D1	ro	rw	0x0	o_rxdatahs_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.236 CORE_DIG_IOCTRL_R_DPHY_PPI_LANE1_OVR_2

Reg. 0x1212

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	I_TXDATAHS_D1_INT	ro	rw	0x0	i_txdatahs_d1_int override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.237 CORE_DIG_IOCTRL_R_DPHY_PPI_LANE1_OVR_3

Reg. 0x1213

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
0	I_TXREQUESTESC_D1_INT	ro	rw	0x0	i_txrequestesc_d1_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	I_TXLPDTESC_D1_INT	ro	rw	0x0	i_txlpdtesc_d1_int override multiplexer output. Used for debug purposes. (volatile)

					volatile : true
2	I_TXULPSEXIT_D1_INT	ro	rw	0x0	i_txulpsexit_d1_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
3	I_TXULPSESC_D1_INT	ro	rw	0x0	i_txulpsesc_d1_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
4	I_TXVALIDESC_D1_INT	ro	rw	0x0	i_txvalidesc_d1_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
5	O_TXREADYESC_D1	ro	rw	0x0	o_txreadyesc_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
9:6	I_TXTRIGGERESC_D1_INT	ro	rw	0x0	i_txtriggeresc_d1_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
10	I_TXALTERNATECALHS_D1_INT	ro	rw	0x0	i_txalternatecalhs_d1_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
11	I_TXSKEWCALHS_D1_INT	ro	rw	0x0	i_txskewcalhs_d1_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
12	I_TXREQUESTHS_D1_INT	ro	rw	0x0	i_txrequesths_d1_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
13	I_TXDATATRANSFERENHS_D1_INT	ro	rw	0x0	i_txdatatransferenhs_d1_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
14	O_TXREADYHS_D1	ro	rw	0x0	o_txreadyhs_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15	O_TXWORDCLKHS_D1	ro	rw	0x0	o_txwordclkhs_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.238 CORE_DIG_IOCTRL_R_DPHY_PPI_LANE1_OVR_4

Reg.

0x1214

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
7:0	I_TXDATAESC_D1_INT	ro	rw	0x0	i_txdataesc_d1_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.239 CORE_DIG_IOCTRL_R_DPHY_PPI_LANE1_OVR_5

Reg.

0x1215

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
0	O_RXCLKESC_D1	ro	rw	0x0	o_rxclkesc_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	O_RXLPDTESC_D1	ro	rw	0x0	o_rxlpdtesc_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
2	O_RXULPSESC_D1	ro	rw	0x0	o_rxulpsesc_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
3	O_RXVALIDESC_D1	ro	rw	0x0	o_rxvalidesc_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true

7:4	O_RXTRIGGERESC_D1	ro	rw	0x0	o_rxtriggeresc_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:8	O_RXDATAESC_D1	ro	rw	0x0	o_rxdataesc_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.240 CORE_DIG_IOCTRL_R_DPHY_PPI_LANE1_OVR_6

Reg. 0x1216

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
0	I_ENABLE_D1_INT	ro	rw	0x0	i_enable_d1_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	O_STOPSTATE_D1	ro	rw	0x0	o_stopstate_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
2	O_ULPSACTIVENOT_D1	ro	rw	0x0	o_ulpsactivenot_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
3	I_TURNREQUEST_D1_INT	ro	rw	0x0	i_turnrequest_d1_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
4	I_TURNDISABLE_D1_INT	ro	rw	0x0	i_turndisable_d1_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
5	O_DIRECTION_D1	ro	rw	0x0	o_direction_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
6	I_FORCERXMODE_D1_INT	ro	rw	0x0	i_forcerxmode_d1_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
7	I_FORCETXSTOPMODE_D1_INT	ro	rw	0x0	i_forcetxstopmode_d1_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
8	O_ERRESC_D1	ro	rw	0x0	o_erresc_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
9	O_ERRSYNCESC_D1	ro	rw	0x0	o_errsyncesc_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
10	O_ERRCONTROL_D1	ro	rw	0x0	o_errcontrol_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
11	O_ERRCONTENTIONLP0_D1	ro	rw	0x0	o_errcontentionlp0_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
12	O_ERRCONTENTIONLP1_D1	ro	rw	0x0	o_errcontentionlp1_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
13	O_ERRSOTHS_D1	ro	rw	0x0	o_errsoths_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
14	O_ERRSOTSYNCHS_D1	ro	rw	0x0	o_errsotsynchs_d1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.242 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_0

Reg. 0x1220

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_C1_OVR_VAL	rw	ro	0x0	o_rxdatahs_c1 override value. Used for debug purposes.

1.1.1.243 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_1

Reg. 0x1221

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_C1_OVR_VAL	rw	ro	0x0	o_rxdatahs_c1 override value. Used for debug purposes.

1.1.1.244 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_2

Reg. 0x1222

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXACTIVEHS_C1_OVR_VAL	rw	ro	0x0	o_rxactivehs_c1 override value. Used for debug purposes.
2:1	O_RXSYNCHS_C1_OVR_VAL	rw	ro	0x0	o_rxsynchs_c1 override value. Used for debug purposes.
4:3	O_RXVALIDHS_C1_OVR_VAL	rw	ro	0x0	o_rxvalidhs_c1 override value. Used for debug purposes.
6:5	O_RXINVALIDCODEHS_C1_OVR_VAL	rw	ro	0x0	o_rxinvalidcodehs_c1 override value. Used for debug purposes.
7	O_RXWORDCLKHS_C1_OVR_VAL	rw	ro	0x0	o_rxwordclkhs_c1 override value. Used for debug purposes.
10:8	O_RXSYNCTYPEHS0_C1_OVR_VAL	rw	ro	0x0	o_rxsynctypehs0_c1 override value. Used for debug purposes.
13:11	O_RXSYNCTYPEHS1_C1_OVR_VAL	rw	ro	0x0	o_rxsynctypehs1_c1 override value. Used for debug purposes.
15:14	O_RXALPVALIDHS_C1_OVR_VAL	rw	ro	0x0	o_rxalpvalidhs_c1 override value. Used for debug purposes.

1.1.1.245 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_3

Reg. 0x1223

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXALPVALIDHS_C1_OVR_EN	rw	ro	0x0	o_rxalpvalidhs_c1 override enable. Active high. Used for debug purposes.
4:1	O_RXALPCODE0_C1_OVR_VAL	rw	ro	0x0	o_rxalpcode0_c1 override value. Used for debug purposes.
8:5	O_RXALPCODE1_C1_OVR_VAL	rw	ro	0x0	o_rxalpcode1_c1 override value. Used for debug purposes.
9	O_RXALPNIBBLE0_C1_OVR_EN	rw	ro	0x0	o_rxalpnibble0_c1 override enable. Active high. Used for debug purposes.
10	O_RXALPNIBBLE1_C1_OVR_EN	rw	ro	0x0	o_rxalpnibble1_c1 override enable. Active high. Used for debug purposes.
11	O_RXACTIVEHS_C1_OVR_EN	rw	ro	0x0	o_rxactivehs_c1 override enable. Active high. Used for debug purposes.
12	O_RXSYNCHS_C1_OVR_EN	rw	ro	0x0	o_rxsynchs_c1 override enable. Active high. Used for debug purposes.
13	O_RXVALIDHS_C1_OVR_EN	rw	ro	0x0	o_rxvalidhs_c1 override enable. Active high. Used for debug purposes.
14	O_RXINVALIDCODEHS_C1_OVR_EN	rw	ro	0x0	o_rxinvalidcodehs_c1 override enable. Active high. Used for debug purposes.
15	O_RXWORDCLKHS_C1_OVR_EN	rw	ro	0x0	o_rxwordclkhs_c1 override enable. Active high. Used for debug purposes.

1.1.1.246 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_4

Reg. 0x1224

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXSYNCTYPEHS0_C1_OVR_EN	rw	ro	0x0	o_rxsynctypehs0_c1 override enable. Active high. Used for debug purposes.
1	O_RXSYNCTYPEHS1_C1_OVR_EN	rw	ro	0x0	o_rxsynctypehs1_c1 override enable. Active high. Used for debug purposes.
2	O_RXDATAHS_C1_OVR_EN	rw	ro	0x0	o_rxdatahs_c1 override enable. Active high. Used for debug purposes.
6:3	O_RXALPNIBBLE0_C1_OVR_VAL	rw	ro	0x0	o_rxalpnibble0_c1 override value. Used for debug purposes.
10:7	O_RXALPNIBBLE1_C1_OVR_VAL	rw	ro	0x0	o_rxalpnibble1_c1 override value. Used for debug purposes.
11	O_RXALPCODE0_C1_OVR_EN	rw	ro	0x0	o_rxalpcode0_c1 override enable. Active high. Used for debug purposes.
12	O_RXALPCODE1_C1_OVR_EN	rw	ro	0x0	o_rxalpcode1_c1 override enable. Active high. Used for debug purposes.
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.247 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_5

Reg. 0x1225

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
2:0	I_TXSYNCTYPEHS0_C1_OVR_VAL	rw	ro	0x0	i_txsynctypehs0_c1 override value. Used for debug purposes.
5:3	I_TXSYNCTYPEHS1_C1_OVR_VAL	rw	ro	0x0	i_txsynctypehs1_c1 override value. Used for debug purposes.
7:6	I_TXSENDSYNCHS_C1_OVR_VAL	rw	ro	0x0	i_txsendsynchs_c1 override value. Used for debug purposes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.248 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_6

Reg. 0x1226

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	I_TXDATAHS_C1_OVR_VAL	rw	ro	0x0	i_txdatahs_c1 override value. Used for debug purposes.

1.1.1.249 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_7

Reg. 0x1227

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	I_TXDATAHS_C1_OVR_VAL	rw	ro	0x0	i_txdatahs_c1 override value. Used for debug purposes.

1.1.1.250 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_8

Reg. 0x1228

Digital hard macro interface override

access : read-write

bits	name	s/w	h/w	default	description
0	I_TXREQUESTESC_C1_OVR_VAL	rw	ro	0x0	i_txrequestesc_c1 override value. Used for debug purposes.
1	I_TXLPDTESC_C1_OVR_VAL	rw	ro	0x0	i_txlpdtesc_c1 override value. Used for debug purposes.
2	I_TXULPSEXIT_C1_OVR_VAL	rw	ro	0x0	i_txulpsexit_c1 override value. Used for debug purposes.
3	I_TXULPSESC_C1_OVR_VAL	rw	ro	0x0	i_txulpsesc_c1 override value. Used for debug purposes.
4	I_TXVALIDESC_C1_OVR_VAL	rw	ro	0x0	i_txvalidesc_c1 override value. Used for debug purposes.
5	O_TXREADYESC_C1_OVR_VAL	rw	ro	0x0	o_txreadyesc_c1 override value. Used for debug purposes.
9:6	I_TXTRIGGERESC_C1_OVR_VAL	rw	ro	0x0	i_txtriggeresc_c1 override value. Used for debug purposes.
10	I_TXDATAESC_C1_OVR_EN	rw	ro	0x0	i_txdataesc_c1 override enable. Active high. Used for debug purposes.
11	I_TXREQUESTHS_C1_OVR_VAL	rw	ro	0x0	i_txrequesths_c1 override value. Used for debug purposes.
12	I_TXDATATRANSFERENHS_C1_OVR_VAL	rw	ro	0x0	i_txdatatransferenhs_c1 override value. Used for debug purposes.
13	O_TXREADYHS_C1_OVR_VAL	rw	ro	0x0	o_txreadyhs_c1 override value. Used for debug purposes.
14	O_TXWORDCLKHS_C1_OVR_VAL	rw	ro	0x0	o_txwordclkhs_c1 override value. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.251 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_9

Reg. 0x1229

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_TXREQUESTESC_C1_OVR_EN	rw	ro	0x0	i_txrequestesc_c1 override enable. Active high. Used for debug purposes.
1	I_TXLPDTESC_C1_OVR_EN	rw	ro	0x0	i_txlpdtesc_c1 override enable. Active high. Used for debug purposes.
2	I_TXULPSEXIT_C1_OVR_EN	rw	ro	0x0	i_txulpsexit_c1 override enable. Active high. Used for debug purposes.
3	I_TXULPSESC_C1_OVR_EN	rw	ro	0x0	i_txulpsesc_c1 override enable. Active high. Used for debug purposes.
4	I_TXVALIDESC_C1_OVR_EN	rw	ro	0x0	i_txvalidesc_c1 override enable. Active high. Used for debug purposes.
5	O_TXREADYESC_C1_OVR_EN	rw	ro	0x0	o_txreadyesc_c1 override enable. Active high. Used for debug purposes.
6	I_TXTRIGGERESC_C1_OVR_EN	rw	ro	0x0	i_txtriggeresc_c1 override enable. Active high. Used for debug purposes.
14:7	I_TXDATAESC_C1_OVR_VAL	rw	ro	0x0	i_txdataesc_c1 override value. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.252 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_10

Reg. 0x122A

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXCLKESC_C1_OVR_VAL	rw	ro	0x0	o_rxclkesc_c1 override value. Used for debug purposes.
1	O_RXLPDTESC_C1_OVR_VAL	rw	ro	0x0	o_rxlpdtesc_c1 override value. Used for debug purposes.
2	O_RXULPSESC_C1_	rw	ro	0x0	o_rxulpsesc_c1 override value. Used for debug purposes.

	OVR_VAL				
3	O_RXVALIDESC_C1_OVR_VAL	rw	ro	0x0	o_rxvalidesc_c1 override value. Used for debug purposes.
7:4	O_RXTRIGGERESC_C1_OVR_VAL	rw	ro	0x0	o_rxtriggeresc_c1 override value. Used for debug purposes.
15:8	O_RXDATAESC_C1_OVR_VAL	rw	ro	0x0	o_rxdataesc_c1 override value. Used for debug purposes.

1.1.1.253 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_11

Reg. 0x122B

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	O_RXCLKESC_C1_OVR_EN	rw	ro	0x0	o_rxclkesc_c1 override enable. Active high. Used for debug purposes.
1	O_RXLPDTESC_C1_OVR_EN	rw	ro	0x0	o_rxlpdtesc_c1 override enable. Active high. Used for debug purposes.
2	O_RXULPSESC_C1_OVR_EN	rw	ro	0x0	o_rxulpsesc_c1 override enable. Active high. Used for debug purposes.
3	O_RXVALIDESC_C1_OVR_EN	rw	ro	0x0	o_rxvalidesc_c1 override enable. Active high. Used for debug purposes.
4	O_RXTRIGGERESC_C1_OVR_EN	rw	ro	0x0	o_rxtriggeresc_c1 override enable. Active high. Used for debug purposes.
5	O_RXDATAESC_C1_OVR_EN	rw	ro	0x0	o_rxdataesc_c1 override enable. Active high. Used for debug purposes.
6	I_TXREQUESTHS_C1_OVR_EN	rw	ro	0x0	i_txrequesths_c1 override enable. Active high. Used for debug purposes.
7	I_TXDATATRANSFERENHS_C1_OVR_EN	rw	ro	0x0	i_txdatatransferenhs_c1 override enable. Active high. Used for debug purposes.
8	O_TXREADYHS_C1_OVR_EN	rw	ro	0x0	o_txreadyhs_c1 override enable. Active high. Used for debug purposes.
9	O_TXWORDCLKHS_C1_OVR_EN	rw	ro	0x0	o_txwordclkhs_c1 override enable. Active high. Used for debug purposes.
10	I_TXDATAHS_C1_OVR_EN	rw	ro	0x0	i_txdatahs_c1 override enable. Active high. Used for debug purposes.
11	I_TXSENDSYNCHS_C1_OVR_EN	rw	ro	0x0	i_txsendsynchs_c1 override enable. Active high. Used for debug purposes.
12	I_TXSYNCTYPEHS0_C1_OVR_EN	rw	ro	0x0	i_txsynctypehs0_c1 override enable. Active high. Used for debug purposes.
13	I_TXSYNCTYPEHS1_C1_OVR_EN	rw	ro	0x0	i_txsynctypehs1_c1 override enable. Active high. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.254 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_12

Reg. 0x122C

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_ENABLE_C1_OVR_VAL	rw	ro	0x0	i_enable_c1 override value. Used for debug purposes.
1	O_STOPSTATE_C1_OVR_VAL	rw	ro	0x0	o_stopstate_c1 override value. Used for debug purposes.
2	O_ULPSACTIVENOT_C1_OVR_VAL	rw	ro	0x0	o_ulpsactivenot_c1 override value. Used for debug purposes.
3	I_TURNREQUEST_C1_OVR_VAL	rw	ro	0x0	i_turnrequest_c1 override value. Used for debug purposes.
4	I_TURNDISABLE_C1_OVR_VAL	rw	ro	0x0	i_turndisable_c1 override value. Used for debug purposes.
5	O_DIRECTION_C1_OVR_VAL	rw	ro	0x0	o_direction_c1 override value. Used for debug purposes.
6	I_FORCERXMODE_C1_OVR_VAL	rw	ro	0x0	i_forcerxmode_c1 override value. Used for debug purposes.

7	I_FORCETXSTOPMODE_C1_OVR_VAL	rw	ro	0x0	i_forcetxstopmode_c1 override value. Used for debug purposes.
8	O_ERRESC_C1_OVR_VAL	rw	ro	0x0	o_erresc_c1 override value. Used for debug purposes.
9	O_ERRSYNCESC_C1_OVR_VAL	rw	ro	0x0	o_errsyncesc_c1 override value. Used for debug purposes.
10	O_ERRCONTROL_C1_OVR_VAL	rw	ro	0x0	o_errcontrol_c1 override value. Used for debug purposes.
11	O_ERRCONTENTIONLP0_C1_OVR_VAL	rw	ro	0x0	o_errcontentionlp0_c1 override value. Used for debug purposes.
12	O_ERRCONTENTIONLP1_C1_OVR_VAL	rw	ro	0x0	o_errcontentionlp1_c1 override value. Used for debug purposes.
13	O_ERRSOTHS_C1_OVR_VAL	rw	ro	0x0	o_errsoths_c1 override value. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.255 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_13

Reg. 0x122D

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_ENABLE_C1_OVR_EN	rw	ro	0x0	i_enable_c1 override enable. Active high. Used for debug purposes.
1	O_STOPSTATE_C1_OVR_EN	rw	ro	0x0	o_stopstate_c1 override enable. Active high. Used for debug purposes.
2	O_ULPSACTIVENOT_C1_OVR_EN	rw	ro	0x0	o_ulpsactivenot_c1 override enable. Active high. Used for debug purposes.
3	I_TURNREQUEST_C1_OVR_EN	rw	ro	0x0	i_turnrequest_c1 override enable. Active high. Used for debug purposes.
4	I_TURNDISABLE_C1_OVR_EN	rw	ro	0x0	i_turndisable_c1 override enable. Active high. Used for debug purposes.
5	O_DIRECTION_C1_OVR_EN	rw	ro	0x0	o_direction_c1 override enable. Active high. Used for debug purposes.
6	I_FORCERXMODE_C1_OVR_EN	rw	ro	0x0	i_forcerxmode_c1 override enable. Active high. Used for debug purposes.
7	I_FORCETXSTOPMODE_C1_OVR_EN	rw	ro	0x0	i_forcetxstopmode_c1 override enable. Active high. Used for debug purposes.
8	O_ERRESC_C1_OVR_EN	rw	ro	0x0	o_erresc_c1 override enable. Active high. Used for debug purposes.
9	O_ERRSYNCESC_C1_OVR_EN	rw	ro	0x0	o_errsyncesc_c1 override enable. Active high. Used for debug purposes.
10	O_ERRCONTROL_C1_OVR_EN	rw	ro	0x0	o_errcontrol_c1 override enable. Active high. Used for debug purposes.
11	O_ERRCONTENTIONLP0_C1_OVR_EN	rw	ro	0x0	o_errcontentionlp0_c1 override enable. Active high. Used for debug purposes.
12	O_ERRCONTENTIONLP1_C1_OVR_EN	rw	ro	0x0	o_errcontentionlp1_c1 override enable. Active high. Used for debug purposes.
13	O_ERRSOTHS_C1_OVR_EN	rw	ro	0x0	o_errsoths_c1 override enable. Active high. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.256 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_14

Reg. 0x122E

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_TXALPCODE0_C1_OVR_EN	rw	ro	0x0	i_txalpcode0_c1 override enable. Active high. Used for debug purposes.
1	I_TXALPCODE1_C1_OVR_EN	rw	ro	0x0	i_txalpcode1_c1 override enable. Active high. Used for debug purposes.
3:2	I_TXSENDALPHS_C1_OVR_VAL	rw	ro	0x0	i_txsendalphs_c1 override value. Used for debug purposes.

7:4	I_TXALPNIBBLE0_C1_OVR_VAL	rw	ro	0x0	i_txalpnibble0_c1 override value. Used for debug purposes.
11:8	I_TXALPNIBBLE1_C1_OVR_VAL	rw	ro	0x0	i_txalpnibble1_c1 override value. Used for debug purposes.
14:12	I_ALPWAKESTATE_C1_OVR_VAL	rw	ro	0x0	i_alpwakestate_c1 override value. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.257 CORE_DIG_IOCTRL_RW_CPHY_PPI_LANE1_OVR_15

Reg. 0x122F

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_TXSENDALPHS_C1_OVR_EN	rw	ro	0x0	i_txsendalphs_c1 override enable. Active high. Used for debug purposes.
1	I_TXALPNIBBLE0_C1_OVR_EN	rw	ro	0x0	i_txalpnibble0_c1 override enable. Active high. Used for debug purposes.
2	I_TXALPNIBBLE1_C1_OVR_EN	rw	ro	0x0	i_txalpnibble1_c1 override enable. Active high. Used for debug purposes.
3	I_ALPWAKESTATE_C1_OVR_EN	rw	ro	0x0	i_alpwakestate_c1 override enable. Active high. Used for debug purposes.
7:4	I_TXALPCODE0_C1_OVR_VAL	rw	ro	0x0	i_txalpcode0_c1 override value. Used for debug purposes.
11:8	I_TXALPCODE1_C1_OVR_VAL	rw	ro	0x0	i_txalpcode1_c1 override value. Used for debug purposes.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.258 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_0

Reg. 0x1230

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_C1	ro	rw	0x0	o_rxdatahs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.259 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_1

Reg. 0x1231

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_C1	ro	rw	0x0	o_rxdatahs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.260 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_2

Reg. 0x1232

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_C1	ro	rw	0x0	o_rxdatahs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.261 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_3

Reg. 0x1233

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
0	O_RXACTIVEHS_C1	ro	rw	0x0	o_rxactivehs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
2:1	O_RXSYNCHS_C1	ro	rw	0x0	o_rxsynchs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
4:3	O_RXVALIDHS_C1	ro	rw	0x0	o_rxvalidhs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
6:5	O_RXINVALIDCODEHS_C1	ro	rw	0x0	o_rxinvalidcodehs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
7	O_RXWORDCLKHS_C1	ro	rw	0x0	o_rxwordclkhs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
10:8	O_RXSYNCTYPEHS0_C1	ro	rw	0x0	o_rxsynctypehs0_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
13:11	O_RXSYNCTYPEHS1_C1	ro	rw	0x0	o_rxsynctypehs1_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.262 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_4

Reg. 0x1234

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
3:0	O_RXALPCODE0_C1	ro	rw	0x0	o_rxalpcode0_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
7:4	O_RXALPCODE1_C1	ro	rw	0x0	o_rxalpcode1_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.263 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_5

Reg. 0x1235

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
2:0	I_TXSYNCTYPEHS0_C1_INT	ro	rw	0x0	i_txsynctypehs0_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
5:3	I_TXSYNCTYPEHS1_C1_INT	ro	rw	0x0	i_txsynctypehs1_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
13:6	I_TXDATAESC_C1_INT	ro	rw	0x0	i_txdataesc_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.264 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_6

Reg. 0x1236

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
1:0	O_RXALPVALIDHS_C1	ro	rw	0x0	o_rxalpvalidhs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
5:2	O_RXALPNIBBLE0_C1	ro	rw	0x0	o_rxalpnibble0_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
9:6	O_RXALPNIBBLE1_C1	ro	rw	0x0	o_rxalpnibble1_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
11:10	I_TXSENDSYNCHS_C1_INT	ro	rw	0x0	i_txsendsynchs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.265 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_7

Reg. 0x1237

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	I_TXDATAHS_C1_INT	ro	rw	0x0	i_txdatahs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.266 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_8

Reg. 0x1238

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	I_TXDATAHS_C1_INT	ro	rw	0x0	i_txdatahs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.267 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_9

Reg. 0x1239

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
0	I_TXREQUESTESC_C1_INT	ro	rw	0x0	i_txrequestesc_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	I_TXLPDTESC_C1_INT	ro	rw	0x0	i_txlpdtesc_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
2	I_TXULPSEXIT_C1_INT	ro	rw	0x0	i_txulpsexit_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
3	I_TXULPSESC_C1_INT	ro	rw	0x0	i_txulpsesc_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
4	I_TXVALIDESC_C1_INT	ro	rw	0x0	i_txvalidesc_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
5	O_TXREADYESC_C1	ro	rw	0x0	o_txreadyesc_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true

9:6	I_TXTRIGGERESC_C1_INT	ro	rw	0x0	i_txtriggeresc_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
10	I_TXREQUESTHS_C1_INT	ro	rw	0x0	i_txrequesths_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
11	I_TXDATATRANSFERENHS_C1_INT	ro	rw	0x0	i_txdatatransferenhs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
12	O_TXREADYHS_C1	ro	rw	0x0	o_txreadyhs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
13	O_TXWORDCLKHS_C1	ro	rw	0x0	o_txwordclkhs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.268 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_10

Reg. 0x123A

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
0	O_RXCLKESC_C1	ro	rw	0x0	o_rxclkesc_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	O_RXLPDTESC_C1	ro	rw	0x0	o_rxlpdtesc_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
2	O_RXULPSESC_C1	ro	rw	0x0	o_rxulpsesc_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
3	O_RXVALIDESC_C1	ro	rw	0x0	o_rxvalidesc_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
7:4	O_RXTRIGGERESC_C1	ro	rw	0x0	o_rxtriggeresc_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:8	O_RXDATAESC_C1	ro	rw	0x0	o_rxdataesc_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.269 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_11

Reg. 0x123B

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
0	I_ENABLE_C1_INT	ro	rw	0x0	i_enable_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	O_STOPSTATE_C1	ro	rw	0x0	o_stopstate_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
2	O_ULPSACTIVENOT_C1	ro	rw	0x0	o_ulpsactivenot_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
3	I_TURNREQUEST_C1_INT	ro	rw	0x0	i_turnrequest_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
4	I_TURNDISABLE_C1_INT	ro	rw	0x0	i_turndisable_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
5	O_DIRECTION_C1	ro	rw	0x0	o_direction_c1 override multiplexer output. Used for debug purposes. (volatile)

					volatile : true
6	I_FORCERXMODE_C1_INT	ro	rw	0x0	i_forcerxmode_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
7	I_FORCETXSTOPMODE_C1_INT	ro	rw	0x0	i_forcetxstopmode_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
8	O_ERRESC_C1	ro	rw	0x0	o_erresc_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
9	O_ERRSYNCESC_C1	ro	rw	0x0	o_errsyncesc_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
10	O_ERRCONTROL_C1	ro	rw	0x0	o_errcontrol_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
11	O_ERRCONTENTIONLP0_C1	ro	rw	0x0	o_errcontentionlp0_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
12	O_ERRCONTENTIONLP1_C1	ro	rw	0x0	o_errcontentionlp1_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
13	O_ERRSOTHS_C1	ro	rw	0x0	o_errsoths_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.270 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_12

Reg. 0x123C

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_C1	ro	rw	0x0	o_rxdatahs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.271 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_13

Reg. 0x123D

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	O_RXDATAHS_C1	ro	rw	0x0	o_rxdatahs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.272 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_14

Reg. 0x123E

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
1:0	I_TXSENDALPHS_C1_INT	ro	rw	0x0	i_txsendalphs_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
5:2	I_TXALPCODE0_C1_INT	ro	rw	0x0	i_txalpcode0_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
9:6	I_TXALPCODE1_C1_INT	ro	rw	0x0	i_txalpcode1_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true

12:10	I_ALPWAKESTATE_C1_INT	ro	rw	0x0	i_alpwakestate_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.273 CORE_DIG_IOCTRL_R_CPHY_PPI_LANE1_OVR_15

Reg. 0x123F

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
3:0	I_TXALPNIBBLE0_C1_INT	ro	rw	0x0	i_txalpnibble0_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
7:4	I_TXALPNIBBLE1_C1_INT	ro	rw	0x0	i_txalpnibble1_c1 override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.274 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_0

Reg. 0x1240

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
10:0	OA_LANE1_SPARE_IN	rw	ro	0x0	Lane 1 input spare bus (bits[10:9] independent current programmability 0-100% 1-75% 2-150% 3-125%; bit[8] vt drift compensation bypass; bit[7] dcc programmability 0-filter bandwidth 100% 1-filter bandwidth 200%; bits[6:0] spare bus) This signal is quasi-static.
11	OA_LANE1_SHORT_LB_EN	rw	ro	0x0	oa_lane1_short_lb_en bit configuration.This signal is quasi-static. Please check table for more details.
12	OA_LANE1_HSTX_LOWCAP_EN_OVR_EN	rw	ro	0x0	oa_lane1_hstx_lowcap_en override enable. Active high. Used for debug purposes.
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.275 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_1

Reg. 0x1241

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
4:0	OA_LANE1_HSRX_DPHY_DDL_BIAS_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_bias override value. Used for debug purposes.
11:5	OA_LANE1_HSRX_DPHY_DLL_FBK_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_dphy_dll_fbk override value. Used for debug purposes.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.276 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_2

Reg. 0x1242

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_LANE1_SEL_LANE_CFG	rw	ro	0x0	Lane 1 D-PHY/C-PHY configuration. 1'b0: D-PHY data lane (when phy_mode is 1'b0); C-PHY slave lane (when phy_mode is 1'b1). 1'b1: D-PHY clock lane (when phy_mode is 1'b0); C-PHY master lane (when phy_mode is 1'b1). This signal is quasi-static. Please check table for more details.
1	OA_LANE1_HSRX_CPHY_CDR_FBK_FAS	rw	ro	0x0	oa_lane1_hsrx_cphy_cdr_fbk_fast_lock_en override enable. Active high. Used for debug purposes.

	T_LOCK_EN_OVR_EN				
2	OA_LANE1_HSRX_TERM_EN200OHMS	rw	ro	0x0	Lane 1 HS-RX termination value. Please check table for more details.
3	OA_LANE1_HSRX_DPHY_DDL_PON_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_pon override value. Used for debug purposes.
5:4	OA_LANE1_HSTX_LOWCAP_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hstx_lowcap_en override value. Used for debug purposes.
6	OA_LANE1_HSTX_DIV_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hstx_div_en override value. Used for debug purposes.
7	OA_LANE1_HSTX_DATA_BC_OVR_EN	rw	ro	0x0	oa_lane1_hstx_data_ca override enable. Active high. Used for debug purposes.
8	OA_LANE1_HSTX_DATA_CA_OVR_EN	rw	ro	0x0	oa_lane1_hstx_data_ca override enable. Active high. Used for debug purposes.
10:9	OA_LANE1_HSTX_TERM_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hstx_term_en override value. Used for debug purposes.
11	OA_LANE1_HSRX_DPHY_DDL_EN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_en override enable. Active high. Used for debug purposes.
12	OA_LANE1_HSRX_CDPHY_SEL_FAST_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_cdphy_sel_fast override enable. Active high. Used for debug purposes.
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.277 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_3

Reg. 0x1243

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
1:0	OA_LANE1_HSTX_PON_OVR_VAL	rw	ro	0x0	oa_lane1_hstx_pon override value. Used for debug purposes.
3:2	OA_LANE1_HSTX_BOOST_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hstx_boost_en override value. Used for debug purposes.
4	OA_LANE1_HSTX_SEL_PHASE0	rw	ro	0x1	Lane 1 HS-TX clock phase selection. 1'b0: 90 (for D-PHY clock lane configuration). 1'b1: 0 (for both C-PHY and D-PHY data lane configurations). This signal is quasi-static. Please check table for more details.
7:5	OA_LANE1_HSTX_EQA	rw	ro	0x0	Lane 1 HS-TX de-emphasis word (upper-half). This signal is quasi-static. Please check table for more details.
8	OA_LANE1_HSTX_SEL_CLKLB	rw	ro	0x1	Lane 1 HS-TX clock source. 1'b0: External PLL clock. 1'b1: Common block internal DCO clock. This signal is quasi-static.
9	OA_LANE1_LPTX_DIN_DN_OVR_VAL	rw	ro	0x0	oa_lane1_lptx_din_dn override value. Used for debug purposes.
10	OA_LANE1_LPTX_DIN_DP_OVR_VAL	rw	ro	0x0	oa_lane1_lptx_din_dp override value. Used for debug purposes.
11	OA_LANE1_HSRX_DPHY_DDL_DCC_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_dcc_en override value. Used for debug purposes.
12	OA_LANE1_HSRX_DPHY_DDL_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_en override value. Used for debug purposes.
13	OA_LANE1_HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_cphy_cdr_fbk_fast_lock_en override value. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.278 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_4

Reg. 0x1244

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description

0	OA_LANE1_HSTX_PON_OVR_EN	rw	ro	0x0	oa_lane1_hstx_pon override enable. Active high. Used for debug purposes.
1	OA_LANE1_HSTX_BOOST_EN_OVR_EN	rw	ro	0x0	oa_lane1_hstx_boost_en override enable. Active high. Used for debug purposes.
4:2	OA_LANE1_HSTX_EQB	rw	ro	0x0	Lane 1 HS-TX de-emphasis word (lower-half). This signal is quasi-static. Please check table for more details.
5	OA_LANE1_HSTX_CLK_OBS_EN	rw	ro	0x0	Lane 1 HS clock pattern driven in the lines (debug feature). Active high. This signal is quasi-static.
6	OA_LANE1_LPTX_DIN_DN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes.
7	OA_LANE1_LPTX_DIN_DP_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes.
9:8	OA_LANE1_LPTX_SR_BYPASS_EN	rw	ro	0x0	oa_lane1_lptx_sr_bypass_en override enable. Active high. Used for debug purposes.
10	OA_LANE1_HSTX_TERM_EN_OVR_EN	rw	ro	0x0	oa_lane1_hstx_term_en override enable. Active high. Used for debug purposes.
11	OA_LANE1_HSRX_DPHY_DDL_DCC_EN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.279 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_5

Reg. 0x1245

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
15:0	OA_LANE1_HSTX_DATA_AB_DPHY_OVR_VAL	rw	ro	0x0	oa_lane1_hstx_data_ab_dphy override value. Used for debug purposes.

1.1.1.280 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_6

Reg. 0x1246

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
13:0	OA_LANE1_HSTX_DATA_BC_OVR_VAL	rw	ro	0x0	oa_lane1_hstx_data_bc override value. Used for debug purposes.
14	OA_LANE1_HSTX_DATA_AB_DPHY_OVR_EN	rw	ro	0x0	oa_lane1_hstx_data_ab_dphy override enable. Active high. Used for debug purposes.
15	OA_LANE1_HSRX_DPHY_DDL_PON_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_pon override enable. Active high. Used for debug purposes.

1.1.1.281 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_7

Reg. 0x1247

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
13:0	OA_LANE1_HSTX_DATA_CA_OVR_VAL	rw	ro	0x0	oa_lane1_hstx_data_ca override value. Used for debug purposes.
15:14	OA_LANE1_HSRX_GMODE	rw	ro	0x2	Lane 1 HS-RX preamplifier bandwidth configuration. This signal is quasi-static. Please check table for more details.

1.1.1.282 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_8

Reg. 0x1248

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
1:0	OA_LANE1_LPTX_EN_OVR_VAL	rw	ro	0x0	oa_lane1_lptx_en override value. Used for debug purposes.

3:2	OA_LANE1_LPTX_PON_OVR_VAL	rw	ro	0x0	oa_lane1_lptx_pon override value. Used for debug purposes.
5:4	OA_LANE1_LPTX_PULLDWN_EN_OVR_VAL	rw	ro	0x0	oa_lane1_lptx_pulldwn_en override value. Used for debug purposes.
6	OA_LANE1_LPRX_LP_PON_OVR_EN	rw	ro	0x0	oa_lane1_lprx_lp_pon override enable. Active high. Used for debug purposes.
7	OA_LANE1_LPRX_CD_PON_OVR_EN	rw	ro	0x0	oa_lane1_lprx_cd_pon override enable. Active high. Used for debug purposes.
8	OA_LANE1_LPRX_ULP_PON_OVR_EN	rw	ro	0x0	oa_lane1_lprx_ulp_pon override enable. Active high. Used for debug purposes.
9	OA_LANE1_HSRX_CPHY_CDR_FBK_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_cphy_cdr_fbk_en override value. Used for debug purposes.
13:10	OA_LANE1_HSRX_CPHY_CDR_FBK_CAP_PROG	rw	ro	0x7	Lane 1 C-PHY low-pass filter bandwidth (symbol rate dependent). This signal is quasi-static. Please check table for more details.
14	OA_LANE1_HSRX_VCM_DET_SYNC_BYPASS	rw	ro	0x0	Enable vcm detector filter bypass which controls CDR input propagation. This signal is quasi-static. Please check table for more details.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.283 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_9

Reg. 0x1249

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
1:0	OA_LANE1_LPRX_LP_PON_OVR_VAL	rw	ro	0x0	oa_lane1_lprx_lp_pon override value. Used for debug purposes.
3:2	OA_LANE1_LPRX_CD_PON_OVR_VAL	rw	ro	0x0	oa_lane1_lprx_cd_pon override value. Used for debug purposes.
5:4	OA_LANE1_LPRX_ULP_PON_OVR_VAL	rw	ro	0x0	oa_lane1_lprx_ulp_pon override value. Used for debug purposes.
6	OA_LANE1_LPTX_EN_OVR_EN	rw	ro	0x0	oa_lane1_lptx_en override enable. Active high. Used for debug purposes.
7	OA_LANE1_LPTX_PON_OVR_EN	rw	ro	0x0	oa_lane1_lptx_pon override enable. Active high. Used for debug purposes.
8	OA_LANE1_LPTX_PULLDWN_EN_OVR_EN	rw	ro	0x0	oa_lane1_lptx_pulldwn_en override enable. Active high. Used for debug purposes.
9	OA_LANE1_HSRX_CPHY_CDR_FBK_EN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_cphy_cdr_fbk_en override enable. Active high. Used for debug purposes.
10	OA_LANE1_HSRX_CPHY_MASK_CHANGE_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_cphy_mask_change override value. Used for debug purposes.
11	OA_LANE1_HSRX_CPHY_DELAY_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_cphy_delay override enable. Active high. Used for debug purposes.
12	OA_LANE1_HSRX_CDPHY_SEL_FAST_OVR_VAL	rw	ro	0x1	oa_lane1_hsrx_cdphy_sel_fast override value. Please check table for more details.
14:13	OA_LANE1_HSRX_CDPHY_SEL_TYPE	rw	ro	0x0	oa_lane1_hsrx_cdphy_sel_type override value. Active high. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.284 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_10

Reg. 0x124A

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
2:0	OA_LANE1_HSRX_EQUALIZER_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_equalizer override value. Used for debug purposes.

5:3	OA_LANE1_HSRX_HS_CLK_DIV	rw	ro	0x7	Lane 1 D-PHY DDR clock lane divider (data rate dependent). This signal is quasi-static. Please check table for more details.
6	OA_LANE1_HSRX_SEL_GATED_POLARITY	rw	ro	0x0	Lane <0> deserializer output polarity (D-PHY related). Active high. This signal is quasi-static. Please check table for more details.
9:7	OA_LANE1_HSRX_CPHY_CDR_DIV	rw	ro	0x5	Lane 1 C-PHY oscillation clock divider (for calibration). This signal is quasi-static. Please check table for more details.
14:10	OA_LANE1_HSRX_CPHY_DELAY_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_cphy_delay override value. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.285 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_11

Reg. 0x124B

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_LANE1_HSRX_TERM_RIGHT_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_term_right_en override value. Used for debug purposes.
1	OA_LANE1_HSRX_TERM_LEFT_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_term_left_en override value. Used for debug purposes.
2	OA_LANE1_HSRX_DPHY_CLK_CHANNEL_PULL_EN	rw	ro	0x0	Lane 1 D-PHY clock channel pull-up/pull-down enable. Active high. This signal is quasi-static. Please check table for more details.
3	OA_LANE1_HSRX_HS_CLK_DIV_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_hs_clk_div_en override value. Used for debug purposes.
4	OA_LANE1_HSRX_DESERIALIZER_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_deserializer_en override value. Used for debug purposes.
5	OA_LANE1_HSRX_DESERIALIZER_DATA_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_deserializer_data_en override value. Used for debug purposes.
6	OA_LANE1_HSRX_DESERIALIZER_DIV_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_deserializer_div_en override value. Used for debug purposes.
7	OA_LANE1_HSRX_OFFCAL_OBS_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_offcal_obs_en override value. Used for debug purposes.
8	OA_LANE1_HSRX_VCM_DET_PON_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_vcm_det_pon override value. Used for debug purposes.
9	OA_LANE1_HSRX_VCM_DET_OUT_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_vcm_det_out_en override value. Used for debug purposes.
10	OA_LANE1_HSRX_CPHY_ALP_DET_RIGHT_PON_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_cphy_alp_det_right_pon override value. Used for debug purposes.
11	OA_LANE1_HSRX_CPHY_ALP_DET_LEFT_PON_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_cphy_alp_det_left_pon override value. Used for debug purposes.
12	OA_LANE1_HSRX_CPHY_MASK_CHANGE_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_cphy_mask_change override enable. Active high. Used for debug purposes.
13	OA_LANE1_HSRX_PON_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_pon override enable. Active high. Used for debug purposes.
14	OA_LANE1_HSRX_EN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_en override enable. Active high. Used for debug purposes.
15	OA_LANE1_HSTX_DIV_EN_OVR_EN	rw	ro	0x0	oa_lane1_hstx_div_en override enable. Active high. Used for debug purposes.

1.1.1.286 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_12

Reg. 0x124C

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_LANE1_HSRX_TERM_RIGHT_EN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_term_right_en override enable. Active high. Used for debug purposes.
1	OA_LANE1_HSRX_TERM_LEFT_EN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_term_left_en override enable. Active high. Used for debug purposes.
2	OA_LANE1_HSRX_HS_CLK_DIV_EN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_hs_clk_div_en override enable. Active high. Used for debug purposes.
3	OA_LANE1_HSRX_DESERIALIZER_EN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_deserializer_en override enable. Active high. Used for debug purposes.
4	OA_LANE1_HSRX_DESERIALIZER_DATA_EN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_deserializer_data_en override enable. Active high. Used for debug purposes.
5	OA_LANE1_HSRX_DESERIALIZER_DIV_EN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_deserializer_div_en override enable. Active high. Used for debug purposes.
6	OA_LANE1_HSRX_OFFCAL_OBS_EN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_offcal_obs_en override enable. Active high. Used for debug purposes.
7	OA_LANE1_HSRX_VCM_DET_PON_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_vcm_det_pon override enable. Active high. Used for debug purposes.
8	OA_LANE1_HSRX_VCM_DET_OUT_EN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_vcm_det_out_en override enable. Active high. Used for debug purposes.
9	OA_LANE1_HSRX_CPHY_ALP_DET_RIGHT_PON_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_cphy_alp_det_right_pon override enable. Active high. Used for debug purposes.
10	OA_LANE1_HSRX_CPHY_ALP_DET_LEFT_PON_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_cphy_alp_det_left_pon override enable. Active high. Used for debug purposes.
12:11	OA_LANE1_HSRX_PON_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_pon override value. Used for debug purposes.
14:13	OA_LANE1_HSRX_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_en override value. Used for debug purposes.
15	OA_LANE1_HSRX_CPHY_SR_BYPASS_Z	rw	ro	0x0	Enable for the slew rate control latch bypass inside CDR. This signal is quasi-static. Please check table for more details.

1.1.1.287 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_13

Reg. 0x124D

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_LANE1_HSRX_DPHY_DDL_BIAS_BYPASS_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_bias_bypass_en override value. Used for debug purposes.
1	OA_LANE1_HSRX_DPHY_DDL_BYPASS_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_bypass_en override value. Used for debug purposes.
2	OA_LANE1_HSRX_DPHY_DDL_PHASE_CHANGE_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_phase_change override value. Used for debug purposes.
3	OA_LANE1_HSRX_DPHY_DLL_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_dphy_dll_en override value. Used for debug purposes.
4	OA_LANE1_HSRX_DPHY_PREAMBLE_CAL_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_dphy_preamble_cal_en override value. Used for debug purposes.
9:5	OA_LANE1_HSRX_DPHY_DDL_VT_COMP	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_vt_comp_bias override value. Used for debug purposes.

	_BIAS_OVR_VAL				
10	OA_LANE1_HSRX_DPHY_DATA_DELAY_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_data_delay override enable. Active high. Used for debug purposes.
13:11	OA_LANE1_HSRX_DPHY_DDL_DIV	rw	ro	0x2	Lane 1 HS-RX DDL oscillation clock divider. This signal is quasi-static. Please check table for more details.
15:14	OA_LANE1_HSRX_CPHY_FINE_RANGE	rw	ro	0x0	Delay line fine delay cell setting for DDL. This signal is quasi-static. Please check table for more details.

1.1.1.288 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_14

Reg. 0x124E

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_LANE1_HSRX_DPHY_DDL_BIAS_BYPASS_EN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_bias_bypass_en override enable. Active high. Used for debug purposes.
1	OA_LANE1_HSRX_DPHY_DDL_BYPASS_EN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_bypass_en override enable. Active high. Used for debug purposes.
2	OA_LANE1_HSRX_DPHY_DDL_PHASE_CHANGE_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_phase_change override enable. Active high. Used for debug purposes.
3	OA_LANE1_HSRX_DPHY_DLL_EN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_dll_en override enable. Active high. Used for debug purposes.
4	OA_LANE1_HSRX_DPHY_PREAMBLE_CAL_EN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_preamble_cal_en override enable. Active high. Used for debug purposes.
5	OA_LANE1_HSRX_DPHY_DDL_VT_COMP_EN_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_vt_comp_en override enable. Used for debug purposes.
9:6	OA_LANE1_HSRX_DPHY_DATA_DELAY_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_dphy_data_delay override value. Used for debug purposes.
10	OA_LANE1_HSRX_DPHY_DDL_BIAS_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_bias override enable. Active high. Used for debug purposes.
11	OA_LANE1_HSRX_DPHY_DDL_COARSE_BANK_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_coarse_bank override enable. Active high. Used for debug purposes.
12	OA_LANE1_HSRX_DPHY_DDL_TUNE_MODE_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_tune_mode override enable. Active high. Used for debug purposes.
13	OA_LANE1_HSRX_DPHY_DLL_FBK_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_dll_fbk override enable. Active high. Used for debug purposes.
14	OA_LANE1_HSRX_EQUALIZER_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_equalizer override enable. Active high. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.289 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_15

Reg. 0x124F

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
3:0	OA_LANE1_HSRX_DPHY_DDL_COARSE_BANK_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_coarse_bank override value. Used for debug purposes.
5:4	OA_LANE1_HSRX_DPHY_DDL_TUNE_MODE_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_tune_mode override value. Used for debug purposes.
6	OA_LANE1_HSRX_DPHY_DDL_VT_COMP_EN_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_vt_comp_en override value. Used for debug purposes.

7	OA_LANE1_HSRX_DPHY_DDL_VT_COMP_BIAS_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_vt_comp_bias override enable. Used for debug purposes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.290 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_16

Reg. 0x1250

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
2:0	OA_LANE1_HSRX_DPHY_DLL_CP_PROG	rw	ro	0x4	Lane 1 D-PHY HS-RX DDL charge pump gain configuration. This signal is quasi-static. Please check table for more details.
4:3	OA_LANE1_HSRX_DPHY_CLK_CHANNEL	rw	ro	0x0	Lane 1 D-PHY HS-RX clock channel selection. This signal is quasi-static. Please check table for more details.
5	OA_LANE1_HSRX_OFFCAL_RIGHT_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_offcal_right override enable. Active high. Used for debug purposes.
6	OA_LANE1_HSRX_OFFCAL_LEFT_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_offcal_left override enable. Active high. Used for debug purposes.
7	OA_LANE1_HSRX_DPHY_DDL_PHASE_RIGHT_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_phase_right override enable. Active high. Used for debug purposes.
8	OA_LANE1_HSRX_DPHY_DDL_PHASE_MID_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_phase_mid override enable. Active high. Used for debug purposes.
9	OA_LANE1_HSRX_DPHY_DDL_PHASE_LEFT_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_phase_left override enable. Active high. Used for debug purposes.
10	OA_LANE1_HSRX_MODE_OVR_EN	rw	ro	0x0	oa_lane1_hsrx_mode override enable. Active high. Used for debug purposes.
15:11	OA_LANE1_ATB_SW	rw	ro	0x0	Lane 1 analog test bus signal selection. This signal is quasi-static. Please check table for more details.

1.1.1.291 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_17

Reg. 0x1251

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
7:0	OA_LANE1_HSRX_OFFCAL_RIGHT_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_offcal_right override value. Used for debug purposes.
15:8	OA_LANE1_HSRX_OFFCAL_LEFT_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_offcal_left override value. Used for debug purposes.

1.1.1.292 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_18

Reg. 0x1252

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
10:0	OA_LANE1_HSRX_DPHY_DDL_PHASE_RIGHT_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_phase_right override value. Used for debug purposes.
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.293 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_19

Reg. 0x1253

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
10:0	OA_LANE1_HSRX_DPHY_DDL_PHASE_MID_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_phase_mid override value. Used for debug purposes.
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.294 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_20 Reg. 0x1254

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
10:0	OA_LANE1_HSRX_DPHY_DDL_PHASE_LEFT_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_dphy_ddl_phase_left override value. Used for debug purposes.
13:11	OA_LANE1_HSRX_MODE_OVR_VAL	rw	ro	0x0	oa_lane1_hsrx_mode override value. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.295 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_21 Reg. 0x1255

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
15:0	IA_LANE1_HSRX_DATA_AB_LEFT_OVR_VAL	rw	ro	0x0	ia_lane1_hsrx_data_ab_left override value. Used for debug purposes.

1.1.1.296 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_22 Reg. 0x1256

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
15:0	IA_LANE1_HSRX_DATA_BC_MID_OVR_VAL	rw	ro	0x0	ia_lane1_hsrx_data_bc_left override value. Used for debug purposes.

1.1.1.297 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_23 Reg. 0x1257

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
15:0	IA_LANE1_HSRX_DATA_CA_RIGHT_OVR_VAL	rw	ro	0x0	ia_lane1_hsrx_data_ca_right override value. Used for debug purposes.

1.1.1.298 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_24 Reg. 0x1258

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
0	IA_LANE1_HSRX_DATA_AB_LEFT_OVR_EN	rw	ro	0x0	ia_lane1_hsrx_data_ab_left override enable. Active high. Used for debug purposes.
1	IA_LANE1_HSRX_DATA_BC_MID_OVR_EN	rw	ro	0x0	ia_lane1_hsrx_data_bc_mid override enable. Active high. Used for debug purposes.
2	IA_LANE1_HSRX_DATA_CA_RIGHT_OVR_EN	rw	ro	0x0	ia_lane1_hsrx_data_ca_right override enable. Active high. Used for debug purposes.

3	IA_LANE1_HSRX_WORD_CLK_OVR_EN	rw	ro	0x0	ia_lane1_hsrx_word_clk override enable. Active high. Used for debug purposes.
4	IA_LANE1_HSRX_HS_CLK_DIV_OUT_OVR_EN	rw	ro	0x0	ia_lane1_hsrx_hs_clk_div_out override enable. Active high. Used for debug purposes.
5	IA_LANE1_HSTX_WORD_CLK_OVR_EN	rw	ro	0x0	ia_lane1_hstx_word_clk override enable. Active high. Used for debug purposes.
6	IA_LANE1_HSRX_VCM_DET_OUT_OVR_EN	rw	ro	0x0	ia_lane1_hsrx_vcm_det_out override enable. Active high. Used for debug purposes.
7	IA_LANE1_HSRX_OUT_CAL_LEFT_N_OVR_EN	rw	ro	0x0	ia_lane1_hsrx_out_cal_left_n override enable. Active high. Used for debug purposes.
8	IA_LANE1_HSRX_OUT_CAL_LEFT_P_OVR_EN	rw	ro	0x0	ia_lane1_hsrx_out_cal_left_p override enable. Active high. Used for debug purposes.
9	IA_LANE1_HSRX_OUT_CAL_RIGHT_N_OVR_EN	rw	ro	0x0	ia_lane1_hsrx_out_cal_right_n override enable. Active high. Used for debug purposes.
10	IA_LANE1_HSRX_OUT_CAL_RIGHT_P_OVR_EN	rw	ro	0x0	ia_lane1_hsrx_out_cal_right_p override enable. Active high. Used for debug purposes.
11	IA_LANE1_HSRX_DPHY_DDL_OSC_CLK_OVR_EN	rw	ro	0x0	ia_lane1_hsrx_dphy_ddl_osc_clk override enable. Active high. Used for debug purposes.
12	IA_LANE1_HSRX_CPHY_ALP_DET_LEFT_OUT_OVR_EN	rw	ro	0x0	ia_lane1_hsrx_cphy_alp_det_left_out override enable. Active high. Used for debug purposes.
13	IA_LANE1_HSRX_CPHY_ALP_DET_RIGHT_OUT_OVR_EN	rw	ro	0x0	ia_lane1_hsrx_cphy_alp_det_right_out override enable. Active high. Used for debug purposes.
14	IA_LANE1_HSRX_CPHY_CDR_OSC_CLK_OVR_EN	rw	ro	0x0	ia_lane1_hsrx_cphy_cdr_osc_clk override enable. Active high. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.299 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_25

Reg. 0x1259

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
0	IA_LANE1_HSRX_DPHY_DDL_OSC_CLK_OVR_VAL	rw	ro	0x0	ia_lane1_hsrx_dphy_ddl_osc_clk override value. Used for debug purposes.
1	IA_LANE1_HSRX_CPHY_ALP_DET_LEFT_OUT_OVR_VAL	rw	ro	0x0	ia_lane1_hsrx_cphy_alp_det_left_out override value. Used for debug purposes.
2	IA_LANE1_HSRX_CPHY_ALP_DET_RIGHT_OUT_OVR_VAL	rw	ro	0x0	ia_lane1_hsrx_cphy_alp_det_right_out override value. Used for debug purposes.
3	IA_LANE1_HSRX_CPHY_CDR_OSC_CLK_OVR_VAL	rw	ro	0x0	ia_lane1_hsrx_cphy_cdr_osc_clk override value. Used for debug purposes.
5:4	IA_LANE1_LPRX_DOUTCD_OVR_VAL	rw	ro	0x0	ia_lane1_lprx_doutcd override value. Used for debug purposes.
7:6	IA_LANE1_LPRX_DOUTLP_OVR_VAL	rw	ro	0x0	ia_lane1_lprx_doutlp override value. Used for debug purposes.
9:8	IA_LANE1_LPRX_DOUTULP_OVR_VAL	rw	ro	0x0	ia_lane1_lprx_doutulp override value. Used for debug purposes.
13:10	IA_LANE1_SPARE_OUT_OVR_VAL	rw	ro	0x0	ia_lane1_spare_out override value. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.300 CORE_DIG_IOCTRL_RW_AFE_LANE1_CTRL_26

Reg. 0x125A

Analog macro lane 1 control
access : read-write

bits	name	s/w	h/w	default	description
0	IA_LANE1_LPRX_DOUTCD_OVR_EN	rw	ro	0x0	ia_lane1_lprx_doutcd override enable. Active high. Used for debug purposes.
1	IA_LANE1_LPRX_DOUTLP_OVR_EN	rw	ro	0x0	ia_lane1_lprx_doutlp override enable. Active high. Used for debug purposes.
2	IA_LANE1_LPRX_DOUTULP_OVR_EN	rw	ro	0x0	ia_lane1_lprx_doutulp override enable. Active high. Used for debug purposes.
3	IA_LANE1_SPARE_OUT_OVR_EN	rw	ro	0x0	ia_lane1_spare_out override enable. Active high. Used for debug purposes.
4	IA_LANE1_HSRX_WORD_CLK_OVR_VAL	rw	ro	0x0	ia_lane1_hsrx_word_clk override value. Used for debug purposes.
5	IA_LANE1_HSRX_HS_CLK_DIV_OUT_OVR_VAL	rw	ro	0x0	ia_lane1_hsrx_hs_clk_div_out override value. Used for debug purposes.
6	IA_LANE1_HSTX_WORD_CLK_OVR_VAL	rw	ro	0x0	ia_lane1_hstx_word_clk override value. Used for debug purposes.
7	IA_LANE1_HSRX_VCM_DET_OUT_OVR_VAL	rw	ro	0x0	ia_lane1_hsrx_vcm_det_out override value. Used for debug purposes.
8	IA_LANE1_HSRX_OUT_CAL_LEFT_N_OVR_VAL	rw	ro	0x0	ia_lane1_hsrx_out_cal_left_n override value. Used for debug purposes.
9	IA_LANE1_HSRX_OUT_CAL_LEFT_P_OVR_VAL	rw	ro	0x0	ia_lane1_hsrx_out_cal_left_p override value. Used for debug purposes.
10	IA_LANE1_HSRX_OUT_CAL_RIGHT_N_OVR_VAL	rw	ro	0x0	ia_lane1_hsrx_out_cal_right_n override value. Used for debug purposes.
11	IA_LANE1_HSRX_OUT_CAL_RIGHT_P_OVR_VAL	rw	ro	0x0	ia_lane1_hsrx_out_cal_right_p override value. Used for debug purposes.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.302 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_0

Reg.

0x1260

Analog macro lane 1 observability
access : read-only

bits	name	s/w	h/w	default	description
1:0	OA_LANE1_HSTX_PON	ro	rw	0x0	oa_lane1_hstx_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
3:2	OA_LANE1_HSTX_BOOST_EN	ro	rw	0x0	oa_lane1_hstx_boost_en multiplexer output. Used for debug purposes. (volatile) volatile : true
4	OA_LANE1_HSRX_DPHY_DDL_PON	ro	rw	0x0	oa_lane1_hsrx_dphy_ddl_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
6:5	OA_LANE1_HSTX_LOWCAP_EN	ro	rw	0x0	oa_lane1_hstx_lowcap_en multiplexer output. Used for debug purposes. (volatile) volatile : true
7	OA_LANE1_LPTX_DIN_DN	ro	rw	0x0	oa_lane1_lptx_din_dn multiplexer output. Used for debug purposes. (volatile) volatile : true
8	OA_LANE1_LPTX_DIN_DP	ro	rw	0x0	oa_lane1_lptx_din_dp multiplexer output. Used for debug purposes. (volatile) volatile : true
9	OA_LANE1_HSRX_DPHY_DDL_DCC_EN	ro	rw	0x0	oa_lane1_hsrx_dphy_ddl_dcc_en multiplexer output. Used for debug purposes. (volatile) volatile : true
10	OA_LANE1_HSRX_DPHY_DDL_EN	ro	rw	0x0	oa_lane1_hsrx_dphy_ddl_en multiplexer output. Used for debug purposes. (volatile) volatile : true
11	OA_LANE1_HSRX_CPHY_CDR_FBK_FAS	ro	rw	0x0	oa_lane1_hsrx_cphy_cdr_fbk_fast_lock_en multiplexer output. Used for debug purposes. (volatile)

	T_LOCK_EN				volatile : true
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.303 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_1

Reg. 0x1261

Analog macro lane 1 observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	OA_LANE1_HSTX_DATA_AB_DPHY	ro	rw	0x0	oa_lane1_hstx_data_ab_dphy multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.304 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_2

Reg. 0x1262

Analog macro lane 1 observability
access : read-only

bits	name	s/w	h/w	default	description
13:0	OA_LANE1_HSTX_DATA_BC	ro	rw	0x0	oa_lane1_hstx_data_bc multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	OA_LANE1_HSTX_TERM_EN	ro	rw	0x0	oa_lane1_hstx_term_en multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.305 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_3

Reg. 0x1263

Analog macro lane 1 observability
access : read-only

bits	name	s/w	h/w	default	description
13:0	OA_LANE1_HSTX_DATA_CA	ro	rw	0x0	oa_lane1_hstx_data_ca[multiplexer output. Used for debug purposes. (volatile) volatile : true
14	OA_LANE1_HSTX_DIV_EN	ro	rw	0x0	oa_lane1_hstx_div_en multiplexer output. Used for debug purposes. (volatile) volatile : true
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.306 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_4

Reg. 0x1264

Analog macro lane 1 observability
access : read-only

bits	name	s/w	h/w	default	description
1:0	OA_LANE1_LPTX_EN	ro	rw	0x0	oa_lane1_lptx_en multiplexer output. Used for debug purposes. (volatile) volatile : true
3:2	OA_LANE1_LPTX_PON	ro	rw	0x0	oa_lane1_lptx_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
5:4	OA_LANE1_LPTX_PULLDWN_EN	ro	rw	0x0	oa_lane1_lptx_pulldwn_en multiplexer output. Used for debug purposes. (volatile) volatile : true
7:6	OA_LANE1_LPRX_LP_PON	ro	rw	0x0	oa_lane1_lprx_lp_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
9:8	OA_LANE1_LPRX_CD_PON	ro	rw	0x0	oa_lane1_lprx_cd_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
11:10	OA_LANE1_LPRX_ULP_PON	ro	rw	0x0	oa_lane1_lprx_ulp_pon multiplexer output. Used for debug purposes. (volatile) volatile : true

12	OA_LANE1_HSRX_CPHY_CDR_FBK_EN	ro	rw	0x0	oa_lane1_hsrx_cphy_cdr_fbk_en multiplexer output. Used for debug purposes. (volatile) volatile : true
13	OA_LANE1_HSRX_CPHY_MASK_CHANGE	ro	rw	0x0	oa_lane1_hsrx_cphy_mask_change multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.307 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_5

Reg. 0x1265

Analog macro lane 1 observability
access : read-only

bits	name	s/w	h/w	default	description
0	OA_LANE1_HSRX_TERM_RIGHT_EN	ro	rw	0x0	oa_lane1_hsrx_term_right_en multiplexer output. Used for debug purposes. (volatile) volatile : true
1	OA_LANE1_HSRX_TERM_LEFT_EN	ro	rw	0x0	oa_lane1_hsrx_term_left_en multiplexer output. Used for debug purposes. (volatile) volatile : true
2	OA_LANE1_HSRX_HS_CLK_DIV_EN	ro	rw	0x0	oa_lane1_hsrx_hs_clk_div_en multiplexer output. Used for debug purposes. (volatile) volatile : true
3	OA_LANE1_HSRX_DESERIALIZER_EN	ro	rw	0x0	oa_lane1_hsrx_deserializer_en multiplexer output. Used for debug purposes. (volatile) volatile : true
4	OA_LANE1_HSRX_DESERIALIZER_DATA_EN	ro	rw	0x0	oa_lane1_hsrx_deserializer_data_en multiplexer output. Used for debug purposes. (volatile) volatile : true
5	OA_LANE1_HSRX_DESERIALIZER_DIV_EN	ro	rw	0x0	oa_lane1_hsrx_deserializer_div_en multiplexer output. Used for debug purposes. (volatile) volatile : true
6	OA_LANE1_HSRX_OFFCAL_OBS_EN	ro	rw	0x0	oa_lane1_hsrx_offcal_obs_en multiplexer output. Used for debug purposes. (volatile) volatile : true
7	OA_LANE1_HSRX_VCM_DET_PON	ro	rw	0x0	oa_lane1_hsrx_vcm_det_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
8	OA_LANE1_HSRX_VCM_DET_OUT_EN	ro	rw	0x0	oa_lane1_hsrx_vcm_det_out_en multiplexer output. Used for debug purposes. (volatile) volatile : true
9	OA_LANE1_HSRX_CPHY_ALP_DET_RIGHT_PON	ro	rw	0x0	oa_lane1_hsrx_cphy_alp_det_right_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
10	OA_LANE1_HSRX_CPHY_ALP_DET_LEFT_PON	ro	rw	0x0	oa_lane1_hsrx_cphy_alp_det_left_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
12:11	OA_LANE1_HSRX_PON	ro	rw	0x0	oa_lane1_hsrx_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
14:13	OA_LANE1_HSRX_EN	ro	rw	0x0	oa_lane1_hsrx_en multiplexer output. Used for debug purposes. (volatile) volatile : true
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.308 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_6

Reg. 0x1266

Analog macro lane 1 observability
access : read-only

bits	name	s/w	h/w	default	description
0	OA_LANE1_HSRX_DPHY_DDL_BIAS_BYPASS_EN	ro	rw	0x0	oa_lane1_hsrx_dphy_ddl_bias_bypass_en multiplexer output. Used for debug purposes. (volatile) volatile : true
1	OA_LANE1_HSRX_DPHY_DDL_BYPASS_EN	ro	rw	0x0	oa_lane1_hsrx_dphy_ddl_bypass_en multiplexer output. Used for debug purposes. (volatile) volatile : true

2	OA_LANE1_HSRX_DPHY_DDL_PHASE_CHANGE	ro	rw	0x0	oa_lane1_hsrx_dphy_ddl_phase_change multiplexer output. Used for debug purposes. (volatile) volatile : true
3	OA_LANE1_HSRX_DPHY_DLL_EN	ro	rw	0x0	oa_lane1_hsrx_dphy_dll_en multiplexer output. Used for debug purposes. (volatile) volatile : true
4	OA_LANE1_HSRX_DPHY_PREAMBLE_CAL_EN	ro	rw	0x0	oa_lane1_hsrx_dphy_preamble_cal_en multiplexer output. Used for debug purposes. (volatile) volatile : true
8:5	OA_LANE1_HSRX_DPHY_DATA_DELAY	ro	rw	0x0	oa_lane1_hsrx_dphy_data_delay multiplexer output. Used for debug purposes. (volatile) volatile : true
9	OA_LANE1_HSRX_DPHY_DDL_VT_COMP_EN	ro	rw	0x0	oa_lane1_hsrx_dphy_ddl_vt_comp_en multiplexer output. Used for debug purposes. (volatile) volatile : true
14:10	OA_LANE1_HSRX_DPHY_DDL_VT_COMP_BIAS	ro	rw	0x0	oa_lane1_hsrx_dphy_ddl_vt_comp_bias multiplexer output. Used for debug purposes. (volatile) volatile : true
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.309 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_7

Reg. 0x1267

Analog macro lane 1 observability
access : read-only

bits	name	s/w	h/w	default	description
4:0	OA_LANE1_HSRX_DPHY_DDL_BIAS	ro	rw	0x0	oa_lane1_hsrx_dphy_ddl_bias multiplexer output. Used for debug purposes. (volatile) volatile : true
8:5	OA_LANE1_HSRX_DPHY_DDL_COARSE_BANK	ro	rw	0x0	oa_lane1_hsrx_dphy_ddl_coarse_bank multiplexer output. Used for debug purposes. (volatile) volatile : true
10:9	OA_LANE1_HSRX_DPHY_DDL_TUNE_MODE	ro	rw	0x0	oa_lane1_hsrx_dphy_ddl_tune_mode multiplexer output. Used for debug purposes. (volatile) volatile : true
15:11	OA_LANE1_HSRX_CPHY_DELAY	ro	rw	0x0	oa_lane1_hsrx_cphy_delay multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.310 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_8

Reg. 0x1268

Analog macro lane 1 observability
access : read-only

bits	name	s/w	h/w	default	description
6:0	OA_LANE1_HSRX_DPHY_DLL_FBK	ro	rw	0x0	oa_lane1_hsrx_dphy_dll_fbk multiplexer output. Used for debug purposes. (volatile) volatile : true
9:7	OA_LANE1_HSRX_EQUALIZER	ro	rw	0x0	oa_lane1_hsrx_equalizer multiplexer output. Used for debug purposes. (volatile) volatile : true
10	OA_LANE1_HSRX_CDPHY_SEL_FAST	ro	rw	0x0	oa_lane1_hsrx_cdphy_sel_fast multiplexer output. Used for debug purposes. (volatile) volatile : true
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.311 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_9

Reg. 0x1269

Analog macro lane 1 observability
access : read-only

bits	name	s/w	h/w	default	description
7:0	OA_LANE1_HSRX_OFFCAL_RIGHT	ro	rw	0x0	oa_lane1_hsrx_offcal_right multiplexer output. Used for debug purposes. (volatile) volatile : true

15:8	OA_LANE1_HSRX_OFFCAL_LEFT	ro	rw	0x0	oa_lane1_hsrx_offcal_left multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.312 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_10

Reg. 0x126A

Analog macro lane 1 observability
access : read-only

bits	name	s/w	h/w	default	description
10:0	OA_LANE1_HSRX_DPHY_DDL_PHASE_RIGHT	ro	rw	0x0	oa_lane1_hsrx_dphy_ddl_phase_right multiplexer output. Used for debug purposes. (volatile) volatile : true
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.313 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_11

Reg. 0x126B

Analog macro lane 1 observability
access : read-only

bits	name	s/w	h/w	default	description
10:0	OA_LANE1_HSRX_DPHY_DDL_PHASE_MID	ro	rw	0x0	oa_lane1_hsrx_dphy_ddl_phase_mid multiplexer output. Used for debug purposes. (volatile) volatile : true
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.314 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_12

Reg. 0x126C

Analog macro lane 1 observability
access : read-only

bits	name	s/w	h/w	default	description
10:0	OA_LANE1_HSRX_DPHY_DDL_PHASE_LEFT	ro	rw	0x0	oa_lane1_hsrx_dphy_ddl_phase_left multiplexer output. Used for debug purposes. (volatile) volatile : true
13:11	OA_LANE1_HSRX_MODE	ro	rw	0x0	oa_lane1_hsrx_mode multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.315 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_13

Reg. 0x126D

Analog macro lane 1 observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	IA_LANE1_HSRX_DATA_AB_LEFT_INT	ro	rw	0x0	ia_lane1_hsrx_data_ab_left multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.316 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_14

Reg. 0x126E

Analog macro lane 1 observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	IA_LANE1_HSRX_DATA_BC_MID_INT	ro	rw	0x0	ia_lane1_hsrx_data_bc_mid_ multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.317 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_15

Reg. 0x126F

Analog macro lane 1 observability

access : read-only

bits	name	s/w	h/w	default	description
15:0	IA_LANE1_HSRX_DATA_CA_RIGHT_INT	ro	rw	0x0	ia_lane1_hsrx_data_ca_right multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.318 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_16

Reg. 0x1270

Analog macro lane 1 observability
access : read-only

bits	name	s/w	h/w	default	description
0	IA_LANE1_HSRX_WORD_CLK_INT	ro	rw	0x0	ia_lane1_hsrx_word_clk multiplexer output. (volatile) volatile : true
1	IA_LANE1_HSRX_HS_CLK_DIV_OUT_INT	ro	rw	0x0	ia_lane1_hsrx_hs_clk_div_out multiplexer output. Used for debug purposes. (volatile) volatile : true
2	IA_LANE1_HSTX_WORD_CLK_INT	ro	rw	0x0	ia_lane1_hstx_word_clk multiplexer output. Used for debug purposes. (volatile) volatile : true
3	IA_LANE1_HSRX_VCM_DET_OUT_INT	ro	rw	0x0	ia_lane1_hsrx_vcm_det_out multiplexer output. Used for debug purposes. (volatile) volatile : true
4	IA_LANE1_HSRX_OUT_CAL_LEFT_N_INT	ro	rw	0x0	ia_lane1_hsrx_out_cal_left_n multiplexer output. Used for debug purposes. (volatile) volatile : true
5	IA_LANE1_HSRX_OUT_CAL_LEFT_P_INT	ro	rw	0x0	ia_lane1_hsrx_out_cal_left_p multiplexer output. Used for debug purposes. (volatile) volatile : true
6	IA_LANE1_HSRX_OUT_CAL_RIGHT_N_INT	ro	rw	0x0	ia_lane1_hsrx_out_cal_right_n multiplexer output. Used for debug purposes. (volatile) volatile : true
7	IA_LANE1_HSRX_OUT_CAL_RIGHT_P_INT	ro	rw	0x0	ia_lane1_hsrx_out_cal_right_p multiplexer output. Used for debug purposes. (volatile) volatile : true
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.319 CORE_DIG_IOCTRL_R_AFE_LANE1_CTRL_17

Reg. 0x1271

Analog macro lane 1 observability
access : read-only

bits	name	s/w	h/w	default	description
0	IA_LANE1_HSRX_DPHY_DDL_OSC_CLK_INT	ro	rw	0x0	ia_lane1_hsrx_dphy_ddl_osc_clk multiplexer output. Used for debug purposes. (volatile) volatile : true
1	IA_LANE1_HSRX_CPHY_ALP_DET_LEFT_OUT_INT	ro	rw	0x0	ia_lane1_hsrx_cphy_alp_det_left_out multiplexer output. Used for debug purposes. (volatile) volatile : true
2	IA_LANE1_HSRX_CPHY_ALP_DET_RIGHT_OUT_INT	ro	rw	0x0	ia_lane1_hsrx_cphy_alp_det_right_out multiplexer output. Used for debug purposes. (volatile) volatile : true
3	IA_LANE1_HSRX_CPHY_CDR_OSC_CLK_INT	ro	rw	0x0	ia_lane1_hsrx_cphy_cdr_osc_clk multiplexer output. Used for debug purposes. (volatile) volatile : true
5:4	IA_LANE1_LPRX_DOUTCD_INT	ro	rw	0x0	ia_lane1_lprx_doutcd multiplexer output. Used for debug purposes. (volatile) volatile : true
7:6	IA_LANE1_LPRX_DOUTLP_INT	ro	rw	0x0	ia_lane1_lprx_doutlp multiplexer output. Used for debug purposes. (volatile) volatile : true
9:8	IA_LANE1_LPRX_DOUTULP_INT	ro	rw	0x0	ia_lane1_lprx_doutulp multiplexer output. Used for debug purposes. (volatile) volatile : true
13:10	IA_LANE1_SPARE_OUT_INT	ro	rw	0x0	ia_lane1_spare_out multiplexer output. Used for debug purposes. (volatile)

					volatile : true
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.321 CORE_DIG_RW_TRIO1_0

Reg. 0x1280

Configurations for Trio 1
access : read-write

bits	name	s/w	h/w	default	description
2:0	DESERIALIZER_DATA_EN_DELAY_THRESH	rw	ro	0x2	Counter for deserializer_data_en delay. Quasi static. 0 is a forbidden value.
5:3	DESERIALIZER_DIV_EN_DELAY_THRESH	rw	ro	0x1	Counter for deserializer_div_en delay. In dco_clk cycles. Quasi static. 0 is a forbidden value.
8:6	DESERIALIZER_DIV_EN_DELAY_DEASS_THRESH	rw	ro	0x1	Counter for deassertion of deserializer_div_en after deassertion of deserializer_data_en. In dco_clk cycles, for higher datarates in word_clk cycles. Quasi Static. 0 is a forbidden value.
15:9	POST_RECEIVED_RESET_THRESH	rw	ro	0x2	Counter for resetting the post detected flag. In word_clk cycles. Quasi static.

1.1.1.322 CORE_DIG_RW_TRIO1_1

Reg. 0x1281

Configurations for Trio 1
access : read-write

bits	name	s/w	h/w	default	description
15:0	POST_DET_DELAY_THRESH	rw	ro	0xA	Counter for deassertion of deserializer_data_en after Post2 reception. In dco_clk cycles. Quasi static.

1.1.1.323 CORE_DIG_RW_TRIO1_2

Reg. 0x1282

Configurations for Trio 1
access : read-write

bits	name	s/w	h/w	default	description
7:0	DESERIALIZER_EN_DELAY_DEASS_THRESH	rw	ro	0xA	Counter for deassertion of deserializer_en after deassertion of deserializer_data_en. In dco_clk cycles. Quasi Static. 0 is a forbidden value.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.325 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_0

Reg. 0x1440

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
10:0	OA_LANE2_SPARE_IN	rw	ro	0x0	Lane 2 input spare bus (bits[10:9] independent current programmability 0-100% 1-75% 2-150% 3-125%; bit[8] vt drift compensation bypass; bit[7] dcc programmability 0-filter bandwidth 100% 1-filter bandwidth 200%; bits[6:0] spare bus) This signal is quasi-static.
11	OA_LANE2_SHORT_LB_EN	rw	ro	0x0	oa_lane2_short_lb_en bit configuration.This signal is quasi-static. Please check table for more details.
12	OA_LANE2_HSTX_LOWCAP_EN_OVR_EN	rw	ro	0x0	oa_lane2_hstx_lowcap_en override enable. Active high. Used for debug purposes.
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.326 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_1

Reg. 0x1441

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
4:0	OA_LANE2_HSRX_DPHY_DDL_BIAS_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_bias override value. Used for debug purposes.
11:5	OA_LANE2_HSRX_DPHY_DLL_FBK_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_dll_fbk override value. Used for debug purposes.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.327 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_2

Reg. 0x1442

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_LANE2_SEL_LANE_CFG	rw	ro	0x0	Lane 2 D-PHY/C-PHY configuration. 1'b0: D-PHY data lane (when phy_mode is 1'b0); C-PHY slave lane (when phy_mode is 1'b1). 1'b1: D-PHY clock lane (when phy_mode is 1'b0); C-PHY master lane (when phy_mode is 1'b1). This signal is quasi-static. Please check table for more details.
1	OA_LANE2_HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_cphy_cdr_fbk_fast_lock_en override enable. Active high. Used for debug purposes.
2	OA_LANE2_HSRX_TERM_EN200OHMS	rw	ro	0x0	Lane 2 HS-RX termination value. Please check table for more details.
3	OA_LANE2_HSRX_DPHY_DDL_PON_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_pon override value. Used for debug purposes.
5:4	OA_LANE2_HSTX_LOWCAP_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hstx_lowcap_en override value. Used for debug purposes.
6	OA_LANE2_HSTX_DIV_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hstx_div_en override value. Used for debug purposes.
7	OA_LANE2_HSTX_DATA_BC_OVR_EN	rw	ro	0x0	oa_lane2_hstx_data_ca override enable. Active high. Used for debug purposes.
8	OA_LANE2_HSTX_DATA_CA_OVR_EN	rw	ro	0x0	oa_lane2_hstx_data_ca override enable. Active high. Used for debug purposes.
10:9	OA_LANE2_HSTX_TERM_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hstx_term_en override value. Used for debug purposes.
11	OA_LANE2_HSRX_DPHY_DDL_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_en override enable. Active high. Used for debug purposes.
12	OA_LANE2_HSRX_CDPHY_SEL_FAST_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_cdphy_sel_fast override enable. Active high. Used for debug purposes.
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.328 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_3

Reg. 0x1443

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
1:0	OA_LANE2_HSTX_PON_OVR_VAL	rw	ro	0x0	oa_lane2_hstx_pon override value. Used for debug purposes.
3:2	OA_LANE2_HSTX_BOOST_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hstx_boost_en override value. Used for debug purposes.
4	OA_LANE2_HSTX_SEL_PHASE0	rw	ro	0x1	Lane 2 HS-TX clock phase selection. 1'b0: 90 (for D-PHY clock lane configuration). 1'b1: 0 (for both C-PHY and D-PHY data lane configurations). This signal is quasi-static. Please check table for more details.
7:5	OA_LANE2_HSTX_EQA	rw	ro	0x0	Lane 2 HS-TX de-emphasis word (upper-half). This signal is quasi-static. Please check table for more details.

8	OA_LANE2_HSTX_SEL_CLKLB	rw	ro	0x1	Lane 2 HS-TX clock source. 1'b0: External PLL clock. 1'b1: Common block internal DCO clock. This signal is quasi-static.
9	OA_LANE2_LPTX_DIN_DN_OVR_VAL	rw	ro	0x0	oa_lane2_lptx_din_dn override value. Used for debug purposes.
10	OA_LANE2_LPTX_DIN_DP_OVR_VAL	rw	ro	0x0	oa_lane2_lptx_din_dp override value. Used for debug purposes.
11	OA_LANE2_HSRX_DPHY_DDL_DCC_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_dcc_en override value. Used for debug purposes.
12	OA_LANE2_HSRX_DPHY_DDL_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_en override value. Used for debug purposes.
13	OA_LANE2_HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_cphy_cdr_fbk_fast_lock_en override value. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.329 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_4

Reg. 0x1444

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_LANE2_HSTX_PON_OVR_EN	rw	ro	0x0	oa_lane2_hstx_pon override enable. Active high. Used for debug purposes.
1	OA_LANE2_HSTX_BOOST_EN_OVR_EN	rw	ro	0x0	oa_lane2_hstx_boost_en override enable. Active high. Used for debug purposes.
4:2	OA_LANE2_HSTX_EQB	rw	ro	0x0	Lane 2 HS-TX de-emphasis word (lower-half). This signal is quasi-static. Please check table for more details.
5	OA_LANE2_HSTX_CLK_OBS_EN	rw	ro	0x0	Lane 2 HS clock pattern driven in the lines (debug feature). Active high. This signal is quasi-static.
6	OA_LANE2_LPTX_DIN_DN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes.
7	OA_LANE2_LPTX_DIN_DP_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes.
9:8	OA_LANE2_LPTX_SR_BYPASS_EN	rw	ro	0x0	oa_lane2_lptx_sr_bypass_en override enable. Active high. Used for debug purposes.
10	OA_LANE2_HSTX_TERM_EN_OVR_EN	rw	ro	0x0	oa_lane2_hstx_term_en override enable. Active high. Used for debug purposes.
11	OA_LANE2_HSRX_DPHY_DDL_DCC_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.330 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_5

Reg. 0x1445

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
15:0	OA_LANE2_HSTX_DATA_AB_DPHY_OVR_VAL	rw	ro	0x0	oa_lane2_hstx_data_ab_dphy override value. Used for debug purposes.

1.1.1.331 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_6

Reg. 0x1446

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
13:0	OA_LANE2_HSTX_DATA_BC_OVR_VAL	rw	ro	0x0	oa_lane2_hstx_data_bc override value. Used for debug purposes.
14	OA_LANE2_HSTX_DATA_AB_DPHY_OVR	rw	ro	0x0	oa_lane2_hstx_data_ab_dphy override enable. Active high. Used for debug purposes.

	_EN				
15	OA_LANE2_HSRX_DPHY_DDL_PON_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_pon override enable. Active high. Used for debug purposes.

1.1.1.332 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_7

Reg. 0x1447

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
13:0	OA_LANE2_HSTX_DATA_CA_OVR_VAL	rw	ro	0x0	oa_lane2_hstx_data_ca override value. Used for debug purposes.
15:14	OA_LANE2_HSRX_GMODE	rw	ro	0x2	Lane 2 HS-RX preamplifier bandwidth configuration. This signal is quasi-static. Please check table for more details.

1.1.1.333 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_8

Reg. 0x1448

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
1:0	OA_LANE2_LPTX_EN_OVR_VAL	rw	ro	0x0	oa_lane2_lptx_en override value. Used for debug purposes.
3:2	OA_LANE2_LPTX_PON_OVR_VAL	rw	ro	0x0	oa_lane2_lptx_pon override value. Used for debug purposes.
5:4	OA_LANE2_LPTX_PULLDWN_EN_OVR_VAL	rw	ro	0x0	oa_lane2_lptx_pulldwn_en override value. Used for debug purposes.
6	OA_LANE2_LPRX_LP_PON_OVR_EN	rw	ro	0x0	oa_lane2_lprx_lp_pon override enable. Active high. Used for debug purposes.
7	OA_LANE2_LPRX_CD_PON_OVR_EN	rw	ro	0x0	oa_lane2_lprx_cd_pon override enable. Active high. Used for debug purposes.
8	OA_LANE2_LPRX_ULP_PON_OVR_EN	rw	ro	0x0	oa_lane2_lprx_ulp_pon override enable. Active high. Used for debug purposes.
9	OA_LANE2_HSRX_CPHY_CDR_FBK_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_cphy_cdr_fbk_en override value. Used for debug purposes.
13:10	OA_LANE2_HSRX_CPHY_CDR_FBK_CAP_PROG	rw	ro	0x7	Lane 2 C-PHY low-pass filter bandwidth (symbol rate dependent). This signal is quasi-static. Please check table for more details.
14	OA_LANE2_HSRX_VCM_DET_SYNC_BYPASS	rw	ro	0x0	Enable vcm detector filter bypass which controls CDR input propagation. This signal is quasi-static. Please check table for more details.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.334 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_9

Reg. 0x1449

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
1:0	OA_LANE2_LPRX_LP_PON_OVR_VAL	rw	ro	0x0	oa_lane2_lprx_lp_pon override value. Used for debug purposes.
3:2	OA_LANE2_LPRX_CD_PON_OVR_VAL	rw	ro	0x0	oa_lane2_lprx_cd_pon override value. Used for debug purposes.
5:4	OA_LANE2_LPRX_ULP_PON_OVR_VAL	rw	ro	0x0	oa_lane2_lprx_ulp_pon override value. Used for debug purposes.
6	OA_LANE2_LPTX_EN_OVR_EN	rw	ro	0x0	oa_lane2_lptx_en override enable. Active high. Used for debug purposes.
7	OA_LANE2_LPTX_PON_OVR_EN	rw	ro	0x0	oa_lane2_lptx_pon override enable. Active high. Used for debug purposes.
8	OA_LANE2_LPTX_PULLDWN_EN_OVR_EN	rw	ro	0x0	oa_lane2_lptx_pulldwn_en override enable. Active high. Used for debug purposes.

9	OA_LANE2_HSRX_CPHY_CDR_FBK_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_cphy_cdr_fbk_en override enable. Active high. Used for debug purposes.
10	OA_LANE2_HSRX_CPHY_MASK_CHANGE_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_cphy_mask_change override value. Used for debug purposes.
11	OA_LANE2_HSRX_CPHY_DELAY_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_cphy_delay override enable. Active high. Used for debug purposes.
12	OA_LANE2_HSRX_CDPHY_SEL_FAST_OVR_VAL	rw	ro	0x1	oa_lane2_hsrx_cdphy_sel_fast override value. Please check table for more details.
14:13	OA_LANE2_HSRX_CDPHY_SEL_TYPE	rw	ro	0x0	oa_lane2_hsrx_cdphy_sel_type override value. Active high. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.335 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_10

Reg. 0x144A

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
2:0	OA_LANE2_HSRX_EQUALIZER_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_equalizer override value. Used for debug purposes.
5:3	OA_LANE2_HSRX_HS_CLK_DIV	rw	ro	0x7	Lane 2 D-PHY DDR clock lane divider (data rate dependent). This signal is quasi-static. Please check table for more details.
6	OA_LANE2_HSRX_SEL_GATED_POLARITY	rw	ro	0x0	Lane <0> deserializer output polarity (D-PHY related). Active high. This signal is quasi-static. Please check table for more details.
9:7	OA_LANE2_HSRX_CPHY_CDR_DIV	rw	ro	0x5	Lane 2 C-PHY oscillation clock divider (for calibration). This signal is quasi-static. Please check table for more details.
14:10	OA_LANE2_HSRX_CPHY_DELAY_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_cphy_delay override value. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.336 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_11

Reg. 0x144B

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_LANE2_HSRX_TERM_RIGHT_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_term_right_en override value. Used for debug purposes.
1	OA_LANE2_HSRX_TERM_LEFT_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_term_left_en override value. Used for debug purposes.
2	OA_LANE2_HSRX_DPHY_CLK_CHANNEL_PULL_EN	rw	ro	0x0	Lane 2 D-PHY clock channel pull-up/pull-down enable. Active high. This signal is quasi-static. Please check table for more details.
3	OA_LANE2_HSRX_HS_CLK_DIV_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_hs_clk_div_en override value. Used for debug purposes.
4	OA_LANE2_HSRX_DESERIALIZER_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_deserializer_en override value. Used for debug purposes.
5	OA_LANE2_HSRX_DESERIALIZER_DATA_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_deserializer_data_en override value. Used for debug purposes.
6	OA_LANE2_HSRX_DESERIALIZER_DIV_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_deserializer_div_en override value. Used for debug purposes.
7	OA_LANE2_HSRX_OFFCAL_OBS_EN_OV	rw	ro	0x0	oa_lane2_hsrx_offcal_obs_en override value. Used for debug purposes.

	R_VAL				
8	OA_LANE2_HSRX_VCM_DET_PON_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_vcm_det_pon override value. Used for debug purposes.
9	OA_LANE2_HSRX_VCM_DET_OUT_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_vcm_det_out_en override value. Used for debug purposes.
10	OA_LANE2_HSRX_CPHY_ALP_DET_RIGHT_PON_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_cphy_alp_det_right_pon override value. Used for debug purposes.
11	OA_LANE2_HSRX_CPHY_ALP_DET_LEFT_PON_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_cphy_alp_det_left_pon override value. Used for debug purposes.
12	OA_LANE2_HSRX_CPHY_MASK_CHANGE_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_cphy_mask_change override enable. Active high. Used for debug purposes.
13	OA_LANE2_HSRX_PON_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_pon override enable. Active high. Used for debug purposes.
14	OA_LANE2_HSRX_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_en override enable. Active high. Used for debug purposes.
15	OA_LANE2_HSTX_DIV_EN_OVR_EN	rw	ro	0x0	oa_lane2_hstx_div_en override enable. Active high. Used for debug purposes.

1.1.1.337 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_12

Reg.

0x144C

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_LANE2_HSRX_TERM_RIGHT_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_term_right_en override enable. Active high. Used for debug purposes.
1	OA_LANE2_HSRX_TERM_LEFT_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_term_left_en override enable. Active high. Used for debug purposes.
2	OA_LANE2_HSRX_HS_CLK_DIV_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_hs_clk_div_en override enable. Active high. Used for debug purposes.
3	OA_LANE2_HSRX_DESERIALIZER_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_deserializer_en override enable. Active high. Used for debug purposes.
4	OA_LANE2_HSRX_DESERIALIZER_DATA_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_deserializer_data_en override enable. Active high. Used for debug purposes.
5	OA_LANE2_HSRX_DESERIALIZER_DIV_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_deserializer_div_en override enable. Active high. Used for debug purposes.
6	OA_LANE2_HSRX_OFFCAL_OBS_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_offcal_obs_en override enable. Active high. Used for debug purposes.
7	OA_LANE2_HSRX_VCM_DET_PON_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_vcm_det_pon override enable. Active high. Used for debug purposes.
8	OA_LANE2_HSRX_VCM_DET_OUT_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_vcm_det_out_en override enable. Active high. Used for debug purposes.
9	OA_LANE2_HSRX_CPHY_ALP_DET_RIGHT_PON_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_cphy_alp_det_right_pon override enable. Active high. Used for debug purposes.
10	OA_LANE2_HSRX_CPHY_ALP_DET_LEFT_PON_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_cphy_alp_det_left_pon override enable. Active high. Used for debug purposes.
12:11	OA_LANE2_HSRX_PON_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_pon override value. Used for debug purposes.
14:13	OA_LANE2_HSRX_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_en override value. Used for debug purposes.

15	OA_LANE2_HSRX_CPHY_SR_BYPASS_Z	rw	ro	0x0	Enable for the slew rate control latch bypass inside CDR. This signal is quasi-static. Please check table for more details.

1.1.1.338 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_13

Reg. 0x144D

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_LANE2_HSRX_DPHY_DDL_BIAS_BYPASS_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_bias_bypass_en override value. Used for debug purposes.
1	OA_LANE2_HSRX_DPHY_DDL_BYPASS_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_bypass_en override value. Used for debug purposes.
2	OA_LANE2_HSRX_DPHY_DDL_PHASE_CHANGE_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_phase_change override value. Used for debug purposes.
3	OA_LANE2_HSRX_DPHY_DLL_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_dll_en override value. Used for debug purposes.
4	OA_LANE2_HSRX_DPHY_PREAMBLE_CAL_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_preamble_cal_en override value. Used for debug purposes.
9:5	OA_LANE2_HSRX_DPHY_DDL_VT_COMP_BIAS_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_vt_comp_bias override value. Used for debug purposes.
10	OA_LANE2_HSRX_DPHY_DATA_DELAY_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_data_delay override enable. Active high. Used for debug purposes.
13:11	OA_LANE2_HSRX_DPHY_DDL_DIV	rw	ro	0x2	Lane 2 HS-RX DDL oscillation clock divider. This signal is quasi-static. Please check table for more details.
15:14	OA_LANE2_HSRX_CPHY_FINE_RANGE	rw	ro	0x0	Delay line fine delay cell setting for DDL. This signal is quasi-static. Please check table for more details.

1.1.1.339 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_14

Reg. 0x144E

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_LANE2_HSRX_DPHY_DDL_BIAS_BYPASS_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_bias_bypass_en override enable. Active high. Used for debug purposes.
1	OA_LANE2_HSRX_DPHY_DDL_BYPASS_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_bypass_en override enable. Active high. Used for debug purposes.
2	OA_LANE2_HSRX_DPHY_DDL_PHASE_CHANGE_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_phase_change override enable. Active high. Used for debug purposes.
3	OA_LANE2_HSRX_DPHY_DLL_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_dll_en override enable. Active high. Used for debug purposes.
4	OA_LANE2_HSRX_DPHY_PREAMBLE_CAL_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_preamble_cal_en override enable. Active high. Used for debug purposes.
5	OA_LANE2_HSRX_DPHY_DDL_VT_COMP_EN_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_vt_comp_en override enable. Used for debug purposes.
9:6	OA_LANE2_HSRX_DPHY_DATA_DELAY_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_data_delay override value. Used for debug purposes.
10	OA_LANE2_HSRX_DPHY_DDL_BIAS_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_bias override enable. Active high. Used for debug purposes.

11	OA_LANE2_HSRX_DPHY_DDL_COARSE_BANK_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_coarse_bank override enable. Active high. Used for debug purposes.
12	OA_LANE2_HSRX_DPHY_DDL_TUNE_MODE_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_tune_mode override enable. Active high. Used for debug purposes.
13	OA_LANE2_HSRX_DPHY_DLL_FBK_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_dll_fbk override enable. Active high. Used for debug purposes.
14	OA_LANE2_HSRX_EQUALIZER_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_equalizer override enable. Active high. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.340 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_15

Reg. 0x144F

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
3:0	OA_LANE2_HSRX_DPHY_DDL_COARSE_BANK_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_coarse_bank override value. Used for debug purposes.
5:4	OA_LANE2_HSRX_DPHY_DDL_TUNE_MODE_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_tune_mode override value. Used for debug purposes.
6	OA_LANE2_HSRX_DPHY_DDL_VT_COMP_EN_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_vt_comp_en override value. Used for debug purposes.
7	OA_LANE2_HSRX_DPHY_DDL_VT_COMP_BIAS_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_vt_comp_bias override enable. Used for debug purposes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.341 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_16

Reg. 0x1450

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
2:0	OA_LANE2_HSRX_DPHY_DLL_CP_PROG	rw	ro	0x4	Lane 2 D-PHY HS-RX DDL charge pump gain configuration. This signal is quasi-static. Please check table for more details.
4:3	OA_LANE2_HSRX_DPHY_CLK_CHANNEL	rw	ro	0x0	Lane 2 D-PHY HS-RX clock channel selection. This signal is quasi-static. Please check table for more details.
5	OA_LANE2_HSRX_OFFCAL_RIGHT_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_offcal_right override enable. Active high. Used for debug purposes.
6	OA_LANE2_HSRX_OFFCAL_LEFT_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_offcal_left override enable. Active high. Used for debug purposes.
7	OA_LANE2_HSRX_DPHY_DDL_PHASE_RIGHT_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_phase_right override enable. Active high. Used for debug purposes.
8	OA_LANE2_HSRX_DPHY_DDL_PHASE_MID_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_phase_mid override enable. Active high. Used for debug purposes.
9	OA_LANE2_HSRX_DPHY_DDL_PHASE_LEFT_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_phase_left override enable. Active high. Used for debug purposes.
10	OA_LANE2_HSRX_MODE_OVR_EN	rw	ro	0x0	oa_lane2_hsrx_mode override enable. Active high. Used for debug purposes.
15:11	OA_LANE2_ATB_SW	rw	ro	0x0	Lane 2 analog test bus signal selection. This signal is quasi-static. Please check table for more details.

1.1.1.342 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_17

Reg. 0x1451

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
7:0	OA_LANE2_HSRX_OFFCAL_RIGHT_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_offcal_right override value. Used for debug purposes.
15:8	OA_LANE2_HSRX_OFFCAL_LEFT_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_offcal_left override value. Used for debug purposes.

1.1.1.343 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_18

Reg. 0x1452

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
10:0	OA_LANE2_HSRX_DPHY_DDL_PHASE_RIGHT_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_phase_right override value. Used for debug purposes.
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.344 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_19

Reg. 0x1453

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
10:0	OA_LANE2_HSRX_DPHY_DDL_PHASE_MID_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_phase_mid override value. Used for debug purposes.
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.345 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_20

Reg. 0x1454

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
10:0	OA_LANE2_HSRX_DPHY_DDL_PHASE_LEFT_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_dphy_ddl_phase_left override value. Used for debug purposes.
13:11	OA_LANE2_HSRX_MODE_OVR_VAL	rw	ro	0x0	oa_lane2_hsrx_mode override value. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.346 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_21

Reg. 0x1455

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
15:0	IA_LANE2_HSRX_DATA_AB_LEFT_OVR_VAL	rw	ro	0x0	ia_lane2_hsrx_data_ab_left override value. Used for debug purposes.

1.1.1.347 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_22

Reg. 0x1456

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
15:0	IA_LANE2_HSRX_DATA_BC_MID_OVR_	rw	ro	0x0	ia_lane2_hsrx_data_bc_left override value. Used for debug purposes.

	VAL				

1.1.1.348 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_23 Reg. 0x1457

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
15:0	IA_LANE2_HSRX_DATA_CA_RIGHT_OVR_VAL	rw	ro	0x0	ia_lane2_hsrx_data_ca_right override value. Used for debug purposes.

1.1.1.349 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_24 Reg. 0x1458

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
0	IA_LANE2_HSRX_DATA_AB_LEFT_OVR_EN	rw	ro	0x0	ia_lane2_hsrx_data_ab_left override enable. Active high. Used for debug purposes.
1	IA_LANE2_HSRX_DATA_BC_MID_OVR_EN	rw	ro	0x0	ia_lane2_hsrx_data_bc_mid override enable. Active high. Used for debug purposes.
2	IA_LANE2_HSRX_DATA_CA_RIGHT_OVR_EN	rw	ro	0x0	ia_lane2_hsrx_data_ca_right override enable. Active high. Used for debug purposes.
3	IA_LANE2_HSRX_WORD_CLK_OVR_EN	rw	ro	0x0	ia_lane2_hsrx_word_clk override enable. Active high. Used for debug purposes.
4	IA_LANE2_HSRX_HS_CLK_DIV_OUT_OVR_EN	rw	ro	0x0	ia_lane2_hsrx_hs_clk_div_out override enable. Active high. Used for debug purposes.
5	IA_LANE2_HSTX_WORD_CLK_OVR_EN	rw	ro	0x0	ia_lane2_hstx_word_clk override enable. Active high. Used for debug purposes.
6	IA_LANE2_HSRX_VCM_DET_OUT_OVR_EN	rw	ro	0x0	ia_lane2_hsrx_vcm_det_out override enable. Active high. Used for debug purposes.
7	IA_LANE2_HSRX_OUT_CAL_LEFT_N_OVR_EN	rw	ro	0x0	ia_lane2_hsrx_out_cal_left_n override enable. Active high. Used for debug purposes.
8	IA_LANE2_HSRX_OUT_CAL_LEFT_P_OVR_EN	rw	ro	0x0	ia_lane2_hsrx_out_cal_left_p override enable. Active high. Used for debug purposes.
9	IA_LANE2_HSRX_OUT_CAL_RIGHT_N_OVR_EN	rw	ro	0x0	ia_lane2_hsrx_out_cal_right_n override enable. Active high. Used for debug purposes.
10	IA_LANE2_HSRX_OUT_CAL_RIGHT_P_OVR_EN	rw	ro	0x0	ia_lane2_hsrx_out_cal_right_p override enable. Active high. Used for debug purposes.
11	IA_LANE2_HSRX_DPHY_DDL_OSC_CLK_OVR_EN	rw	ro	0x0	ia_lane2_hsrx_dphy_ddl_osc_clk override enable. Active high. Used for debug purposes.
12	IA_LANE2_HSRX_CPHY_ALP_DET_LEFT_OUT_OVR_EN	rw	ro	0x0	ia_lane2_hsrx_cphy_alp_det_left_out override enable. Active high. Used for debug purposes.
13	IA_LANE2_HSRX_CPHY_ALP_DET_RIGHT_OUT_OVR_EN	rw	ro	0x0	ia_lane2_hsrx_cphy_alp_det_right_out override enable. Active high. Used for debug purposes.
14	IA_LANE2_HSRX_CPHY_CDR_OSC_CLK_OVR_EN	rw	ro	0x0	ia_lane2_hsrx_cphy_cdr_osc_clk override enable. Active high. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.350 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_25 Reg. 0x1459

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
0	IA_LANE2_HSRX_DPHY_DDL_OSC_CLK_OVR_VAL	rw	ro	0x0	ia_lane2_hsrx_dphy_ddl_osc_clk override value. Used for debug purposes.
1	IA_LANE2_HSRX_CPHY_ALP_DET_LEFT_OUT_OVR_VAL	rw	ro	0x0	ia_lane2_hsrx_cphy_alp_det_left_out override value. Used for debug purposes.
2	IA_LANE2_HSRX_CPHY_ALP_DET_RIGHT_OUT_OVR_VAL	rw	ro	0x0	ia_lane2_hsrx_cphy_alp_det_right_out override value. Used for debug purposes.
3	IA_LANE2_HSRX_CPHY_CDR_OSC_CLK_OVR_VAL	rw	ro	0x0	ia_lane2_hsrx_cphy_cdr_osc_clk override value. Used for debug purposes.
5:4	IA_LANE2_LPRX_DOUTCD_OVR_VAL	rw	ro	0x0	ia_lane2_lprx_doutcd override value. Used for debug purposes.
7:6	IA_LANE2_LPRX_DOUTLP_OVR_VAL	rw	ro	0x0	ia_lane2_lprx_doutlp override value. Used for debug purposes.
9:8	IA_LANE2_LPRX_DOUTULP_OVR_VAL	rw	ro	0x0	ia_lane2_lprx_doutulp override value. Used for debug purposes.
13:10	IA_LANE2_SPARE_OUT_OVR_VAL	rw	ro	0x0	ia_lane2_spare_out override value. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.351 CORE_DIG_IOCTRL_RW_AFE_LANE2_CTRL_26

Reg. 0x145A

Analog macro lane 2 control
access : read-write

bits	name	s/w	h/w	default	description
0	IA_LANE2_LPRX_DOUTCD_OVR_EN	rw	ro	0x0	ia_lane2_lprx_doutcd override enable. Active high. Used for debug purposes.
1	IA_LANE2_LPRX_DOUTLP_OVR_EN	rw	ro	0x0	ia_lane2_lprx_doutlp override enable. Active high. Used for debug purposes.
2	IA_LANE2_LPRX_DOUTULP_OVR_EN	rw	ro	0x0	ia_lane2_lprx_doutulp override enable. Active high. Used for debug purposes.
3	IA_LANE2_SPARE_OUT_OVR_EN	rw	ro	0x0	ia_lane2_spare_out override enable. Active high. Used for debug purposes.
4	IA_LANE2_HSRX_WORD_CLK_OVR_VAL	rw	ro	0x0	ia_lane2_hsrx_word_clk override value. Used for debug purposes.
5	IA_LANE2_HSRX_HS_CLK_DIV_OUT_OVR_VAL	rw	ro	0x0	ia_lane2_hsrx_hs_clk_div_out override value. Used for debug purposes.
6	IA_LANE2_HSTX_WORD_CLK_OVR_VAL	rw	ro	0x0	ia_lane2_hstx_word_clk override value. Used for debug purposes.
7	IA_LANE2_HSRX_VCM_DET_OUT_OVR_VAL	rw	ro	0x0	ia_lane2_hsrx_vcm_det_out override value. Used for debug purposes.
8	IA_LANE2_HSRX_OUT_CAL_LEFT_N_OVR_VAL	rw	ro	0x0	ia_lane2_hsrx_out_cal_left_n override value. Used for debug purposes.
9	IA_LANE2_HSRX_OUT_CAL_LEFT_P_OVR_VAL	rw	ro	0x0	ia_lane2_hsrx_out_cal_left_p override value. Used for debug purposes.
10	IA_LANE2_HSRX_OUT_CAL_RIGHT_N_OVR_VAL	rw	ro	0x0	ia_lane2_hsrx_out_cal_right_n override value. Used for debug purposes.
11	IA_LANE2_HSRX_OUT_CAL_RIGHT_P_OVR_VAL	rw	ro	0x0	ia_lane2_hsrx_out_cal_right_p override value. Used for debug purposes.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.353 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_0

Reg. 0x1460

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
1:0	OA_LANE2_HSTX_PON	ro	rw	0x0	oa_lane2_hstx_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
3:2	OA_LANE2_HSTX_BOOST_EN	ro	rw	0x0	oa_lane2_hstx_boost_en multiplexer output. Used for debug purposes. (volatile) volatile : true
4	OA_LANE2_HSRX_DPHY_DDL_PON	ro	rw	0x0	oa_lane2_hsrx_dphy_ddl_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
6:5	OA_LANE2_HSTX_LOWCAP_EN	ro	rw	0x0	oa_lane2_hstx_lowcap_en multiplexer output. Used for debug purposes. (volatile) volatile : true
7	OA_LANE2_LPTX_DIN_DN	ro	rw	0x0	oa_lane2_lptx_din_dn multiplexer output. Used for debug purposes. (volatile) volatile : true
8	OA_LANE2_LPTX_DIN_DP	ro	rw	0x0	oa_lane2_lptx_din_dp multiplexer output. Used for debug purposes. (volatile) volatile : true
9	OA_LANE2_HSRX_DPHY_DDL_DCC_EN	ro	rw	0x0	oa_lane2_hsrx_dphy_ddl_dcc_en multiplexer output. Used for debug purposes. (volatile) volatile : true
10	OA_LANE2_HSRX_DPHY_DDL_EN	ro	rw	0x0	oa_lane2_hsrx_dphy_ddl_en multiplexer output. Used for debug purposes. (volatile) volatile : true
11	OA_LANE2_HSRX_CPHY_CDR_FBK_FAST_LOCK_EN	ro	rw	0x0	oa_lane2_hsrx_cphy_cdr_fbk_fast_lock_en multiplexer output. Used for debug purposes. (volatile) volatile : true
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.354 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_1

Reg. 0x1461

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	OA_LANE2_HSTX_DATA_AB_DPHY	ro	rw	0x0	oa_lane2_hstx_data_ab_dphy multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.355 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_2

Reg. 0x1462

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
13:0	OA_LANE2_HSTX_DATA_BC	ro	rw	0x0	oa_lane2_hstx_data_bc multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	OA_LANE2_HSTX_TERM_EN	ro	rw	0x0	oa_lane2_hstx_term_en multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.356 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_3

Reg. 0x1463

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
13:0	OA_LANE2_HSTX_DATA_CA	ro	rw	0x0	oa_lane2_hstx_data_ca[multiplexer output. Used for debug purposes. (volatile) volatile : true

14	OA_LANE2_HSTX_DIV_EN	ro	rw	0x0	oa_lane2_hstx_div_en multiplexer output. Used for debug purposes. (volatile) volatile : true
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.357 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_4

Reg. 0x1464

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
1:0	OA_LANE2_LPTX_EN	ro	rw	0x0	oa_lane2_lptx_en multiplexer output. Used for debug purposes. (volatile) volatile : true
3:2	OA_LANE2_LPTX_PON	ro	rw	0x0	oa_lane2_lptx_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
5:4	OA_LANE2_LPTX_PULLDWN_EN	ro	rw	0x0	oa_lane2_lptx_pulldwn_en multiplexer output. Used for debug purposes. (volatile) volatile : true
7:6	OA_LANE2_LPRX_LP_PON	ro	rw	0x0	oa_lane2_lprx_lp_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
9:8	OA_LANE2_LPRX_CD_PON	ro	rw	0x0	oa_lane2_lprx_cd_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
11:10	OA_LANE2_LPRX_ULP_PON	ro	rw	0x0	oa_lane2_lprx_ulp_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
12	OA_LANE2_HSRX_CPHY_CDR_FBK_EN	ro	rw	0x0	oa_lane2_hsrx_cphy_cdr_fbk_en multiplexer output. Used for debug purposes. (volatile) volatile : true
13	OA_LANE2_HSRX_CPHY_MASK_CHANGE	ro	rw	0x0	oa_lane2_hsrx_cphy_mask_change multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.358 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_5

Reg. 0x1465

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
0	OA_LANE2_HSRX_TERM_RIGHT_EN	ro	rw	0x0	oa_lane2_hsrx_term_right_en multiplexer output. Used for debug purposes. (volatile) volatile : true
1	OA_LANE2_HSRX_TERM_LEFT_EN	ro	rw	0x0	oa_lane2_hsrx_term_left_en multiplexer output. Used for debug purposes. (volatile) volatile : true
2	OA_LANE2_HSRX_HS_CLK_DIV_EN	ro	rw	0x0	oa_lane2_hsrx_hs_clk_div_en multiplexer output. Used for debug purposes. (volatile) volatile : true
3	OA_LANE2_HSRX_DESERIALIZER_EN	ro	rw	0x0	oa_lane2_hsrx_deserializer_en multiplexer output. Used for debug purposes. (volatile) volatile : true
4	OA_LANE2_HSRX_DESERIALIZER_DATA_EN	ro	rw	0x0	oa_lane2_hsrx_deserializer_data_en multiplexer output. Used for debug purposes. (volatile) volatile : true
5	OA_LANE2_HSRX_DESERIALIZER_DIV_EN	ro	rw	0x0	oa_lane2_hsrx_deserializer_div_en multiplexer output. Used for debug purposes. (volatile) volatile : true
6	OA_LANE2_HSRX_OFFCAL_OBS_EN	ro	rw	0x0	oa_lane2_hsrx_offcal_obs_en multiplexer output. Used for debug purposes. (volatile) volatile : true
7	OA_LANE2_HSRX_VCM_DET_PON	ro	rw	0x0	oa_lane2_hsrx_vcm_det_pon multiplexer output. Used for debug purposes. (volatile) volatile : true

8	OA_LANE2_HSRX_VCM_DET_OUT_EN	ro	rw	0x0	oa_lane2_hsrx_vcm_det_out_en multiplexer output. Used for debug purposes. (volatile) volatile : true
9	OA_LANE2_HSRX_CPHY_ALP_DET_RIGHT_PON	ro	rw	0x0	oa_lane2_hsrx_cphy_alp_det_right_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
10	OA_LANE2_HSRX_CPHY_ALP_DET_LEFT_PON	ro	rw	0x0	oa_lane2_hsrx_cphy_alp_det_left_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
12:11	OA_LANE2_HSRX_PON	ro	rw	0x0	oa_lane2_hsrx_pon multiplexer output. Used for debug purposes. (volatile) volatile : true
14:13	OA_LANE2_HSRX_EN	ro	rw	0x0	oa_lane2_hsrx_en multiplexer output. Used for debug purposes. (volatile) volatile : true
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.359 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_6

Reg. 0x1466

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
0	OA_LANE2_HSRX_DPHY_DDL_BIAS_BYPASS_EN	ro	rw	0x0	oa_lane2_hsrx_dphy_ddl_bias_bypass_en multiplexer output. Used for debug purposes. (volatile) volatile : true
1	OA_LANE2_HSRX_DPHY_DDL_BYPASS_EN	ro	rw	0x0	oa_lane2_hsrx_dphy_ddl_bypass_en multiplexer output. Used for debug purposes. (volatile) volatile : true
2	OA_LANE2_HSRX_DPHY_DDL_PHASE_CHANGE	ro	rw	0x0	oa_lane2_hsrx_dphy_ddl_phase_change multiplexer output. Used for debug purposes. (volatile) volatile : true
3	OA_LANE2_HSRX_DPHY_DLL_EN	ro	rw	0x0	oa_lane2_hsrx_dphy_dll_en multiplexer output. Used for debug purposes. (volatile) volatile : true
4	OA_LANE2_HSRX_DPHY_PREAMBLE_CAL_EN	ro	rw	0x0	oa_lane2_hsrx_dphy_preamble_cal_en multiplexer output. Used for debug purposes. (volatile) volatile : true
8:5	OA_LANE2_HSRX_DPHY_DATA_DELAY	ro	rw	0x0	oa_lane2_hsrx_dphy_data_delay multiplexer output. Used for debug purposes. (volatile) volatile : true
9	OA_LANE2_HSRX_DPHY_DDL_VT_COMP_EN	ro	rw	0x0	oa_lane2_hsrx_dphy_ddl_vt_comp_en multiplexer output. Used for debug purposes. (volatile) volatile : true
14:10	OA_LANE2_HSRX_DPHY_DDL_VT_COMP_BIAS	ro	rw	0x0	oa_lane2_hsrx_dphy_ddl_vt_comp_bias multiplexer output. Used for debug purposes. (volatile) volatile : true
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.360 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_7

Reg. 0x1467

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
4:0	OA_LANE2_HSRX_DPHY_DDL_BIAS	ro	rw	0x0	oa_lane2_hsrx_dphy_ddl_bias multiplexer output. Used for debug purposes. (volatile) volatile : true
8:5	OA_LANE2_HSRX_DPHY_DDL_COARSE_BANK	ro	rw	0x0	oa_lane2_hsrx_dphy_ddl_coarse_bank multiplexer output. Used for debug purposes. (volatile) volatile : true
10:9	OA_LANE2_HSRX_DPHY_DDL_TUNE_MODE	ro	rw	0x0	oa_lane2_hsrx_dphy_ddl_tune_mode multiplexer output. Used for debug purposes. (volatile) volatile : true
15:11	OA_LANE2_HSRX_CPHY_DELAY	ro	rw	0x0	oa_lane2_hsrx_cphy_delay multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.361 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_8

Reg. 0x1468

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
6:0	OA_LANE2_HSRX_DPHY_DLL_FBK	ro	rw	0x0	oa_lane2_hsrx_dphy_dll_fbk multiplexer output. Used for debug purposes. (volatile) volatile : true
9:7	OA_LANE2_HSRX_EQUALIZER	ro	rw	0x0	oa_lane2_hsrx_equalizer multiplexer output. Used for debug purposes. (volatile) volatile : true
10	OA_LANE2_HSRX_CDPHY_SEL_FAST	ro	rw	0x0	oa_lane2_hsrx_cdphy_sel_fast multiplexer output. Used for debug purposes. (volatile) volatile : true
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.362 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_9

Reg. 0x1469

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
7:0	OA_LANE2_HSRX_OFFCAL_RIGHT	ro	rw	0x0	oa_lane2_hsrx_offcal_right multiplexer output. Used for debug purposes. (volatile) volatile : true
15:8	OA_LANE2_HSRX_OFFCAL_LEFT	ro	rw	0x0	oa_lane2_hsrx_offcal_left multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.363 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_10

Reg. 0x146A

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
10:0	OA_LANE2_HSRX_DPHY_DDL_PHASE_RIGHT	ro	rw	0x0	oa_lane2_hsrx_dphy_ddl_phase_right multiplexer output. Used for debug purposes. (volatile) volatile : true
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.364 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_11

Reg. 0x146B

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
10:0	OA_LANE2_HSRX_DPHY_DDL_PHASE_MID	ro	rw	0x0	oa_lane2_hsrx_dphy_ddl_phase_mid multiplexer output. Used for debug purposes. (volatile) volatile : true
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.365 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_12

Reg. 0x146C

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
10:0	OA_LANE2_HSRX_DPHY_DDL_PHASE_LEFT	ro	rw	0x0	oa_lane2_hsrx_dphy_ddl_phase_left multiplexer output. Used for debug purposes. (volatile) volatile : true
13:11	OA_LANE2_HSRX_MODE	ro	rw	0x0	oa_lane2_hsrx_mode multiplexer output. Used for debug purposes. (volatile)

					volatile : true
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.366 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_13

Reg. 0x146D

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	IA_LANE2_HSRX_DATA_AB_LEFT_INT	ro	rw	0x0	ia_lane2_hsrx_data_ab_left multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.367 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_14

Reg. 0x146E

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	IA_LANE2_HSRX_DATA_BC_MID_INT	ro	rw	0x0	ia_lane2_hsrx_data_bc_mid_ multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.368 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_15

Reg. 0x146F

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	IA_LANE2_HSRX_DATA_CA_RIGHT_INT	ro	rw	0x0	ia_lane2_hsrx_data_ca_right multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.369 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_16

Reg. 0x1470

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
0	IA_LANE2_HSRX_WORD_CLK_INT	ro	rw	0x0	ia_lane2_hsrx_word_clk multiplexer output. (volatile) volatile : true
1	IA_LANE2_HSRX_HS_CLK_DIV_OUT_INT	ro	rw	0x0	ia_lane2_hsrx_hs_clk_div_out multiplexer output. Used for debug purposes. (volatile) volatile : true
2	IA_LANE2_HSTX_WORD_CLK_INT	ro	rw	0x0	ia_lane2_hstx_word_clk multiplexer output. Used for debug purposes. (volatile) volatile : true
3	IA_LANE2_HSRX_VCM_DET_OUT_INT	ro	rw	0x0	ia_lane2_hsrx_vcm_det_out multiplexer output. Used for debug purposes. (volatile) volatile : true
4	IA_LANE2_HSRX_OUT_CAL_LEFT_N_INT	ro	rw	0x0	ia_lane2_hsrx_out_cal_left_n multiplexer output. Used for debug purposes. (volatile) volatile : true
5	IA_LANE2_HSRX_OUT_CAL_LEFT_P_INT	ro	rw	0x0	ia_lane2_hsrx_out_cal_left_p multiplexer output. Used for debug purposes. (volatile) volatile : true
6	IA_LANE2_HSRX_OUT_CAL_RIGHT_N_INT	ro	rw	0x0	ia_lane2_hsrx_out_cal_right_n multiplexer output. Used for debug purposes. (volatile) volatile : true
7	IA_LANE2_HSRX_OUT_CAL_RIGHT_P_INT	ro	rw	0x0	ia_lane2_hsrx_out_cal_right_p multiplexer output. Used for debug purposes. (volatile) volatile : true
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.370 CORE_DIG_IOCTRL_R_AFE_LANE2_CTRL_17

Reg. 0x1471

Analog macro lane 2 observability
access : read-only

bits	name	s/w	h/w	default	description
0	IA_LANE2_HSRX_DPHY_DDL_OSC_CLK_INT	ro	rw	0x0	ia_lane2_hsrx_dphy_ddl_osc_clk multiplexer output. Used for debug purposes. (volatile) volatile : true
1	IA_LANE2_HSRX_CPHY_ALP_DET_LEFT_OUT_INT	ro	rw	0x0	ia_lane2_hsrx_cphy_alp_det_left_out multiplexer output. Used for debug purposes. (volatile) volatile : true
2	IA_LANE2_HSRX_CPHY_ALP_DET_RIGHT_OUT_INT	ro	rw	0x0	ia_lane2_hsrx_cphy_alp_det_right_out multiplexer output. Used for debug purposes. (volatile) volatile : true
3	IA_LANE2_HSRX_CPHY_CDR_OSC_CLK_INT	ro	rw	0x0	ia_lane2_hsrx_cphy_cdr_osc_clk multiplexer output. Used for debug purposes. (volatile) volatile : true
5:4	IA_LANE2_LPRX_DOUTCD_INT	ro	rw	0x0	ia_lane2_lprx_doutcd multiplexer output. Used for debug purposes. (volatile) volatile : true
7:6	IA_LANE2_LPRX_DOUTLP_INT	ro	rw	0x0	ia_lane2_lprx_doutlp multiplexer output. Used for debug purposes. (volatile) volatile : true
9:8	IA_LANE2_LPRX_DOUTULP_INT	ro	rw	0x0	ia_lane2_lprx_doutulp multiplexer output. Used for debug purposes. (volatile) volatile : true
13:10	IA_LANE2_SPARE_OUT_INT	ro	rw	0x0	ia_lane2_spare_out multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.372 CORE_DIG_IOCTRL_RW_DPHY_PPI_CLK_OVR_0

Reg. 0x1A00

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_ENABLE_DCK_OVR_VAL	rw	ro	0x0	i_enable_dck override value. Used for debug purposes.
1	O_STOPSTATE_DCK_OVR_VAL	rw	ro	0x0	o_stopstate_dck override value. Used for debug purposes.
2	O_ULPSACTIVENOT_DCK_OVR_VAL	rw	ro	0x0	o_ulpsactivenot_dck override value. Used for debug purposes.
3	O_RXULPSCLKNOT_DCK_OVR_VAL	rw	ro	0x0	o_rxulpsclknot_dck override value. Used for debug purposes.
4	O_RXCLKACTIVEHS_DCK_OVR_VAL	rw	ro	0x0	o_rxclkactivehs_dck override value. Used for debug purposes.
5	I_TXREQUESTHS_DCK_OVR_VAL	rw	ro	0x0	i_txrequesths_dck override value. Used for debug purposes.
6	I_FORCETXSTOPMODE_DCK_OVR_VAL	rw	ro	0x0	i_forcetxstopmode_dck override value. Used for debug purposes.
7	I_FORCERXMODE_DCK_OVR_VAL	rw	ro	0x0	i_forcerxmode_dck override value. Used for debug purposes.
8	I_TXULPSCLK_DCK_OVR_VAL	rw	ro	0x0	i_txulpsclk_dck override value. Used for debug purposes.
9	I_TXULPSEXIT_DCK_OVR_VAL	rw	ro	0x0	i_txulpsexit_dck override value. Used for debug purposes.
10	I_TXHSIDLECLKHS_OVR_VAL	rw	ro	0x0	i_txhsidleclkhs override value. Used for debug purposes.
11	O_TXHSIDLECLKREADYHS_OVR_VAL	rw	ro	0x0	o_txhsidleclkreadyhs override value. Used for debug purposes.
14:12	I_DPHY_RX_CLK_AG_OVR_VAL	rw	ro	0x0	i_dphy_rx_clk_ag override value. Used for debug purposes.
15	I_DPHY_RX_CLK_AG_OVR_EN	rw	ro	0x0	i_dphy_rx_clk_ag override enable. Active high. Used for debug purposes.

1.1.1.373 CORE_DIG_IOCTRL_RW_DPHY_PPI_CLK_OVR_1 Reg. 0x1A01

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_ENABLE_DCK_OVR_EN	rw	ro	0x0	i_enable_dck override enable. Active high. Used for debug purposes.
1	O_STOPSTATE_DCK_OVR_EN	rw	ro	0x0	o_stopstate_dck override enable. Active high. Used for debug purposes.
2	O_ULPSACTIVENOT_DCK_OVR_EN	rw	ro	0x0	o_ulpsactivenot_dck override enable. Active high. Used for debug purposes.
3	O_RXULPSCLKNOT_DCK_OVR_EN	rw	ro	0x0	o_rxulpsclknot_dck override enable. Active high. Used for debug purposes.
4	O_RXCLKACTIVEHS_DCK_OVR_EN	rw	ro	0x0	o_rxclkactivehs_ride enable. Active high. Used for debug purposes.
5	I_TXREQUESTHS_DCK_OVR_EN	rw	ro	0x0	i_txrequesths_dck override enable. Active high. Used for debug purposes.
6	I_FORCETXSTOPMODE_DCK_OVR_EN	rw	ro	0x0	i_forcetxstopmode_dck override enable. Active high. Used for debug purposes.
7	I_FORCERXMODE_DCK_OVR_EN	rw	ro	0x0	i_forcerxmode_dck override enable. Active high. Used for debug purposes.
8	I_TXULPSCLK_DCK_OVR_EN	rw	ro	0x0	i_txulpsclk_dck override enable. Active high. Used for debug purposes.
9	I_TXULPSEXIT_DCK_OVR_EN	rw	ro	0x0	i_txulpsexit_dck override enable. Active high. Used for debug purposes.
10	I_TXHSIDLECLKHS_OVR_EN	rw	ro	0x0	i_txhsidleclkhs override enable. Active high. Used for debug purposes.
11	O_TXHSIDLECLKREADYHS_OVR_EN	rw	ro	0x0	o_txhsidleclkreadyhs override enable. Active high. Used for debug purposes.
14:12	O_DPHY_RX_CLK_AG_OVR_VAL	rw	ro	0x0	o_dphy_rx_clk_ag override value. Used for debug purposes.
15	O_DPHY_RX_CLK_AG_OVR_EN	rw	ro	0x0	o_dphy_rx_clk_ag override enable. Active high. Used for debug purposes.

1.1.1.374 CORE_DIG_IOCTRL_RW_DPHY_PPI_CLK_OVR_2 Reg. 0x1A02

Digital hard macro interface observability
access : read-write

bits	name	s/w	h/w	default	description
0	I_DPHY_HSACTIVERX_AG_OVR_VAL	rw	ro	0x0	i_dphy_hsactiverx_ag override value. Used for debug purposes.
1	O_DPHY_HSACTIVERX_AG_OVR_VAL	rw	ro	0x0	o_dphy_hsactiverx_ag override value. Used for debug purposes.
2	I_DPHY_HSACTIVERX_AG_OVR_EN	rw	ro	0x0	i_dphy_hsactiverx_ag override enable. Active high. Used for debug purposes.
3	O_DPHY_HSACTIVERX_AG_OVR_EN	rw	ro	0x0	o_dphy_hsactiverx_ag override enable. Active high. Used for debug purposes.
15:4	RESERVED_15_4	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.375 CORE_DIG_IOCTRL_R_DPHY_PPI_CLK_OVR_0 Reg. 0x1A03

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
0	I_ENABLE_DCK_INT	ro	rw	0x0	i_enable_dck_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	O_STOPSTATE_DCK	ro	rw	0x0	o_stopstate_dck override multiplexer output. Used for debug purposes. (volatile) volatile : true
2	O_ULPSACTIVENOT_DCK	ro	rw	0x0	o_ulpsactivenot_dck override multiplexer output. Used for debug purposes. (volatile)

					volatile : true
3	O_RXULPSCLKNOT_DCK	ro	rw	0x0	o_rxulpsclknot_dck override multiplexer output. Used for debug purposes. (volatile) volatile : true
4	O_RXCLKACTIVEHS_DCK_INT	ro	rw	0x0	o_rxclkactivehs_dck_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
5	I_TXREQUESTHS_DCK	ro	rw	0x0	i_txrequesths_dck override multiplexer output. Used for debug purposes. (volatile) volatile : true
6	I_FORCETXSTOPMODE_DCK_INT	ro	rw	0x0	i_forcetxstopmode_dck override multiplexer output. Used for debug purposes. (volatile) volatile : true
7	I_FORCERXMODE_DCK_INT	ro	rw	0x0	i_forcerxmode_dck override multiplexer output. Used for debug purposes. (volatile) volatile : true
8	I_TXULPSCLK_DCK_INT	ro	rw	0x0	i_txulpsclk_dck override multiplexer output. Used for debug purposes. (volatile) volatile : true
9	I_TXULPSEXIT_DCK_INT	ro	rw	0x0	i_txulpsexit_dck override multiplexer output. Used for debug purposes. (volatile) volatile : true
10	I_TXHSIDLECLKHS_INT	ro	rw	0x0	i_txhsidleclkhs override multiplexer output. Used for debug purposes. (volatile) volatile : true
11	O_TXHSIDLECLKREADYHS_INT	ro	rw	0x0	o_txhsidleclkreadyhs override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.376 CORE_DIG_IOCTRL_R_DPHY_PPI_CLK_OVR_1

Reg. 0x1A04

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
2:0	I_DPHY_RX_CLK_AG_INT	ro	rw	0x0	i_dphy_rx_clk_ag override multiplexer output. Used for debug purposes. (volatile) volatile : true
5:3	O_DPHY_RX_CLK_AG_INT	ro	rw	0x0	o_dphy_rx_clk_ag override multiplexer output. Used for debug purposes. (volatile) volatile : true
6	I_DPHY_HSACTIVERX_AG_INT	ro	rw	0x0	i_dphy_hsactiverx_ag_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
7	O_DPHY_HSACTIVERX_AG_INT	ro	rw	0x0	o_dphy_hsactiverx_ag_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.378 CORE_DIG_IOCTRL_RW_COMMON_PPI_OVR_0

Reg. 0x1C00

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_CFG_CLK_OVR_VAL	rw	ro	0x0	i_cfg_clk override value. Used for debug purposes.
1	I_TXCLKESC_OVR_VAL	rw	ro	0x0	i_txclkesc override value. Used for debug purposes.
2	I_RST_N_OVR_VAL	rw	ro	0x0	i_rst_n override value. Used for debug purposes.
3	I_PHY_MODE_OVR_VAL	rw	ro	0x0	i_phy_mode override value. Used for debug purposes.
4	I_CONT_EN_OVR_VAL	rw	ro	0x0	i_cont_en override value. Used for debug purposes.
5	I_TEST_STOP_CLK_EN_OVR_VAL	rw	ro	0x0	i_test_stop_clk_en override value. Used for debug purposes.

6	O_OCLA_CLK_OVR_VAL	rw	ro	0x0	o_ocla_clk override value. Used for debug purposes.
7	O_MON_OUT_VALID_OVR_VAL	rw	ro	0x0	o_mon_out_valid override value. Used for debug purposes.
8	I_PHY_STATE_OVR_EN	rw	ro	0x0	i_phy_state override enable. Active high. Used for debug purposes.
9	I_PHY_CALIB_IN_OVR_EN	rw	ro	0x0	i_phy_calib_in override enable. Active high. Used for debug purposes.
10	O_PHY_CALIB_OUT_OVR_EN	rw	ro	0x0	o_phy_calib_out override enable. Active high. Used for debug purposes.
11	I_RX_TX_N_OVR_VAL	rw	ro	0x0	i_rx_tn_n override value. Used for debug purposes.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.379 CORE_DIG_IOCTRL_RW_COMMON_PPI_OVR_1

Reg. 0x1C01

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
0	I_CFG_CLK_OVR_EN	rw	ro	0x0	i_cfg_clk override enable. Active high. Used for debug purposes.
1	I_TXCLKESC_OVR_EN	rw	ro	0x0	i_txclkesc override enable. Active high. Used for debug purposes.
2	I_RST_N_OVR_EN	rw	ro	0x0	i_rst_n override enable. Active high. Used for debug purposes.
3	I_PHY_MODE_OVR_EN	rw	ro	0x0	i_phy_mode override enable. Active high. Used for debug purposes.
4	I_CONT_EN_OVR_EN	rw	ro	0x0	i_cont_en override enable. Active high. Used for debug purposes.
5	I_TEST_STOP_CLK_EN_OVR_EN	rw	ro	0x0	i_test_stop_clk_en override enable. Active high. Used for debug purposes.
6	O_OCLA_CLK_OVR_EN	rw	ro	0x0	o_ocla_clk override enable. Active high. Used for debug purposes.
7	O_MON_OUT_VALID_OVR_EN	rw	ro	0x0	o_mon_out_valid override enable. Active high. Used for debug purposes.
8	O_MON_OUT_OVR_EN	rw	ro	0x0	o_mon_out override enable. Active high. Used for debug purposes.
9	O_CONT_DATA_OVR_EN	rw	ro	0x0	o_cont_data override enable. Active high. Used for debug purposes.
10	O_DTB_OUT_OVR_EN	rw	ro	0x0	o_dtb_out override enable. Active high. Used for debug purposes.
11	I_RX_TX_N_OVR_EN	rw	ro	0x0	i_rx_tx_n override enable. Active high. Used for debug purposes.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.380 CORE_DIG_IOCTRL_RW_COMMON_PPI_OVR_2

Reg. 0x1C02

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
4:0	I_PHY_STATE_OVR_VAL	rw	ro	0x0	i_phy_state override value. Used for debug purposes.
11:5	O_CONT_DATA_OVR_VAL	rw	ro	0x0	o_cont_data override value. Used for debug purposes.
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.381 CORE_DIG_IOCTRL_RW_COMMON_PPI_OVR_3

Reg. 0x1C03

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	I_PHY_CALIB_IN_OVR_VAL	rw	ro	0x0	i_phy_calib_in[15:0] override value. Used for debug purposes.

1.1.1.382 CORE_DIG_IOCTRL_RW_COMMON_PPI_OVR_4

Reg. 0x1C04

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	I_PHY_CALIB_IN_OVR_VAL	rw	ro	0x0	i_phy_calib_in[31:16] override value. Used for debug purposes.

1.1.1.383 CORE_DIG_IOCTRL_RW_COMMON_PPI_OVR_5

Reg. 0x1C05

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
7:0	I_PHY_CALIB_IN_OVR_VAL	rw	ro	0x0	i_phy_calib_in[39:32] override value. Used for debug purposes.
15:8	O_DTB_OUT_OVR_VAL	rw	ro	0x0	o_dtb_out override value. Used for debug purposes.

1.1.1.384 CORE_DIG_IOCTRL_RW_COMMON_PPI_OVR_6

Reg. 0x1C06

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	O_PHY_CALIB_OUT_OVR_VAL	rw	ro	0x0	o_phy_calib_out[15:0] override value. Used for debug purposes.

1.1.1.385 CORE_DIG_IOCTRL_RW_COMMON_PPI_OVR_7

Reg. 0x1C07

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	O_MON_OUT_OVR_VAL	rw	ro	0x0	o_mon_out[15:0] override value. Used for debug purposes.

1.1.1.386 CORE_DIG_IOCTRL_RW_COMMON_PPI_OVR_8

Reg. 0x1C08

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	O_MON_OUT_OVR_VAL	rw	ro	0x0	o_mon_out[31:16] override value. Used for debug purposes.

1.1.1.387 CORE_DIG_IOCTRL_RW_COMMON_PPI_OVR_9

Reg. 0x1C09

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	O_MON_OUT_OVR_VAL	rw	ro	0x0	o_mon_out[47:32] override value. Used for debug purposes.

1.1.1.388 CORE_DIG_IOCTRL_RW_COMMON_PPI_OVR_10

Reg. 0x1C0A

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
15:0	O_MON_OUT_OVR_VAL	rw	ro	0x0	o_mon_out[63:48] override value. Used for debug purposes.

1.1.1.389 CORE_DIG_IOCTRL_RW_COMMON_PPI_OVR_11

Reg. 0x1C0B

Digital hard macro interface override
access : read-write

bits	name	s/w	h/w	default	description
7:0	O_PHY_CALIB_OUT_OVR_VAL	rw	ro	0x0	o_phy_calib_out[23:16] override value. Used for debug purposes.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.391 CORE_DIG_IOCTRL_R_COMMON_PPI_OVR_0

Reg. 0x1C10

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
0	I_CFG_CLK_INT	ro	rw	0x0	i_cfg_clk override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	I_TXCLKESC_INT	ro	rw	0x0	i_txclkesc override multiplexer output. Used for debug purposes. (volatile) volatile : true
2	I_RST_N_INT	ro	rw	0x0	i_rst_n override multiplexer output. Used for debug purposes. (volatile) volatile : true
3	I_PHY_MODE_INT	ro	rw	0x0	i_phy_mode override multiplexer output. Used for debug purposes. (volatile) volatile : true
4	I_CONT_EN_INT	ro	rw	0x0	i_cont_en override multiplexer output. Used for debug purposes. (volatile) volatile : true
5	I_TEST_STOP_CLK_EN_INT	ro	rw	0x0	i_test_stop_clk_en override multiplexer output. Used for debug purposes. (volatile) volatile : true
6	O_OCLA_CLK	ro	rw	0x0	o_ocla_clk override multiplexer output. Used for debug purposes. (volatile) volatile : true
7	O_MON_OUT_VALID	ro	rw	0x0	o_mon_out_valid override multiplexer output. Used for debug purposes. (volatile) volatile : true
8	I_RX_TX_N	ro	rw	0x0	i_rx_tx_n override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:9	RESERVED_15_9	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.392 CORE_DIG_IOCTRL_R_COMMON_PPI_OVR_1

Reg. 0x1C11

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
4:0	I_PHY_STATE_INT	ro	rw	0x0	i_phy_state override multiplexer output. Used for debug purposes. (volatile) volatile : true
11:5	O_CONT_DATA	ro	rw	0x0	o_cont_data override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.393 CORE_DIG_IOCTRL_R_COMMON_PPI_OVR_2

Reg. 0x1C12

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	I_PHY_CALIB_IN_INT	ro	rw	0x0	i_phy_calib_in override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.394 CORE_DIG_IOCTRL_R_COMMON_PPI_OVR_3

Reg. 0x1C13

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	I_PHY_CALIB_IN_INT	ro	rw	0x0	i_phy_calib_in override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.395 CORE_DIG_IOCTRL_R_COMMON_PPI_OVR_4

Reg. 0x1C14

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
7:0	I_PHY_CALIB_IN_INT	ro	rw	0x0	i_phy_calib_in override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:8	O_DTB_OUT	ro	rw	0x0	o_dtb_out override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.396 CORE_DIG_IOCTRL_R_COMMON_PPI_OVR_5

Reg. 0x1C15

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	O_PHY_CALIB_OUT	ro	rw	0x0	o_phy_calib_out[15:0] override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.397 CORE_DIG_IOCTRL_R_COMMON_PPI_OVR_6

Reg. 0x1C16

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	O_MON_OUT	ro	rw	0x0	o_mon_out override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.398 CORE_DIG_IOCTRL_R_COMMON_PPI_OVR_7

Reg. 0x1C17

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	O_MON_OUT	ro	rw	0x0	o_mon_out override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.399 CORE_DIG_IOCTRL_R_COMMON_PPI_OVR_8

Reg. 0x1C18

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	O_MON_OUT	ro	rw	0x0	o_mon_out override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.400 CORE_DIG_IOCTRL_R_COMMON_PPI_OVR_9

Reg. 0x1C19

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	O_MON_OUT	ro	rw	0x0	o_mon_out override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.401 CORE_DIG_IOCTRL_R_COMMON_PPI_OVR_10

Reg. 0x1C1A

Digital hard macro interface observability
access : read-only

bits	name	s/w	h/w	default	description
7:0	O_PHY_CALIB_OUT	ro	rw	0x0	o_phy_calib_out[23:16] override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.403 CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_0

Reg. 0x1C20

Analog macro common block control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_SEL_CPHY_DPHY_OVR_VAL	rw	ro	0x0	oa_sel_cphy_dphy override value. Used for debug purposes.
1	OA_CB_ATB_CLK_OVR_VAL	rw	ro	0x0	oa_cb_atb_clk override value. Used for debug purposes.
2	OA_CB_CHOP_CLK_OVR_VAL	rw	ro	0x0	oa_cb_chop_clk override value. Used for debug purposes.
3	OA_CB_CHOP_CLK_EN_OVR_VAL	rw	ro	0x0	oa_cb_chop_clk_en override value. Used for debug purposes.
4	OA_CB_PON_OVR_VAL	rw	ro	0x0	oa_cb_pon override value. Used for debug purposes.
5	OA_CB_BG_PON_OVR_VAL	rw	ro	0x0	oa_cb_bg_pon override value. Used for debug purposes.
6	OA_CB_CAL_PON_OVR_VAL	rw	ro	0x0	oa_cb_cal_pon override value. Used for debug purposes.
7	OA_CB_CAL_UP_EN_OVR_VAL	rw	ro	0x0	oa_cb_cal_up_en override value. Used for debug purposes.
8	OA_CB_CAL_DOWN_EN_OVR_VAL	rw	ro	0x0	oa_cb_cal_down_en override value. Used for debug purposes.
9	OA_CB_ATB_COMP_PON_OVR_VAL	rw	ro	0x0	oa_cb_atb_comp_pon override value. Used for debug purposes.
10	OA_CB_HSTX_VCOMM_REG_PON_OVR_VAL	rw	ro	0x0	oa_cb_hstx_vcomm_reg_pon override value. Used for debug purposes.
11	OA_CB_IBIAS_PON_OVR_VAL	rw	ro	0x0	oa_cb_ibias_pon override value. Used for debug purposes.
12	OA_CB_AMP1200_PON_OVR_VAL	rw	ro	0x0	oa_cb_amp1200_pon override value. Used for debug purposes.
13	OA_CB_VPCLK_REG_PON_OVR_VAL	rw	ro	0x0	oa_cb_vpclk_reg_pon override value. Used for debug purposes.
14	OA_CB_ATB_SEL_DAC_OVR_EN	rw	ro	0x0	oa_cb_atb_sel_dac override enable. Active high. Used for debug purposes.

15	OA_CB_HSTXLB_DCO_CLK90_EN_OVR_VAL	rw	ro	0x0	oa_cb_hstxlb_dco_clk90_en override value. Used for debug purposes.

1.1.1.404 CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_1

Reg. 0x1C21

Analog macro common block control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_SEL_CPHY_DPHY_OVR_EN	rw	ro	0x0	oa_sel_cphy_dphy override enable. Active high. Used for debug purposes.
1	OA_CB_ATB_CLK_OVR_EN	rw	ro	0x0	oa_cb_atb_clk override enable. Active high. Used for debug purposes.
2	OA_CB_CHOP_CLK_OVR_EN	rw	ro	0x0	oa_cb_chop_clk override enable. Active high. Used for debug purposes.
3	OA_CB_CHOP_CLK_EN_OVR_EN	rw	ro	0x0	oa_cb_chop_clk_en override enable. Active high. Used for debug purposes.
4	OA_CB_PON_OVR_EN	rw	ro	0x0	oa_cb_pon override enable. Active high. Used for debug purposes.
5	OA_CB_BG_PON_OVR_EN	rw	ro	0x0	oa_cb_bg_pon override enable. Active high. Used for debug purposes.
6	OA_CB_CAL_PON_OVR_EN	rw	ro	0x0	oa_cb_cal_pon override enable. Active high. Used for debug purposes.
7	OA_CB_CAL_UP_EN_OVR_EN	rw	ro	0x0	oa_cb_cal_up_en override enable. Active high. Used for debug purposes.
8	OA_CB_CAL_DOWN_EN_OVR_EN	rw	ro	0x0	oa_cb_cal_down_en override enable. Active high. Used for debug purposes.
9	OA_CB_ATB_COMP_PON_OVR_EN	rw	ro	0x0	oa_cb_atb_comp_pon override enable. Active high. Used for debug purposes.
10	OA_CB_HSTX_VCOMM_REG_PON_OVR_EN	rw	ro	0x0	oa_cb_hstx_vcomm_reg_pon override enable. Active high. Used for debug purposes.
11	OA_CB_IBIAS_PON_OVR_EN	rw	ro	0x0	oa_cb_ibias_pon override enable. Active high. Used for debug purposes.
12	OA_CB_AMP1200_PON_OVR_EN	rw	ro	0x0	oa_cb_amp1200_pon override enable. Active high. Used for debug purposes.
13	OA_CB_VPCLK_REG_PON_OVR_EN	rw	ro	0x0	oa_cb_vpclk_reg_pon override enable. Active high. Used for debug purposes.
14	OA_CB_ATB_SEL_OVR_EN	rw	ro	0x0	oa_cb_atb_sel override enable. Active high. Used for debug purposes.
15	OA_CB_HSTXLB_DCO_CLK0_EN_OVR_VAL	rw	ro	0x0	oa_cb_hstxlb_dco_clk0_en override value. Used for debug purposes.

1.1.1.405 CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_2

Reg. 0x1C22

Analog macro common block control
access : read-write

bits	name	s/w	h/w	default	description
9:0	OA_CB_ATB_SEL_DAC_OVR_VAL	rw	ro	0x0	oa_cb_atb_sel_dac override value. Used for debug purposes.
11:10	OA_CB_ATB_SEL_OVR_VAL	rw	ro	0x0	oa_cb_atb_sel override value. Used for debug purposes.
12	OA_CB_ATB_EXT_CON	rw	ro	0x0	Enable allowing to directly connect ATB line to ATB pin. Active high.
13	OA_CB_ATB_PROBE_BOOST_EN	rw	ro	0x0	Enable to use boost vctrl as input for ATB comparator. Active high.
14	OA_CB_ATB_PROBE_VBE_EN	rw	ro	0x0	Enable to perform temperature measurement through ATB. Active high.
15	OA_CB_PLL_BUSTIEZ	rw	ro	0x0	Enable for grounding PLL input phases (0 and 90). Active low.

1.1.1.406 CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_3

Reg. 0x1C23

Analog macro common block control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_CB_SEL_LPTX_VREF	rw	ro	0x0	Programmability for LP-TX driver amplitude. 0 : 1200mV ; 1 : 1100mV.
3:1	OA_SEL_LPTX_PROG	rw	ro	0x3	LP-TX bias current programmability. Check table for more details.
6:4	OA_CB_SEL_MPLL_REG_VREF	rw	ro	0x7	Programmable voltage reference for MPLL regulator. Check table for more details.
7	OA_CB_SEL_HSTXLB_DCO_VREF	rw	ro	0x1	Source of reference used in HSTX loopback DCO. 0 : mpll_vref ; 1 : ATB DAC
8	OA_CB_HSTXLB_DCO_CLK0_EN_OVR_EN	rw	ro	0x0	oa_cb_hstxlb_dco_clk0_en override enable. Active high. Used for debug purposes.
9	OA_CB_HSTXLB_DCO_CLK90_EN_OVR_EN	rw	ro	0x0	oa_cb_hstxlb_dco_clk90_en override enable. Active high. Used for debug purposes.
11:10	OA_CB_HSTXLB_DCO_SEL_DIV	rw	ro	0x0	Divider configuration used in the generation of HSTX loop-back phases (0 and 90).
14:12	OA_CB_HSTX_BOOST_PROG	rw	ro	0x4	HSTX boost current programmability. Check table for more details.
15	OA_CB_HSTX_VCOMM_REG_STBON	rw	ro	0x0	Enable of internal stability loop for HS-TX vcomm regulator. Active high.

1.1.1.407 CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_4

Reg. 0x1C24

Analog macro common block control
access : read-write

bits	name	s/w	h/w	default	description
2:0	OA_CB_SEL_TRIO0_ALP_VREF	rw	ro	0x2	ALP pause wake up detector sign and offset magnitude control for trio0. Check table for more details.
5:3	OA_CB_SEL_TRIO1_ALP_VREF	rw	ro	0x2	ALP pause wake up detector sign and offset magnitude control for trio1. Check table for more details.
8:6	OA_CB_SEL_TRIO2_ALP_VREF	rw	ro	0x2	ALP pause wake up detector sign and offset magnitude control for trio2. Check table for more details.
10:9	OA_CB_SEL_HSRX_CM_DET_VREF	rw	ro	0x1	Programmability of used reference voltage in common mode detector. Check table for more details.
13:11	OA_CB_SEL_VCOMM_PROG	rw	ro	0x4	Programmability of HS-TX driver amplitude.
14	OA_CB_VCOMM_UNTERM_MODE	rw	ro	0x0	Selector control for unterminated mode. Active high.
15	OA_CB_CAL_SINK_EN_OVR_VAL	rw	ro	0x0	oa_cb_cal_sink_en override value. Used for debug purposes.

1.1.1.408 CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_5

Reg. 0x1C25

Analog macro common block control
access : read-write

bits	name	s/w	h/w	default	description
3:0	OA_CB_SPARE_IN	rw	ro	0x0	Spare pins reserved for analog macro common block control
7:4	OA_SETR_CALIB_VT	rw	ro	0x0	Vt drift control for termination.
8	OA_CB_SEL_45OHM_50OHM	rw	ro	0x1	Programmability of tuning resistance used in calibration: 0- 50 ohms; 1- 45 ohms
9	OA_CB_REXT_IOCONT_EN_OVR_VAL	rw	ro	0x0	oa_cb_rext_iocont_en override value. Used for debug purposes.
11:10	OA_CB_VPCLK_REG_MODE	rw	ro	0x0	Vpclk regulator mode:. Check table for more details.
13:12	OA_CB_DSK_CLK_CHANNEL	rw	ro	0x0	Programmability for D-PHY Internal deskew clock channel. Check table for more details.

14	OA_CB_SEL_EXT_INT_CHOP_CLK	rw	ro	0x1	Source selector for chop clock used under bandgap circuit : 0 - internal clock from dco; 1 - external clock from cb_refclk
15	OA_CB_CAL_SINK_EN_OVR_EN	rw	ro	0x0	oa_cb_cal_sink_en override enable. Active high. Used for debug purposes.

1.1.1.409 CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_6

Reg. 0x1C26

Analog macro common block control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_CB_LP_DCO_PON_OVR_VAL	rw	ro	0x0	oa_cb_lp_dco_pon override value. Used for debug purposes.
1	OA_CB_LP_DCO_EN_OVR_VAL	rw	ro	0x0	oa_cb_lp_dco_en override value. Used for debug purposes.
2	OA_CB_LP_DCO_CLK_EN_OVR_VAL	rw	ro	0x0	oa_cb_lp_dco_clk_en override value. Used for debug purposes.
3	OA_CB_LP_DCO_FWORD_CHANGE_OVR_VAL	rw	ro	0x0	oa_cb_lp_dco_fword_change override value. Used for debug purposes.
10:4	OA_CB_LP_DCO_FWORD_OVR_VAL	rw	ro	0x0	oa_cb_lp_dco_fword override value. Used for debug purposes.
11	OA_CB_HSTXLB_DCO_FWORD_OVR_EN	rw	ro	0x0	oa_cb_hstxlb_dco_fword override enable. Active high. Used for debug purposes.
12	OA_CB_HSTXLB_DCO_PON_OVR_EN	rw	ro	0x0	oa_cb_hstxlb_dco_pon override enable. Active high. Used for debug purposes.
13	OA_CB_HSTXLB_DCO_EN_OVR_EN	rw	ro	0x0	oa_cb_hstxlb_dco_en override enable. Active high. Used for debug purposes.
14	OA_CB_HSTXLB_DCO_TUNE_CLKDIG_EN_OVR_EN	rw	ro	0x0	oa_cb_hstxlb_dco_tune_clkdig_en override enable. Active high. Used for debug purposes.
15	OA_CB_REXT_IOCONT_EN_OVR_EN	rw	ro	0x0	oa_cb_rext_iocont_en override enable. Active high. Used for debug purposes.

1.1.1.410 CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_7

Reg. 0x1C27

Analog macro common block control
access : read-write

bits	name	s/w	h/w	default	description
0	OA_CB_LP_DCO_PON_OVR_EN	rw	ro	0x0	oa_cb_lp_dco_pon override enable. Active high. Used for debug purposes.
1	OA_CB_LP_DCO_EN_OVR_EN	rw	ro	0x0	oa_cb_lp_dco_en override enable. Active high. Used for debug purposes.
2	OA_CB_LP_DCO_CLK_EN_OVR_EN	rw	ro	0x0	oa_cb_lp_dco_clk_en override enable. Active high. Used for debug purposes.
3	OA_CB_LP_DCO_FWORD_CHANGE_OVR_EN	rw	ro	0x0	oa_cb_lp_dco_fword_change override enable. Active high. Used for debug purposes.
4	OA_CB_LP_DCO_FWORD_OVR_EN	rw	ro	0x0	oa_cb_lp_dco_fword override enable. Active high. Used for debug purposes.
7:5	OA_CB_HSTXLB_DCO_FWORD_OVR_VAL	rw	ro	0x0	oa_cb_hstxlb_dco_fword override value. Used for debug purposes.
8	OA_CB_HSTXLB_DCO_PON_OVR_VAL	rw	ro	0x0	oa_cb_hstxlb_dco_pon override value. Used for debug purposes.
9	OA_CB_HSTXLB_DCO_EN_OVR_VAL	rw	ro	0x0	oa_cb_hstxlb_dco_en override value. Used for debug purposes.
10	OA_CB_HSTXLB_DCO_TUNE_CLKDIG_EN_OVR_VAL	rw	ro	0x0	oa_cb_hstxlb_dco_tune_clkdig_en override value. Used for debug purposes.
11	OA_SETR_OVR_EN	rw	ro	0x0	oa_setr override enable. Active high. Used for debug purposes.
12	OA_SETR_CALIB_OVR_EN	rw	ro	0x0	oa_setr_calib override enable. Active high. Used for debug purposes.
13	OA_SETRA_OVR_EN	rw	ro	0x0	oa_setra override enable. Active high. Used for debug purposes.

14	OA_SETRB_OVR_EN	rw	ro	0x0	oa_setrb override enable. Active high. Used for debug purposes.
15	OA_CB_DSK_CLK_MODE_OVR_EN	rw	ro	0x0	oa_cb_dsk_clk_mode override enable. Active high. Used for debug purposes.

1.1.1.411 CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_8

Reg. 0x1C28

Analog macro common block control
access : read-write

bits	name	s/w	h/w	default	description
3:0	OA_SETR_OVR_VAL	rw	ro	0x0	oa_setr override value. Used for debug purposes.
7:4	OA_SETR_CALIB_OVR_VAL	rw	ro	0x0	oa_setr_calib override value. Used for debug purposes.
10:8	OA_SETRA_OVR_VAL	rw	ro	0x0	oa_setra override value. Used for debug purposes.
13:11	OA_SETRB_OVR_VAL	rw	ro	0x0	oa_setrb override value. Used for debug purposes.
15:14	OA_CB_DSK_CLK_MODE_OVR_VAL	rw	ro	0x0	oa_cb_dsk_clk_mode override value. Used for debug purposes.

1.1.1.412 CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_9

Reg. 0x1C29

Analog macro common block control
access : read-write

bits	name	s/w	h/w	default	description
0	IA_CB_ATB_COMP_OUT_OVR_VAL	rw	ro	0x0	ia_cb_atb_comp_out override value. Used for debug purposes.
1	IA_CB_DET_VP_OVR_VAL	rw	ro	0x0	ia_cb_det_vp override value. Used for debug purposes.
2	IA_CB_DET_VPH_OVR_VAL	rw	ro	0x0	ia_cb_det_vph override value. Used for debug purposes.
3	IA_CB_HSTXLB_CLKDIG_OVR_VAL	rw	ro	0x0	ia_cb_hstxlb_clkdig override value. Used for debug purposes.
4	IA_CB_LP_DCO_CLK_OVR_VAL	rw	ro	0x0	ia_cb_lp_dco_clk override value. Used for debug purposes.
5	IA_CB_REXT_IOCONT_OVR_VAL	rw	ro	0x0	ia_cb_rext_iocont override value. Used for debug purposes.
9:6	IA_CB_SPARE_OUT_OVR_VAL	rw	ro	0x0	ia_cb_spare_out override value. Used for debug purposes.
15:10	RESERVED_15_10	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.413 CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_10

Reg. 0x1C2A

Analog macro common block control
access : read-write

bits	name	s/w	h/w	default	description
0	IA_CB_ATB_COMP_OUT_OVR_EN	rw	ro	0x0	ia_cb_atb_comp_out override enable. Active high. Used for debug purposes.
1	IA_CB_DET_VP_OVR_EN	rw	ro	0x0	ia_cb_det_vp override enable. Active high. Used for debug purposes.
2	IA_CB_DET_VPH_OVR_EN	rw	ro	0x0	ia_cb_det_vph override enable. Active high. Used for debug purposes.
3	IA_CB_HSTXLB_CLKDIG_OVR_EN	rw	ro	0x0	ia_cb_hstxlb_clkdig override enable. Active high. Used for debug purposes.
4	IA_CB_LP_DCO_CLK_OVR_EN	rw	ro	0x0	ia_cb_lp_dco_clk override enable. Active high. Used for debug purposes.
5	IA_CB_REXT_IOCONT_OVR_EN	rw	ro	0x0	ia_cb_rext_iocont override enable. Active high. Used for debug purposes.
6	IA_CB_SPARE_OUT_OVR_EN	rw	ro	0x0	ia_cb_spare_out override enable. Active high. Used for debug purposes.
15:7	RESERVED_15_7	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.414 CORE_DIG_IOCTRL_RW_AFE_CB_CTRL_11

Reg. | 0x1C2B

Analog macro common block control
access : read-write

bits	name	s/w	h/w	default	description
2:0	OA_CB_VP2_PROG	rw	ro	0x4	Programmability for the reference voltage used for biasing. Check table for more details.
3	OA_A2D_16_BUS_EN	rw	ro	0x0	Enable of 16 bit wide interface
15:4	RESERVED_15_4	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.416 CORE_DIG_IOCTRL_R_AFE_CB_CTRL_0

Reg. | 0x1C30

Analog macro common block observability
access : read-only

bits	name	s/w	h/w	default	description
0	OA_SEL_CPHY_DPHY	ro	rw	0x0	oa_sel_cphy_dphy override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	OA_CB_ATB_CLK	ro	rw	0x0	oa_cb_atb_clk override multiplexer output. Used for debug purposes. (volatile) volatile : true
2	OA_CB_CHOP_CLK	ro	rw	0x0	oa_cb_chop_clk override multiplexer output. Used for debug purposes. (volatile) volatile : true
3	OA_CB_CHOP_CLK_EN	ro	rw	0x0	oa_cb_chop_clk_en override multiplexer output. Used for debug purposes. (volatile) volatile : true
4	OA_CB_PON	ro	rw	0x0	oa_cb_pon override multiplexer output. Used for debug purposes. (volatile) volatile : true
5	OA_CB_BG_PON	ro	rw	0x0	oa_cb_bg_pon override multiplexer output. Used for debug purposes. (volatile) volatile : true
6	OA_CB_CAL_PON	ro	rw	0x0	oa_cb_cal_pon override multiplexer output. Used for debug purposes. (volatile) volatile : true
7	OA_CB_CAL_UP_EN	ro	rw	0x0	oa_cb_cal_up_en override multiplexer output. Used for debug purposes. (volatile) volatile : true
8	OA_CB_CAL_DOWN_EN	ro	rw	0x0	oa_cb_cal_down_en override multiplexer output. Used for debug purposes. (volatile) volatile : true
9	OA_CB_ATB_COMP_PON	ro	rw	0x0	oa_cb_atb_comp_pon override multiplexer output. Used for debug purposes. (volatile) volatile : true
10	OA_CB_HSTX_VCOMM_REG_PON	ro	rw	0x0	oa_cb_hstx_vcomm_reg_pon override multiplexer output. Used for debug purposes. (volatile) volatile : true
11	OA_CB_IBIAS_PON	ro	rw	0x0	oa_cb_ibias_pon override multiplexer output. Used for debug purposes. (volatile) volatile : true
12	OA_CB_AMP1200_PON	ro	rw	0x0	oa_cb_amp1200_pon override multiplexer output. Used for debug purposes. (volatile) volatile : true
13	OA_CB_VPCLK_REG_PON	ro	rw	0x0	oa_cb_vpclk_reg_pon override multiplexer output. Used for debug purposes. (volatile) volatile : true
14	OA_CB_HSTXLB_DCO_CLK90_EN	ro	rw	0x0	oa_cb_hstxlb_dco_clk90_en override multiplexer output. Used for debug purposes. (volatile) volatile : true
15	OA_CB_REXT_IOCONT_EN	ro	rw	0x0	oa_cb_rext_iocont_en override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.417 CORE_DIG_IOCTRL_R_AFE_CB_CTRL_1

Reg. 0x1C31

Analog macro common block observability
access : read-only

bits	name	s/w	h/w	default	description
9:0	OA_CB_ATB_SEL_DAC	ro	rw	0x0	oa_cb_atb_sel_dac override multiplexer output. Used for debug purposes. (volatile) volatile : true
11:10	OA_CB_ATB_SEL	ro	rw	0x0	oa_cb_atb_sel override multiplexer output. Used for debug purposes. (volatile) volatile : true
12	OA_CB_CAL_SINK_EN	ro	rw	0x0	oa_cb_cal_sink_en override multiplexer output. Used for debug purposes. (volatile) volatile : true
13	OA_CB_HSTXLB_DCO_CLK0_EN	ro	rw	0x0	oa_cb_hstxlb_dco_clk0_en override multiplexer output. Used for debug purposes. (volatile) volatile : true
14	OA_CB_HSTXLB_DCO_TUNE_CLKDIG_EN	ro	rw	0x0	oa_cb_hstxlb_dco_tune_clkdig_en override multiplexer output. Used for debug purposes. (volatile) volatile : true
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.418 CORE_DIG_IOCTRL_R_AFE_CB_CTRL_2

Reg. 0x1C32

Analog macro common block observability
access : read-only

bits	name	s/w	h/w	default	description
0	OA_CB_LP_DCO_PON	ro	rw	0x0	oa_cb_lp_dco_pon override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	OA_CB_LP_DCO_EN	ro	rw	0x0	oa_cb_lp_dco_en override multiplexer output. Used for debug purposes. (volatile) volatile : true
2	OA_CB_LP_DCO_CLK_EN	ro	rw	0x0	oa_cb_lp_dco_clk_en override multiplexer output. Used for debug purposes. (volatile) volatile : true
3	OA_CB_LP_DCO_FWORD_CHANGE	ro	rw	0x0	oa_cb_lp_dco_fword_change override multiplexer output. Used for debug purposes. (volatile) volatile : true
10:4	OA_CB_LP_DCO_FWORD	ro	rw	0x0	oa_cb_lp_dco_fword override multiplexer output. Used for debug purposes. (volatile) volatile : true
13:11	OA_CB_HSTXLB_DCO_FWORD	ro	rw	0x0	oa_cb_hstxlb_dco_fword override multiplexer output. Used for debug purposes. (volatile) volatile : true
14	OA_CB_HSTXLB_DCO_PON	ro	rw	0x0	oa_cb_hstxlb_dco_pon override multiplexer output. Used for debug purposes. (volatile) volatile : true
15	OA_CB_HSTXLB_DCO_EN	ro	rw	0x0	oa_cb_hstxlb_dco_en override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.419 CORE_DIG_IOCTRL_R_AFE_CB_CTRL_3

Reg. 0x1C33

Analog macro common block observability
access : read-only

bits	name	s/w	h/w	default	description
3:0	OA_SETR	ro	rw	0x0	oa_setr override multiplexer output. Used for debug purposes. (volatile) volatile : true
7:4	OA_SETR_CALIB	ro	rw	0x0	oa_setr_calib override multiplexer output. Used for debug purposes. (volatile)

					volatile : true
10:8	OA_SETRA	ro	rw	0x0	oa_setra override multiplexer output. Used for debug purposes. (volatile) volatile : true
13:11	OA_SETRB	ro	rw	0x0	oa_setrb override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:14	OA_CB_DSK_CLK_MODE	ro	rw	0x0	oa_cb_dsk_clk_mode override multiplexer output. Used for debug purposes. (volatile) volatile : true

1.1.1.420 CORE_DIG_IOCTRL_R_AFE_CB_CTRL_4

Reg. 0x1C34

Analog macro common block observability
access : read-only

bits	name	s/w	h/w	default	description
0	IA_CB_ATB_COMP_OUT_INT	ro	rw	0x0	ia_cb_atb_comp_out_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
1	IA_CB_DET_VP_INT	ro	rw	0x0	ia_cb_det_vp_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
2	IA_CB_DET_VPH_INT	ro	rw	0x0	ia_cb_det_vph_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
3	IA_CB_HSTXLB_CLKDIG_INT	ro	rw	0x0	ia_cb_hstxlb_clkdig_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
4	IA_CB_LP_DCO_CLK_INT	ro	rw	0x0	ia_cb_lp_dco_clk_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
5	IA_CB_REXT_IOCONT_INT	ro	rw	0x0	ia_cb_rext_iocont_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
9:6	IA_CB_SPARE_OUT_INT	ro	rw	0x0	ia_cb_spare_out_int override multiplexer output. Used for debug purposes. (volatile) volatile : true
15:10	RESERVED_15_10	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.422 CORE_DIG_RW_COMMON_0

Reg. 0x1C40

Common configuration
access : read-write

bits	name	s/w	h/w	default	description
0	DPHY_PREAMBLE_EN_REG	rw	ro	0x0	DPHY preamble support enable.
1	DPHY_RX_CLK_AG_EN	rw	ro	0x0	DPHY RX Aggregation feature enable. Quasi static.
13:2	HSRX_DPHY_DLL_EN_DLY	rw	ro	0x0	DPHY HSRX DLL enable delay. In dco clock cycles. Quasi static.
14	GEN2_SEL	rw	ro	0x0	Controls the A2D interface width. Used to support higher data rates, up to DPHY 6.5Gbps and CPHY 6.5Gsps. Please check "Startup Sequence". Quasi static.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.423 CORE_DIG_RW_COMMON_1

Reg. 0x1C41

OCLA Interface
access : read-write

bits	name	s/w	h/w	default	description
5:0	OCLA_DATA_SEL	rw	ro	0x0	All clock domains data enables
15:6	RESERVED_15_6	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.424 CORE_DIG_RW_COMMON_2

Reg. 0x1C42

OCLA Interface
access : read-write

bits	name	s/w	h/w	default	description
4:0	OCLA_DATA_SEL	rw	ro	0x0	All clock domains data enables
15:5	RESERVED_15_5	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.425 CORE_DIG_RW_COMMON_3

Reg. 0x1C43

OCLA Interface
access : read-write

bits	name	s/w	h/w	default	description
5:0	OCLA_CLK_SEL	rw	ro	0x0	All clock domains clock enables
15:6	RESERVED_15_6	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.426 CORE_DIG_RW_COMMON_4

Reg. 0x1C44

OCLA Interface
access : read-write

bits	name	s/w	h/w	default	description
4:0	OCLA_CLK_SEL	rw	ro	0x0	All clock domains clock enables
15:5	RESERVED_15_5	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.427 CORE_DIG_RW_COMMON_5

Reg. 0x1C45

Common configuration
access : read-write

bits	name	s/w	h/w	default	description
0	INPUT_SAMPLING_REG	rw	ro	0x0	Enables input sampling of AFE data.
8:1	DTB_SELECT	rw	ro	0x0	dtb output mux selector.
9	HSRX_DPHY_DLL_EN_DRV	rw	ro	0x0	hsrx_dphy_dll_en data lanes driver (0->clock,1->data)
11:10	WORD_CLK_SEL_DLANE	rw	ro	0x0	DPHY HS-TX word clock common source
13:12	WORD_CLK_SEL_CLANE	rw	ro	0x0	CPHY HS-TX word clock common source
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.428 CORE_DIG_RW_COMMON_6

Reg. 0x1C46

Common configuration
access : read-write

bits	name	s/w	h/w	default	description
2:0	DESERIALIZER_DIV_EN_DELAY_THRESH_D	rw	ro	0x1	Counter for assertion of deserializer_div_en of dphy lanes. In dco_clk cycles. Quasi static. 0 is a forbidden value.
5:3	DESERIALIZER_EN_DEASS_COUNT_THRESH_D	rw	ro	0x1	Counter for deassertion of deserializer_en of dphy lanes. In dco_clk cycles. Quasi static.
6	HIGHDATARATE_POST_REG	rw	ro	0x0	Selects datapath to be used for Post circuit. Quasi static.
7	POST_DELAY_REG	rw	ro	0x1	Selects whether to apply delay to post detection. Quasi static
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.429 CORE_DIG_RW_COMMON_7

Reg. 0x1C47

Common configuration
access : read-write

bits	name	s/w	h/w	default	description
1:0	LANE0_HSRX_WORD_CLK_SEL_GATING_REG	rw	ro	0x1	Analog lane 0 word clock gating configuration. Quasi static.
3:2	LANE1_HSRX_WORD_CLK_SEL_GATING_REG	rw	ro	0x1	Analog lane 1 word clock gating configuration. Quasi static.
5:4	LANE2_HSRX_WORD_CLK_SEL_GATING_REG	rw	ro	0x1	Analog lane 2 word clock gating configuration. Quasi static.
6	LANE0_CLK_EN_SYNC_BYPASS_REG	rw	ro	0x0	Selects synchronizer bypass in clock gating cell. Quasi static.
7	LANE1_CLK_EN_SYNC_BYPASS_REG	rw	ro	0x0	Selects synchronizer bypass in clock gating cell. Quasi static.
8	LANE2_CLK_EN_SYNC_BYPASS_REG	rw	ro	0x0	Selects synchronizer bypass in clock gating cell. Quasi static.
15:9	RESERVED_15_9	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.430 CORE_DIG_RW_COMMON_8

Reg. 0x1C48

Common configuration
access : read-write

bits	name	s/w	h/w	default	description
0	LANE0_HSRX_WORD_CLK_GATING_OVR_EN	rw	ro	0x0	Analog lane 0 word clock gating override enable. Quasi static.
1	LANE0_HSRX_WORD_CLK_GATING_OVR_VAL	rw	ro	0x0	Analog lane 0 word clock gating override value. Quasi static.
2	LANE1_HSRX_WORD_CLK_GATING_OVR_EN	rw	ro	0x0	Analog lane 1 word clock gating override enable. Quasi static.
3	LANE1_HSRX_WORD_CLK_GATING_OVR_VAL	rw	ro	0x0	Analog lane 1 word clock gating override value. Quasi static.
4	LANE2_HSRX_WORD_CLK_GATING_OVR_EN	rw	ro	0x0	Analog lane 2 word clock gating override enable. Quasi static.
5	LANE2_HSRX_WORD_CLK_GATING_OVR_VAL	rw	ro	0x0	Analog lane 2 word clock gating override value. Quasi static.
15:6	RESERVED_15_6	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.431 CORE_DIG_RW_COMMON_9

Reg. 0x1C49

Common configuration
access : read-write

bits	name	s/w	h/w	default	description
0	LP_DCO_CLK_GATING_OVR_EN	rw	ro	0x0	LP DCO clock gating override enable. Quasi static.
1	LP_DCO_CLK_GATING_OVR_VAL	rw	ro	0x0	LP DCO clock gating override value. Quasi static.
3:2	LP_DCO_CLK_SEL_GATING_REG	rw	ro	0x3	LP DCO clock gating configuration. Quasi static.
4	HSTXLB_DCO_CLK_GATING_OVR_EN	rw	ro	0x0	HSTXLB DCO clock gating override enable. Quasi static.
5	HSTXLB_DCO_CLK_GATING_OVR_VAL	rw	ro	0x0	HSTXLB DCO clock gating override value. Quasi static.

7:6	HSTXLB_DCO_CLK_SEL_GATING_REG	rw	ro	0x3	HSTXLB DCO clock gating configuration. Quasi static.
8	LPRX_DOUTLP_SYNC_SEL	rw	ro	0x0	Select lprx_doutlp synchronization (LP-DCO clock). Active high. Quasi static.
9	DPHY_HS_IDLE_EN_REG	rw	ro	0x0	DPHY hs idle support enable. Quasi static.
15:10	RESERVED_15_10	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.432 CORE_DIG_RW_COMMON_10

Reg. 0x1C4A

Common configuration
access : read-write

bits	name	s/w	h/w	default	description
1:0	LANE0_CDROSC_CLK_SEL_GATING_REG	rw	ro	0x3	CDR-OSC lane 0 clock gating configuration. Quasi static.
3:2	LANE2_CDROSC_CLK_SEL_GATING_REG	rw	ro	0x3	CDR-OSC lane 2 clock gating configuration. Quasi static.
15:4	RESERVED_15_4	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.433 CORE_DIG_RW_COMMON_11

Reg. 0x1C4B

Common configuration
access : read-write

bits	name	s/w	h/w	default	description
0	LANE0_CDROSC_CLK_GATING_OVR_EN	rw	ro	0x0	CDR-OSC lane 0 clock gating override enable. Quasi static.
1	LANE0_CDROSC_CLK_GATING_OVR_VAL	rw	ro	0x0	CDR-OSC lane 0 clock gating override value. Quasi static.
2	LANE2_CDROSC_CLK_GATING_OVR_EN	rw	ro	0x0	CDR-OSC lane 2 clock gating override enable. Quasi static.
3	LANE2_CDROSC_CLK_GATING_OVR_VAL	rw	ro	0x0	CDR-OSC lane 2 clock gating override value. Quasi static.
15:4	RESERVED_15_4	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.434 CORE_DIG_RW_COMMON_12

Reg. 0x1C4C

Common configuration
access : read-write

bits	name	s/w	h/w	default	description
1:0	LANE0_DDL_OSC_SEL_GATING_REG	rw	ro	0x1	Analog lane 0 ddl osc clock gating configuration. Quasi static.
3:2	LANE1_DDL_OSC_SEL_GATING_REG	rw	ro	0x1	Analog lane 1 ddl osc clock gating configuration. Quasi static.
5:4	LANE2_DDL_OSC_SEL_GATING_REG	rw	ro	0x1	Analog lane 2 ddl osc clock gating configuration. Quasi static.
15:6	RESERVED_15_6	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.435 CORE_DIG_RW_COMMON_13

Reg. 0x1C4D

Common configuration
access : read-write

bits	name	s/w	h/w	default	description
0	LANE0_DDL_OSC_GATING_OVR_EN	rw	ro	0x0	Analog lane 0 ddl osc clock gating override enable. Quasi static.
1	LANE0_DDL_OSC_GATING_OVR_VAL	rw	ro	0x0	Analog lane 0 ddl osc clock gating override value. Quasi static.

2	LANE1_DDL_OSC_GATING_OVR_EN	rw	ro	0x0	Analog lane 1 ddl osc clock gating override enable. Quasi static.
3	LANE1_DDL_OSC_GATING_OVR_VAL	rw	ro	0x0	Analog lane 1 ddl osc clock gating override value. Quasi static.
4	LANE2_DDL_OSC_GATING_OVR_EN	rw	ro	0x0	Analog lane 2 ddl osc clock gating override enable. Quasi static.
5	LANE2_DDL_OSC_GATING_OVR_VAL	rw	ro	0x0	Analog lane 2 ddl osc clock gating override value. Quasi static.
15:6	RESERVED_15_6	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.436 CORE_DIG_RW_COMMON_14

Reg. 0x1C4E

Common configuration
access : read-write

bits	name	s/w	h/w	default	description
1:0	LANE0_HSTX_WORD_CLK_SEL_GATING_REG	rw	ro	0x3	Analog lane 0 Tx word clock gating configuration. Quasi static.
3:2	LANE1_HSTX_WORD_CLK_SEL_GATING_REG	rw	ro	0x3	Analog lane 1 Tx word clock gating configuration. Quasi static.
5:4	LANE2_HSTX_WORD_CLK_SEL_GATING_REG	rw	ro	0x3	Analog lane 2 Tx word clock gating configuration. Quasi static.
15:6	RESERVED_15_6	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.437 CORE_DIG_RW_COMMON_15

Reg. 0x1C4F

Common configuration
access : read-write

bits	name	s/w	h/w	default	description
0	LANE0_HSTX_WORD_CLK_GATING_OVR_EN	rw	ro	0x0	Analog lane 0 Tx word clock gating override enable. Quasi static.
1	LANE0_HSTX_WORD_CLK_GATING_OVR_VAL	rw	ro	0x0	Analog lane 0 Tx word clock gating override value. Quasi static.
2	LANE1_HSTX_WORD_CLK_GATING_OVR_EN	rw	ro	0x0	Analog lane 1 Tx word clock gating override enable. Quasi static.
3	LANE1_HSTX_WORD_CLK_GATING_OVR_VAL	rw	ro	0x0	Analog lane 1 Tx word clock gating override value. Quasi static.
4	LANE2_HSTX_WORD_CLK_GATING_OVR_EN	rw	ro	0x0	Analog lane 2 Tx word clock gating override enable. Quasi static.
5	LANE2_HSTX_WORD_CLK_GATING_OVR_VAL	rw	ro	0x0	Analog lane 2 Tx word clock gating override value. Quasi static.
15:6	RESERVED_15_6	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.439 CORE_DIG_ANACTRL_RW_COMMON_ANACTRL_0

Reg. 0x1CF0

Power on analog control configuration
access : read-write

bits	name	s/w	h/w	default	description
1:0	CB_DSK_CLK_MODE_CFG	rw	ro	0x1	Configuration of internal deskew clock source mode. This field is quasi-static.
7:2	CB_LP_DCO_EN_DLY	rw	ro	0x1B	Configurable delay from cb_lp_dco_pon to cb_lp_dco_en. Measured in Config clock cycles. This field is quasi-static.

13:8	CB_LP_DCO_CLK_EN_DLY	rw	ro	0x1B	Configurable delay from cb_lp_dco_pon to cb_lp_dco_clk_en. Measured in Config clock cycles. This field is quasi-static.
15:14	CB_CHOP_CLK_DIV_SEL	rw	ro	0x0	Select division factor for cb_chop_clk. This field is quasi-static. -2'd0: Division by 1 -2'd1: Division by 2 -2'd2: Division by 4 -2'd3: Not used

1.1.1.440 CORE_DIG_ANACTRL_RW_COMMON_ANACTRL_1

Reg. 0x1CF1

Power on analog control configuration
access : read-write

bits	name	s/w	h/w	default	description
5:0	CB_LP_DCO_CLK_EN_DLY	rw	ro	0x1B	Configurable delay from cb_lp_dco_pon to cb_lp_dco_fword_change. Measured in Config clock cycles. This field is quasi-static.
8:6	HSRX_DLY	rw	ro	0x2	Configurable delay from all lane?_hsrx_pon to all lane?_hsrx_*. Measured in Config clock cycles. This field is quasi-static.
15:9	RESERVED_15_9	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.441 CORE_DIG_ANACTRL_RW_COMMON_ANACTRL_2

Reg. 0x1CF2

Power on analog control configuration
access : read-write

bits	name	s/w	h/w	default	description
3:0	CB_HSTXLB_DCO_EN_DLY	rw	ro	0x4	Configurable delay from cb_hstxlb_dco_pon to cb_hstxlb_dco_en delay. Measured in Config clock cycles. This field is quasi-static.
7:4	CB_HSTXLB_DCO_CLK_EN_DLY	rw	ro	0x4	Configurable delay from cb_hstxlb_dco_pon to cb_hstxlb_dco_clk0/90_en. Measured in Config clock cycles. This field is quasi-static.
11:8	CB_HSTXLB_DCO_TUNE_CLKDIG_EN_DLY	rw	ro	0x4	Configurable delay from cb_hstxlb_dco_pon to cb_hstxlb_dco_tune_clkdig_en. Measured in Config clock cycles. This field is quasi-static.
12	GLOBAL_ULPS_OVR_EN	rw	ro	0x0	Global ULPS override enable. Active high. Used for debug purposes.
13	GLOBAL_ULPS_OVR_VAL	rw	ro	0x0	Global ULPS override value. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.442 CORE_DIG_ANACTRL_RW_COMMON_ANACTRL_3

Reg. 0x1CF3

Power on analog control configuration
access : read-write

bits	name	s/w	h/w	default	description
7:0	HSTX_DIV_EN_CNTR_DLY	rw	ro	0x4	Configurable delay from PHY_READY to hstx_div_en. Measured in Config clock cycles. This field is quasi-static.
15:8	HIBERNATE_DLY	rw	ro	0x4	Configurable delay for the deassertion of the clock gating signals in hibernate mode. Measured in Config clock cycles. This field is quasi-static.

1.1.1.444 CORE_DIG_COMMON_RW_DESKEW_FINE_MEM

Reg. 0x1FF0

DPHY deskew fine FSM state jumps programmability
access : read-write

bits	name	s/w	h/w	default	description
2:0	DESKEW_FINE_MEM_VALUE	rw	ro	0x0	Selects state value.
9:3	DESKEW_FINE_MEM_ADDR	rw	ro	0x0	Selects state address. Must be set to allow observability.
10	DESKEW_FINE_MEM_WR_EN	rw	ro	0x0	FSM programming write enable. Writes the content DESKEW_FINE_MEM_VALUE into address DESKEW_FINE_MEM_ADDR. Active high. Set to 1'b0 to allow observability of memory content without re-programming.
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.445 CORE_DIG_COMMON_R_DESKEW_FINE_MEM

Reg. 0x1FF1

DPHY deskew fine FSM state jumps observability
access : read-only

bits	name	s/w	h/w	default	description
2:0	DESKEW_FINE_MEM_VALUE	ro	ro	0x0	Memory contents of position defined by field DESKEW_FINE_MEM_ADDR.
15:3	RESERVED_15_3	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.447 PPI_RW_DPHY_LANE0_LBERT_0

Reg. 0x2000

DPHY loopback control
access : read-write

bits	name	s/w	h/w	default	description
3:0	LBERT_PM_MODE	rw	ro	0x0	Pattern matcher mode. This bus is quasi-static. - 4'b0000: pattern matcher disabled - 4'b0001: PRBS31 (x^31 + x^28 + 1) - 4'b0010: PRBS23 (x^23 + x^18 + 1) - 4'b0011: PRBS23 (x^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1) - 4'b0100: PRBS16 (x^16 + x^5 + x^4 + x^3 + 1) - 4'b0101: PRBS15 (x^15 + x^14 + 1) - 4'b0110: PRBS11 (x^11 + x^9 + 1) - 4'b0111: PRBS9 (x^9 + x^5 + 1) - 4'b1000: PRBS7 (x^7 + x^6 + 1) - 4'b1001: Custom 8 bit pattern - 4'b1010: DC balanced custom 8 bit pattern (pat[7:0], ~pat[7:0]) - all others reserved
4	LBERT_PM_START_OVR_VAL	rw	ro	0x0	Pattern matcher start override value. Used for debug purposes.
5	LBERT_PM_START_OVR_EN	rw	ro	0x0	Pattern matcher start override enable. Active high. Used for debug purposes.
6	LBERT_PM_SAMPLE_COUNTER_OVR_VAL	rw	ro	0x0	Pattern matcher error counter sampling override value. Used for debug purposes.
7	LBERT_PM_SAMPLE_COUNTER_OVR_EN	rw	ro	0x0	Pattern matcher error counter sampling override enable. Active high. Used for debug purposes.
11:8	LBERT_PG_MODE	rw	ro	0x0	Pattern generator mode. This bus is quasi-static. - 4'b0000: pattern generator disabled - 4'b0001: PRBS31 (x^31 + x^28 + 1) - 4'b0010: PRBS23 (x^23 + x^18 + 1) - 4'b0011: PRBS23 (x^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1) - 4'b0100: PRBS16 (x^16 + x^5 + x^4 + x^3 + 1) - 4'b0101: PRBS15 (x^15 + x^14 + 1) - 4'b0110: PRBS11 (x^11 + x^9 + 1) - 4'b0111: PRBS9 (x^9 + x^5 + 1) - 4'b1000: PRBS7 (x^7 + x^6 + 1) - 4'b1001: Custom 8 bit pattern - 4'b1010: DC balanced custom 8 bit pattern (pat[7:0], ~pat[7:0]) - all others reserved

12	LBERT_PG_START_OVR_VAL	rw	ro	0x0	Pattern generator start override value. Used for debug purposes.
13	LBERT_PG_START_OVR_EN	rw	ro	0x0	Pattern generator start override enable. Active high. Used for debug purposes.
14	LBERT_PG_ERROR_INJECTION	rw	ro	0x0	Injects 1 bit error on output pattern. Active high. Each rising edge inserts 1 error.
15	LBERT_PM_DATA_SWAP	rw	ro	0x0	Controls lane mux to choose normal or swapped data (actual reset value is 0xX)

1.1.1.448 PPI_RW_DPHY_LANE0_LBERT_1

Reg. 0x2001

DPHY loopback control
access : read-write

bits	name	s/w	h/w	default	description
7:0	LBERT_PG_USER_PATTERN	rw	ro	0x0	Custom 8 bit pattern. Requires LBERT_PG_MODE to be set to 4'b1001 or 4'b1010. This bus is quasi-static.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.449 PPI_R_DPHY_LANE0_LBERT_0

Reg. 0x2002

DPHY loopback observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	LBERT_PM_ERROR_COUNTER	ro	ro	0x1	Pattern matcher error counter. Readouts are valid after a rising edge on LBERT_PM_SAMPLE_COUNTER.

1.1.1.450 PPI_R_DPHY_LANE0_LBERT_1

Reg. 0x2003

DPHY loopback observability
access : read-only

bits	name	s/w	h/w	default	description
0	LBERT_PG_ENABLED	ro	ro	0x0	Pattern generator enable observability. Active high.
15:1	RESERVED_15_1	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.451 PPI_RW_DPHY_LANE0_SPARE

Reg. 0x2004

DPHY spare registers
access : read-write

bits	name	s/w	h/w	default	description
15:0	DPHY_LANE_0_SPARE	rw	ro	0x0	Spare registers for future use

1.1.1.453 PPI_RW_DPHY_LANE1_LBERT_0

Reg. 0x2200

DPHY loopback control
access : read-write

bits	name	s/w	h/w	default	description
3:0	LBERT_PM_MODE	rw	ro	0x0	Pattern matcher mode. This bus is quasi-static. - 4'b0000: pattern matcher disabled - 4'b0001: PRBS31 (x^31 + x^28 + 1) - 4'b0010: PRBS23 (x^23 + x^18 + 1) - 4'b0011: PRBS23 (x^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1) - 4'b0100: PRBS16 (x^16 + x^5 + x^4 + x^3 + 1) - 4'b0101: PRBS15 (x^15 + x^14 + 1) - 4'b0110: PRBS11 (x^11 + x^9 + 1) - 4'b0111: PRBS9 (x^9 + x^5 + 1) - 4'b1000: PRBS7 (x^7 + x^6 + 1)

					- 4'b1001: Custom 8 bit pattern - 4'b1010: DC balanced custom 8 bit pattern (pat[7:0], ~pat[7:0]) - all others reserved
4	LBERT_PM_START_OVR_VAL	rw	ro	0x0	Pattern matcher start override value. Used for debug purposes.
5	LBERT_PM_START_OVR_EN	rw	ro	0x0	Pattern matcher start override enable. Active high. Used for debug purposes.
6	LBERT_PM_SAMPLE_COUNTER_OVR_VAL	rw	ro	0x0	Pattern matcher error counter sampling override value. Used for debug purposes.
7	LBERT_PM_SAMPLE_COUNTER_OVR_EN	rw	ro	0x0	Pattern matcher error counter sampling override enable. Active high. Used for debug purposes.
11:8	LBERT_PG_MODE	rw	ro	0x0	Pattern generator mode. This bus is quasi-static. - 4'b0000: pattern generator disabled - 4'b0001: PRBS31 (x^31 + x^28 + 1) - 4'b0010: PRBS23 (x^23 + x^18 + 1) - 4'b0011: PRBS23 (x^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1) - 4'b0100: PRBS16 (x^16 + x^5 + x^4 + x^3 + 1) - 4'b0101: PRBS15 (x^15 + x^14 + 1) - 4'b0110: PRBS11 (x^11 + x^9 + 1) - 4'b0111: PRBS9 (x^9 + x^5 + 1) - 4'b1000: PRBS7 (x^7 + x^6 + 1) - 4'b1001: Custom 8 bit pattern - 4'b1010: DC balanced custom 8 bit pattern (pat[7:0], ~pat[7:0]) - all others reserved
12	LBERT_PG_START_OVR_VAL	rw	ro	0x0	Pattern generator start override value. Used for debug purposes.
13	LBERT_PG_START_OVR_EN	rw	ro	0x0	Pattern generator start override enable. Active high. Used for debug purposes.
14	LBERT_PG_ERROR_INJECTION	rw	ro	0x0	Injects 1 bit error on output pattern. Active high. Each rising edge inserts 1 error.
15	LBERT_PM_DATA_SWAP	rw	ro	0x0	Controls lane mux to choose normal or swapped data (actual reset value is 0xX)

1.1.1.454 PPI_RW_DPHY_LANE1_LBERT_1

Reg. 0x2201

DPHY loopback control
access : read-write

bits	name	s/w	h/w	default	description
7:0	LBERT_PG_USER_PATTERN	rw	ro	0x0	Custom 8 bit pattern. Requires LBERT_PG_MODE to be set to 4'b1001 or 4'b1010. This bus is quasi-static.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.455 PPI_R_DPHY_LANE1_LBERT_0

Reg. 0x2202

DPHY loopback observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	LBERT_PM_ERROR_COUNTER	ro	ro	0x1	Pattern matcher error counter. Readouts are valid after a rising edge on LBERT_PM_SAMPLE_COUNTER.

1.1.1.456 PPI_R_DPHY_LANE1_LBERT_1

Reg. 0x2203

DPHY loopback observability
access : read-only

bits	name	s/w	h/w	default	description
0	LBERT_PG_ENABLED	ro	ro	0x0	Pattern generator enable observability. Active high.
15:1	RESERVED_15_1	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.457 PPI_RW_DPHY_LANE1_SPARE

Reg. 0x2204

DPHY spare registers
access : read-write

bits	name	s/w	h/w	default	description
15:0	DPHY_LANE_1_SPARE	rw	ro	0x0	Spare registers for future use

1.1.1.459 CORE_DIG_DLANE_0_RW_CFG_0

Reg. 0x3000

DPHY lane configuration
access : read-write

bits	name	s/w	h/w	default	description
0	CFG_0_LP_PIN_SWAP_REG	rw	ro	0x0	Swap dp and dn lines. Applies to low power mode. This field is quasi-static. - 1'b0: positive on dp / negative on dn; - 1'b1: positive on dn / negative on dp;
1	CFG_0_HS_PIN_SWAP_REG	rw	ro	0x0	Swap dp and dn lines. Applies to high speed mode. This field is quasi-static. - 1'b0: positive on dp / negative on dn; - 1'b1: positive on dn / negative on dp;
2	LOOPBACK_MODE_EN	rw	ro	0x0	Primes the lane in loopback mode by enabling the LP-TX and LP-RX at the same time. Active high. This field is quasi-static.
15:3	RESERVED_15_3	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.460 CORE_DIG_DLANE_0_RW_CFG_1

Reg. 0x3001

DPHY lane configuration
access : read-write

bits	name	s/w	h/w	default	description
0	CFG_1_PREAMBLE_EN_REG	rw	ro	0x0	Enables support of data burst with preamble (DPHY specification 2.0 and above). Active high.
1	CFG_1_BACKWARDS_DESKEW_REG	rw	ro	0x0	Enables internal skew calibration for DPHY1.1 modes. Active high.
2	CFG_1_DESKEW_SUPPORTED_REG	rw	ro	0x0	Selects whether deskew bursts (DPHY specification 1.2 and above) with 16'hFFFF sync headers are supported. Active high.
3	CFG_1_SOT_DETECTION_REG	rw	ro	0x0	Selects whether start of transmission (SoT) soft error is flagged. Active high.
15:4	RESERVED_15_4	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.461 CORE_DIG_DLANE_0_RW_CFG_2

Reg. 0x3002

DPHY lane configuration
access : read-write

bits	name	s/w	h/w	default	description
15:0	CFG_2_SPARE	rw	ro	0x0	Spare registers for future use.

1.1.1.463 CORE_DIG_DLANE_0_RW_LP_0

Reg. 0x3040

Low power subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
3:0	LP_0_TTAGET_REG	rw	ro	0xC	BTA timing control. Defines the time that the new transmitter drives LP000 after taking control of the lines. Ttaget timer counter (resolution of 1/2 txclkesc period). This

					field is quasi-static. Effective timer size is LP_0_TTAGET - LP_0_TTASURE
7:4	LP_0_TTASURE_REG	rw	ro	0x3	BTA timing control. Defines the time that the new transmitter waits, after the LP10 state before driving LP00. Tta-sure timer counter (resolution of 1/2 txclkesc period). This field is quasi-static.
11:8	LP_0_TTAGO_REG	rw	ro	0x6	BTA timing control. Defines the time that the transmitter drives LP00 before releasing control of the lines. Tta-go timer counter (resolution of 1/2 txclkesc period). This field is quasi-static.
15:12	LP_0_ITMINRX_REG	rw	ro	0x4	LP-RX pulse filter width (in dco_clk cycles). Used to reject pulses smaller than the desired size. This field is quasi-static.

1.1.1.464 CORE_DIG_DLANE_0_RW_LP_1

Reg. 0x3041

Low power subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	LP_1_ERRCONTENTION_THRES_REG	rw	ro	0x10	Error contention detection filter size (in dco_clk cycles). Defines the time that the system tolerates contention before asserting errcontentionlp* flags. This field is quasi-static.
15:8	LP_1_LPTX_PON_TIMER_REG	rw	ro	0x80	LP-TX power on timer (in txclkesc cycles). Defines the time when switching from the ULP pull down back to the LP-TX driver. This field is quasi-static.

1.1.1.465 CORE_DIG_DLANE_0_RW_LP_2

Reg. 0x3042

Low power subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
0	LP_2_FILTER_INPUT_SAMPLING_REG	rw	ro	0x1	LPRX filter input data sampling
15:1	RESERVED_15_1	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.467 CORE_DIG_DLANE_0_R_LP_0

Reg. 0x3050

Low power subsystem status
access : read-only

bits	name	s/w	h/w	default	description
0	LP_0_HSACTIVERX	ro	ro	0x0	Signal which indicates that the HS entry transition LP01 -> LP00 has been observed. Active high.
1	LP_0_RXHSRQST	ro	ro	0x0	Signal which indicates that the HS entry transition LP11 -> LP01 has been observed. Active high.
15:2	RESERVED_15_2	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.468 CORE_DIG_DLANE_0_R_LP_1

Reg. 0x3051

Low power subsystem status
access : read-only

bits	name	s/w	h/w	default	description
3:0	LP_1_STATE_BTA	ro	ro	0x0	BTA FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion.
7:4	LP_1_STATE_LPRX	ro	ro	0x0	LP-RX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion.
12:8	LP_1_STATE_LPTX	ro	ro	0x0	LP-TX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion.
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.470 CORE_DIG_DLANE_0_R_HS_TX_0

Reg. 0x3070

High speed TX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
3:0	STATE_DHSTX	ro	ro	0x0	HS-TX word clock FSM state
7:4	STATE_DCO_DHSTX	ro	ro	0x0	HS-TX DCO clock FSM state
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.472 CORE_DIG_DLANE_0_RW_HS_RX_0

Reg. 0x3080

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_RX_0_TCLKSETTLE_REG	rw	ro	0x1D	DPHY Tclk-settle timer counter (dco_clk cycles). Defines the time interval between the detection of the LP01 -> LP00 transition and the enabling of the reception logic
15:8	HS_RX_0_THSSETTLE_REG	rw	ro	0x9	DPHY Ths-settle timer counter (dco_clk cycles). Defines the time interval between the detection of the LP01 -> LP00 transition and the enabling of the HS data path.

1.1.1.473 CORE_DIG_DLANE_0_RW_HS_RX_1

Reg. 0x3081

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_RX_1_FILTER_SIZE_DESKEW_REG	rw	ro	0x10	Deskew algorithm filter size (word clock cycles). Corresponds to the number of samples used to assess the quality of a phase setting.
15:8	HS_RX_1_FILTER_SIZE_SKEWCAL_REG	rw	ro	0x40	Skew calibration algorithm filter size (word_clk cycles). Corresponds to the number of samples used to assess the quality of a phase setting.

1.1.1.474 CORE_DIG_DLANE_0_RW_HS_RX_2

Reg. 0x3082

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
2:0	HS_RX_2_LATENCY_DESKEW_REG	rw	ro	0x3	Number of cycles to wait for to account for the AFE's latency during deskew (word clock cycles)
4:3	HS_RX_2_LATENCY_SKEWCAL_REG	rw	ro	0x3	Number of cycles to wait for to account for the AFE's latency during skew calibration (word clock cycles)
6:5	HS_RX_2_JUMP2STEPS_SKEWCAL_REG	rw	ro	0x0	How many phase settings to jump after detecting the edge during skew calibration algorithm
7	HS_RX_2_POLARITY_SKEWCAL_REG	rw	ro	0x1	Inverts the data from the AFE's polarity during skew calibration. (Active high)
8	HS_RX_2_RECAL_SKEWCAL_REG	rw	ro	0x0	Signal used to trigger a skew recalibration. (Active high)
9	HS_RX_2_UPDATE_SETTINGS_DESKEW_REG	rw	ro	0x1	Signal used to update the deskew algorithm's settings (Active high)
10	HS_RX_2_UPDATE_SETTINGS_SKEWCAL_REG	rw	ro	0x1	Signal used to update the skew calibration algorithm's settings (Active high)
11	HS_RX_2_IGNORE_ALTERNCAL_REG	rw	ro	0x0	Signal used to ignore alternate calibration patterns. (Active high)
12	HS_RX_2_ROUNDUP_DESKEW_REG	rw	ro	0x1	Selects whether to average the final calibration result up (Active high)
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.475 CORE_DIG_DLANE_0_RW_HS_RX_3

Reg. 0x3083

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
3:0	HS_RX_3_STEP_SIZE_DESKEW_REG	rw	ro	0x2	Size of the deskew algorithm's phase settings step.
9:4	HS_RX_3_FJUMP_DESKEW_REG	rw	ro	0x1	After detecting the left edge this bus selects how many phases to jump during the deskew algorithm. In phase steps.
12:10	HS_RX_3_SHIFT_STEP_DESKEW_REG	rw	ro	0x1	Shift step size for fine calibration of the deskew algorithm. In phase steps.
15:13	HS_RX_3_SHRINK_STEP_DESKEW_REG	rw	ro	0x1	Shrink step size for fine calibration of the deskew algorithm. In phase steps.

1.1.1.476 CORE_DIG_DLANE_0_RW_HS_RX_4

Reg. 0x3084

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_RX_4_MAX_ITERATIONS_DESKEW_REG	rw	ro	0x96	Maximum number of iterations of the deskew algorithm (word_clk cycles)

1.1.1.477 CORE_DIG_DLANE_0_RW_HS_RX_5

Reg. 0x3085

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
10:0	HS_RX_5_DDL_LEFT_INIT_REG	rw	ro	0x0	Initial DDL setting for the left pointer of the deskew algorithm
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.478 CORE_DIG_DLANE_0_RW_HS_RX_6

Reg. 0x3086

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
10:0	HS_RX_6_MIN_EYE_OPENING_DESKEW_REG	rw	ro	0x2D	Minimum eye opening after deskew algorithm is complete not to flag an error. Used to obtain error information. (in DDL steps)
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.479 CORE_DIG_DLANE_0_RW_HS_RX_7

Reg. 0x3087

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_RX_7_TCLKMISS_REG	rw	ro	0x6	Tclkmiss timer counter (dco_clk cycles). Defines the minimum time with absence of clock before flagging clock miss. This field is quasi-static.
8	HS_RX_7_INVORDER_RX_REG	rw	ro	0x1	Signal used to invert MSB to LSB reception order (Active high). This field is quasi-static.
9	HS_RX_7_INITIAL_CALIBRATION_REG	rw	ro	0x1	Select deskew initial calibration (Active high) If 0 triggers a periodic calibration.
10	HS_RX_7_THSEXIT_MIN_REG	rw	ro	0x0	Controls lane aligner. Used for lower bitrates if bursts received have minimum Ths-exit. This field is quasi-static.

12:11	HS_RX_7_DESKEW_CNF_REG	rw	ro	0x3	Deskew pattern length configuration for aligner's pattern search. Used for debug purposes. This field is quasi-static. - 2'b00 - Minimum deskew pattern length of 10 bits - 2'b01 - Minimum deskew pattern length of 12 bits - 2'b10 - Minimum deskew pattern length of 14 bits - 2'b11 - Minimum deskew pattern length of 16 bits (default)
13	HS_RX_7_DESKEW_AUTO_ALGO_SEL_REG	rw	ro	0x1	Select manual or automatic deskew algorithm selection. - 1'b0 - Manual control of the algorithm. HS_RX_7_INITIAL_CALIBRATION_REG selects whether to run an initial calibration or a fine calibration. - 1'b1 - Automatic control of the algorithm. After the first successful initial calibration always run a fine one.
14	HS_RX_7_DESKEW_REARM_INITIAL_REG	rw	ro	0x0	Allows running an initial calibration after a previous successful one when in automatic mode. This feature shall be used in continuous clock mode.
15	HS_RX_7_SELECT_ALTERNATE_ALGO_REG	rw	ro	0x0	Selects which algorithm is triggered by the alternate calibration pattern. - 1'b0 - Triggers coarse calibration - 1'b1 - Triggers fine calibration

1.1.1.480 CORE_DIG_DLANE_0_RW_HS_RX_8

Reg. 0x3088

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
0	HS_RX_8_FILTER_DITHERING_EN_REG	rw	ro	0x0	Enable dithering to the deskew algorithm's filter size (Active high)
8:1	HS_RX_8_START_DELAY_REG	rw	ro	0x0	Selects an initial delay for the deskew algorithm (word_clk cycles)
9	HS_ALIGN_BYPASS_REG	rw	ro	0x0	Bypasses alignment and sync detection.
15:10	RESERVED_15_10	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.481 CORE_DIG_DLANE_0_RW_HS_RX_9

Reg. 0x3089

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
10:0	HS_RX_9_PHASE_BOUND_REG	rw	ro	0xFF	Maximum phase allowed during Deskew algorithm
11	HS_RX_9_EQUALIZATION_RESTORE_COARSE_VALUES_REG	rw	ro	0x0	Restore deskew coarse calibration results at the beginning of each fine tuning calibration. This field is quasi-static.
12	HS_RX_9_EQUALIZATION_BYPASS_FSM_STATES_REG	rw	ro	0x0	Bypass certain states of the fine tuning algorithm FSM. This field is quasi-static.
13	HS_RX_9_EQUALIZATION_ENABLE_REG	rw	ro	0x0	Enables RX Equalization for deskew fine tuning algorithm. This field is quasi-static.
14	HS_RX_9_EQUALIZATION_DIVIDE_FILTER_SIZE_REG	rw	ro	0x0	Divide filter size maximum value by 4 for deskew fine tuning algorithm. This field is quasi-static.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.482 CORE_DIG_DLANE_0_RW_HS_RX_10

Reg. 0x308A

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
10:0	HS_RX_10_DDL_MID_INIT_REG	rw	ro	0x1	Initial DDL setting for the mid pointer of the deskew algorithm

15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.483 CORE_DIG_DLANE_0_RW_HS_RX_11

Reg. 0x308B

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
10:0	HS_RX_11_DDL_RIGHT_INIT_REG	rw	ro	0x2	Initial DDL setting for the right pointer of the deskew algorithm
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.484 CORE_DIG_DLANE_0_RW_HS_RX_12

Reg. 0x308C

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_RX_12_WINDOW_SIZE_DESKEW_REG	rw	ro	0x3	Used by the deskew algorithm; Consists of the number of consecutive good settings needed to detect the left edge. Used to prevent false edge detection (word clock cycles)
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.486 CORE_DIG_DLANE_0_R_HS_RX_0

Reg. 0x3090

High speed RX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
0	DESKEWCALDONE	ro	ro	0x0	Signals that the skew calibration has completed. (Active high)
1	DESKEWCALFAILED	ro	ro	0x0	Signals a skew calibration with errors (Active high)
9:2	DESKEW_CAL_STATUS	ro	ro	0x0	Bus with status information of the deskew algorithm. - [0] - signals that the deskew algorithm has finished; - [1] - signals that an initial calibration has finished successfully; - [2] - signals that an initial calibration has finished with an unsatisfactory eye size; - [3] - signals that an initial calibration has failed; - [4] - signals that a fine calibration has finished with convergence; - [5] - signals that a fine calibration ran out of time but found a new best setting; - [6] - signals that a fine calibration ran out of time with no best setting; - [7] - signals that during either calibration the phase setting went out of bounds.
15:10	RESERVED_15_10	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.487 CORE_DIG_DLANE_0_R_HS_RX_1

Reg. 0x3091

High speed RX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
15:0	DESKEWCALTIME	ro	ro	0x0	Bus containing information on how many cycles the deskew calibration took (word_clk cycles)

1.1.1.488 CORE_DIG_DLANE_0_R_HS_RX_2

Reg. 0x3092

High speed RX subsystem status
access : read-only

bits	name	s/w	h/w	default	description

7:0	DESKEW_STATE	ro	ro	0xA0	Deskew algorithm FSM's state
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.489 CORE_DIG_DLANE_0_R_HS_RX_3

Reg. 0x3093

High speed RX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
3:0	DESKEW_PREV_ACTION	ro	ro	0x0	Deskew algorithm previous action
4	DESKEW_PREV_RESULT	ro	ro	0x0	Deskew algorithm previous action's result
8:5	DESKEW_CURR_ACTION	ro	ro	0x0	Deskew algorithm current action
9	DESKEW_FAILED_LEFT	ro	ro	0x0	Result of the deskew algorithm left pointers' comparison
10	DESKEW_FAILED_RIGHT	ro	ro	0x0	Result of the deskew algorithm right pointers' comparison
11	DESKEW_ALL_DIFF	ro	ro	0x0	Result of the deskew algorithm three pointers' comparison
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.490 CORE_DIG_DLANE_0_R_HS_RX_4

Reg. 0x3094

High speed RX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
7:0	EDGE1POINTER_SKEWCAL	ro	ro	0x0	Skewcal algorithm's first edge
15:8	EDGE2POINTER_SKEWCAL	ro	ro	0x0	Skewcal algorithm's second edge

1.1.1.492 CORE_DIG_DLANE_0_RW_HS_TX_0

Reg. 0x3100

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_0_THSTRAIL_REG	rw	ro	0x9	Tclk-trail/Ths-trail setting (word clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.493 CORE_DIG_DLANE_0_RW_HS_TX_1

Reg. 0x3101

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_1_THSZERO_REG	rw	ro	0x20	Tclk-zero/Ths-zero setting (word clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.494 CORE_DIG_DLANE_0_RW_HS_TX_2

Reg. 0x3102

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_2_TCLKPRE_REG	rw	ro	0x3	Tclk-pre setting (word clock cycles). Clock lane related. This field is quasi-static. Please check table for more details.

1.1.1.495 CORE_DIG_DLANE_0_RW_HS_TX_3

Reg. 0x3103

High speed TX subsystem parameters control

access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_TX_3_TLPTXOVERLAP_REG	rw	ro	0x6	LP-TX/HS-TX drivers enable overlap (DCO clock cycles). This field is quasi-static. Please check table for more details.
8	HS_TX_3_INVORDER_TX_REG	rw	ro	0x0	Invert TX data's MSB to LSB transmission order. Active high. This field is quasi-static.
9	HS_TX_3_STATE_OVR_EN_REG	rw	ro	0x0	HS-TX FSM state (word clock) override enable. Active high. Used for debug purposes.
13:10	HS_TX_3_STATE_OVR_REG	rw	ro	0x0	HS-TX FSM state (word clock) override value. Used for debug purposes.
14	HS_TX_3_HSDIRECT_REG	rw	ro	0x0	Reserved.
15	HS_TX_3_PIN_SWAP_REG	rw	ro	0x0	Swap dp and dn lines. Applies to high speed mode. This field is quasi-static. - 1'b0: positive on dp / negative on dn; - 1'b1: positive on dn / negative on dp;

1.1.1.496 CORE_DIG_DLANE_0_RW_HS_TX_4

Reg. 0x3104

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_4_TLPX_DCO_REG	rw	ro	0x7	Tlpx value (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.497 CORE_DIG_DLANE_0_RW_HS_TX_5

Reg. 0x3105

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_5_THSTRAIL_DCO_REG	rw	ro	0x7	Tclk-trail/Ths-trail value (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.498 CORE_DIG_DLANE_0_RW_HS_TX_6

Reg. 0x3106

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_6_TLP11END_DCO_REG	rw	ro	0xA	HS2LP final LP11 setting (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.499 CORE_DIG_DLANE_0_RW_HS_TX_7

Reg. 0x3107

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
8:0	HS_TX_7_ALTCALSEED_REG	rw	ro	0xFF	Alternate calibration PRBS seed. Used for debug purposes.
9	HS_TX_7_STATE_DCO_OVR_EN_REG	rw	ro	0x0	HS-TX FSM state (DCO clock) override enable. Active high. Used for debug purposes.
13:10	HS_TX_7_STATE_DCO_OVR_VAL_REG	rw	ro	0x0	HS-TX FSM state (DCO clock) override value. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.500 CORE_DIG_DLANE_0_RW_HS_TX_8

Reg. 0x3108

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_8_TCLKPOST_REG	rw	ro	0x1C	Tclk-post setting (word clock cycles). Clock lane related. This field is quasi-static. Please check table for more details.

1.1.1.501 CORE_DIG_DLANE_0_RW_HS_TX_9

Reg. 0x3109

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_9_THSPRPR_DCO_REG	rw	ro	0xA	Tclk-prepare/Ths-prepare setting (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.502 CORE_DIG_DLANE_0_RW_HS_TX_10

Reg. 0x310A

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_10_TLP11INIT_DCO_REG	rw	ro	0xA	LP2HS initial LP11 setting (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.503 CORE_DIG_DLANE_0_RW_HS_TX_11

Reg. 0x310B

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_11_TPREAMBLE_REG	rw	ro	0x7	Reserved.

1.1.1.504 CORE_DIG_DLANE_0_RW_HS_TX_12

Reg. 0x310C

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_12_THSEXIT_DCO_REG	rw	ro	0x14	Ths-exit setting (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.506 CORE_DIG_DLANE_1_RW_CFG_0

Reg. 0x3200

DPHY lane configuration
access : read-write

bits	name	s/w	h/w	default	description
0	CFG_0_LP_PIN_SWAP_REG	rw	ro	0x0	Swap dp and dn lines. Applies to low power mode. This field is quasi-static. - 1'b0: positive on dp / negative on dn; - 1'b1: positive on dn / negative on dp;
1	CFG_0_HS_PIN_SWAP_REG	rw	ro	0x0	Swap dp and dn lines. Applies to high speed mode. This field is quasi-static. - 1'b0: positive on dp / negative on dn; - 1'b1: positive on dn / negative on dp;
2	LOOPBACK_MODE_EN	rw	ro	0x0	Primes the lane in loopback mode by enabling the LP-TX and LP-RX at the same time. Active high. This field is quasi-static.
15:3	RESERVED_15_3	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.507 CORE_DIG_DLANE_1_RW_CFG_1

Reg. 0x3201

DPHY lane configuration

access : read-write

bits	name	s/w	h/w	default	description
0	CFG_1_PREAMBLE_EN_REG	rw	ro	0x0	Enables support of data burst with preamble (DPHY specification 2.0 and above). Active high.
1	CFG_1_BACKWARDS_DESKEW_REG	rw	ro	0x0	Enables internal skew calibration for DPHY1.1 modes. Active high.
2	CFG_1_DESKEW_SUPPORTED_REG	rw	ro	0x0	Selects whether deskew bursts (DPHY specification 1.2 and above) with 16'hFFFF sync headers are supported. Active high.
3	CFG_1_SOT_DETECTION_REG	rw	ro	0x0	Selects whether start of transmission (SoT) soft error is flagged. Active high.
15:4	RESERVED_15_4	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.508 CORE_DIG_DLANE_1_RW_CFG_2

Reg. 0x3202

DPHY lane configuration
access : read-write

bits	name	s/w	h/w	default	description
15:0	CFG_2_SPARE	rw	ro	0x0	Spare registers for future use.

1.1.1.510 CORE_DIG_DLANE_1_RW_LP_0

Reg. 0x3240

Low power subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
3:0	LP_0_TTAGET_REG	rw	ro	0xC	BTA timing control. Defines the time that the new transmitter drives LP000 after taking control of the lines. Tta-get timer counter (resolution of 1/2 txclkesc period). This field is quasi-static. Effective timer size is LP_0_TTAGET - LP_0_TTASURE
7:4	LP_0_TTASURE_REG	rw	ro	0x3	BTA timing control. Defines the time that the new transmitter waits, after the LP10 state before driving LP00. Tta-sure timer counter (resolution of 1/2 txclkesc period). This field is quasi-static.
11:8	LP_0_TTAGO_REG	rw	ro	0x6	BTA timing control. Defines the time that the transmitter drives LP00 before releasing control of the lines. Tta-go timer counter (resolution of 1/2 txclkesc period). This field is quasi-static.
15:12	LP_0_ITMINRX_REG	rw	ro	0x4	LP-RX pulse filter width (in dco_clk cycles). Used to reject pulses smaller than the desired size. This field is quasi-static.

1.1.1.511 CORE_DIG_DLANE_1_RW_LP_1

Reg. 0x3241

Low power subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	LP_1_ERRCONTENTION_THRES_REG	rw	ro	0x10	Error contention detection filter size (in dco_clk cycles). Defines the time that the system tolerates contention before asserting errcontentionlp* flags. This field is quasi-static.
15:8	LP_1_LPTX_PON_TIMER_REG	rw	ro	0x80	LP-TX power on timer (in txclkesc cycles). Defines the time when switching from the ULP pull down back to the LP-TX driver. This field is quasi-static.

1.1.1.512 CORE_DIG_DLANE_1_RW_LP_2

Reg. 0x3242

Low power subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
0	LP_2_FILTER_INPUT_SAMPLING_REG	rw	ro	0x1	LPRX filter input data sampling

15:1	RESERVED_15_1	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.514 CORE_DIG_DLANE_1_R_LP_0

Reg. 0x3250

Low power subsystem status
access : read-only

bits	name	s/w	h/w	default	description
0	LP_0_HSACTIVERX	ro	ro	0x0	Signal which indicates that the HS entry transition LP01 -> LP00 has been observed. Active high.
1	LP_0_RXHSRQST	ro	ro	0x0	Signal which indicates that the HS entry transition LP11 -> LP01 has been observed. Active high.
15:2	RESERVED_15_2	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.515 CORE_DIG_DLANE_1_R_LP_1

Reg. 0x3251

Low power subsystem status
access : read-only

bits	name	s/w	h/w	default	description
3:0	LP_1_STATE_BTA	ro	ro	0x0	BTA FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion.
7:4	LP_1_STATE_LPRX	ro	ro	0x0	LP-RX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion.
12:8	LP_1_STATE_LPTX	ro	ro	0x0	LP-TX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion.
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.517 CORE_DIG_DLANE_1_R_HS_TX_0

Reg. 0x3270

High speed TX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
3:0	STATE_DHSTX	ro	ro	0x0	HS-TX word clock FSM state
7:4	STATE_DCO_DHSTX	ro	ro	0x0	HS-TX DCO clock FSM state
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.519 CORE_DIG_DLANE_1_RW_HS_RX_0

Reg. 0x3280

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_RX_0_TCLKSETTLE_REG	rw	ro	0x1D	DPHY Tclk-settle timer counter (dco_clk cycles). Defines the time interval between the detection of the LP01 -> LP00 transition and the enabling of the reception logic
15:8	HS_RX_0_THSSETTLE_REG	rw	ro	0x9	DPHY Ths-settle timer counter (dco_clk cycles). Defines the time interval between the detection of the LP01 -> LP00 transition and the enabling of the HS data path.

1.1.1.520 CORE_DIG_DLANE_1_RW_HS_RX_1

Reg. 0x3281

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_RX_1_FILTER_SIZE_DESKEW_REG	rw	ro	0x10	Deskew algorithm filter size (word clock cycles). Corresponds to the number of samples used to assess the quality of a phase setting.

15:8	HS_RX_1_FILTER_SIZE_SKEWCAL_REG	rw	ro	0x40	Skew calibration algorithm filter size (word_clk cycles). Corresponds to the number of samples used to assess the quality of a phase setting.

1.1.1.521 CORE_DIG_DLANE_1_RW_HS_RX_2

Reg. 0x3282

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
2:0	HS_RX_2_LATENCY_DESKEW_REG	rw	ro	0x3	Number of cycles to wait for to account for the AFE's latency during deskew (word clock cycles)
4:3	HS_RX_2_LATENCY_SKEWCAL_REG	rw	ro	0x3	Number of cycles to wait for to account for the AFE's latency during skew calibration (word clock cycles)
6:5	HS_RX_2_JUMP2STEPS_SKEWCAL_REG	rw	ro	0x0	How many phase settings to jump after detecting the edge during skew calibration algorithm
7	HS_RX_2_POLARITY_SKEWCAL_REG	rw	ro	0x1	Inverts the data from the AFE's polarity during skew calibration. (Active high)
8	HS_RX_2_RECAL_SKEWCAL_REG	rw	ro	0x0	Signal used to trigger a skew recalibration. (Active high)
9	HS_RX_2_UPDATE_SETTINGS_DESKEW_REG	rw	ro	0x1	Signal used to update the deskew algorithm's settings (Active high)
10	HS_RX_2_UPDATE_SETTINGS_SKEWCAL_REG	rw	ro	0x1	Signal used to update the skew calibration algorithm's settings (Active high)
11	HS_RX_2_IGNORE_ALTERNCAL_REG	rw	ro	0x0	Signal used to ignore alternate calibration patterns. (Active high)
12	HS_RX_2_ROUNDUP_DESKEW_REG	rw	ro	0x1	Selects whether to average the final calibration result up (Active high)
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.522 CORE_DIG_DLANE_1_RW_HS_RX_3

Reg. 0x3283

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
3:0	HS_RX_3_STEP_SIZE_DESKEW_REG	rw	ro	0x2	Size of the deskew algorithm's phase settings step.
9:4	HS_RX_3_FJUMP_DESKEW_REG	rw	ro	0x1	After detecting the left edge this bus selects how many phases to jump during the deskew algorithm. In phase steps.
12:10	HS_RX_3_SHIFT_STEP_DESKEW_REG	rw	ro	0x1	Shift step size for fine calibration of the deskew algorithm. In phase steps.
15:13	HS_RX_3_SHRINK_STEP_DESKEW_REG	rw	ro	0x1	Shrink step size for fine calibration of the deskew algorithm. In phase steps.

1.1.1.523 CORE_DIG_DLANE_1_RW_HS_RX_4

Reg. 0x3284

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_RX_4_MAX_ITERATIONS_DESKEW_REG	rw	ro	0x96	Maximum number of iterations of the deskew algorithm (word_clk cycles)

1.1.1.524 CORE_DIG_DLANE_1_RW_HS_RX_5

Reg. 0x3285

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description

10:0	HS_RX_5_DDL_LEFT_INIT_REG	rw	ro	0x0	Initial DDL setting for the left pointer of the deskew algorithm
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.525 CORE_DIG_DLANE_1_RW_HS_RX_6

Reg. 0x3286

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
10:0	HS_RX_6_MIN_EYE_OPENING_DESKEW_REG	rw	ro	0x2D	Minimum eye opening after deskew algorithm is complete not to flag an error. Used to obtain error information. (in DDL steps)
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.526 CORE_DIG_DLANE_1_RW_HS_RX_7

Reg. 0x3287

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_RX_7_TCLKMISS_REG	rw	ro	0x6	Tclkmiss timer counter (dco_clk cycles). Defines the minimum time with absence of clock before flagging clock miss. This field is quasi-static.
8	HS_RX_7_INVORDER_RX_REG	rw	ro	0x1	Signal used to invert MSB to LSB reception order (Active high). This field is quasi-static.
9	HS_RX_7_INITIAL_CALIBRATION_REG	rw	ro	0x1	Select deskew initial calibration (Active high) If 0 triggers a periodic calibration.
10	HS_RX_7_THSEXIT_MIN_REG	rw	ro	0x0	Controls lane aligner. Used for lower bitrates if bursts received have minimum Ths-exit. This field is quasi-static.
12:11	HS_RX_7_DESKEW_CNF_REG	rw	ro	0x3	Deskew pattern length configuration for aligner's pattern search. Used for debug purposes. This field is quasi-static. - 2'b00 - Minimum deskew pattern length of 10 bits - 2'b01 - Minimum deskew pattern length of 12 bits - 2'b10 - Minimum deskew pattern length of 14 bits - 2'b11 - Minimum deskew pattern length of 16 bits (default)
13	HS_RX_7_DESKEW_AUTO_ALGO_SEL_REG	rw	ro	0x1	Select manual or automatic deskew algorithm selection. - 1'b0 - Manual control of the algorithm. HS_RX_7_INITIAL_CALIBRATION_REG selects whether to run an initial calibration or a fine calibration. - 1'b1 - Automatic control of the algorithm. After the first successful initial calibration always run a fine one.
14	HS_RX_7_DESKEW_REARM_INITIAL_REG	rw	ro	0x0	Allows running an initial calibration after a previous successful one when in automatic mode. This feature shall be used in continuous clock mode.
15	HS_RX_7_SELECT_ALTERNATE_ALGO_REG	rw	ro	0x0	Selects which algorithm is triggered by the alternate calibration pattern. - 1'b0 - Triggers coarse calibration - 1'b1 - Triggers fine calibration

1.1.1.527 CORE_DIG_DLANE_1_RW_HS_RX_8

Reg. 0x3288

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
0	HS_RX_8_FILTER_DITHERING_EN_REG	rw	ro	0x0	Enable dithering to the deskew algorithm's filter size (Active high)
8:1	HS_RX_8_START_DELAY_REG	rw	ro	0x0	Selects an initial delay for the deskew algorithm (word_clk cycles)
9	HS_ALIGN_BYPASS_REG	rw	ro	0x0	Bypasses alignment and sync detection.
15:10	RESERVED_15_10	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.528 CORE_DIG_DLANE_1_RW_HS_RX_9

Reg. 0x3289

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
10:0	HS_RX_9_PHASE_BOUND_REG	rw	ro	0xFF	Maximum phase allowed during Deskew algorithm
11	HS_RX_9_EQUALIZATION_RESTORE_COARSE_VALUES_REG	rw	ro	0x0	Restore deskew coarse calibration results at the beginning of each fine tuning calibration. This field is quasi-static.
12	HS_RX_9_EQUALIZATION_BYPASS_FSM_STATES_REG	rw	ro	0x0	Bypass certain states of the fine tuning algorithm FSM. This field is quasi-static.
13	HS_RX_9_EQUALIZATION_ENABLE_REG	rw	ro	0x0	Enables RX Equalization for deskew fine tuning algorithm. This field is quasi-static.
14	HS_RX_9_EQUALIZATION_DIVIDE_FILTER_SIZE_REG	rw	ro	0x0	Divide filter size maximum value by 4 for deskew fine tuning algorithm. This field is quasi-static.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.529 CORE_DIG_DLANE_1_RW_HS_RX_10

Reg. 0x328A

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
10:0	HS_RX_10_DDL_MID_INIT_REG	rw	ro	0x1	Initial DDL setting for the mid pointer of the deskew algorithm
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.530 CORE_DIG_DLANE_1_RW_HS_RX_11

Reg. 0x328B

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
10:0	HS_RX_11_DDL_RIGHT_INIT_REG	rw	ro	0x2	Initial DDL setting for the right pointer of the deskew algorithm
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.531 CORE_DIG_DLANE_1_RW_HS_RX_12

Reg. 0x328C

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_RX_12_WINDOW_SIZE_DESKEW_REG	rw	ro	0x3	Used by the deskew algorithm; Consists of the number of consecutive good settings needed to detect the left edge. Used to prevent false edge detection (word clock cycles)
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.533 CORE_DIG_DLANE_1_R_HS_RX_0

Reg. 0x3290

High speed RX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
0	DESKEWCALDONE	ro	ro	0x0	Signals that the skew calibration has completed. (Active high)
1	DESKEWCALFAILED	ro	ro	0x0	Signals a skew calibration with errors (Active high)

9:2	DESKEW_CAL_STATUS	ro	ro	0x0	Bus with status information of the deskew algorithm. - [0] - signals that the deskew algorithm has finished; - [1] - signals that an initial calibration has finished successfully; - [2] - signals that an initial calibration has finished with an unsatisfactory eye size; - [3] - signals that an initial calibration has failed; - [4] - signals that a fine calibration has finished with convergence; - [5] - signals that a fine calibration ran out of time but found a new best setting; - [6] - signals that a fine calibration ran out of time with no best setting; - [7] - signals that during either calibration the phase setting went out of bounds.
15:10	RESERVED_15_10	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.534 CORE_DIG_DLANE_1_R_HS_RX_1

Reg. 0x3291

High speed RX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
15:0	DESKEWCALTIME	ro	ro	0x0	Bus containing information on how many cycles the deskew calibration took (word_clk cycles)

1.1.1.535 CORE_DIG_DLANE_1_R_HS_RX_2

Reg. 0x3292

High speed RX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
7:0	DESKEW_STATE	ro	ro	0xA0	Deskew algorithm FSM's state
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.536 CORE_DIG_DLANE_1_R_HS_RX_3

Reg. 0x3293

High speed RX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
3:0	DESKEW_PREV_ACTION	ro	ro	0x0	Deskew algorithm previous action
4	DESKEW_PREV_RESULT	ro	ro	0x0	Deskew algorithm previous action's result
8:5	DESKEW_CURR_ACTION	ro	ro	0x0	Deskew algorithm current action
9	DESKEW_FAILED_LEFT	ro	ro	0x0	Result of the deskew algorithm left pointers' comparison
10	DESKEW_FAILED_RIGHT	ro	ro	0x0	Result of the deskew algorithm right pointers' comparison
11	DESKEW_ALL_DIFF	ro	ro	0x0	Result of the deskew algorithm three pointers' comparison
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.537 CORE_DIG_DLANE_1_R_HS_RX_4

Reg. 0x3294

High speed RX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
7:0	EDGE1POINTER_SKEWCAL	ro	ro	0x0	Skewcal algorithm's first edge
15:8	EDGE2POINTER_SKEWCAL	ro	ro	0x0	Skewcal algorithm's second edge

1.1.1.539 CORE_DIG_DLANE_1_RW_HS_TX_0

Reg. 0x3300

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_0_THSTRAIL_REG	rw	ro	0x9	Tclk-trail/Ths-trail setting (word clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.540 CORE_DIG_DLANE_1_RW_HS_TX_1

Reg. 0x3301

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_1_THSZERO_REG	rw	ro	0x20	Tclk-zero/Ths-zero setting (word clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.541 CORE_DIG_DLANE_1_RW_HS_TX_2

Reg. 0x3302

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_2_TCLKPRE_REG	rw	ro	0x3	Tclk-pre setting (word clock cycles). Clock lane related. This field is quasi-static. Please check table for more details.

1.1.1.542 CORE_DIG_DLANE_1_RW_HS_TX_3

Reg. 0x3303

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_TX_3_TLPTXOVERLAP_REG	rw	ro	0x6	LP-TX/HS-TX drivers enable overlap (DCO clock cycles). This field is quasi-static. Please check table for more details.
8	HS_TX_3_INVORDER_TX_REG	rw	ro	0x0	Invert TX data's MSB to LSB transmission order. Active high. This field is quasi-static.
9	HS_TX_3_STATE_OVR_EN_REG	rw	ro	0x0	HS-TX FSM state (word clock) override enable. Active high. Used for debug purposes.
13:10	HS_TX_3_STATE_OVR_REG	rw	ro	0x0	HS-TX FSM state (word clock) override value. Used for debug purposes.
14	HS_TX_3_HSDIRECT_REG	rw	ro	0x0	Reserved.
15	HS_TX_3_PIN_SWAP_REG	rw	ro	0x0	Swap dp and dn lines. Applies to high speed mode. This field is quasi-static. - 1'b0: positive on dp / negative on dn; - 1'b1: positive on dn / negative on dp;

1.1.1.543 CORE_DIG_DLANE_1_RW_HS_TX_4

Reg. 0x3304

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_4_TLPX_DCO_REG	rw	ro	0x7	Tlpx value (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.544 CORE_DIG_DLANE_1_RW_HS_TX_5

Reg. 0x3305

High speed TX subsystem parameters control

access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_5_THSTRAIL_DCO_REG	rw	ro	0x7	Tclk-trail/Ths-trail value (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.545 CORE_DIG_DLANE_1_RW_HS_TX_6

Reg. 0x3306

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_6_TLP11END_DCO_REG	rw	ro	0xA	HS2LP final LP11 setting (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.546 CORE_DIG_DLANE_1_RW_HS_TX_7

Reg. 0x3307

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
8:0	HS_TX_7_ALTCALSEED_REG	rw	ro	0xFF	Alternate calibration PRBS seed. Used for debug purposes.
9	HS_TX_7_STATE_DCO_OVR_EN_REG	rw	ro	0x0	HS-TX FSM state (DCO clock) override enable. Active high. Used for debug purposes.
13:10	HS_TX_7_STATE_DCO_OVR_VAL_REG	rw	ro	0x0	HS-TX FSM state (DCO clock) override value. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.547 CORE_DIG_DLANE_1_RW_HS_TX_8

Reg. 0x3308

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_8_TCLKPOST_REG	rw	ro	0x1C	Tclk-post setting (word clock cycles). Clock lane related. This field is quasi-static. Please check table for more details.

1.1.1.548 CORE_DIG_DLANE_1_RW_HS_TX_9

Reg. 0x3309

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_9_THSPRPR_DCO_REG	rw	ro	0xA	Tclk-prepare/Ths-prepare setting (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.549 CORE_DIG_DLANE_1_RW_HS_TX_10

Reg. 0x330A

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_10_TLP11INIT_DCO_REG	rw	ro	0xA	LP2HS initial LP11 setting (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.550 CORE_DIG_DLANE_1_RW_HS_TX_11

Reg. 0x330B

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_11_TPREAM	rw	ro	0x7	Reserved.

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1.1.1.551 CORE_DIG_DLANE_1_RW_HS_TX_12

Reg. 0x330C

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_12_THSEXIT_DCO_REG	rw	ro	0x14	Ths-exit setting (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.553 CORE_DIG_DLANE_CLK_RW_CFG_0

Reg. 0x3800

DPHY lane configuration
access : read-write

bits	name	s/w	h/w	default	description
0	CFG_0_LP_PIN_SWAP_REG	rw	ro	0x0	Swap dp and dn lines. Applies to low power mode. This field is quasi-static. - 1'b0: positive on dp / negative on dn; - 1'b1: positive on dn / negative on dp;
1	CFG_0_HS_PIN_SWAP_REG	rw	ro	0x0	Swap dp and dn lines. Applies to high speed mode. This field is quasi-static. - 1'b0: positive on dp / negative on dn; - 1'b1: positive on dn / negative on dp;
2	LOOPBACK_MODE_EN	rw	ro	0x0	Primes the lane in loopback mode by enabling the LP-TX and LP-RX at the same time. Active high. This field is quasi-static.
15:3	RESERVED_15_3	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.554 CORE_DIG_DLANE_CLK_RW_CFG_1

Reg. 0x3801

DPHY lane configuration
access : read-write

bits	name	s/w	h/w	default	description
0	CFG_1_PREAMBLE_EN_REG	rw	ro	0x0	Enables support of data burst with preamble (DPHY specification 2.0 and above). Active high.
1	CFG_1_BACKWARDS_DESKEW_REG	rw	ro	0x0	Enables internal skew calibration for DPHY1.1 modes. Active high.
2	CFG_1_DESKEW_SUPPORTED_REG	rw	ro	0x0	Selects whether deskew bursts (DPHY specification 1.2 and above) with 16'hFFFF sync headers are supported. Active high.
3	CFG_1_SOT_DETECTION_REG	rw	ro	0x0	Selects whether start of transmission (SoT) soft error is flagged. Active high.
15:4	RESERVED_15_4	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.555 CORE_DIG_DLANE_CLK_RW_CFG_2

Reg. 0x3802

DPHY lane configuration
access : read-write

bits	name	s/w	h/w	default	description
15:0	CFG_2_SPARE	rw	ro	0x0	Spare registers for future use.

1.1.1.557 CORE_DIG_DLANE_CLK_RW_LP_0

Reg. 0x3840

Low power subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
3:0	LP_0_TTAGET_REG	rw	ro	0xC	BTA timing control. Defines the time that the new transmitter drives LP000 after taking control of the lines. Ttaget timer counter (resolution of 1/2 txclkesc period). This

					field is quasi-static. Effective timer size is LP_0_TTAGET - LP_0_TTASURE
7:4	LP_0_TTASURE_REG	rw	ro	0x3	BTA timing control. Defines the time that the new transmitter waits, after the LP10 state before driving LP00. Tta-sure timer counter (resolution of 1/2 txclkesc period). This field is quasi-static.
11:8	LP_0_TTAGO_REG	rw	ro	0x6	BTA timing control. Defines the time that the transmitter drives LP00 before releasing control of the lines. Tta-go timer counter (resolution of 1/2 txclkesc period). This field is quasi-static.
15:12	LP_0_ITMINRX_REG	rw	ro	0x4	LP-RX pulse filter width (in dco_clk cycles). Used to reject pulses smaller than the desired size. This field is quasi-static.

1.1.1.558 CORE_DIG_DLANE_CLK_RW_LP_1

Reg. 0x3841

Low power subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	LP_1_ERRCONTENTION_THRES_REG	rw	ro	0x10	Error contention detection filter size (in dco_clk cycles). Defines the time that the system tolerates contention before asserting errcontentionlp* flags. This field is quasi-static.
15:8	LP_1_LPTX_PON_TIMER_REG	rw	ro	0x80	LP-TX power on timer (in txclkesc cycles). Defines the time when switching from the ULP pull down back to the LP-TX driver. This field is quasi-static.

1.1.1.559 CORE_DIG_DLANE_CLK_RW_LP_2

Reg. 0x3842

Low power subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
0	LP_2_FILTER_INPUT_SAMPLING_REG	rw	ro	0x1	LPRX filter input data sampling
15:1	RESERVED_15_1	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.561 CORE_DIG_DLANE_CLK_R_LP_0

Reg. 0x3850

Low power subsystem status
access : read-only

bits	name	s/w	h/w	default	description
0	LP_0_HSACTIVERX	ro	ro	0x0	Signal which indicates that the HS entry transition LP01 -> LP00 has been observed. Active high.
1	LP_0_RXHSRQST	ro	ro	0x0	Signal which indicates that the HS entry transition LP11 -> LP01 has been observed. Active high.
15:2	RESERVED_15_2	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.562 CORE_DIG_DLANE_CLK_R_LP_1

Reg. 0x3851

Low power subsystem status
access : read-only

bits	name	s/w	h/w	default	description
3:0	LP_1_STATE_BTA	ro	ro	0x0	BTA FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion.
7:4	LP_1_STATE_LPRX	ro	ro	0x0	LP-RX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion.
12:8	LP_1_STATE_LPTX	ro	ro	0x0	LP-TX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion.
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.564 CORE_DIG_DLANE_CLK_R_HS_TX_0

Reg. 0x3870

High speed TX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
3:0	STATE_DHSTX	ro	ro	0x0	HS-TX word clock FSM state
7:4	STATE_DCO_DHSTX	ro	ro	0x0	HS-TX DCO clock FSM state
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.566 CORE_DIG_DLANE_CLK_RW_HS_RX_0

Reg. 0x3880

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_RX_0_TCLKSETTLE_REG	rw	ro	0x1D	DPHY Tclk-settle timer counter (dco_clk cycles). Defines the time interval between the detection of the LP01 -> LP00 transition and the enabling of the reception logic
15:8	HS_RX_0_THSSETTLE_REG	rw	ro	0x9	DPHY Ths-settle timer counter (dco_clk cycles). Defines the time interval between the detection of the LP01 -> LP00 transition and the enabling of the HS data path.

1.1.1.567 CORE_DIG_DLANE_CLK_RW_HS_RX_1

Reg. 0x3881

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_RX_1_FILTER_SIZE_DESKEW_REG	rw	ro	0x10	Deskew algorithm filter size (word clock cycles). Corresponds to the number of samples used to assess the quality of a phase setting.
15:8	HS_RX_1_FILTER_SIZE_SKEWCAL_REG	rw	ro	0x40	Skew calibration algorithm filter size (word_clk cycles). Corresponds to the number of samples used to assess the quality of a phase setting.

1.1.1.568 CORE_DIG_DLANE_CLK_RW_HS_RX_2

Reg. 0x3882

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
2:0	HS_RX_2_LATENCY_DESKEW_REG	rw	ro	0x3	Number of cycles to wait for to account for the AFE's latency during deskew (word clock cycles)
4:3	HS_RX_2_LATENCY_SKEWCAL_REG	rw	ro	0x3	Number of cycles to wait for to account for the AFE's latency during skew calibration (word clock cycles)
6:5	HS_RX_2_JUMP2STEPS_SKEWCAL_REG	rw	ro	0x0	How many phase settings to jump after detecting the edge during skew calibration algorithm
7	HS_RX_2_POLARITY_SKEWCAL_REG	rw	ro	0x1	Inverts the data from the AFE's polarity during skew calibration. (Active high)
8	HS_RX_2_RECAL_SKEWCAL_REG	rw	ro	0x0	Signal used to trigger a skew recalibration. (Active high)
9	HS_RX_2_UPDATE_SETTINGS_DESKEW_REG	rw	ro	0x1	Signal used to update the deskew algorithm's settings (Active high)
10	HS_RX_2_UPDATE_SETTINGS_SKEWCAL_REG	rw	ro	0x1	Signal used to update the skew calibration algorithm's settings (Active high)
11	HS_RX_2_IGNORE_ALTERNCAL_REG	rw	ro	0x0	Signal used to ignore alternate calibration patterns. (Active high)
12	HS_RX_2_ROUNDUP_DESKEW_REG	rw	ro	0x1	Selects whether to average the final calibration result up (Active high)
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.569 CORE_DIG_DLANE_CLK_RW_HS_RX_3

Reg. 0x3883

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
3:0	HS_RX_3_STEP_SIZE_DESKEW_REG	rw	ro	0x2	Size of the deskew algorithm's phase settings step.
9:4	HS_RX_3_FJUMP_DESKEW_REG	rw	ro	0x1	After detecting the left edge this bus selects how many phases to jump during the deskew algorithm. In phase steps.
12:10	HS_RX_3_SHIFT_STEP_DESKEW_REG	rw	ro	0x1	Shift step size for fine calibration of the deskew algorithm. In phase steps.
15:13	HS_RX_3_SHRINK_STEP_DESKEW_REG	rw	ro	0x1	Shrink step size for fine calibration of the deskew algorithm. In phase steps.

1.1.1.570 CORE_DIG_DLANE_CLK_RW_HS_RX_4

Reg. 0x3884

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_RX_4_MAX_ITERATIONS_DESKEW_REG	rw	ro	0x96	Maximum number of iterations of the deskew algorithm (word_clk cycles)

1.1.1.571 CORE_DIG_DLANE_CLK_RW_HS_RX_5

Reg. 0x3885

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
10:0	HS_RX_5_DDL_LEFT_INIT_REG	rw	ro	0x0	Initial DDL setting for the left pointer of the deskew algorithm
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.572 CORE_DIG_DLANE_CLK_RW_HS_RX_6

Reg. 0x3886

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
10:0	HS_RX_6_MIN_EYE_OPENING_DESKEW_REG	rw	ro	0x2D	Minimum eye opening after deskew algorithm is complete not to flag an error. Used to obtain error information. (in DDL steps)
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.573 CORE_DIG_DLANE_CLK_RW_HS_RX_7

Reg. 0x3887

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_RX_7_TCLKMISS_REG	rw	ro	0x6	Tclkmiss timer counter (dco_clk cycles). Defines the minimum time with absence of clock before flagging clock miss. This field is quasi-static.
8	HS_RX_7_INVORDER_RX_REG	rw	ro	0x1	Signal used to invert MSB to LSB reception order (Active high). This field is quasi-static.
9	HS_RX_7_INITIAL_CALIBRATION_REG	rw	ro	0x1	Select deskew initial calibration (Active high) If 0 triggers a periodic calibration.
10	HS_RX_7_THSEXIT_MIN_REG	rw	ro	0x0	Controls lane aligner. Used for lower bitrates if bursts received have minimum Ths-exit. This field is quasi-static.

12:11	HS_RX_7_DESKEW_CNF_REG	rw	ro	0x3	Deskew pattern length configuration for aligner's pattern search. Used for debug purposes. This field is quasi-static. - 2'b00 - Minimum deskew pattern length of 10 bits - 2'b01 - Minimum deskew pattern length of 12 bits - 2'b10 - Minimum deskew pattern length of 14 bits - 2'b11 - Minimum deskew pattern length of 16 bits (default)
13	HS_RX_7_DESKEW_AUTO_ALGO_SEL_REG	rw	ro	0x1	Select manual or automatic deskew algorithm selection. - 1'b0 - Manual control of the algorithm. HS_RX_7_INITIAL_CALIBRATION_REG selects whether to run an initial calibration or a fine calibration. - 1'b1 - Automatic control of the algorithm. After the first successful initial calibration always run a fine one.
14	HS_RX_7_DESKEW_REARM_INITIAL_REG	rw	ro	0x0	Allows running an initial calibration after a previous successful one when in automatic mode. This feature shall be used in continuous clock mode.
15	HS_RX_7_SELECT_ALTERNATE_ALGO_REG	rw	ro	0x0	Selects which algorithm is triggered by the alternate calibration pattern. - 1'b0 - Triggers coarse calibration - 1'b1 - Triggers fine calibration

1.1.1.574 CORE_DIG_DLANE_CLK_RW_HS_RX_8

Reg. 0x3888

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
0	HS_RX_8_FILTER_DITHERING_EN_REG	rw	ro	0x0	Enable dithering to the deskew algorithm's filter size (Active high)
8:1	HS_RX_8_START_DELAY_REG	rw	ro	0x0	Selects an initial delay for the deskew algorithm (word_clk cycles)
9	HS_ALIGN_BYPASS_REG	rw	ro	0x0	Bypasses alignment and sync detection.
15:10	RESERVED_15_10	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.575 CORE_DIG_DLANE_CLK_RW_HS_RX_9

Reg. 0x3889

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
10:0	HS_RX_9_PHASE_BOUND_REG	rw	ro	0xFF	Maximum phase allowed during Deskew algorithm
11	HS_RX_9_EQUALIZATION_RESTORE_COARSE_VALUES_REG	rw	ro	0x0	Restore deskew coarse calibration results at the beginning of each fine tuning calibration. This field is quasi-static.
12	HS_RX_9_EQUALIZATION_BYPASS_FSM_STATES_REG	rw	ro	0x0	Bypass certain states of the fine tuning algorithm FSM. This field is quasi-static.
13	HS_RX_9_EQUALIZATION_ENABLE_REG	rw	ro	0x0	Enables RX Equalization for deskew fine tuning algorithm. This field is quasi-static.
14	HS_RX_9_EQUALIZATION_DIVIDE_FILTER_SIZE_REG	rw	ro	0x0	Divide filter size maximum value by 4 for deskew fine tuning algorithm. This field is quasi-static.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.576 CORE_DIG_DLANE_CLK_RW_HS_RX_10

Reg. 0x388A

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
10:0	HS_RX_10_DDL_MID_INIT_REG	rw	ro	0x1	Initial DDL setting for the mid pointer of the deskew algorithm

15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.577 CORE_DIG_DLANE_CLK_RW_HS_RX_11

Reg. 0x388B

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
10:0	HS_RX_11_DDL_RIGHT_INIT_REG	rw	ro	0x2	Initial DDL setting for the right pointer of the deskew algorithm
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.578 CORE_DIG_DLANE_CLK_RW_HS_RX_12

Reg. 0x388C

High speed RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_RX_12_WINDOW_SIZE_DESKEW_REG	rw	ro	0x3	Used by the deskew algorithm; Consists of the number of consecutive good settings needed to detect the left edge. Used to prevent false edge detection (word clock cycles)
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.580 CORE_DIG_DLANE_CLK_R_HS_RX_0

Reg. 0x3890

High speed RX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
0	DESKEWCALDONE	ro	ro	0x0	Signals that the skew calibration has completed. (Active high)
1	DESKEWCALFAILED	ro	ro	0x0	Signals a skew calibration with errors (Active high)
9:2	DESKEW_CAL_STATUS	ro	ro	0x0	Bus with status information of the deskew algorithm. - [0] - signals that the deskew algorithm has finished; - [1] - signals that an initial calibration has finished successfully; - [2] - signals that an initial calibration has finished with an unsatisfactory eye size; - [3] - signals that an initial calibration has failed; - [4] - signals that a fine calibration has finished with convergence; - [5] - signals that a fine calibration ran out of time but found a new best setting; - [6] - signals that a fine calibration ran out of time with no best setting; - [7] - signals that during either calibration the phase setting went out of bounds.
15:10	RESERVED_15_10	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.581 CORE_DIG_DLANE_CLK_R_HS_RX_1

Reg. 0x3891

High speed RX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
15:0	DESKEWCALTIME	ro	ro	0x0	Bus containing information on how many cycles the deskew calibration took (word_clk cycles)

1.1.1.582 CORE_DIG_DLANE_CLK_R_HS_RX_2

Reg. 0x3892

High speed RX subsystem status
access : read-only

bits	name	s/w	h/w	default	description

7:0	DESKEW_STATE	ro	ro	0xA0	Deskew algorithm FSM's state
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.583 CORE_DIG_DLANE_CLK_R_HS_RX_3

Reg. 0x3893

High speed RX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
3:0	DESKEW_PREV_ACTION	ro	ro	0x0	Deskew algorithm previous action
4	DESKEW_PREV_RESULT	ro	ro	0x0	Deskew algorithm previous action's result
8:5	DESKEW_CURR_ACTION	ro	ro	0x0	Deskew algorithm current action
9	DESKEW_FAILED_LEFT	ro	ro	0x0	Result of the deskew algorithm left pointers' comparison
10	DESKEW_FAILED_RIGHT	ro	ro	0x0	Result of the deskew algorithm right pointers' comparison
11	DESKEW_ALL_DIFF	ro	ro	0x0	Result of the deskew algorithm three pointers' comparison
15:12	RESERVED_15_12	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.584 CORE_DIG_DLANE_CLK_R_HS_RX_4

Reg. 0x3894

High speed RX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
7:0	EDGE1POINTER_SKEWCAL	ro	ro	0x0	Skewcal algorithm's first edge
15:8	EDGE2POINTER_SKEWCAL	ro	ro	0x0	Skewcal algorithm's second edge

1.1.1.586 CORE_DIG_DLANE_CLK_RW_HS_TX_0

Reg. 0x3900

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_0_THSTRAIL_REG	rw	ro	0x9	Tclk-trail/Ths-trail setting (word clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.587 CORE_DIG_DLANE_CLK_RW_HS_TX_1

Reg. 0x3901

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_1_THSZERO_REG	rw	ro	0x20	Tclk-zero/Ths-zero setting (word clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.588 CORE_DIG_DLANE_CLK_RW_HS_TX_2

Reg. 0x3902

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_2_TCLKPRE_REG	rw	ro	0x3	Tclk-pre setting (word clock cycles). Clock lane related. This field is quasi-static. Please check table for more details.

1.1.1.589 CORE_DIG_DLANE_CLK_RW_HS_TX_3

Reg. 0x3903

High speed TX subsystem parameters control

access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_TX_3_TLPTXOVERLAP_REG	rw	ro	0x6	LP-TX/HS-TX drivers enable overlap (DCO clock cycles). This field is quasi-static. Please check table for more details.
8	HS_TX_3_INVORDER_TX_REG	rw	ro	0x0	Invert TX data's MSB to LSB transmission order. Active high. This field is quasi-static.
9	HS_TX_3_STATE_OVR_EN_REG	rw	ro	0x0	HS-TX FSM state (word clock) override enable. Active high. Used for debug purposes.
13:10	HS_TX_3_STATE_OVR_REG	rw	ro	0x0	HS-TX FSM state (word clock) override value. Used for debug purposes.
14	HS_TX_3_HSDIRECT_REG	rw	ro	0x0	Reserved.
15	HS_TX_3_PIN_SWAP_REG	rw	ro	0x0	Swap dp and dn lines. Applies to high speed mode. This field is quasi-static. - 1'b0: positive on dp / negative on dn; - 1'b1: positive on dn / negative on dp;

1.1.1.590 CORE_DIG_DLANE_CLK_RW_HS_TX_4

Reg. 0x3904

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_4_TLPX_DCO_REG	rw	ro	0x7	Tlpx value (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.591 CORE_DIG_DLANE_CLK_RW_HS_TX_5

Reg. 0x3905

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_5_THSTRAIL_DCO_REG	rw	ro	0x7	Tclk-trail/Ths-trail value (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.592 CORE_DIG_DLANE_CLK_RW_HS_TX_6

Reg. 0x3906

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_6_TLP11END_DCO_REG	rw	ro	0xA	HS2LP final LP11 setting (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.593 CORE_DIG_DLANE_CLK_RW_HS_TX_7

Reg. 0x3907

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
8:0	HS_TX_7_ALTCALSEED_REG	rw	ro	0xFF	Alternate calibration PRBS seed. Used for debug purposes.
9	HS_TX_7_STATE_DCO_OVR_EN_REG	rw	ro	0x0	HS-TX FSM state (DCO clock) override enable. Active high. Used for debug purposes.
13:10	HS_TX_7_STATE_DCO_OVR_VAL_REG	rw	ro	0x0	HS-TX FSM state (DCO clock) override value. Used for debug purposes.
15:14	RESERVED_15_14	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.594 CORE_DIG_DLANE_CLK_RW_HS_TX_8

Reg. 0x3908

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_8_TCLKPOST_REG	rw	ro	0x1C	Tclk-post setting (word clock cycles). Clock lane related. This field is quasi-static. Please check table for more details.

1.1.1.595 CORE_DIG_DLANE_CLK_RW_HS_TX_9

Reg. 0x3909

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_9_THSPRPR_DCO_REG	rw	ro	0xA	Tclk-prepare/Ths-prepare setting (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.596 CORE_DIG_DLANE_CLK_RW_HS_TX_10

Reg. 0x390A

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_10_TLP11INIT_DCO_REG	rw	ro	0xA	LP2HS initial LP11 setting (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.597 CORE_DIG_DLANE_CLK_RW_HS_TX_11

Reg. 0x390B

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_11_TPREAMBLE_REG	rw	ro	0x7	Reserved.

1.1.1.598 CORE_DIG_DLANE_CLK_RW_HS_TX_12

Reg. 0x390C

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_12_THSEXIT_DCO_REG	rw	ro	0x14	Ths-exit setting (DCO clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.600 PPI_RW_CPHY_TRIO0_LBERT_0

Reg. 0x4000

CPHY loopback control
access : read-write

bits	name	s/w	h/w	default	description
3:0	LBERT_PM_MODE	rw	ro	0x0	Pattern matcher mode. This bus is quasi-static. - 4'b0000: pattern matcher disabled - 4'b0001: PRBS31 (x^31 + x^28 + 1) - 4'b0010: PRBS23 (x^23 + x^18 + 1) - 4'b0011: PRBS23 (x^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1) - 4'b0100: PRBS16 (x^16 + x^5 + x^4 + x^3 + 1) - 4'b0101: PRBS15 (x^15 + x^14 + 1) - 4'b0110: PRBS11 (x^11 + x^9 + 1) - 4'b0111: PRBS9 (x^9 + x^5 + 1) - 4'b1000: PRBS7 (x^7 + x^6 + 1) - 4'b1001: Custom 8 bit pattern - 4'b1010: DC balanced custom 8 bit pattern (pat[7:0], ~pat[7:0]) - all others reserved
4	LBERT_PM_START_OVR_VAL	rw	ro	0x0	Pattern matcher start override value. Used for debug purposes.

5	LBERT_PM_START_OVR_EN	rw	ro	0x0	Pattern matcher start override enable. Active high. Used for debug purposes.
6	LBERT_PM_SAMPLE_COUNTER_OVR_VAL	rw	ro	0x0	Pattern matcher error counter sampling override value. Used for debug purposes.
7	LBERT_PM_SAMPLE_COUNTER_OVR_EN	rw	ro	0x0	Pattern matcher error counter sampling override enable. Active high. Used for debug purposes.
11:8	LBERT_PG_MODE	rw	ro	0x0	Pattern generator mode. This field is quasi-static. - 4'b0000: pattern generator disabled - 4'b0001: PRBS31 (x^31 + x^28 + 1) - 4'b0010: PRBS23 (x^23 + x^18 + 1) - 4'b0011: PRBS23 (x^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1) - 4'b0100: PRBS16 (x^16 + x^5 + x^4 + x^3 + 1) - 4'b0101: PRBS15 (x^15 + x^14 + 1) - 4'b0110: PRBS11 (x^11 + x^9 + 1) - 4'b0111: PRBS9 (x^9 + x^5 + 1) - 4'b1000: PRBS7 (x^7 + x^6 + 1) - 4'b1001: Custom 8 bit pattern - 4'b1010: DC balanced custom 8 bit pattern (pat[7:0], ~pat[7:0]) - all others reserved
12	LBERT_PG_START_OVR_VAL	rw	ro	0x0	Pattern generator start override value. Used for debug purposes.
13	LBERT_PG_START_OVR_EN	rw	ro	0x0	Pattern generator start override enable. Active high. Used for debug purposes.
14	LBERT_PG_ERROR_INJECTION	rw	ro	0x0	Injects 1 bit error on output pattern. Active high. Each rising edge inserts 1 error.
15	LBERT_PM_DATA_SWAP	rw	ro	0x0	Controls trio mux to choose normal or swapped data (actual reset value is 0xX)

1.1.1.601 PPI_RW_CPHY_TRIO0_LBERT_1

Reg. 0x4001

CPHY loopback control
access : read-write

bits	name	s/w	h/w	default	description
7:0	LBERT_PG_USER_PATTERN	rw	ro	0x0	Custom 8 bit pattern. Requires LBERT_PG_MODE to be set to 4'b1001 or 4'b1010. This bus is quasi-static.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.602 PPI_R_CPHY_TRIO0_LBERT_0

Reg. 0x4002

CPHY loopback observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	LBERT_PM_ERROR_COUNTER	ro	ro	0x1	Pattern matcher error counter. Readouts are valid after a rising edge on LBERT_PM_SAMPLE_COUNTER.

1.1.1.603 PPI_R_CPHY_TRIO0_LBERT_1

Reg. 0x4003

CPHY loopback observability
access : read-only

bits	name	s/w	h/w	default	description
0	LBERT_PG_ENABLED	ro	ro	0x0	Pattern generator enable observability. Active high.
15:1	RESERVED_15_1	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.604 PPI_RW_CPHY_TRIO0_SPARE

Reg. 0x4004

CPHY spare registers
access : read-write

bits	name	s/w	h/w	default	description
15:0	CPHY_TRIO0_SPARE	rw	ro	0x0	Spare registers for future use

1.1.1.606 PPI_RW_CPHY_TRIO1_LBERT_0

Reg. 0x4200

CPHY loopback control
access : read-write

bits	name	s/w	h/w	default	description
3:0	LBERT_PM_MODE	rw	ro	0x0	Pattern matcher mode. This bus is quasi-static. - 4'b0000: pattern matcher disabled - 4'b0001: PRBS31 (x^31 + x^28 + 1) - 4'b0010: PRBS23 (x^23 + x^18 + 1) - 4'b0011: PRBS23 (x^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1) - 4'b0100: PRBS16 (x^16 + x^5 + x^4 + x^3 + 1) - 4'b0101: PRBS15 (x^15 + x^14 + 1) - 4'b0110: PRBS11 (x^11 + x^9 + 1) - 4'b0111: PRBS9 (x^9 + x^5 + 1) - 4'b1000: PRBS7 (x^7 + x^6 + 1) - 4'b1001: Custom 8 bit pattern - 4'b1010: DC balanced custom 8 bit pattern (pat[7:0], ~pat[7:0]) - all others reserved
4	LBERT_PM_START_OVR_VAL	rw	ro	0x0	Pattern matcher start override value. Used for debug purposes.
5	LBERT_PM_START_OVR_EN	rw	ro	0x0	Pattern matcher start override enable. Active high. Used for debug purposes.
6	LBERT_PM_SAMPLE_COUNTER_OVR_VAL	rw	ro	0x0	Pattern matcher error counter sampling override value. Used for debug purposes.
7	LBERT_PM_SAMPLE_COUNTER_OVR_EN	rw	ro	0x0	Pattern matcher error counter sampling override enable. Active high. Used for debug purposes.
11:8	LBERT_PG_MODE	rw	ro	0x0	Pattern generator mode. This field is quasi-static. - 4'b0000: pattern generator disabled - 4'b0001: PRBS31 (x^31 + x^28 + 1) - 4'b0010: PRBS23 (x^23 + x^18 + 1) - 4'b0011: PRBS23 (x^23 + x^21 + x^16 + x^8 + x^5 + x^2 + 1) - 4'b0100: PRBS16 (x^16 + x^5 + x^4 + x^3 + 1) - 4'b0101: PRBS15 (x^15 + x^14 + 1) - 4'b0110: PRBS11 (x^11 + x^9 + 1) - 4'b0111: PRBS9 (x^9 + x^5 + 1) - 4'b1000: PRBS7 (x^7 + x^6 + 1) - 4'b1001: Custom 8 bit pattern - 4'b1010: DC balanced custom 8 bit pattern (pat[7:0], ~pat[7:0]) - all others reserved
12	LBERT_PG_START_OVR_VAL	rw	ro	0x0	Pattern generator start override value. Used for debug purposes.
13	LBERT_PG_START_OVR_EN	rw	ro	0x0	Pattern generator start override enable. Active high. Used for debug purposes.
14	LBERT_PG_ERROR_INJECTION	rw	ro	0x0	Injects 1 bit error on output pattern. Active high. Each rising edge inserts 1 error.
15	LBERT_PM_DATA_SWAP	rw	ro	0x0	Controls trio mux to choose normal or swapped data (actual reset value is 0xX)

1.1.1.607 PPI_RW_CPHY_TRIO1_LBERT_1

Reg. 0x4201

CPHY loopback control
access : read-write

bits	name	s/w	h/w	default	description
7:0	LBERT_PG_USER_PATTERN	rw	ro	0x0	Custom 8 bit pattern. Requires LBERT_PG_MODE to be set to 4'b1001 or 4'b1010. This bus is quasi-static.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.608 PPI_R_CPHY_TRIO1_LBERT_0

Reg. 0x4202

CPHY loopback observability
access : read-only

bits	name	s/w	h/w	default	description
15:0	LBERT_PM_ERROR_COUNTER	ro	ro	0x1	Pattern matcher error counter. Readouts are valid after a rising edge on LBERT_PM_SAMPLE_COUNTER.

1.1.1.609 PPI_R_CPHY_TRIO1_LBERT_1

Reg. 0x4203

CPHY loopback observability
access : read-only

bits	name	s/w	h/w	default	description
0	LBERT_PG_ENABLED	ro	ro	0x0	Pattern generator enable observability. Active high.
15:1	RESERVED_15_1	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.610 PPI_RW_CPHY_TRIO1_SPARE

Reg. 0x4204

CPHY spare registers
access : read-write

bits	name	s/w	h/w	default	description
15:0	CPHY_TRIO1_SPARE	rw	ro	0x0	Spare registers for future use

1.1.1.612 CORE_DIG_CLANE_0_RW_CFG_0

Reg. 0x5000

CPHY lane configuration
access : read-write

bits	name	s/w	h/w	default	description
2:0	CFG_0_LP_PIN_SWAP_REG	rw	ro	0x0	Swap a, b and c lines. Applies to low power mode. This field is quasi-static. - 3'b000: TX ABC connected to RX ABC - 3'b001: TX ABC connected to RX CBA - 3'b010: TX ABC connected to RX ACB - 3'b011: TX ABC connected to RX BCA - 3'b100: TX ABC connected to RX BAC - 3'b101: TX ABC connected to RX CAB - all others reserved
3	CFG_0_HS_PIN_SWAP_REG	rw	ro	0x0	Select the three lines' order in high speed mode
4	CFG_0_HS_ORDER_SWAP_REG	rw	ro	0x1	Deserializer MSB to LSB swap control
5	CFG_0_HS_DECODE_SWAP_REG	rw	ro	0x1	Decoder swap control : looks from MSB to LSB when de-coding
6	CFG_0_HS_ALIGNER_SWAP_REG	rw	ro	0x1	Aligner output swap control
7	CFG_0_HS_SYNC_DET_SWAP_REG	rw	ro	0x1	Sync detector swap control
8	CFG_0_ALP_ENABLE_REG	rw	ro	0x0	Enable ALP mode
9	CFG_0_SWAP_ENCODE_REG	rw	ro	0x0	Order of encoding LSB to MSB or MSB to LSB
10	LOOPBACK_MODE_EN	rw	ro	0x0	Primes the lane in loopback mode by enabling the LP-TX and LP-RX at the same time. Active high. This field is quasi-static.
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.614 CORE_DIG_CLANE_0_RW_CFG_2

Reg. 0x5002

CPHY lane configuration
access : read-write

bits	name	s/w	h/w	default	description
15:0	CFG_2_SPARE	rw	ro	0x0	Spare registers for future use.

1.1.1.616 CORE_DIG_CLANE_0_RW_LP_0

Reg. 0x5040

Low power subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
3:0	LP_0_TTAGET_REG	rw	ro	0xC	BTA timing control. Defines the time that the new transmitter drives LP000 after taking control of the lines. Tta-get timer counter (resolution of 1/2 txclkesc period). This field is quasi-static. Effective timer size is LP_0_TTAGET - LP_0_TTASURE
7:4	LP_0_TTASURE_REG	rw	ro	0x3	BTA timing control. Defines the time that the new transmitter waits, after the LP100 state before driving LP000. Tta-sure timer counter (resolution of 1/2 txclkesc period). This field is quasi-static.
11:8	LP_0_TTAGO_REG	rw	ro	0x6	BTA timing control. Defines the time that the transmitter drives LP000 before releasing control of the lines. Tta-go timer counter (resolution of 1/2 txclkesc period). This field is quasi-static.
15:12	LP_0_ITMINRX_REG	rw	ro	0x4	LP-RX pulse filter width (in dco_clk cycles). Used to reject pulses smaller than the desired size. This field is quasi-static.

1.1.1.617 CORE_DIG_CLANE_0_RW_LP_1

Reg. 0x5041

Low power subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	LP_1_ERRCONTENTION_THRES_REG	rw	ro	0x10	Error contention detection filter size (in dco_clk cycles). Defines the time that the system tolerates contention before asserting errcontentionlp* flags. This field is quasi-static.
15:8	LP_1_LPTX_PON_TIMER_REG	rw	ro	0x80	LP-TX power on timer (in txclkesc cycles). Defines the time when switching from the ULP pull down back to the LP-TX driver. This field is quasi-static.

1.1.1.618 CORE_DIG_CLANE_0_RW_LP_2

Reg. 0x5042

Low power subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
0	LP_2_FILTER_INPUT_SAMPLING_REG	rw	ro	0x1	LPRX filter input data sampling
15:1	RESERVED_15_1	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.620 CORE_DIG_CLANE_0_R_LP_0

Reg. 0x5050

Low power subsystem status
access : read-only

bits	name	s/w	h/w	default	description
0	LP_0_HSACTIVERX	ro	ro	0x0	Signal which indicates that the HS entry transition LP001 -> LP000 has been observed. Active high.
1	LP_0_RXHSRQST	ro	ro	0x0	Signal which indicates that the HS entry transition LP111 -> LP001 has been observed. Active high.
15:2	RESERVED_15_2	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.621 CORE_DIG_CLANE_0_R_LP_1

Reg. 0x5051

Low power subsystem status
access : read-only

bits	name	s/w	h/w	default	description
3:0	LP_1_STATE_BTA	ro	ro	0x0	BTA FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion.
7:4	LP_1_STATE_LPRX	ro	ro	0x0	LP-RX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion.
12:8	LP_1_STATE_LPTX	ro	ro	0x0	LP-TX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion.
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.623 CORE_DIG_CLANE_0_RW_HS_RX_0

Reg. 0x5080

CPHY HS RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
4:0	HSACTIVERX_DLY_REG	rw	ro	0x5	Timer counter after which hsactiverx is asserted (DCO clock cycles)
7:5	HSRX_CPHY_CDR_FBK_EN_DLY_REG	rw	ro	0x3	Timer counter after which hsrx_cphy_cdr_fbk_en is asserted (word_clk cycles)
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.624 CORE_DIG_CLANE_0_RW_HS_RX_1

Reg. 0x5081

CPHY HS RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
0	HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_REG	rw	ro	0x0	C-PHY CDR delay mask LPF bandwidth extension. Active high.
6:1	HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_DLY_REG	rw	ro	0x3F	Timer counter after which hsrx_cphy_cdr_fbk_fast_lock_en is asserted (word clock cycles)
15:7	RESERVED_15_7	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.626 CORE_DIG_CLANE_0_R_TX_0

Reg. 0x5091

HSTX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
3:0	STATE_CHSTX	ro	ro	0x0	HS-TX word clock FSM state
7:4	STATE_DCO_CHSTX	ro	ro	0x0	HS-TX DCO clock FSM state
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.628 CORE_DIG_CLANE_0_RW_HS_TX_0

Reg. 0x5100

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_0_THSEXIT_DCO_REG	rw	ro	0x14	Ths-exit setting (dco_clk cycles). This field is quasi-static. Please check table for more details.

1.1.1.629 CORE_DIG_CLANE_0_RW_HS_TX_1

Reg. 0x5101

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_1_TPOST_REG	rw	ro	0x3	T3-post setting (word clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.630 CORE_DIG_CLANE_0_RW_HS_TX_2

Reg. 0x5102

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_2_TCALPREAMBLE_REG	rw	ro	0x3	T3-calpreamble setting (word clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.631 CORE_DIG_CLANE_0_RW_HS_TX_3

Reg. 0x5103

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
3:0	HS_TX_3_STATE_OVR_REG	rw	ro	0x0	state override enable. Active high. Used for debug purposes.
4	HS_TX_3_STATE_OVR_EN_REG	rw	ro	0x0	state override value. Used for debug purposes.
7:5	HS_TX_3_BURST_TYPE_REG	rw	ro	0x0	Select burst to transmit type. - 000 For normal burst - 001 for normal burst with programmable sequence - 010 for calibration burst
8	HS_TX_3_HSDIRECT_REG	rw	ro	0x0	Reserved
9	HS_TX_3_INVORDER_REG	rw	ro	0x0	Invert TX data's MSB to LSB transmission order. Active high. This field is quasi-static.
10	HS_TX_3_STATE_DCO_VR_EN_REG	rw	ro	0x0	HS-TX FSM state (DCO clock) override enable. Active high. Used for debug purposes.
14:11	HS_TX_3_STATE_DCO_OVR_VAL_REG	rw	ro	0x0	HS-TX FSM state (DCO clock) override value. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.632 CORE_DIG_CLANE_0_RW_HS_TX_4

Reg. 0x5104

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
2:0	HS_TX_4_PROGSEQSYMB0_REG	rw	ro	0x0	Symbol 0 of the programmable sequence
5:3	HS_TX_4_PROGSEQSYMB1_REG	rw	ro	0x0	Symbol 1 of the programmable sequence
8:6	HS_TX_4_PROGSEQSYMB2_REG	rw	ro	0x0	Symbol 2 of the programmable sequence
11:9	HS_TX_4_PROGSEQSYMB3_REG	rw	ro	0x0	Symbol 3 of the programmable sequence
14:12	HS_TX_4_PROGSEQSYMB4_REG	rw	ro	0x0	Symbol 4 of the programmable sequence
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.633 CORE_DIG_CLANE_0_RW_HS_TX_5

Reg. 0x5105

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
2:0	HS_TX_5_PROGSEQSYMB5_REG	rw	ro	0x0	Symbol 5 of the programmable sequence
5:3	HS_TX_5_PROGSEQSYMB6_REG	rw	ro	0x0	Symbol 6 of the programmable sequence
8:6	HS_TX_5_PROGSEQSYMB7_REG	rw	ro	0x0	Symbol 7 of the programmable sequence
11:9	HS_TX_5_PROGSEQSYMB8_REG	rw	ro	0x0	Symbol 8 of the programmable sequence
14:12	HS_TX_5_PROGSEQSYMB9_REG	rw	ro	0x0	Symbol 9 of the programmable sequence
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.634 CORE_DIG_CLANE_0_RW_HS_TX_6

Reg. 0x5106

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
2:0	HS_TX_6_PROGSEQSYMB10_REG	rw	ro	0x0	Symbol 10 of the programmable sequence
5:3	HS_TX_6_PROGSEQSYMB11_REG	rw	ro	0x0	Symbol 11 of the programmable sequence
8:6	HS_TX_6_PROGSEQSYMB12_REG	rw	ro	0x0	Symbol 12 of the programmable sequence
11:9	HS_TX_6_PROGSEQSYMB13_REG	rw	ro	0x0	Symbol 13 of the programmable sequence
14:12	HS_TX_6_PIN_SWAP_REG	rw	ro	0x0	Swap ABC lines. Applies to high speed mode. This field is quasi-static. - 3'b000: TX ABC connected to RX ABC - 3'b001: TX ABC connected to RX CBA - 3'b010: TX ABC connected to RX ACB - 3'b011: TX ABC connected to RX BCA - 3'b100: TX ABC connected to RX BAC - 3'b101: TX ABC connected to RX CAB - all others reserved
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.635 CORE_DIG_CLANE_0_RW_HS_TX_7

Reg. 0x5107

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_7_T3PRPR_DCO_REG	rw	ro	0xD	Timer counter for T3prepare (DCO clock cycles). Defines the time to wait after driving LP000 to the lines before turning on the HS logic

1.1.1.636 CORE_DIG_CLANE_0_RW_HS_TX_8

Reg. 0x5108

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_8_TLP11END_DCO_REG	rw	ro	0xA	Final time to drive LP111 to the lines (after HS-leave) (DCO clock cycles)

1.1.1.637 CORE_DIG_CLANE_0_RW_HS_TX_9

Reg. 0x5109

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_9_T3POST_DCO_REG	rw	ro	0x6	Timer counter for T3post (DCO clock cycles). Defines how long to keep the HS logic on before moving to LP111

1.1.1.638 CORE_DIG_CLANE_0_RW_HS_TX_10

Reg. 0x510A

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_10_TPREBEGIN_REG	rw	ro	0x2	Timer counter for Tpreamble begin (word_clk cycles). Defines the time to drive the preamble pattern to the lines before sending the programmable sequence (if applicable).

1.1.1.639 CORE_DIG_CLANE_0_RW_HS_TX_11

Reg. 0x510B

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_11_TLPX_DCO_REG	rw	ro	0xA	Timer counter for Tlpx (DCO clock cycles). Defines the time to drive LP001 to the lines.

1.1.1.640 CORE_DIG_CLANE_0_RW_HS_TX_12

Reg. 0x510C

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_12_TLP11INIT_DCO_REG	rw	ro	0xA	Initial time to drive LP111 to the lines (before HS-entry) (DCO clock cycles)

1.1.1.641 CORE_DIG_CLANE_0_RW_HS_TX_13

Reg. 0x510D

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_TX_13_TLPTXOVERLAP_REG	rw	ro	0x6	Counter to define the time the LPTX driver overlaps the HSTX driver. (dco_clk cycles). This field is quasi-static.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.643 CORE_DIG_CLANE_1_RW_CFG_0

Reg. 0x5200

CPHY lane configuration
access : read-write

bits	name	s/w	h/w	default	description
2:0	CFG_0_LP_PIN_SWAP_REG	rw	ro	0x0	Swap a, b and c lines. Applies to low power mode. This field is quasi-static. - 3'b000: TX ABC connected to RX ABC - 3'b001: TX ABC connected to RX CBA - 3'b010: TX ABC connected to RX ACB - 3'b011: TX ABC connected to RX BCA - 3'b100: TX ABC connected to RX BAC - 3'b101: TX ABC connected to RX CAB - all others reserved
3	CFG_0_HS_PIN_SWAP_REG	rw	ro	0x0	Select the three lines' order in high speed mode
4	CFG_0_HS_ORDER_SWAP_REG	rw	ro	0x1	Deserializer MSB to LSB swap control
5	CFG_0_HS_DECODE_SWAP_REG	rw	ro	0x1	Decoder swap control : looks from MSB to LSB when decoding
6	CFG_0_HS_ALIGNE	rw	ro	0x1	Aligner output swap control

	R_SWAP_REG				
7	CFG_0_HS_SYNC_DET_SWAP_REG	rw	ro	0x1	Sync detector swap control
8	CFG_0_ALP_ENABLE_REG	rw	ro	0x0	Enable ALP mode
9	CFG_0_SWAP_ENCODE_REG	rw	ro	0x0	Order of encoding LSB to MSB or MSB to LSB
10	LOOPBACK_MODE_EN	rw	ro	0x0	Primes the lane in loopback mode by enabling the LP-TX and LP-RX at the same time. Active high. This field is quasi-static.
15:11	RESERVED_15_11	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.645 CORE_DIG_CLANE_1_RW_CFG_2

Reg. 0x5202

CPHY lane configuration
access : read-write

bits	name	s/w	h/w	default	description
15:0	CFG_2_SPARE	rw	ro	0x0	Spare registers for future use.

1.1.1.647 CORE_DIG_CLANE_1_RW_LP_0

Reg. 0x5240

Low power subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
3:0	LP_0_TTAGET_REG	rw	ro	0xC	BTA timing control. Defines the time that the new transmitter drives LP000 after taking control of the lines. Tta-get timer counter (resolution of 1/2 txclkesc period). This field is quasi-static. Effective timer size is LP_0_TTAGET - LP_0_TTASURE
7:4	LP_0_TTASURE_REG	rw	ro	0x3	BTA timing control. Defines the time that the new transmitter waits, after the LP100 state before driving LP000. Tta-sure timer counter (resolution of 1/2 txclkesc period). This field is quasi-static.
11:8	LP_0_TTAGO_REG	rw	ro	0x6	BTA timing control. Defines the time that the transmitter drives LP000 before releasing control of the lines. Tta-go timer counter (resolution of 1/2 txclkesc period). This field is quasi-static.
15:12	LP_0_ITMINRX_REG	rw	ro	0x4	LP-RX pulse filter width (in dco_clk cycles). Used to reject pulses smaller than the desired size. This field is quasi-static.

1.1.1.648 CORE_DIG_CLANE_1_RW_LP_1

Reg. 0x5241

Low power subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	LP_1_ERRCONTENTION_THRES_REG	rw	ro	0x10	Error contention detection filter size (in dco_clk cycles). Defines the time that the system tolerates contention before asserting errcontentionlp* flags. This field is quasi-static.
15:8	LP_1_LPTX_PON_TIMER_REG	rw	ro	0x80	LP-TX power on timer (in txclkesc cycles). Defines the time when switching from the ULP pull down back to the LP-TX driver. This field is quasi-static.

1.1.1.649 CORE_DIG_CLANE_1_RW_LP_2

Reg. 0x5242

Low power subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
0	LP_2_FILTER_INPUT_SAMPLING_REG	rw	ro	0x1	LPRX filter input data sampling
15:1	RESERVED_15_1	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.651 CORE_DIG_CLANE_1_R_LP_0

Reg. 0x5250

Low power subsystem status
access : read-only

bits	name	s/w	h/w	default	description
0	LP_0_HSACTIVERX	ro	ro	0x0	Signal which indicates that the HS entry transition LP001 -> LP000 has been observed. Active high.
1	LP_0_RXHSRQST	ro	ro	0x0	Signal which indicates that the HS entry transition LP111 -> LP001 has been observed. Active high.
15:2	RESERVED_15_2	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.652 CORE_DIG_CLANE_1_R_LP_1

Reg. 0x5251

Low power subsystem status
access : read-only

bits	name	s/w	h/w	default	description
3:0	LP_1_STATE_BTA	ro	ro	0x0	BTA FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion.
7:4	LP_1_STATE_LPRX	ro	ro	0x0	LP-RX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion.
12:8	LP_1_STATE_LPTX	ro	ro	0x0	LP-TX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion.
15:13	RESERVED_15_13	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.654 CORE_DIG_CLANE_1_RW_HS_RX_0

Reg. 0x5280

CPHY HS RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
4:0	HSACTIVERX_DLY_REG	rw	ro	0x5	Timer counter after which hsactiverx is asserted (DCO clock cycles)
7:5	HSRX_CPHY_CDR_FBK_EN_DLY_REG	rw	ro	0x3	Timer counter after which hsrx_cphy_cdr_fbk_en is asserted (word_clk cycles)
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.655 CORE_DIG_CLANE_1_RW_HS_RX_1

Reg. 0x5281

CPHY HS RX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
0	HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_REG	rw	ro	0x0	C-PHY CDR delay mask LPF bandwidth extension. Active high.
6:1	HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_DLY_REG	rw	ro	0x3F	Timer counter after which hsrx_cphy_cdr_fbk_fast_lock_en is asserted (word clock cycles)
15:7	RESERVED_15_7	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.657 CORE_DIG_CLANE_1_R_TX_0

Reg. 0x5291

HSTX subsystem status
access : read-only

bits	name	s/w	h/w	default	description
3:0	STATE_CHSTX	ro	ro	0x0	HS-TX word clock FSM state
7:4	STATE_DCO_CHSTX	ro	ro	0x0	HS-TX DCO clock FSM state

15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.659 CORE_DIG_CLANE_1_RW_HS_TX_0

Reg. 0x5300

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_0_THSEXIT_DCO_REG	rw	ro	0x14	Ths-exit setting (dco_clk cycles). This field is quasi-static. Please check table for more details.

1.1.1.660 CORE_DIG_CLANE_1_RW_HS_TX_1

Reg. 0x5301

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_1_TPOST_REG	rw	ro	0x3	T3-post setting (word clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.661 CORE_DIG_CLANE_1_RW_HS_TX_2

Reg. 0x5302

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_2_TCALPREAMBLE_REG	rw	ro	0x3	T3-calpreamble setting (word clock cycles). This field is quasi-static. Please check table for more details.

1.1.1.662 CORE_DIG_CLANE_1_RW_HS_TX_3

Reg. 0x5303

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
3:0	HS_TX_3_STATE_OVR_REG	rw	ro	0x0	state override enable. Active high. Used for debug purposes.
4	HS_TX_3_STATE_OVR_EN_REG	rw	ro	0x0	state override value. Used for debug purposes.
7:5	HS_TX_3_BURST_TYPE_REG	rw	ro	0x0	Select burst to transmit type. - 000 For normal burst - 001 for normal burst with programmable sequence - 010 for calibration burst
8	HS_TX_3_HSDIRECT_REG	rw	ro	0x0	Reserved
9	HS_TX_3_INVORDER_REG	rw	ro	0x0	Invert TX data's MSB to LSB transmission order. Active high. This field is quasi-static.
10	HS_TX_3_STATE_DCO_VR_EN_REG	rw	ro	0x0	HS-TX FSM state (DCO clock) override enable. Active high. Used for debug purposes.
14:11	HS_TX_3_STATE_DCO_OVR_VAL_REG	rw	ro	0x0	HS-TX FSM state (DCO clock) override value. Used for debug purposes.
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.663 CORE_DIG_CLANE_1_RW_HS_TX_4

Reg. 0x5304

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
2:0	HS_TX_4_PROGSEQSYMB0_REG	rw	ro	0x0	Symbol 0 of the programmable sequence
5:3	HS_TX_4_PROGSEQSYMB1_REG	rw	ro	0x0	Symbol 1 of the programmable sequence
8:6	HS_TX_4_PROGSEQ	rw	ro	0x0	Symbol 2 of the programmable sequence

	SYMB2_REG				
11:9	HS_TX_4_PROGSEQ SYMB3_REG	rw	ro	0x0	Symbol 3 of the programmable sequence
14:12	HS_TX_4_PROGSEQ SYMB4_REG	rw	ro	0x0	Symbol 4 of the programmable sequence
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.664 CORE_DIG_CLANE_1_RW_HS_TX_5

Reg. 0x5305

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
2:0	HS_TX_5_PROGSEQ SYMB5_REG	rw	ro	0x0	Symbol 5 of the programmable sequence
5:3	HS_TX_5_PROGSEQ SYMB6_REG	rw	ro	0x0	Symbol 6 of the programmable sequence
8:6	HS_TX_5_PROGSEQ SYMB7_REG	rw	ro	0x0	Symbol 7 of the programmable sequence
11:9	HS_TX_5_PROGSEQ SYMB8_REG	rw	ro	0x0	Symbol 8 of the programmable sequence
14:12	HS_TX_5_PROGSEQ SYMB9_REG	rw	ro	0x0	Symbol 9 of the programmable sequence
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.665 CORE_DIG_CLANE_1_RW_HS_TX_6

Reg. 0x5306

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
2:0	HS_TX_6_PROGSEQ SYMB10_REG	rw	ro	0x0	Symbol 10 of the programmable sequence
5:3	HS_TX_6_PROGSEQ SYMB11_REG	rw	ro	0x0	Symbol 11 of the programmable sequence
8:6	HS_TX_6_PROGSEQ SYMB12_REG	rw	ro	0x0	Symbol 12 of the programmable sequence
11:9	HS_TX_6_PROGSEQ SYMB13_REG	rw	ro	0x0	Symbol 13 of the programmable sequence
14:12	HS_TX_6_PIN_SWAP_REG	rw	ro	0x0	Swap ABC lines. Applies to high speed mode. This field is quasi-static. - 3'b000: TX ABC connected to RX ABC - 3'b001: TX ABC connected to RX CBA - 3'b010: TX ABC connected to RX ACB - 3'b011: TX ABC connected to RX BCA - 3'b100: TX ABC connected to RX BAC - 3'b101: TX ABC connected to RX CAB - all others reserved
15	RESERVED_15_15	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

1.1.1.666 CORE_DIG_CLANE_1_RW_HS_TX_7

Reg. 0x5307

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_7_T3PRPR_DCO_REG	rw	ro	0xD	Timer counter for T3prepare (DCO clock cycles). Defines the time to wait after driving LP000 to the lines before turning on the HS logic

1.1.1.667 CORE_DIG_CLANE_1_RW_HS_TX_8

Reg. 0x5308

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_8_TLP11END_DCO_REG	rw	ro	0xA	Final time to drive LP111 to the lines (after HS-leave) (DCO clock cycles)

1.1.1.668 CORE_DIG_CLANE_1_RW_HS_TX_9

Reg. 0x5309

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_9_T3POST_DCO_REG	rw	ro	0x6	Timer counter for T3post (DCO clock cycles). Defines how long to keep the HS logic on before moving to LP111

1.1.1.669 CORE_DIG_CLANE_1_RW_HS_TX_10

Reg. 0x530A

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_10_TPREBEGIN_REG	rw	ro	0x2	Timer counter for Tpreamble begin (word_clk cycles). Defines the time to drive the preamble pattern to the lines before sending the programmable sequence (if applicable).

1.1.1.670 CORE_DIG_CLANE_1_RW_HS_TX_11

Reg. 0x530B

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_11_TLPX_DCO_REG	rw	ro	0xA	Timer counter for Tlpx (DCO clock cycles). Defines the time to drive LP001 to the lines.

1.1.1.671 CORE_DIG_CLANE_1_RW_HS_TX_12

Reg. 0x530C

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
15:0	HS_TX_12_TLP11INIT_DCO_REG	rw	ro	0xA	Initial time to drive LP111 to the lines (before HS-entry) (DCO clock cycles)

1.1.1.672 CORE_DIG_CLANE_1_RW_HS_TX_13

Reg. 0x530D

High speed TX subsystem parameters control
access : read-write

bits	name	s/w	h/w	default	description
7:0	HS_TX_13_TLPTXOVERLAP_REG	rw	ro	0x6	Counter to define the time the LPTX driver overlaps the HSTX driver. (dco_clk cycles). This field is quasi-static.
15:8	RESERVED_15_8	ro	ro	0x0	Reserved for Future use and actual reset value is 0xX

End RegGroup

End RegGroup