Release Notes

v7.18.0.0
(Aug 4th, 2021)

IDesignSpec™ (IDS)

RTL Enhancement

1. F#14901 - **"enum_package=true"** property is supported for using enum constructs instead of parameters in verilog output.(More Details)

2. F#15644 - **"cdc.clock"** property is supported in VHDL output.(More Details)

UVM Enhancements

1. F#15701 - Removal of hdl_path from the UVM collateral by using **"ignore_prop=hdl_path"** on a particular block.(More Details)

2. B#1231 - Configure function in UVM is now described using named mapping.

3. F#15993- **"uvm_opt"** has been enhanced to replace the 'h prefix in the arrayed register names with a decimal index.(More Details)

C header Enhancements

1. F#15849 - Enhancement has been done in "#define" for reset value of a field when dynamic assignment is used in header output with top property **"cheader_opt=true"**.

2. F#15275 - **"cheader_ignore"** property has been enhanced for removing structs for chip, block, regfile, register address and INV_MASK, VALUE_MASK, INV_VALUE_MASK macros for header with **"cheader_opt = opt"** property.(More Details)

SystemRDL Enhancement

1. F#15238 - Enhancement has been done to change naming convention in UVM and C-header to change the original name as primary instead of an instance name in case of parameter overriding using "**inst_name_cppstyle=true**".(More Details)

Bug Fixes

RTL

1. F#15865 - Fix for missing iterator when repeated sections are used while generating SystemVerilog output.
2. F#15841 - Fix in verilog for multi-bit fields when CDC hardware synchronization is used.
3. F#15843 - Fix in verilog for compilation error when using "**rtl.hw_wp"** on wide registers.
4. B#1308 - Fix "<regname>_<field>_in_enb" port being formed outside the port list in case of **"we"** property in verilog2001.
5. B#1354 - Fix in "rd_valid_out" signal in case of a deep hierarchy of repeated sections in verilog output.
6. F#15558 - Parity is supported with hierarchical repeat in verilog.
7. F#16043 - Fix for parity per byte register when the least significant bit of field in a register is not 0.
8. F#15969 - Fix for generation of unused wires when **"rtl_hw_vector"** property is used to generate verilog output.
9. F#15924 - Fix in **"rtl.hw_enb"** property with read only s/w access:
    a. When the property is applied on top with "-fast" switch
    b. When the property is applied in combination with **"rtl.precedence=sw"**
10. F#15932 - Fix has been done to match the "addr_decode" to stride size when stride is used for verilog output.
11. F#15910 - Fix for "rd_wait signal" logic in verilog when a flopped version of APB widget is used.

12. F#15977 - Fix in parsing issue when lock property in combination with **"rtl.name_format"** is applied.

UVM

1. B#1180 - Fix in the status of individually accessible bits.
2. B#1250 - Fix for interrupt callback.
3. B#1344 - Fix for missing lock callback class when lock registers are specified inside the section and the section itself is referred multiple times along with dynamic assignments.

C Header

1. F#15275 - Fix for removing "_e" from the generated enums in header output with **"cheader_opt=true"**.
2. B#1355 - Fix for spacing issue when **"cheader_name_format"** property is used in Chip-in-Chip scenario for optimized headers.
3. F#15888 - Fixed filter issue in headeralt2 when stride is used in the register specification.

IP-XACT

1. F#15470 - Fix for compilation issue when enums take hex values.
2. F#14700 - Fix for reset value of fields while importing IP-XACT files.

General

1. B#1253 - Fix for non-inclusion of leaf files in the top file has been done for c_api output when **"multi-out(-if)"** option is used.

2. F#14575 - Fix newline issue in markdown output.

3. F#15196 - Fix naming inconsistency in SVHeader output for Chip-in-Chip flow with deep hierarchy.

4. F#15912 - Fix for hiding reserved field's name when **"is_rsv"** property is used along with **"variant"** and **"doc_unused_remove"** for HTMLalt2 output.

5. F#15941 - Fix address calculation of ToC in IDS-Word.

6. F#16085 - Fix stride calculation for repeated registers for HTMLalt2 and PDFalt2 outputs.

7. F#15544 - Fix for importing IP-XACT file in IDS-Calc and IDSExcel.

8. F#15594 - Fix for importing SystemRDL file in IDSExcel.

9. G#IDSBatch#319 - Fix for incorrect offset calculation issue when **"html_show_reserved_bits"** property is used.

10. F#16087 - Fix for generating html file with extension .htm instead of .html.

ISequenceSpec™ (ISS)

Enhancements

1. B#1297 - Enums are supported in the python input format.(More Details)

2. B#1297 - Write/Read registers by accessing structs in Firmware output.(More Details)

3. B#1297 - Users can use Nested structs in the python input format.(More Details)

4. G#IDSCalc#322 - "Return type" option for SystemVerilog is now available in the configure window of IDS-Calc.

5. G#IDSExcel#15 - "Return type" option for SystemVerilog is now available in the configure window of IDS-Excel.

Bug Fixes

1. B#1168 - Fix for missing begin-end in case of fork-join for UVM sequence output.

ARV™

Enhancements

1. B#1212 - Support of repeat property with memory for arv output.(More Details)
2. B#1346 - Supported Sequences for repeated registers.

Bug Fixes

1. B#1276 - Fix for incorrect instantiation of RTL in the "Top.sv" file when both verilog and VHDL are generated with arv.
2. B#1350 - Fix for APB Driver hang issue when both internal and external components are used together in the registermap.

Specta-AV™

Enhancements

1. B#1210 - VHDL RTL is now supported with Specta-AV.(More Details)
2. B#1248 - 'assert', and 'wait' keywords are now supported in python checkers.(More Details)
3. B#1248 - Support for parallelism, i.e., fork-join, fork-join_any, and fork-join_none in python checkers.(More Details)
4. B#1291 - Capability of Checkers in Specta-AV has been enhanced with support of loops in checks: (More Details)
    a. While
    b. Do-while
    c. For

5. B#1347 - Support of Interrupt Classification i.e. intr.out, intr.per_channel in middleware events.(More Details)

Bug Fixes

1. B#1210 - Fix for missing event declaration in ModelUpdater when **"rtl.hw_rp"** property is used.
2. B#1165 - Compilation fix in Specta-AV when no checker is present.
3. B#1352 - Fix in display function in checkers for printing value of variables.
4. B#1258 - Fix for compile error when predefined assign library is used in checkers.
5. B#1210 - Fix in model updater file for deep hierarchy.
6. B#1351 - Support for multiple checks into the checker on the same event.
7. B#1348 - Fix in wrapper file when external register is specified.
8. B#1210 - Fix for deep hierarchy in Model Updater with **"repeat"** property.

SLIP-G™

Bug Fixes

1. G#IDSNG#275 - Fix for missing counter_width parameter in the parameter table of TIMER IP.
2. G#IDSNG#275 - Fix for incorrect count of status and enable register when default generation parameters are used for TIMER IP.
3. G#IDSNG#275 - Fixed register and field repeat value issue for PIC and TIMER IP.
4. B#1292 - Fix for syntactically incorrect code of GPIO IP in the following cases:
   a. When two or more GPIO IPs are defined inside a chip.
   b. When pin width is greater than 32.
   c. When "custom" bus protocol is used.
5. B#1293 - Following fixes are done in I2C IP:
   a. Incorrect instantiation of register map in the top file.
   b. Double port connection of "irq" port in chip and block.

c. Undefined wires in chip file, missing top connections, and unwanted ports connections.
d. Syntactically incorrect code when "custom" bus protocol is used.

6. B#1295 - Following fixes are done in TIMER IP:
    a. Incorrect port connection of irq port while instantiating top in chip file.
    b. Syntactically incorrect code due to duplication of "clk" signal when "custom" bus protocol is used.
    c. When multiple TIMERs are taken inside a chip, then while instantiating the top of each TIMER IP at the chip, there are multiple connections to the "clk" port.

ASVV™

Enhancements

1. B#1306 - Following are the enhancements in ASVV

    a. Chip-in-Chip support
    b. AMBA AHB bus is supported

2. B#1217 - Out of Box 100% coverage supported for all software register accesses.(More Details)

3. B#1172 - Chip support with multi-out option.

4. B#1223 - Single line interrupt support.

Bug Fixes

1. B#1306 - Fixes related to assertion in case of bus protocol violation.

IDS NextGen™ (IDS-NG)

Enhancements

1. G#IDSNG#17 - Supported hinting of multiple sequences, arguments, constants, and variables in sequence view.

2. G#IDSNG#18 - Supported API hinting in Specta-AV™.(More Details)

Bug Fixes

1. G#IDSNG#275 - Fix for parameters according to the register table and define.

2. G#IDSNG#275 - Fix for register insert template according to configure windows value given by user.

3. G#IDSNG#275 - Fix for incorrect width value in signal table.

4. G#IDSNG#21 - Fixed IDS-NG license issue (Now users will be able to use IDS-NG editor, if the license expires).

5. G#IDSNG#22 - Fix for removal of ref template name while switching from register view to spreadsheet view.

6. G#IDSNG#284 - Fixed missing context menu on click in the spreadsheet view.

7. G#IDSNG#284 - Fix for insert, cut, copy, and paste rows and columns in the spreadsheet view.

8. G#IDSBatch#15282 - Fix asp perl compilation issue while importing RDL file.

9. F#16047 - Fix issue of java FX warning message in Runtime environment of IDS-NG.

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