# Release Notes

## v7.16.0.0
***(July 7th, 2021)***
## IDesignSpec™ (IDS)
**RTL Enhancements**

1. B#1017 - **"custom_sync"** property has been introduced to allow users to add their custom logic for FF chain in CDC. (More Details)

2. B#1017 - **"cdc.reset"** property has been enhanced to modify the HW reset with CDC. (More Details)

3. B#1017 - HW write pulse synchronizer has been added in the *handshake_synchronizer.v* file for hw writable single bit fields when combination of **"rtl.hw_enb=false"** and **"cdc.clock=<hw_clock>:handshake"** properties is used. (More Details)

4. F#15644 - Clock Domain Crossing from software side has been supported with AXI bus for VHDL output.(More Details)

5. F#12261 - **"rtl.strict_ports"** property has been introduced for removing write/read ports for external CSRs with read-only/write-only SW access.(More Details)

6. B#1072 - **"external_ack=wishbone_widget_ff"** property has been introduced to remove dependency of read/write transactions of internal registers on external registers. (More Details)

7. F#11576 - **"buffer_trig_reg"** is supported with -fast_verilog switch for speeding up verilog generation process. (More Details)

8. F#14844 -**"widget"** property has been enhanced to support multiple bus domains. (More Details)

9. F#15540 - **"rtl_external_pkg_unique"** property has been introduced in SV output to generate unique package files for all external CSRs.(More Details)

**C header Enhancements**

1. F#15275 - **"cheader_opt"** and **"cheader_add_regmap"** properties have been introduced to support relocatibility of macros and register structs. (More Details)

2. F#15552 - Alternate registers are supported in C-header output.(More Details)

**SystemRDL Enhancements**

1. F#15601 - Dynamic assignment per instance has been supported in SystemRDL output for following properties: (More Details)

a. reset
b. hdl_path
c. name
d. desc

2. F#15598 - Chip-inside-chip flow is now available in SystemRDL output. (More Details)

**General Enhancements**

1. F#15270 - Hardware and software reset signals are now supported in IDS generated IP-XACT output.(More Details)

2. F#11593 - Supported "**ipxact_exclude_venderextensions=true**" property to exclude "spirit:vendorExtensions" nodes from the IP-XACT output.(More Details)

3. G#Java#289 - IDSCalc has been enhanced with enums, defines and params templates.(More Details)

## Bug Fixes

**RTL**

1. F#15429 - Fixed parity per byte with repeat on register/section.

2. F#15097 - Fixed external decode with repeat, stride and alignment on the external register.

3. F#15633 - Fixed iterator name issue for repeat on section with **"explicit_name=true"** property.

4. F#15450 - Fixed lint warnings in case of dynamic assignment of reset.

5. F#15638 - Fixed redundant wire declaration issue when protection is used for external registers.

6. F#15665 - Fixed the compilation issue in case of external components when used with **"addressing=regalign''** property.

7. B#1150 - Fixed read value of fields that are not explicitly defined when **"rsvdset"** property is used.

8. B#966 - Fixed missing 'end' of conditional statement when **"counter=incr/decr"** is present with **"counter.precedence=hw"** property.

9. B#1061 - Fixed syntax issue for missing ‘end’ statement in the generated verilog code when alias registers are used with **“rclr=false”** property.

10. B#890 - Fixed extra ‘end’ issue when **“buffer_trig”** with “**cdc.clock”** property is used.

11. B#1190 - Fixed instantiation of the wrapper file in *top.sv* file when sv and arv output are generated simultaneously.

12. F#15828 - Fixed the empty address issue in case of RAZWI behaviour.

13. F#15800 - Fixed issue where empty addresses were getting generated outside the genvar in case of the external section inside the repeated section.

**UVM**

1. F#15600 - Fixed hdl paths when parameterized values are assigned to the **“hdl_path”** property.

2. F#15693,15710 - Fixed naming issues with **“explicit_name”** property when used along with coverages and alias registers.

3. B#1144 - Fixed callbacks for repeated sections containing alias registers.

**SystemRDL**

1. G#Java#112 - Fixed the tool crash issue for parameterised addrmap in case of definitive definition of component.

2. F#15639 - Fixed non-generation of code in SystemRDL output when **“invalid_addr_err”** property is used.

**C Header**

1. F#15534 - Fixed redeclarations of register union when a register is reused multiple times inside a block in case of SystemRDL input.

2. F#15275 - Fixed variable name of register's union from "w/dw'' to common name "f" with "**cheader_opt**” property in header-alt1 output.

**General**

1. G#Java#274 - Fixed internal Toc hyperlink issue in htmlalt2 output.

2. G#Java#314 - Fixed dynamic assignment issue when signal is given as reset properties' value in pdfalt4 output.

3. G#Java#314 - Fixed enum, param and define value in pdfalt2 output.

4. F#14172 - Fixed issue in htmlalt2 output for the replacement of "\n" character with new line in field's description when enums are used.

5. F#15607 - Fixed address unit in IPXACT input to take up values that are not powers of 2.

6. G#Java#249 - Fixed anchor link and new line issue in Markdown output.

# ISequenceSpec™ (ISS)

**Bug Fixes**

1. F#15623 - Fixed non generation of sequence outputs when the block component has **"addressing=regalign"** property.

# ARV™

**Enhancements**

1. F#15613 - Support for the AldecInc tool, Riviera pro has been provided in ARV. (More Details)

*Note : B#1186 - A sequence library is now available for Riviera pro.*

# Specta-AV™

**Enhancements**

1. B#1195 - Synchronization between VIP agent and Specta-AV bus agent is now available in the custom sequences. (More Details)

2. B#1120 - Pulse property event for middleware has been introduced to provide control over checkers. (More Details)

**Bug Fixes**

1. B#1154 - Fixed port list of the wrapper file when no signals are used in the register specification.

2. B#1067 - Fixed output generation issue when multiple sequences are defined.

3. B#1062 - Fixed ‘makefile’ when a ‘custom’ bus is used for generating Specta-AV.

## ASVV™

**Enhancements**

1. B#1142 - Support of chip-level hierarchy in ASVV.

## IDS NextGen™ (IDS-NG)

**Enhancements**

1. G#Java#222 - Added GUI check-box in config window for quality checks option which is equivalent to command-line switch **'-check_quality'**.(More Details)

2. G#IDSNG#11- Added prop hint for add_vip property in signal table.

3. G#IDSNG#2 - Added hints in the description of all SLIP-G IP’s.

4. G#IDSNG#5 - Supported SLIP-G API’s hinting in sequence view. (More Details)

**Bug Fixes**

1. G#IDSNG#4 - Fixed offset issue for PIC and Timer IPs.

2. G#IDSNG#5 - Fixed description issue for Timer, DMA ,PWM IPs.