v7.38.0.0
(April 1st, 2022)

IDesignSpec™ (IDS)

RTL Enhancements

1. F#16704 - Support of custom string in lock expressions of a field using eval() expression in the verilog output. More Details

2. F#19998 - Support of "sharedextbus" property along with "external_ack=optimized" property in the verilog output. More Details

3. F#16405 - Introduced a new property "**enum_remove**" to remove the unused enums from the RTL. More Details

General Enhancements

1. F#15957 - Support of a new switch "**-third_party_rtl**" to stop the generation of hardware interface and its instantiation in case of third party RTL. More Details

2. B#1650 - Support of a command line switch "**-c_api_return_type <int/hwint>**" to generate an int/hwint type write API in the generated C APIs. More Details
3. B#1661 - Support of a new top property "**spec_ver**" to add corresponding specification/register input design version in IDS generated outputs for version control of the specification. More Details
4. B#1592 - Enhancement for issue in case of block in Address macro the SIZE macro is replaced by PER_INSTANCE_SIZE macro when cheader_opt=true is used. More Details
5. F#16178 - Support of new property in C-Header "**cheader_map_notpresent**". More Details

6. F#19566 - Support of multiple default values in TOC for HTMLalt2 & PDFalt4. More Details

UVM Enhancements

1. G#JAVA#421 - F#16178 - Support for configure IP/Block Offset in the default_map or the map that the user wants to create and configure accordingly.
2. F#16178 - Support of new property in UVM, namely "**uvm_map_access**" and "**uvm_map_notpresent**". More Details

Bug Fixes

General:

1. F#16F#19805 - Fixed the issue of dynamic assignment of HDL_PATH with inst_name_cppstyle=true property.

2. F#19882 - Fixed the issue with IP-XACT file supported in case of ref in RDL with the UDP "inst_name".
3. F#19494 - Fix for the issue in data slides going blank upon clicking on top slide to extend it for lower level heirarchy in SVGalt2 output.
4. F#16178 - Fix in the name of two properties from uvm_mapispresent and cheader_mapispresent to uvm_map_notpresent and cheader_map_notpresent.
5. F#19830 - Fixed the issue with C-Header STRIDE macro and address macro.

6. F#19804 - Fixed the address macro calculation of array in the regfile.
7. F#19819 - Fixed the ERROR post processing message from idsbatch.log.
8. F#19494 - Fix in the switch -disable_overlap_check to give overlap errors as warnings.
9. F#19884 - Fixed the naming issue in the generated .h file.

10. F#19805 **-** Fixed the issue of cheader_add_regmap_offset.

11. F#19452 - Fixed the issue with the naming of alternate registers when tool throws the annotation error upon giving space in the naming of alternate registers.
12. F#19816 - Fixed the issue with IP XACT to xrsl conversion in case of addressBlock having usage mem in IP XACT file.
13. F#20024- Fixed the issue of extra space added in c-header output in case of buffering trigger signal
14. F#19452 - Fixed the issue of space in namings of some alternate registers.

RTL

1. F#19943 - Fixed issues in the generated verilog output in case of bus read pulse on the hardware side with the property 'rtl.hw_rp' on wide registers in presence of low power switch.

2. F#15843 - Fixed issues in the generated verilog output in case of bus write pulse on the hardware side with the property 'rtl.hw_wp' on wide registers in presence of low power switch.

3. F#19652 - Fixin case of 'rtl.hw_wp' property usage with "external_ack=optimized" in the verilog output.
4. F#19673 - Fixed the issue of compilation fail in the verilog output for 'rtl.name_format' with '%f' value.
5. F#17117 - Fixed the issue for 'aggegation_logic=flopped_all' for the flopped aggregation signal.
6. F#19450 - Fix for repeat on memory value of count greater than 214748364
7. F#19866 - Fix for property "rwpair" on field in verilog output.

UVM

1. F#19670 - Fixed the constraint issue when the constraint value of one field is compared with another register field value.

2. F#19559 - Fixed the compilation error because of the instantiation of reg_block which was not getting generated in UVM.

3. F#20055 - Support the default_map removal through the uvm_map_notpresent UDP.

IDS NextGen™ (IDS-NG)

Enhancements

1. F#19391 - Support of eval expression in 2DReg output in IDS-NG . More Details

2. G#96 - Support of dropdown options with possible values in the property pane in IDS-NG. More Details
3. G#95 - Support of dynamic hinting for assign template in sequence view. More Details
4. G#95 Support of dynamic hinting for step in checker view. More Details
5. G#95 - Support for adding different icons for project and directory in project explorer.
6. G#95 - Support for adding all properties in alphabetical order in the property pane.
7. G#95 - Support for adding all project directories in alphabetical order.

10. G#95 - Support for tilelink in IDS-NG configuration window
11. G#95 - Support for IP-XACT and multi-out 2014 in IDS-NG configuration.
12. G#95 - Support of no lint warn option in advanced verification option in configuration window of IDS-NG.

Bug Fixes

1. G#95 - Fixed issue of update Param Issue in case of error in description.
2. G#95 - Fixed issue for chip level properties was not showing in the property pane.
3. G#95 - Fixed issue for error should be redirected to the right specification.
4. G#95 - Fixed issue for slip-g dynamic hinting in sequence view.
5. G#95 - Fixed issues for checker step column and event hinting.
6. G#95 - Fixed colour issues for all dynamic hinting.
7. G#95 - Fixed click issue for running TCL file.
8. G#95 - Fixed issue for sw and hw dynamic access issues in register view.
9. G#95 - Fixed typo issues in configuration of IDS-NG.
10. G#95 - Fixed the issue for chatbot feedback information was not working .
11. G#95 - Fixed the issue of project explorer collapse when click on generate.
12. G#95 - Fixed the issue for adding the correct drop-down option for sw and hw access.

ARV™

Enhancements

1. B#1697 - Support of explicit_name=true property
2. B#1697 - Support of default_clock_name property
3. B#1697 - Support of default_reset_name property

Bug fixes

1. B#1698 - Fixes in dummy external rtl connection in top.sv both for block and chip level scenarios
2. B#1698 - Fixes in sequences for external components(reg/section)
3. B#1698 - Fixes in register sequence for Sw access = Ro and Hw access= Ro register
4. B#1698 - Fixes in Wo sequence with repeat
5. B#1698 - Fixes in hw_if.sv for mixed access of fields when present together within a single register
6. B#1698 - Fix in hdl_path for Ro register in UVM with ARV output.
7. B#1698 - Fix in hdl_path for external registers in UVM with ARV output.

ASVV™

Enhancements

1. B#1692 - Support of external register, external reg_file and memory.
2. B#1693 - Support of different regwidth i.e. 8,16,32 and 64.
3. B#1694 - Support of Cheader alt4 naming convention.
4. B#1695 - Support for repeat on register and sections.

Bug Fixes:

1. B#1696 - Fixes in naming convention for support Cheader alt4
2. B#1696 - Fixes in ctest for naming convention related Defaults, readmask, writemask and registermask

SLIP-G™

Bug fixes

1. G#223 - Fix for compilation fail in RTL when the generation parameter NUM_SRC=1 was being used for the TIMER IP.