v7.4.10.0

(December 19th, 2020)

IDesignSpec™ (IDS)

RTL Enhancements:

1. "rtl.name_format" has been supported with "sv_interface=struct" property in system verilog output. (More Details)

2. "singlepulse=true" has been supported in both alt1 and alt2 versions of VHDL. (More Details)

3. "svout_filename=<any string>" has been supported to alter the filenames in system verilog output. (More Details)

4. The data type of offset is changed from natural to unsigned (63 downto 0) in VHDL. Now offset can hold value upto 2^63 value in VHDL.

5. "lock.clear", "lock.set", and "lock.toggle" properties are supported with all software accesses and with repeated registers. (More Details)

6. "RAZ/WI" (Read As Zero and Write Ignore) behaviour has been supported in verilog output. (More Details)

7. Arrayed signals are supported in "buffer_trig_reg" property for verilog output. (More Details)

UVM Enhancements:

1. Supported chip-in-chip functionality along with "-vertical_reuse" switch in UVM RAL output. (More Details)

C Header Enhancements:

1. Flexibility of suppressing descriptions is now provided in cheader output using the "description" property. (More Details)

SystemRDL Enhancements:

1. There is a change in behavior for register with sw access = r and hw access = w to comply with SystemRDL 2.0 Standard. Earlier IDS created a flop now there will be a wire/bus hardware assignment. (More Details)

General Enhancements:

1. Parameter overriding has been supported for uvm and cheader output. (More Details)

2. Chip-inside-chip has been supported for vheader, svheader, HTML-alt2 and cheader output. (More Details)

3. "doc.rm_signal" and "doc.rm_variant" properties have been supported for removing signal and variant tables in HTML-alt2 output. Users can remove multiple tables by specifying multiple values in this property separated by a comma, e.g., "doc.rm=signal,variant,enum,define" property. (More Details)

4. Dynamic array assignment has been supported in HTML-alt2 output. (More Details)

5. "Lock" property has been enhanced with repeat on section in uvm and rtl output. (More Details)

6. Stride on repeated instances of any block, section, or register entity that refers to the address of an instance's address in an array of components. (More Details)

Bug Fixes:

RTL

1. Fix for mbd in VHDL-alt2 output.
2. Fix for verilog generation when "secded=false" is used on registers.
3. Fix for hex values in multiple default values with repeat on register.
4. Fix in redundant *_enb signal formation when rtl.reg_enb=false property is applied in system verilog output.

5. Fix in verilog output for an extra "generate" and "endgenerate" construct, when "intr.irq_per_channel" property is applied.

6. Fix in block_size parameter value for verilog2001 output.

7. Fix in module_name property for file generation and naming issue, when a block is referred multiple times in the same top chip container.

8. Fix for verilog generation when "buffer_trig_reg" property is used.

UVM

1. Fix for issues in asynchronous logic for AXI4FULL widget.
2. Fix for the hex values in multiple default for repeated registers.

ARV

1. Fix for sequences not being hit leading to reduced coverage when repeat is used on register/section.

2. Fix for "reset_level" property for improving coverages in ARV.

General

1. Fix for null pointer issue in "desc" property along with chip-in-chip functionality in HTML-alt2 output.

2. Fix for integer variable name in case of "-c_type" switch with stride property in cheader output.

3. Fix for size issue in IP-XACT parser.

4. Fix for IP-XACT and System RDL import issue in IDS-Word and IDS-Excel.

5. Fix for back annotation issue for large spec in IDS-Word.

6. Fix for "BigInteger Length" issue in HTML-alt2 output.

IDS NextGen™ (IDS-NG)

Enhancements:

1. First row of param view, containing bit indices, is now freezed when scrolling down.

Fix:

1. Fix in eval function for dynamic names and properties. (More Details)