v7.8.0.0

(March 3rd, 2021)

IDesignSpec™ (IDS)

RTL Enhancements

1. 'Next' property is enhanced to support two-way conditional assignment of next input value in a field. These conditions can be read/write events of another internal register of the block IP. (More Details)

2. Single and double bit errors can now be injected while using SECDED with the help of property "secded_error_inject". (More Details)

3. Interrupts are now supported with repeat on multiple components in hierarchy. (More Details)

4. "rwpair" is supported at field level in Verilog. (More Details)

5. I2C is now supported in VHDL. (More Details)

6. "param.name_format" property is supported to customize the name of the count parameters in Verilog and SystemVerilog. (More Details)

UVM Enhancements

1. Multiple bus domains have been supported with different accesses of fields within a register. (More Details)

2. "rtl.sw_write = clear" property is supported in UVM to clear register values in the next cycle. (More Details)

3. "uvm_class_name_inst" property is supported to generate classes with the instance name to maintain backward compatibility with 6.x series. (More Details)

SystemRDL Enhancements

1. A pulse will be generated at the hardware interface when a field is accessed by software using "swacc" UDP. (More Details)

Cheader Enhancements

1. Property “ispresent=true/false”/”is_rsv=true/false” is supported in Cheader output. (More Details)

General Enhancements

1. Supported "show_display_name" property to use display name instead of instance name in html-alt2 and pdf-alt4 output . (More Details)
2. Japanese characters are supported for pdf-alt2 output. (More Details)

3. “field_sort=true” property is supported to sort field bits in ascending order in html-alt2 output. (More Details)

Bug Fixes

RTL

1. Fix for “sv_guard_band” property with “sv_interface = struct” property in System verilog output.

2. Fix for clock connection issue in SystemVerilog structs while using CDC.

UVM

1. Fix for issue in dynamic assignment of reset while referring components.

2. Fix for “dontcompare” property with third party output.

3. Fix for vertical reuse issue in case of chip-in-chip functionality.

4. Fix for issues in file header for endianness being used while generating output.

5. Fix for documentation level parameters on top-level while referring sub-components.

General

1. Fix for declaration and usage of parameters at chip level in vheader output.

2. Fix for address calculation incase of “multiout” option in Cheader output.

3. Removed an extra mask macro for single bit field to avoid ambiguity in Cheader output.

4. Fix for unwanted spaces in description of output files when generated using tcl format.

5. Fix for size/offset calculations in case of "addr_mux" property while importing IP-XACT input file.

6. Fix for MISRA-C output to make it compliant with MISRA-C standard.

7. Following fixes are done in SystemRDL compiler:
   a. For UDPs whose boolean values are not specified, by default. Now, it will be considered as true.
   b. For usage of defines in register specification. Defines can now be used with ` character.

8. Fix for new line issue in description of field when using enum on particular field component in html-alt2 output.

9. Fix for issue in dynamic assignment of reset while referring components in html-alt2 output.

10. Fix for [br] tag in pdf-alt2 output while using SystemRDL input.

SLIP-G™

1. Following IPs have been added in the standard library:

   a. SPI (More Details)
   b. DMA (More Details)
2. Decrement feature is now available in TIMER IP. (More Details)

ISequenceSpec™ (ISS)

1. PSS 2.0 version is now available as output in ISS. (More Details)

SoC-E™

1. ASVV™ environment can be created for the top SoC design assembled using SoC-E. (More Details)

IDS NextGen™ (IDS-NG)

Enhancements

- Separate pane for properties in IDS is now available for providing hints. (More Details)
- Supported Hierarchy outline to view hierarchy of current spec like : name, modules and address. (More Details)