v7.48.0.0

(Aug 30th, 2022)

IDesignSpec™ (IDS)

RTL Enhancements

1. F#20951 - Support for protection property in aggregation logic for read and write data protection which can be applied on a block.

Bug Fixes

General

1. F#20435 - Fixed Chinese character issue for PDF and HTMLalt2output in case of excel input.
2. F#21173 - Fixed the default 32-bit signed integer value in JSON output.
3. F#20049 - Fixed IP-XACT 2014 generation issue from configuration in IDS-NextGen.
4. F#20681 - Fixed file generation issue with the switch "-tool VCS" in the command line option in IDS-Word.
5. G#463 - Supported special characters in folder name in IDS-Word input spec.

RTL

1. F#21111 - Fixed synthesis issue in the generated verilog construct incase of fields with multiple reset values.
2. F#21137 - Fixed "reg_hw" property which did not work in the GUI test case when applied on register.
3. F#21210 - Fixed an issue in block_prot=true property in case of third_party RTL.
4. F#21219 - Fixed an issue in the "*_rd_pulse" logic when "rtl.hw_rp" property is used with AXI bus.
5. F#21209 - Fixed an issue in "intr.detect" property when it is applied on a block.
6. F#20478 - Fixed the issue of"rvalid" getting de-asserted before "rready" is asserted incase of back-to-back read in flopped axi4lite widget.

UVM

1. F#19752 - Fixed default value for fields in case of section having multiple default values
2. F#20681 - Fixed the parity callback issue in UVM.
3. F#21184 - Fixed "enum_remove=uvm" property for register and field.
4. F#21272 - Fixed the class name issue incase of a referred element for dynamic assignment.

IDS NextGen™ (IDS-NG)

Bug Fixes

1. G#471 - Fixed FSM template issue in case of switch register view to spreadsheet view in IDS-NG.