Release Notes
v7.10.0.0
(April 6th, 2021)
IDesignSpec™ (IDS)
RTL Enhancements

1. APB flopped widget is now supported in VHDL output . (More Details)
2. "tmr_error" property is now supported in SystemVerilog output. (More Details)
3. Alternate Registers are supported inside sections for Verilog output. (More Details)
4. "intr.detect_nometa" property is enhanced to remove two flop synchronizers. (More Details)

SystemVerilog Enhancements

1. Structs have been supported for chip-inside-chip. (More Details)

UVM Enhancements

1. "rwpair" is supported at field level in UVM-RAL. (More Details)

C Header Enhancements

1. Users can add customised code at the top of header files using [Cheader loc="top"] ... [\Cheader] in description of input spec. (More Details)

General Enhancements

1. IDS generated outputs can be stored on OneDrive in IDSWord and IDSExcel.
2. TCL script is generated using Apache velocity template to instruct synthesis tool to avoid deletion of flops having TMR. (More Details)
3. Support for multiple browse options in the output directory is added in IDSWord and IDSExcel.
4. IDSCalc flavor has been enhanced with SystemVerilog output.
5. Quality checks have been supported in IDS to ensure improved register-map quality using switch 'check_quality'. (More Details)

Bug Fixes

RTL

1. Fix for incorrect error message if top component is not specified when multiple addrmaps are used along with regfile.

2. Fix done for dynamic assignment of parameterized software access of field in htmlalt2 output.

3. Changes in naming convention of referred blocks when multi-out option is used for Verilog output in IDSWord and IDSExcel. Henceforth, naming will depend upon the name of the blocks, instead of the foremost register inside the block.

4. Fix for incorrect code generation when "rtl.bit_enable=true" property is used along with "rtl.byte_enable=false" property.

5. Fix for compilation error when write pulse is used with "rtl.byte_enable=false" and "rtl.bit_enable=false" properties.

6. Fix for reserved lsb of register while generating Verilog output when either "rsvdset" or "rsvdsetX" property is used in register specification.

7. Fix for extra begin-end when alias property is used with hard reset.

8. Fix for missing iterators when "registered = false" with repeat property for deep hierarchy.

9. Fix for asynchronous reset in chip-in-chip flow.

10. Fix for making enum names unique when same name enums are used on different registers for Verilog output.

SystemVerilog

1. Fix for formation of redundant wires when repeat property is used on multiple components in deep hierarchy.

UVM

1. Fix for combination of multi-valued reset fields and single-valued reset fields defined inside a register.

2. Fix for missing iterator in add_submap when "uvm_add_regmap" property is used along with repeat.

3. Fix for lock registers when declared inside repeated blocks.

4. Fix for incorrect RAL generation when parameters are declared in input specification but not used.

5. Fix for naming convention while using "%p" format specifier in "uvm.reg_name_format" property.

C Header

1. Fix for generation of fillers when reserved registers are used.

SystemRDL

1. Fix for "ids_we" UDP to take up values in the following format:

   <register>@<property>

IP-XACT

1. Fix done for "snps_ralgen=1" property when used along with hdl_path.

2. Fix for reserved empty blocks when PDF-alt2 output is generated using IP-XACT input specification.

General

1. Fix for -html_css switch while generating single file for HTML-alt2.

2. Fix for incorrect configuration in XML files when exported from IDSExcel specification.

3. Fix for "\n" in description for Markdown output.

4. Fix for line break issue in HTML and SystemRDL output.

5. Fix for [sp] tag (space issue) in SystemRDL 2.0 output.

6. Fix for multiple enums being used inside a register when HTML-alt2 and PDF-alt4 outputs are generated.

7. Fix for properties column header in IDSExcel input while generating Verilog and VHDL output.

8. Fix for issue in code generation when "sv_param=true" property is used for SVHeader output.

9. Fix in enum property to make it compatible to be used on fields, as per their sizes for SVHeader and VHeader outputs.

SLIP-G™

1. Following IPs have been added in the standard library:
   a. AES (More Details)
   b. PWM (More Details)

2. SPI (More Details) and DMA (More Details) IPs are now available in IDSWord.

Bug Fixes

1. Fix for interrupt generation of GPIO and TIMER IP at chip-level.

2. Fix for core of IPs not being included in the chip.

3. Fix for incorrect instantiation of register map in the core of PIC and GPIO IP.

4. Fix for incorrect generation of ports in TIMER IP.

ISequenceSpec™ (ISS)

Enhancements

1. Support for variants in sequences to control their flow. (More Details)

2. Read/write operations are supported on hardware interfaces(More Details) and memories(More Details).

3. "enum.name_format" property is supported in sequences to uniquify mnemonic names of enum for SystemVerilog and Firmware sequences. (More Details)

Bug Fixes

1 . Fix usage of parameters, defines and enums in sequences. The values for these can now be taken from the register specification.

ARV™

Enhancements

1. Memory is supported in ARV with VHDL RTL. (More Details)

Note:- Sequences will be encrypted moving forward.

Bug Fixes

1. Fix for compile error in external memory and external register.

ASVV™

Enhancements

1. Customised sequences are now supported. (More Details)
2. Mentor simulator is supported to be used with ASVV generated files. (More Details)

IDS NextGen™ (IDS-NG)

Enhancements

1. Outline views for C-APIs, Checkers and sequences are now available in hierarchy views.
2. Property Views has been added for register views in IDS-NG (More Details).