v7.6.0.0

(February 3rd, 2021)

IDesignSpec™ (IDS)

Verilog/SystemVerilog

1. SRAM based register implementation has been supported with "mapto_dpsram" property. (More Details)

2. Wide access memory is enhanced to aggregate the individual smaller reads by introducing read back buffer stages via "wide_external_access = true:r" property. (More Details)

3. Functionality of error injection is added in TMR to ensure a more reliable system. (More Details)

4. SECDED is enhanced with "ro" hw access. (More Details)

5. Support for conditional next assignment in field w.r.t software read/write events of another internal register in the IP. (More Details)

6. Dynamic assignment of conditional next input value in a field w.r.t iterations on its repeated parent register/register group depending on read/write events of another internal register in IP. (More Details)

7. New property "rtl.field_enb" is introduced to indicate that the master has a transaction on the field. (More Details)

8. "dynamic_empty_address" property is now supported for AXI and AXI4FULL bus in Verilog output. (More Details)

VHDL

9. "assign" property is now supported for VHDL output.(More Details)

10. AXI4FULL bus widget is supported in VHDL. (More Details)

11. Tilelink bus is now supported for both alt1 and alt2 versions of VHDL output. (More Details)

PDF-alt2

12. Supported stride on repeated instances of block, section, or register in PDF-alt2 output. (More Details)

13. "doc.rm_signal" and "doc.rm_variant" properties are now supported in PDF-alt2 output for removing signal and variant tables. Users can remove multiple tables by specifying multiple comma separated values in this property, e.g., "doc.rm=signal,variant,enum,define". (More Details)

14. Supported standard constructs (BB Code) of SystemRDL in PDF-alt2 output. (More Details)

HTML-alt2

15. Supported markdown input for "add_doc" property in HTML-alt2 output. (More Details)

16. Generation time for generating HTML-alt2 output has been significantly improved.

17. Earlier, the default existing sw and hw accesses for field definition were used to be statically unchanged. But now, we can overwrite the software access of any register during run time using parameters.

PDF-alt4 (New Output)

18. IDesignSpec has been enhanced with following new outputs:
    a. PDF-alt4 output, which will give capability of customization to the users (More Details)
    b. Markdown output (More Details)

    Note- Both the above mentioned outputs are supported with Advance and SoC licenses

UVM Enhancement

19. Enhancement done for changing the sw and hw accesses for the field definition on run time which are usually statically unchanged, using parameters in UVM output. (More Details)

SystemRDL Enhancement

20. The default reset value of the field is changed from 0 to unknown(x) to match System RDL specification. For maintaining backward compatibility, users may use -top_property "default_reset = 0" in the command line or may specify "default_reset = 0" in the specification itself. (More Details)

21. Guard band has been supported in SystemRDL output.

ARV Enhancements

22. Tilelink bus is supported in ARV.

23. Sequences for lock.clear, lock.set, and lock.toggle property are updated.

Bug Fixes

SystemVerilog

1. Fix for duplicate naming of instances of bus interfaces in case of multiple bus domains when the same type of bus is used multiple times.

2. Fix for issue in naming convention when "sv_interface=struct" UDP is used while generating system verilog output.

3. Fix for removal of "`include" directives from top chip in case of "-filelist" switch.

VHDL

4. Fix for passing part selection of signal as a value in "next" property.

Verilog

5. Following fixes are done for TMR:
   a. Fix for "tmr" property when used along with interrupt.
   b. Fixes in "tmr" and "tmr_error" properties in port declaration.
   c. Fixes for "tmr" and "tmr_error" properties when used with repeat.
   d. Fixes in"tmr" property with -lowpower switch.

6. Following fixes are done for SECDED:

a. When default value is passed as value to the property.

b. Flops being optimized away and the secded_gen modules being deleted.

c. When reserved fields are used in the registers.

7. Fix done for interrupt registers when repeated sections are used inside another section.

8. Fix for port declaration issue for third party output RTL in 2001 version of Verilog.

9. Fix for incorrect generation of verilog code when post register is not defined while using interrupts.

General

10. Fix for RDLFormatCode constructs, like, list, [instname], [index], and [parent_index] tags in PDF-alt2 and HTML-alt2 output.

11. Fix for issue of getting bare HTML syntax in PDF-alt2 output.

12. Fix for line return (\n) in index file for HTML-alt2 output and in general for all other outputs when SystemRDL is taken as an input.

13. Fix for redirection of child elements and disappearance of descriptions in the index file when chip-inside-chip scenario is used in HTML-alt2 output.

14. Fix for description issue in HTML-alt2 output (with htmlalt2_dep) when enum is used in SystemRDL input.

15. Fix for dynamic array assignment in JSON output.

16. Fix for address and size calculation in chip-inside-chip scenario.

IDS NextGen™ (IDS-NG)

IDS-NG Enhancements

1. Multiple rows can be cut/copied and pasted in the "Param" view. (More Details)

2. Param view and register view are now synchronised to maintain the order of the components in the specification.

3. Resolutions of the buttons and graphics are improved in the toolbar. Also, the dashboard has been updated. (More Details)

4. A single centralized library will now be created in the installation directory, rather than creating a separate library for each project.

5. Added advanced import options, like, “xml_addr_mux”, “ipxact_exclude_param” and “ipxact_compact” for importing IP-XACT files in IDS-NG. (More Details)

IDS-NG Bug Fixes

6. Fix for declaration of parameters and defines in the generated outputs.
7. Fix for extra column issue in creating new spreadsheet spec.
8. Improvement in validation and error messages for variant table.
9. Removed unnecessary warnings messages while starting up a project on linux.