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A flexible and customizable flow for IP connectivity and SoC design assembly

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(Host)

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(Presenter)

Agenda

- Introduction to SoC assembly
- Challenges faced by SoC design companies
  - Handling complexity, size and performance
  - Driving down the cost
  - Shorter product shelf life
  - Enhancing productivity of design teams
- Challenges faced by SoC design engineers
  - Volume of IPs and their connections
  - Combining automation with flexibility
- SoC design methodology changes for assembly
- Solution: SoC Enterprise™
- SoC Enterprise™ Features
- Demo
- Benefits/Features of SoC Enterprise™
- Conclusion

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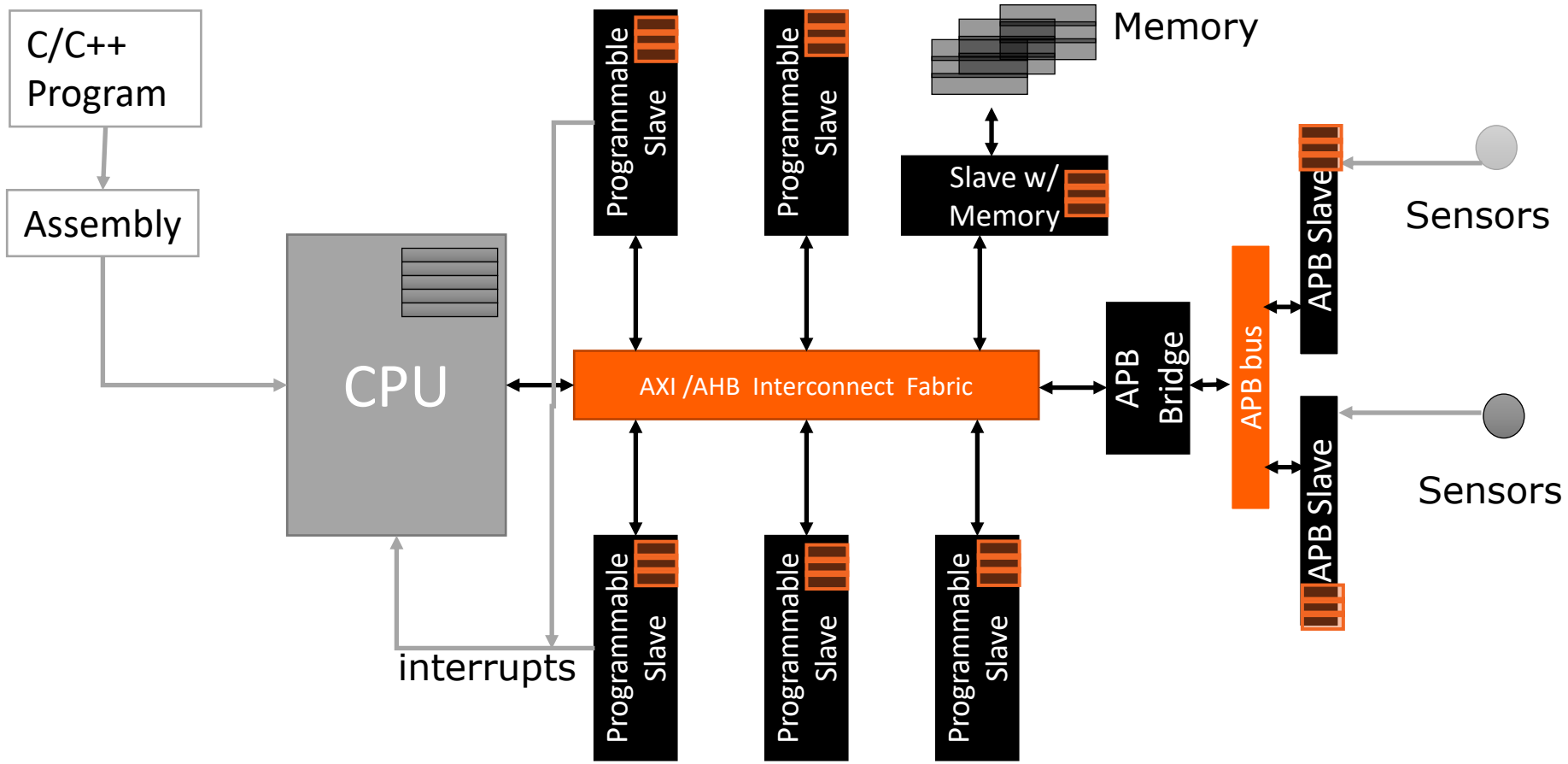
- Introduction to SoC assembly
- Challenges faced by SoC design industry
- Challenges faced by SoC design engineers
- SoC design methodology changes for assembly

Introduction to SoC assembly



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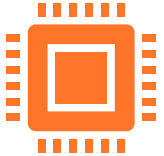
Challenges faced by SoC design companies

- Increasing demands of design complexity and design performance due to convergence of applications on single device

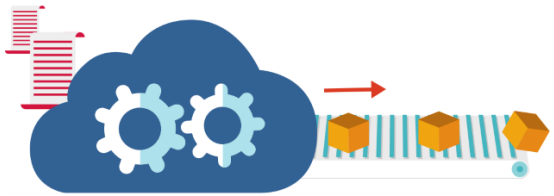


- Driving down the cost of design and amortize it over several applications for a better ROI

- Shrinking market windows due to shorter product shelf lives

- Boosting the productivity of the design teams significantly to utilize the shorter market window besides lowering the costs

- **Solution:** methodology changes that can help accelerate assembly of chips and systems through one or multiple forms of automation



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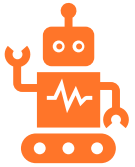
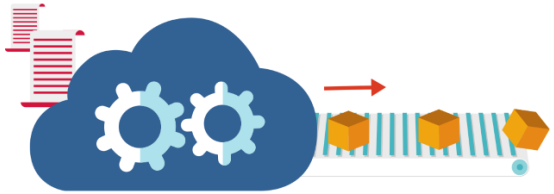
Technical challenges faced by SoC designers

- Volume of IPs, their connections in an SoC grows exponentially with size and complexity making it very difficult to handle
  - Typical SoC may contain 500 or more IPs, having an average of 50 ports each leading to 25,000 or more connections
  - Using spreadsheets to capture connectivity and generating RTL through scripts has scaling limitation

- Combining automation with flexibility to accommodate changes in sub-systems across applications



- **Solution:** Flexible, customizable and configurable IP and sub-systems generators and SoC assembly tool to handle connectivity of large systems automatically



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SoC design methodology changes for assembly

- SoC assembly tools to support architectural level chip assembly
  - Capabilities to create and edit a design on the go through scripts or command line interface
  - Automate the assembly by adding instances in the design, making connections, restructuring, etc.
  - View the resulting schematics for analysis
  - Run checks and generate different output collaterals for design, verification and software teams altogether

- Automatically generate major sub-systems of an SoC design with flexibility to customize and/or configure for accommodating changes

- Using interfaces/structs/bundles for connections reduces the total number of connections to be specified by more than 90%

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Solution: SoC Enterprise™

SoC Enterprise™

- A flexible and customizable environment for design assembly
- A commercial tool which is generic, standards compliant (IP-XACT - now IEEE 1685-2014) and brings a fresh perspective
- Automatically generates integration logic components and sub-systems leveraging already existing and mature register solution along with SLIP-G™
- Supports the latest IP-XACT standard and "standard" vendor extensions in addition to RTL and other IDesignSpec™ supported formats
- Helps create, package, integrate, and reuse IPs and SoC/FPGA

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SoC Enterprise™ features

- Enterprise level SoC development with teams spread around the world
- Smart assembler, as it generates components such as aggregator, bridges, and muxes, as needed
- Supports command mode through text-based APIs and GUI mode fully integrated in IDSNG™
- Can include IPs created from following sources:
  - IPs created by user manually
  - IPs generated by SLIP-G™
  - RTL/IP-XACT generated from specifications using IDesignSpec™,
  - Third party IPs in RTL/IP-XACT format

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SoC Enterprise features

- Ability to import/export RTL
- Ability to define user defined properties, which can be used by generators
- Flexibility to abstract ports to efficiently capture connections
- Ability to easily specify tie-offs, intentional opens and other special cases, where needed
- Ability to easily reconfigure an IP as needed or update the current version with a later version
- Support for interface to internal tools and other third-party tools
- Built in design rule checks to validate design connectivity before generating RTL
- Flexibility to add custom design rule checks for users
- Support for flexibly generating documentation

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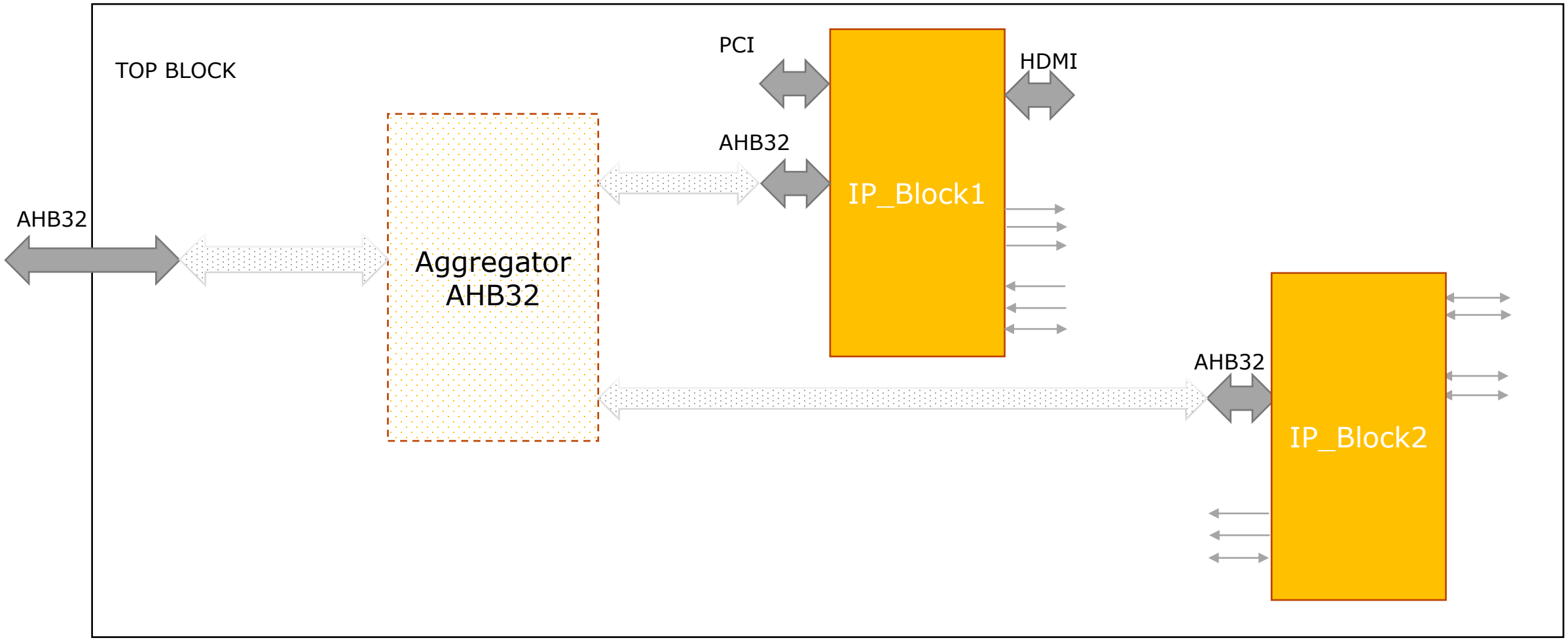
SoC Enterprise™ demo

Auto generation of integration logic in SoC Enterprise™ – bus aggregators



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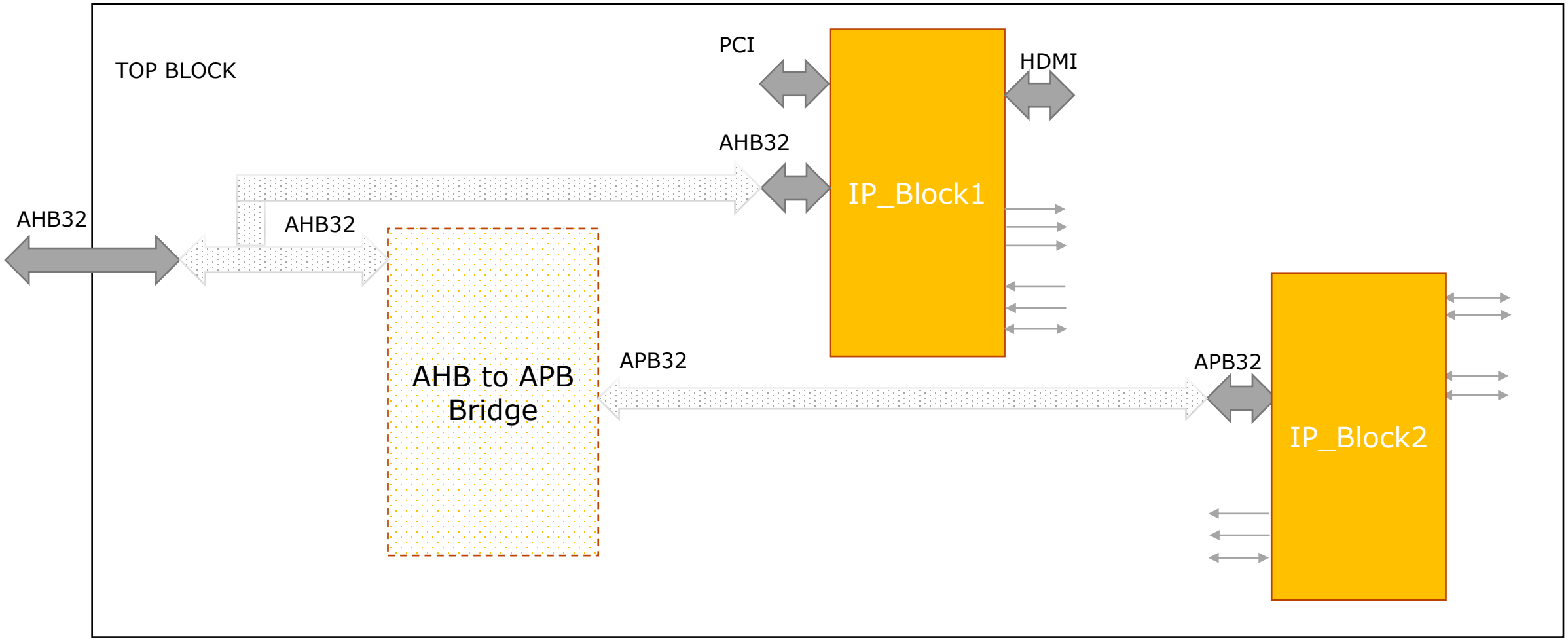
Auto generation of integration logic in SoC Enterprise™ – bus bridges



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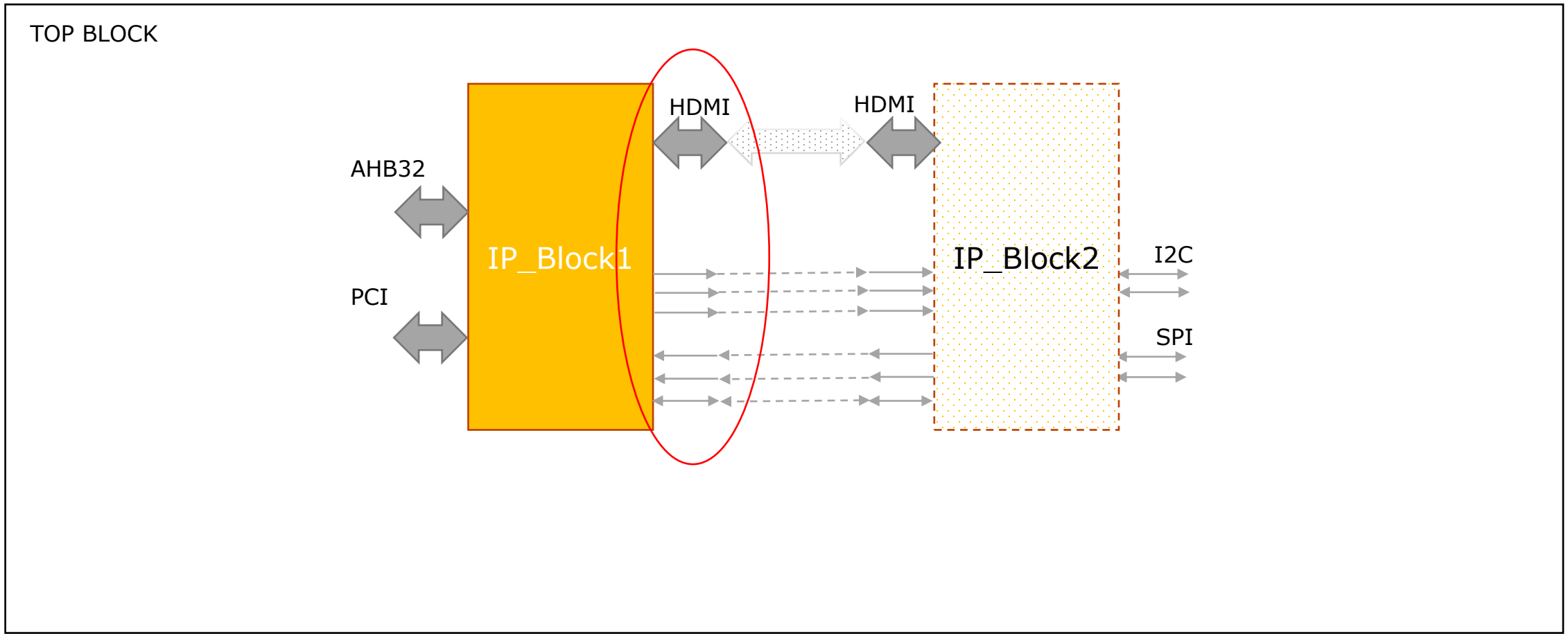
Auto generation of integration logic in SoC Enterprise™ – mirrored block (customizable)



```
press 'soce' to run soce command
SoCE shell activated
help -all for all help
help -create for create command
help -read for read command
help -add for add command
help -connect for connect command
help -promote for promote command
help -generate for generate command

add -type <type> -target <target-name> | -target_inst <target-instance-name> -souce <source-name> | -source_inst <source-instance-name> [-ports <port-list>] [-bus <bus-name>]
    -type /
    -target <target-block-name> | -target_inst <target-instance-name> required when type is block
    -source <source-block-name> | -source_inst <source-instance-name> required when type is block
    [-ports <port-list>
    -bus <bus-name>
```

```
s> help -add
```

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DashBoard | run_sample.tcl ✕ | Graph

```
iread -file {"F:\Work\SoCEnterprise\SoCEnterprise_Demo_May_21\sample\ips\SimpleProperties_ipxact.xml" "F:\Work\SoCEnterprise\SoCEnterprise_Demo_May_21\sample\ips\gpio.v"
"F:\Work\SoCEnterprise\SoCEnterprise_Demo_May_21\sample\ips\timer.v" "F:\Work\SoCEnterprise\SoCEnterprise_Demo_May_21\sample\ips\ahb_master.v"} -bus amba


create -type block -name block1_top -top
add -target block1_top -name Chip1model_ids -inst Chip1model_ids_inst
add -target block1_top -name ahb_master -inst ahb_master_inst
add -target block1_top -name gpio_ids -inst gpio_ids_inst
add -target block1_top -name timer_ids -inst timer_ids_inst
add -type port -target block1_top -bus ahb -ports {p1:input p2:input p3:output:[0:2] p4:input }

connect -target "block1_top.p1" -source_inst "timer_ids_inst.irq"
connect -target_inst "gpio_ids_inst.status_fld_in" -source_inst "timer_ids_inst.counter_F1_r"
connect -target "block1_top" -source_inst "timer_ids_inst" -bus apb

promote -unconnected -source_inst timer_ids_inst -target block1_top

connect -target "block1_top" -source_inst "timer_ids_inst"

generate -out "F:\Work\SoCEnterprise\SoCEnterprise_Demo_May_21\out"
graph
```

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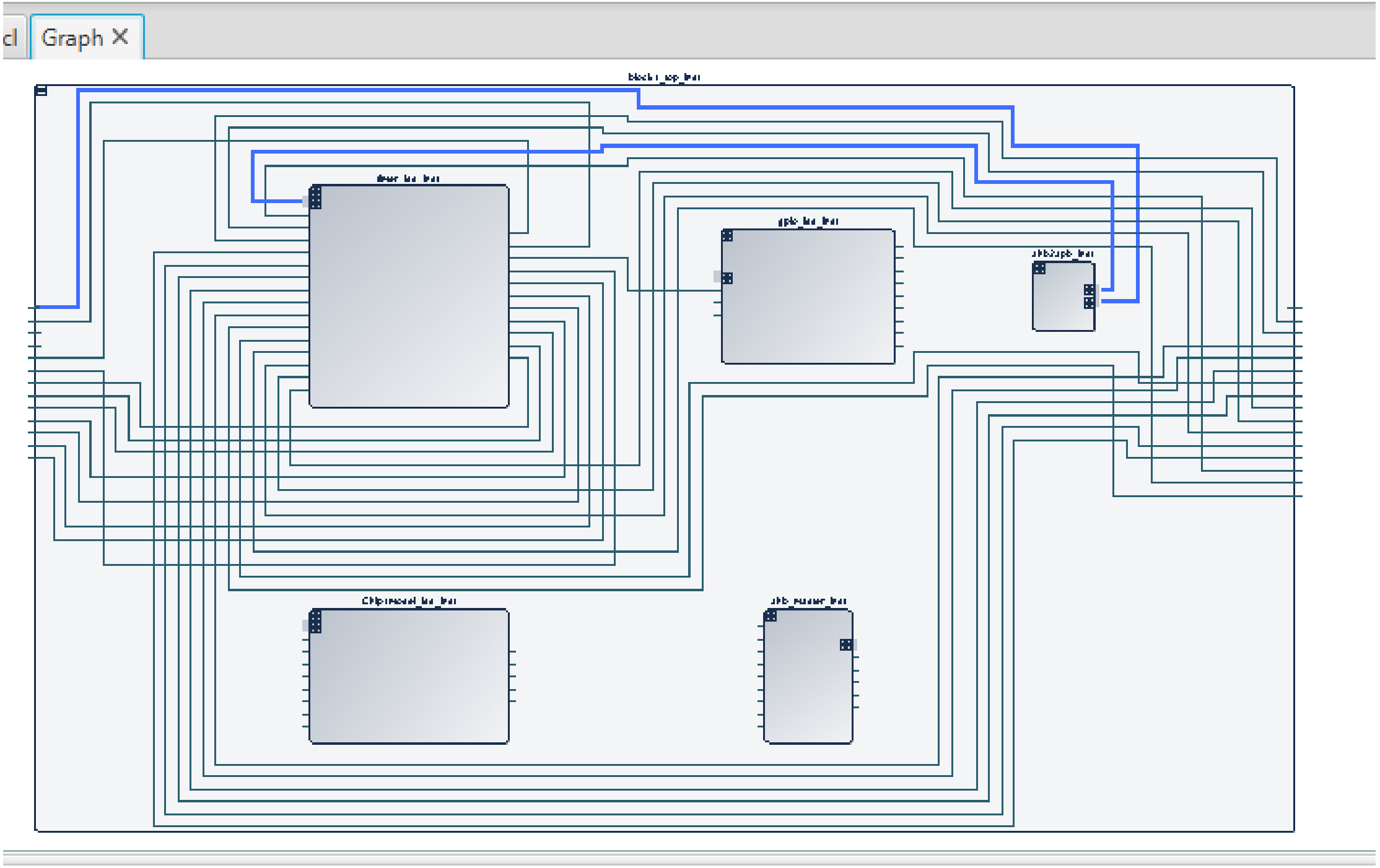
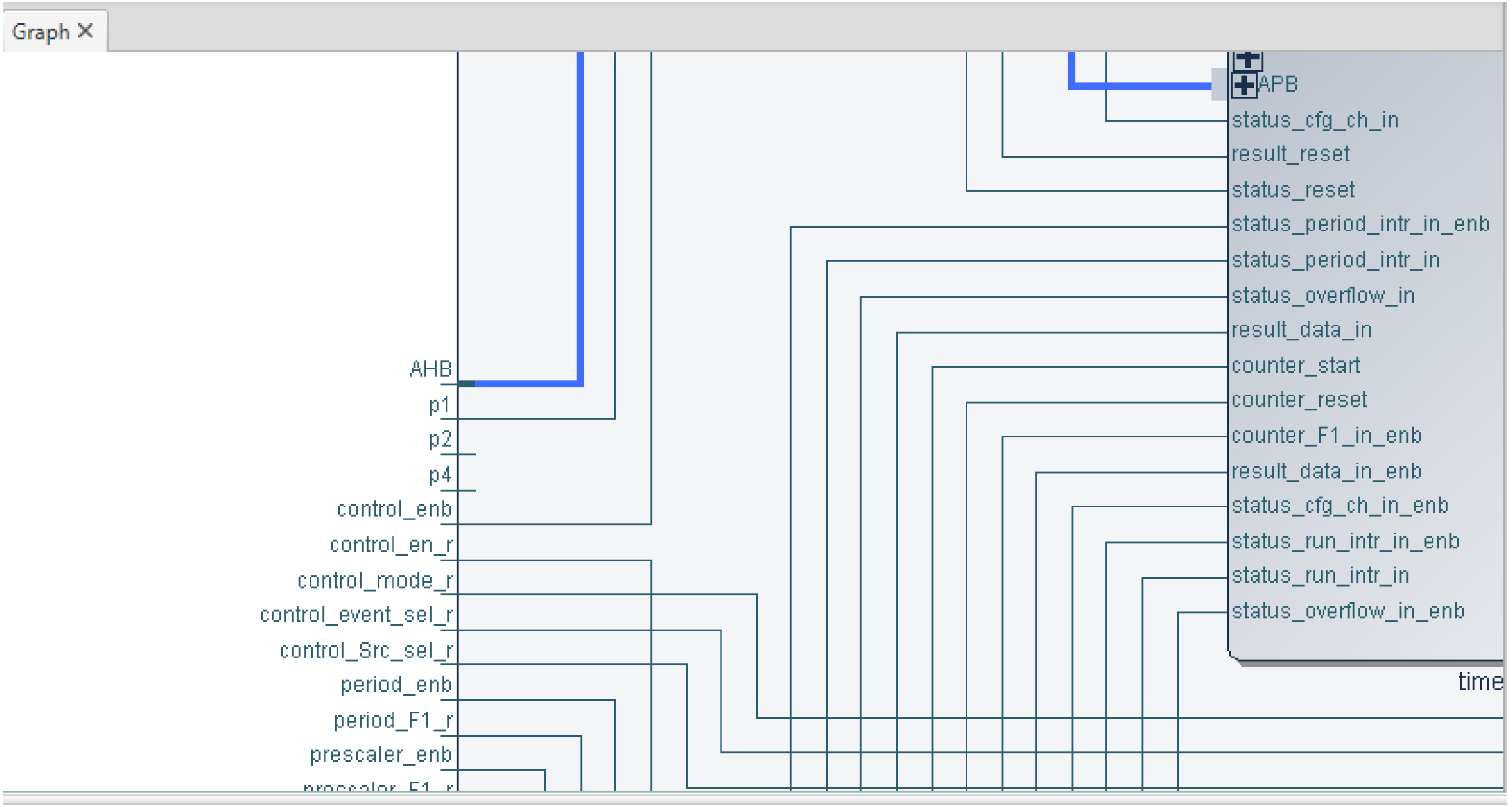
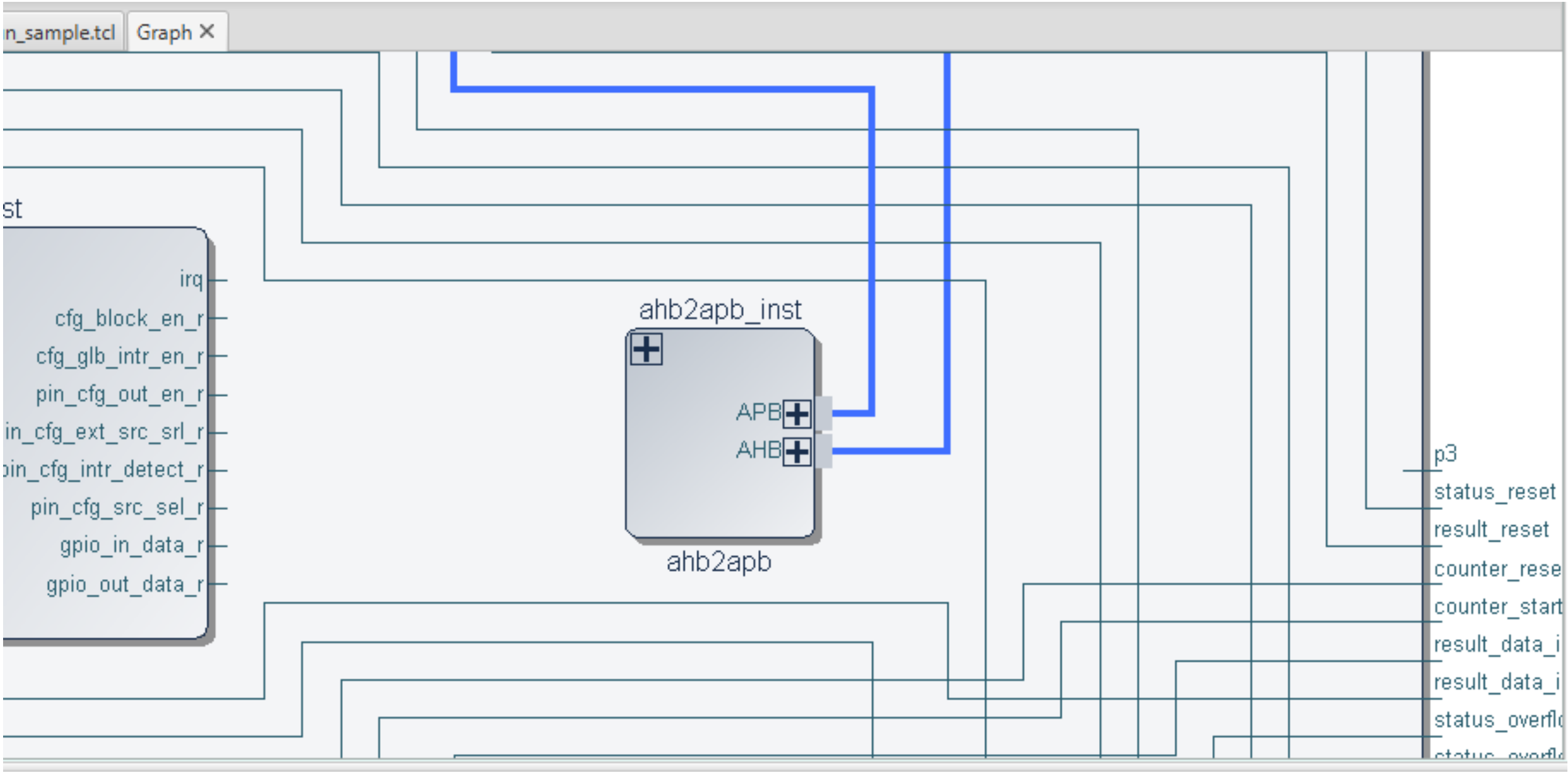
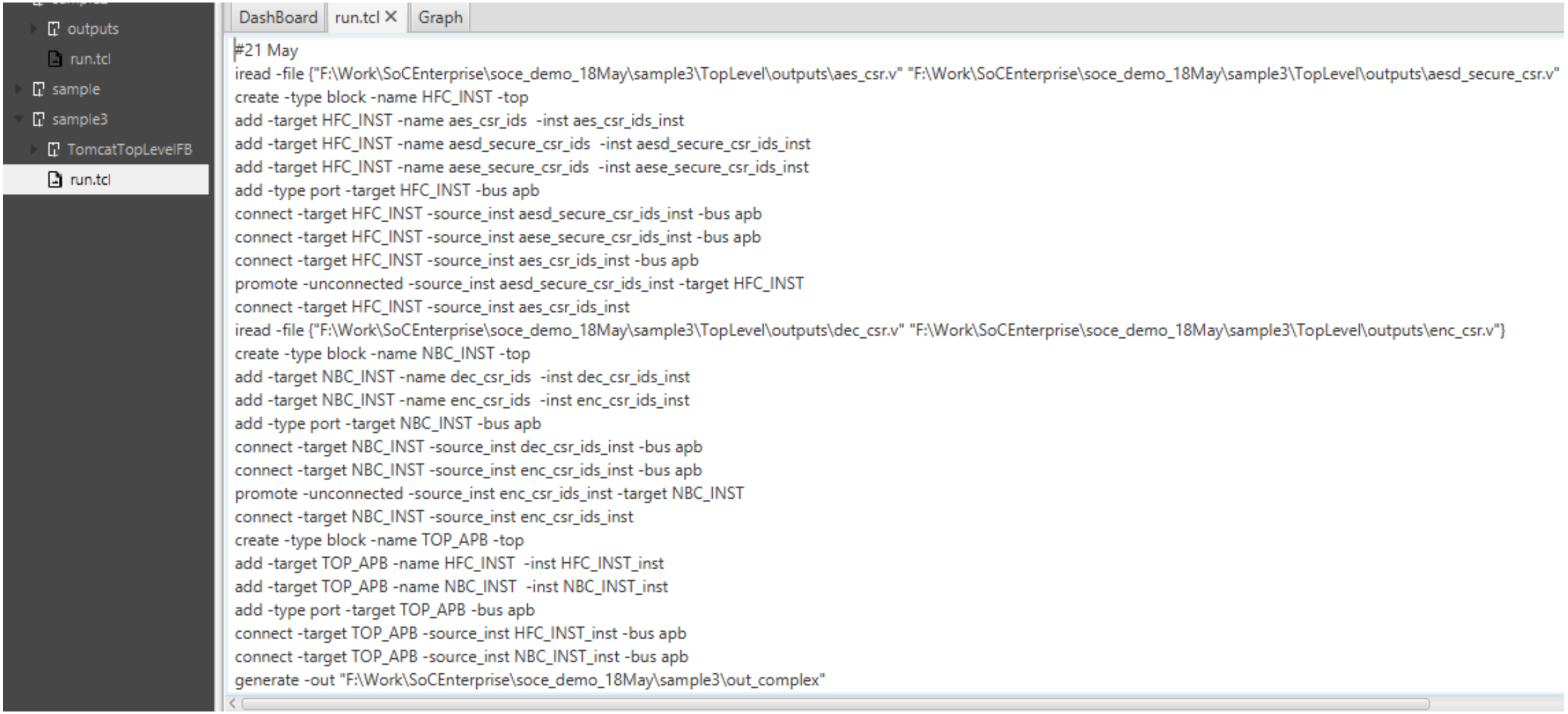

cl
Graph


Graph
APB
status_cfg_ch_in
result_reset
status_reset
status_period_intr_in_enb
status_period_intr_in
status_overflow_in
result_data_in
counter_start
counter_reset
counter_F1_in_enb
result_data_in_enb
status_cfg_ch_in_enb
status_run_intr_in_enb
status_run_intr_in
status_overflow_in_enb
time
AHB
p1
p2
p4
control_enb
control_en_r
control_mode_r
control_event_sel_r
control_Src_sel_r
period_enb
period_F1_r
prescaler_enb


n_sample.tcl
Graph
st
irq
cfg_block_en_r
cfg_glb_intr_en_r
pin_cfg_out_en_r
in_cfg_ext_src_srl_r
in_cfg_intr_detect_r
pin_cfg_src_sel_r
gpio_in_data_r
gpio_out_data_r
ahb2apb_inst
APB
AHB
ahb2apb
p3
status_reset
result_reset
counter_rese
counter_start
result_data_i
result_data_i
status_overfl



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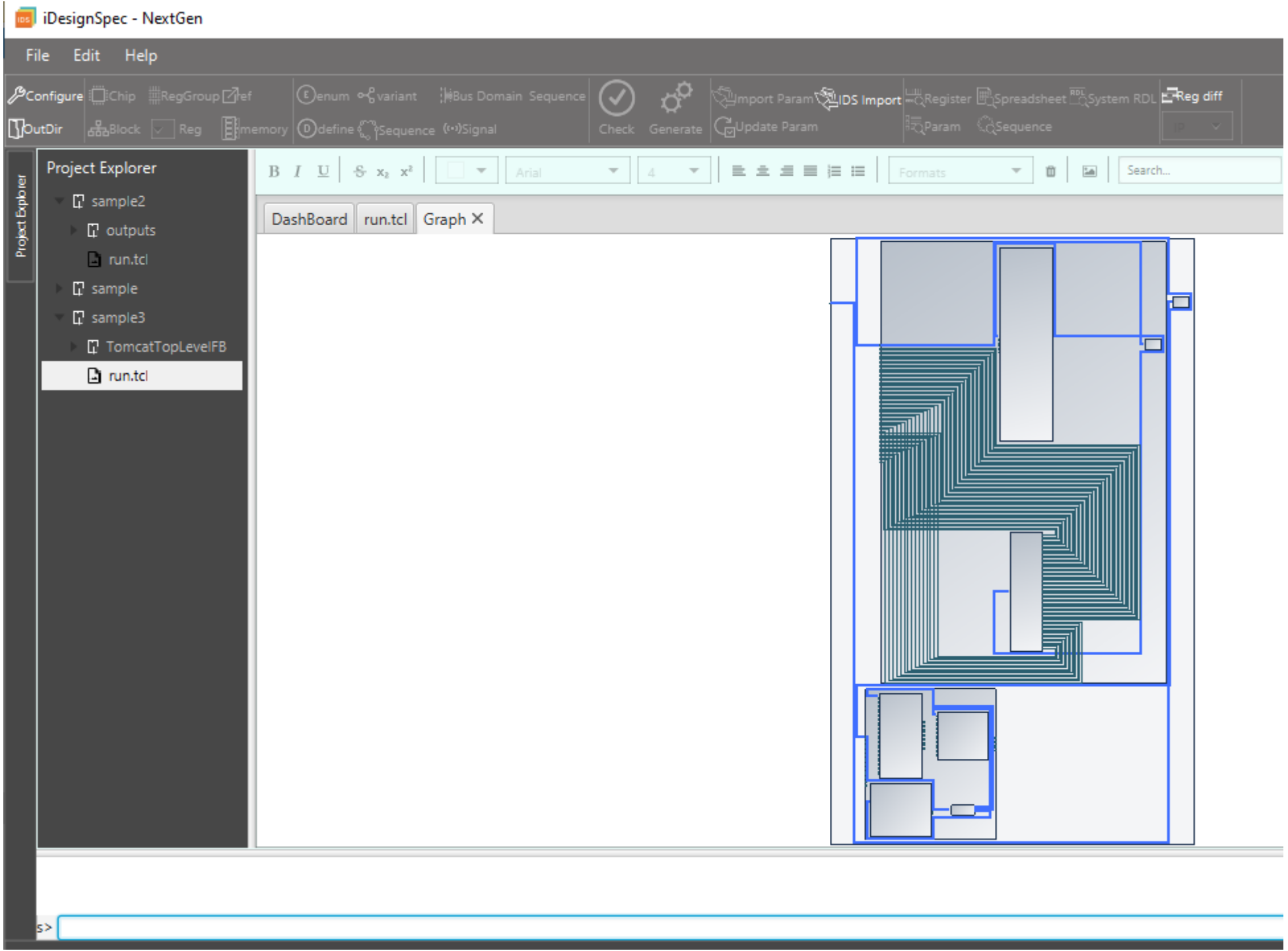

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Benefits

SoC Enterprise™ benefits

- Easier handling of complex and large SoC designs through Tcl like scripts and GUI

- On-the-fly generation
  - IPs and sub-systems are automatically generated with support for customization and configuration

- Boosting productivity of SoC design teams significantly leading to faster time-to-market for competitive advantage

- Reduces SoC design and development cost significantly

- Combines all the benefits of IDesignSpec™ and SLIP-G™

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Conclusion

Conclusion

- Complexity in SoC design and assembly can be handled by using automation at architectural level
- Effective IP (including sub-systems) reuse is possible if the IP generators are flexible, customizable, and configurable
- Its not just about RTL reuse - reuse must also happen in firmware and software
- Invest in tools and flows that help in the SoC design, assembly and generation of not only the RTL but also the collaterals for verification, software, and firmware
- Agnisys can help: IDesignSpec™, SoC Enterprise™, SLIP-G™, ARVV™, ISequenceSpec™

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Agnisys Webinar Series

BRINGING THE LATEST AUTOMATION IN IP/FPGA/SOC TO YOUR HOME!

Time : 10:00 AM – 11:00 AM PDT

08-April-2020	Correct by construction SV UVM code with DVinsight - a smart editor	30-April-2020	Advanced UVM RAL - callbacks, auto-mirroring, coverage model, and more	28-May-2020	Steps to setup RISC-V based SOC Verification Environment
09-April-2020	Creating portable UVM sequences with ISequenceSpec	7-May-2020	Functional safety and security in embedded systems	04-June-2020	Automatic verification using Specta -AV - a boost to verification productivity
16-April-2020	Register automation from SystemRDL to PSS - Basic to Pro	14-May-2020	IP generators - the next wave of design creation	11-June-2020	AI based sequence detection for verification and validation of IP/SoCs
23-April-2020	Cross platform specification to code generation for IP/SoC with IDS-NG	21-May-2020	A flexible and customizable flow for IP connectivity and SoC design assembly	18-June-2020	Understanding clock domain crossings

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About Agnisys

- The EDA leader in solving complex design and verification problems associated with HW/SW interface
- Formed in 2007
- Privately held and profitable
- Headquarters in Boston, MA
  - ~1000 users worldwide
  - ~50 customer companies
- Customer retention rate ~90%
- R&D centers (US and India)
- Support centers - committed to ensure comprehensive support
  - Email : support@agnisys.com
  - Phone : 1-855-VERIFYY
  - Response time within one day; within hours in many cases
  - Multiple time zones (Boston MA, San Jose CA and Noida India)

IDESIGNSPEC™ (IDS) EXECUTABLE REGISTER SPECIFICATION

Automatically generate UVM models, Verilog/VHDL models, coverage model, software model, etc.

AUTOMATIC REGISTER VERIFICATION & VALIDATION (ARVV)

ARV-Sim™ : Create UVM test environment, sequences, and verification plans, and instantly know the status of the verification project

ARV-Formal™ : Create formal properties and assertions, and coverage model from the specification

ISEQUENCESPEC™ (ISS)

Create UVM sequences and firmware routines from the specification

DVinsight™ (DVi)

Smart editor for SystemVerilog and UVM projects

IDS – Next Generation™ (IDS-NG)

Comprehensive SoC/IP spec creation and code generation tool

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