v7.36.0.0
(March 2nd, 2022)

IDesignSpec™ (IDS)

RTL Enhancements

1. F#16704 Support for flattening of fields with repeat property when '%d' identifier is used in its name. More Details
2. F#16704 Lock support for controlling higher bits of a register with their corresponding lower bits or vice-versa in case of fields with flattened repeat. More Details
3. B#1595 Readability enhancements with more comments in the generated code through a new switch '-verbosity high' for generated Verilog/UVM code. More Details
4. F#19572 Support of clock_enable property at section and block level. More Details
5. F#17117 Flopped aggregation logic supported for AMBA-APB. More Details

General Enhancements

1. F#19450 chip-in-chip support in Excel, Calc, CSV and IDS-NG.

2. F#17242 -log_verbose <log_file> switch has been supported to dump out verbose log into separate file. More Details
3. F#19585 +top_property switch has been supported to append existing top_property values instead of overriding them. More Details
4. F#19454 Enhancement in Cheader for address macro in case of register and section when instantiated in array form, which now contains an extra argument (idx). More Details
5. F#19494 Switch -disable_overlap_check has been supported to generate outputs in case of address overlap issue. More Details
6. B#1633 In cheaderalt4, *_OFFSET macro has been moved to its immediate parent's file when the multi-file option is selected. More Details

UVM Enhancements

1. F#16969 hdl_path support through dynamic assignment on arrayed blocks. More Details

SystemRDL Enhancements

1. F#19714 Perl preprocessor speed improvement.

Bug Fixes
General:

1. F#19566 Fixed issue of add_doc and add_doc_above html and PDF was not created properly in IDS-NG.
2. F#19760 Fixed unexpected error issue in case of check and generation.
3. F#19566 Fixed documentation issue (pdf or html) of default values not properly displaying for multiple sections.
4. F#19573 Fixed issue for clock_name throwing java exception for htmlalt2 output.
5. F#17113 Fixed issue for character encoding errors depending on generation level (block or chip).

6. Support for UVM custom code properties at top level for systemRDL input.

7. F#17120 Fixed import in CSV from any other IDS supported inputs.
8. F#16577 Fixed issue for address calculation in case of 32 bits address unit in word output.
9. F#19751 Fixed issue for character length warning error of htmlalt2 output in case of IDS-NG of input format.
10. F#19448 The issue has been fixed for tcl compilation fail syntax error occurring in generation of vheader output when enum are used at chip level.

11. F#19706 Fixed generation issue of CMSIS-SVD format while executing idsbatch.

12. F#19502 Fixed IP-XACT output in case of chip in chip hierarchy case of 1 block in chip in chip hierarchy

13. F#19502 Fixed Chip in chip hierarchy not being preserved when UDP ipxact_exclude_vendorextensions=true is applied
14. F#19763 Inconsistency in the first instance name for Address/Offset macro were fixed in Cheaderalt4
15. F#19704 Fixed the case of multiple instances of regfiles(with or without parameter overrides), the union names in the block struct was not expected in case of inst_name_cppstyle

RTL

1. F#19535 Fixed issues in the generated Verilog RTL when using the property "singlepulse=true" for wide registers.
2. F#15843 Fixed issues in the generated Verilog RTL when generating bus write pulse on the hardware side with the property 'rtl.hw_wp' on wide registers.
3. F#19534 Fixed issues in the generated Verilog RTL with field update of a wide register on a bus write.

4. F#19572 Fixed issue in the generated Verilog output with hw access 'NA' along with the property "clock_enable" on a register.
5. B#1622 Support for complicated expressions in the next UDP.
6. F#19708 Fix for 'custom_error' property in case of empty assignment to the error signal causing compilation fail
7. F#19652 Fix when "rtl.hw_wp" property is used with "external=true" in verilog output.
8. F#19768 Fix for RTL generation when 8 bit external register is used.
9. F#19779 Fix for hw access=na when "registered=false" is used with "rtl_hw_vector" property.

UVM

1. F#15957 Fix for coverage in UVM output while using the property "coverage=af".
2. F#19752 Fix for repeated section having multiple reset value in UVM output.
3. F#19667 Fix for 'uvm_add_regmap' property not working on block element when top element chip is used.
4. F#19727 Fix for external section, when multiple reset value is applied on the fields.
5. F#19733 Fix in hdl_path for external registers.
6. F#19614 Fixed hdl_path property in case of inst_name_cppstyle UDP is applied.
7. F#19657 Fixed hdl_path property in case of alias register when 7.x series is used.
8. F#19532 Fix in case multiple instances of a section are taken in the block, same classes generation compilation issue.
9. F#19382 Special character string fixed by replacing with underscore in case of parameter overriding with UDP "inst_name_cppstyle" and buffer_trig_reg UDP.

IDS NextGen™ (IDS-NG)

Enhancements

1. G#IDSNG#78 Supported copy/paste of parameters from one file to another file in parameter view. More Details
2. G#IDSNG#78 Supported hide/unhide feature for update param. More Details
3. G#IDSNG#68 Supported struct template in IDS-NG. More Details
4. G#IDSNG#71 Enhanced the project selection option to open only IDS-NG projects. More Details
5. F#16668 Supported parameters for register field bits in IDS-NG input format.
6. G#IDSNG#82 Added svgalt2 output in IDS-NG configuration. More Details

Bug Fixes

1. G#IDSNG#80 Removed semicolon from property when added through the property pane on the field description.
2. Fixed spreadsheet and checker view right click issue in IDS-NG.
3. G#IDSNG#80 Fixed all properties not in the list of property pane.
4. G#IDSNG#78 Corrected warning/error message in case of added param.
5. G#IDSNG#78 Fixed issue for copying content from console on linux OS.
6. G#IDS NG#80 Fixed issue of hinting for selection of access types .
7. G#IDS NG#76 Fixed issue for redirection of register view error from sequence/checker view on check and generate.
8. G#IDS NG#76 Fixed issue for redirection of generated output directory in case of systemRDL input.
9. F#19526 Fixed issue for param import giving non-indicative error message in IDS-NG.
10. F#19546 Fixed issue for VHeader output not available in IDS-NG.
11. F#19375 Fixed issue of wrong address offset in case of import word file in IDS-NG.
12. F# 19525 Fixed issue for unexpected behaviour of save as feature of IDS-NG.
13. F#16590 Fixed issue for struct XRSL in case of IDS-NG templates.
14. G#IDSNG#81 Fixed option ADD ROW ABOVE and ADD COLUMN LEFT in spreadsheet view .

ISequenceSpec™

Bug Fixes

1. B#1638 Fixed multiple constraints when applying constraints to a variable in iss_sv.
2. B#1638 Fixed time command in iss_sv
3. B#1638 Fixed generation issue for iss_sv output when use wait command in python input.

ARV™

Enhancements

1. B#1639 Support of lock property sequence for field.

Bug fixes

1. B#1640 Fix when an integer value is provided in lock expression.