coggle
made for free at coggle.it

Version 2.0
Copyright 2023 Agnisys, Inc. All rights reserved.
Confidential and proprietary.

IDesignSpec
Outputs
Flavors
Properties
Types
Register
Memory
Hierarchy
Alias Register
Alternate Register
Counter
External Register
Indirect Register
Interrupt Register
Lock Register
Paged Register
RO, WO Pair Register
Shadow Register
Simple Register
Trigger Buffer(Atomic Update) Register
Multidimensional register
FIFO
Accumulator Register
Reserved
Unreserved
Access
SW (bus)
HW (app logic)
Levels
SoC
Advanced
Professional
Design reuse
Capabilities
Eliminate Inefficiencies
bus domain
clock domain
multiple domain
Functional Safety
Security
SECDED
CRC
Parity
Sniffer
TMR
CDC
Hardware
Software
Velocity Template
Firmware
RTL
Data Formats
IP-XACT
JSON
SystemRDL
Perl
Python
Documentation
Doc Properties
Custom CSV
Custom XML
Datasheet
DITA
HTML
HTML ALT2
SVG
Word alt1
Word alt2
YAML
Cheader
C_type
SVHeader
Textual Formats
Add-ins
Excel Add-in
OpenOffice Add-in
Word Add-in
Textual
XML
CSV
SystemRDL 2.0
SystemRDL 1.0
IP-XACT
custom XML output
custom XML import
custom CSV output
custom CSV import
IDS-Calc
IDS-Excel
IDS-Word
bus domains
checker
define
IDS template
register header
signals
IDS-IPGen
IDS-Batch
IDS-IPGen
SPI
PIC
GPIO
AES
I2C-Master
TIMER
PWM
DMA
RTL
Buses
Properties
Parallel
Serial
AMBA AHB
AMBA AHBLITE
AMBA APB
AMBA AXI4LITE
AMBA AXI4FULL
AMBA AXIS
Avalon
OCP
Tilelink
Wishbone
Custom/Proprietary
pulse ready
Combinational version
Sequential/flipflop version
non-pipelined
pipelined
avalon_noburst
with bursting
asynchronous ack_i
synchronous ack_i
flopped
1_8
1_7
I2C
SPI
SV Header
VHDL
Verilog
Integration logic
Slave Wrapper logic
IDS-Validate
IDS-Verify
JTAG
svout_filename
Automatic Assertion Generation
Automatic Test Generation
Bare metal verification
Co-verification environment
virtual prototyping
OSVVM
UVM
rtl_wrapper
Automatic testbench generation
TCL Configuration APIs
IDS-Integrate
idsbatch -s <TCL script>
TCL APIs for scripts
get_domains
is_null
get_value_constraints
get_params_objects
get_tcl_api_version
get_block
get_reg_width
get_id
get_unit
get_variants
get_config
get_ids_version
get_hierarchy
get_objects
get_top
get_prop
get_type
get_defines
get_enums
get_chip
get_params
get_ids_version
get_board
get_all_sections
get_fields
get_objects_by_name
get_parent
get_default_value_enum
get_unique_name
is_equal
hide_htmlalt2_prop
set_error
check
generate
ids_read
reset_config
set_config
set_inp
set_prop
set_switch
set_multi_out_file
set_vertical_reuse
set_traceability
set_outputs
IDS-Batch CLI
-top (for systemRDL input)
-variant
-fast
-sheet_name <sheet_name>
-cache_dir
-copyright
-top <top_elem_name>
-reg_width <8|16|32|64|128>
-unit <8|16|32|64|128>
-bus
-chip_size <val>
-block_size <val>
-if
-force_out
-company
-traceability
-preserve
-dir <output_dir>
-template_file <csv_template_file>
-velocity "<list of velocity template files>"
-inp
-verbose
-verilog_dep
-uvm_dep
-deprecated_6_36
i2c
wishbone
tilelink
proprietary
ocp
amba3ahblite
apb
amba
spi
axi
avalon
xrsl
csv
ipxact
SystemRDL
openoffice
ralf
word
excel
-out
customcsv
csharp
dita
datasheet
verilog
verilog2001
vhdl
vhdlalt2
ISS output formats
-iss_tcl
-iss_platform
-iss_infact
-iss_perspec
-iss_matlab
-iss_uvm
-iss_firmware
-iss_csv
-iss_sv
-iss_flowchart
sv
vheader
perl
misrac
headeralt2
header
svheader
xrsl
rdlalt2
python
Yaml
ipxact2014
excel
rtl_sysc
html
custom csv
arv
htmlalt2
word2010
svg
ovm
ipxact1_4
autoseq
uvm
pdfalt2
pdf
cpp
formal
erm
ipxact1_5
word2007
rdl
switches for systemC output
-tf_sysc
switches for svheader output
-tf_svheader
switches for UVM output
-auto_mirror
-tf_uvm
-fast_uvm
-reg_port_case
-ctest
ctest_opt
switches for ipxact output
-tf_ipxact
bus_comp
-ipxact_comp "<blockboards>"
switches for html outputs
-tf_html_section
-fast_html
-tf_html
-no_formatting
-hide_htmlalt2_prop
switch for Word output
-doexclude <list_of_table>
-force
switches for RTL design
-in_third_party <d|m>
-low_power
-out_third_party <d>
switches for pdf output
-no_formatting
-lloc
-tf_pdf
switches for RDL input
-incdir
-rdl_version
-no_warn
-rdl
switches for Verilog output
switches for C header output
-c_opt
-vertical_reuse
-c_type <val>
-big_endian <true|false>
-c_tests
-c_api
-little_endian <true|false>
-tf_header
switches for vhdl
-c_type_std
switch for Obfuscated output
-out ovrsl
switches for ARV output in uvm
-illegalbins
-hdlpath
-arv_coverage
-arv_constraint
-arv_assertion
-coverage
-auto_mirror
Properties
clock
Control & Signal
logical operation
reset
stages
signals
access type
addressing
address allocation
accesswidth
constraint_disable
chip inside chip
counter
interrupt
memory
parameters
signals
decimal_encoding
level
ref
wrapper_port
hw_access
rtl.response_tree
rtl_field_err
sw_access
ext_signal
rtl.bit_enable
rd_enb
rsv_rd_val
reg_rd_addr
read_access
sync_reset
endianness
wr_enb
count
addressing
avalon_noburst
block_prot
block_prot_rd/block_prot_wr
aggr_block_offset
aggregation_logic
clock_edge
clock_enable
default_clock_name
exclude_clock_gating
assign
next
rtl.hw_wt
rtl.hw_clear
rtl.hw_rp
rtl.hw_set
rtl.hw_wp
rtl.hw_wdp
rtl.hw_w1p
sing/epulse
sw
dynamic_empty_address
ext_signal
format
ext_byte_enb
ftd_gen/var
header_hormetic
hierarchical_decode
hwenable
hwmask
invalid_addr_err
anded
ored
xored
module_name
not_generate
param.name_format
partial_access_err
default_reset_name
field_reset
hard_reset
reset_level
reset_type
resetsignal
rtl.reset_name
registered
rtl.bit_enable
rtl.bmax
rtl.bmin
rtl_busport_prefix
rtl.byte_enable
rtl.field_enb
rtl.hw_enb
rtl.hw_latch
rtl.default
rtl_hw_vector
rtl.precedence
rtl.name_format
rtl.reg_enb
rtl_port_suffix
rtl.sw_latch
rtl.sw_read
wr_rd_valids
rtl_sw_write
rsvdset
rsvdsetx
single_address_data_out
addr_decode_stages
out_enb_stages
rb_valid_stages
rb_data_stages
rd_stb_stages
wr_stb_stages
swwel
wel
sv/dpnt
unaligned_error
undefined_rd_val
sw_bit_enable
indirect_map
decode_unaligin
hierarchical_decode
lock.toggle
lock.set
lock.clear
rtl loc
decode_unaligned
rtl_single_package
power_opt
define_as_param
external_byte_acc_err
rtl_hw_wt
UVM Properties
Register Test Properties
Coverage Properties
uvm.map
uvm.base_class
uvm.reg_class
uvm.reg_access
uvm.class
uvm.reg_name_format
uvm.package
uvm.user_coverage
has_reset
is_rand
is_acc
dontcompare
index_reg
depth
hdl_path
auto_hdl_path
hdl_path_gate
hdl_path_internal
ignore_prop
constraint
uvm.reset_constraint
volatile
uvm.field_class
uvm.name_format
uvm.handle_name_format
vertical_reuse
uvm_add_regmap
uvm_global_param
uvm_lock_model
uvm_opt
uvm.alter_access
regdef_pkg
auto_volatile
uvm_guard_band
uvm.vreg
config_hdl_path
hdl_path_gate_slice
hdl_path_slice
uvm.enum.name_format
uvm.inst_class
uvm_class_name_inst
no_reg_tests
no_reg_hw_reset_test
no_mem_walk_test
uvm.block_class
uvm.regfile_class
uvm.frontdoor
uvm.type
uvm.backdoor
uvm_package
uvm_field_class
uvm_inst_class
uvm_door
uvm.rm
uvm.transaction
enum.name_format
uvm_context
inst_name
uvm.vreg_class
uvm.vreg_field_class
uvm_add_regmap_offset
uvm_map_notpresent
uvm_map_access
uvm_runtime_buswidth
custom_code_hier
uvm_common_pkg
intr_pending
uvm.loc
uvm_lock_monitor
external_indication
ids_cross
coverage
coverage.at_least
coverage.auto_bin_max
coverage.comment
coverage.cross_num_print_missing
coverage.detect_overlap
coverage.get_inst_coverage
coverage.goal
coverage.option_name
coverage.per_instance
coverage.weight
cross
cross_rd
cross_wr
uvm.coverpoint.b
uvm.coverpoint.b_rd
uvm.coverpoint.b_wr
no_mem_tests
no_mem_access_test
no_reg_access_test
no_reg_bit_bash_test
no_field_tests
doc_add_field_col
remove_html_index
doc_pagination
doc_unused_remove
field_sort
show_display_name
html_show_reserved_bits
doc
add_doc
add_doc_above
data_struct
doc.rm_define
doc.rm_enum
expanded_toc
html_header
html_reglink
regid
doc.rm_variant
doc_repeat_compact
C Header Alt 2
CMSIS-SVD
Mirra C
SystemC alt1
SystemC alt2
C Header
Cheader custom code
cheader_add_regmap_offset
cheader_remove_macro
cheader_map_notpresent
cheader_add_regmap
cheader_opt
cheader.enum.name_format
cheader_filler
cheader_guard_nameformat
cheader.initialization
cheader.name_format
cheader_no_struct
cheader_ignore
cheader.mask_endianess
cheader.struct.maxsize
compiler.arrayindex.maxvalue
description
header.field_mask
header.fnwd_decir
header_package
header.struct_guard
rsv_name_format
vertical_reuse
[cheader loc=top] <user code> [cheader]
[cheader loc=head] <user code>[/cheader]
[cheader loc=bot] <user code> [/cheader]
Mem Dump (documentation output)
Register view
Param view
Sequence view
Text based
Template based
System RDL
Spreadsheet style
Word like
importing yaml file
reflect changes in reg/spreadsheet view
param diff viewer
AI based sequence detection
Template based
Python
Enterprise features
Compact view
Dynamic hinting
Hinting
Search bar
Stop Button
Project
Console
Diff and Merge
Git Integration
Features
IDS-IPGen
Special outputs
Spec formats
IDS-NG
multi-port connection
graph (GUI)
tie values
parameter overriding
support standard verilog and ipxact files
static and dynamic hinting
promoting selective ports
at soc level
at block level
interfaces
outputs
system verilog
ipxact 2009/2014
verilog 1995/2001
idsbatch -e <TCL/Python script>
TCL/Python APIs in console window
IDS-Integrate
soc_delete
soc_disconnect
clear
soc_clean
soc_connect
promote
soc_generate
soc_read
soc_create
soc_add
soc_set
contiguous address locations
Repeat on Memory
memory=rtl/uvm/all" with "repeat" on external reggroup
wide_external_access
Multiple Interfaces on Memory
depth
mapto_dpsram
type=subblock
System
Board
Chip
Block
Section
fifo.width
fifo_depth
fifo.full
fifo.empty
fifo.almost_empty
fifo.almost_full
fifo.almost_full_val
fifo.almost_empty_val
rtl_pack_array
shadow_address
shadow_reg
is_rsv
undefined_rd_val
is_present
buffer_trig
buffer_trig_read
buffer_trig_reg
lock_clear
lock_r
lock_set
lock_toggle
page_count
page_rd_select
page_select
page_wr_select
repair
shadow_address
shadow_reg
enable reg
halt.enable
intr.enable
intr.detect
intr.detect_nometa
intr.in
intr.irq_bit
intr.irq_per_channel
intr.nonsticky
intr.out
intr.overflow
halt.mask
intr.mask
mask reg
intr.pending
intr.post
intr.status
pending reg
post reg
status reg
depth
decimal_encoding
incr_reg
index_reg
datagroup
datagroup.order
hw_rd_trigger
hw_wr_trigger
indirect_map
msb_broadcast
rtl.incr_indirect_reg_flop
virtual
counter
counter.hw.enb
counter.incr.width
counter.precedence
counter.sat
counter.signal
counter.sw.rd
counter.sw.rd.enb
counter.sw.wr
counter.sw.wr.enb
counter.decr.sat
counter.decr.thld
counter.decr.val
counter.incr.sat
counter.incr.thld
counter.incr.val
counter.both.enb
alias
aliased
alt_mode
alt_reg
rtl_error_enb_cntl
errorbus
external
external_ack
external_intf_stages
ext_byte_enb
ext_decode_lines
ext_error
mem_width
sharedextbus
rtl.strict_ports
accumulate
spec_ver
alignment
inst_name_cppstyle
reflvariant
offset
variant
size
type
external
reg_default
byte_addressing
is_rsv
reg_hw
reg_sw
addr_sort
output_file_name
unit
export
type
global_addressing
stride
created_by
display_name
explicit_name
repeat
override
override_refname
out_third_party
ispresent
array_start_index
General