coggle
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Version 2.0
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IDS-NG
- Features
  - Enterprise features
    - Project
    - Console
    - Diff and Merge
    - Git Integration
  - Compact view
  - Dynamic hinting
  - Hinting
  - Search bar
  - Stop Button
- IDS-IPGen
- Special outputs
  - Mem Dump (documentation output)
- Spec formats
  - Register view
    - Text based
      - System RDL
      - Spreadsheet style
      - Word like
    - Template based
  - Param view
    - importing yaml file
    - reflect changes in reg/spreadsheet view
    - param diff viewer
  - Sequence view
    - Text based
      - AI based sequence detection
      - Template based
      - Python

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  - Professional
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      - secded_ded_error
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      - secded_parity
    - CRC
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      - crc_seed
    - Parity
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      - parity_error
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    - Sniffer
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    - TMR
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      - tmr_error
  - Security
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    - field_prot
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    - reg_rprot
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    - bus.domain
    - offset.<bus_domain_name>
  - clock domain
    - clock_name
    - reg_sw.<bus_domain_name>
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    - Hardware
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      - cdc.reset
      - cdc.clock
      - reg_clk
    - CDC
    - Software
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      - Cheader custom code
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        - [cheader loc=bot] =user code= [cheader]
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      - cheader_map_notpresent
      - cheader_add_regmap
      - cheader_opt
      - cheader.enum.name_format
      - cheader.filler
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      - cheader_no_struct
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      - cheader.mask_endianess
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      - compiler.arrayIndex.maxvalue
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      - ipxact_compact
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      - hdl_path_slice
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      - intr
      - mask
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      - field_reset
      - sync
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    - OpenOffice Add-in
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    - define
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    - signals
    - Textual Formats
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  - IDS-Word
    - Textual Formats
    - IDS-IPGen
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    - Excel Add-in
    - OpenOffice Add-In
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  - Textual
    - SystemRDL 2.0
    - SystemRDL 1.0
    - IP-XACT
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      - custom XML import
    - CSV
      - custom CSV output
      - custom CSV import
      - template_file
      - <csv_template_file>
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    - Alias Register
      - alias
      - aliased
    - Alternate Register
      - alt_mode
      - alt_reg
    - Counter
      - decrementing
        - counter.decr.sat
        - counter.decr.thld
        - counter.decr.val
      - incrementing
        - counter.incr.sat
        - counter.incr.thld
        - counter.incr.val
      - accumulate
      - up-down
        - counter.both.enb
        - counter
        - counter.hw.enb
        - counter.incr.width
        - counter.precedence
        - counter.sat
        - counter.signal
        - counter.sw.rd
        - counter.sw.rd.enb
        - counter.sw.wr
        - counter.sw.wr.enb
    - External Register
      - rtl_error_enb_cntl
      - errextbus
      - external
      - external_ack
      - external_intf_stages
      - **ext_byte_enb**
      - ext_decode_lines
      - ext_error
      - **mem_width**
      - sharedextbus
      - rtl.strict_ports
    - Indirect Register
      - depth
      - decimal_encoding
      - incr_reg
      - index_reg
      - indirect map
        - datagroup
        - datagroup.order
        - hw_rd_trigger
        - hw_wr_trigger
        - indirect_map
      - msb_broadcast
      - rtl.incr_indirect_reg_flop
      - **virtual**
    - Interrupt Register
      - enable reg
        - halt.enable
        - intr.enable
      - intr.detect
      - intr.detect_nometa
      - intr.in
      - intr.irq_bit
      - intr.irq_per_channel
      - intr.nonsticky
      - intr.out
      - intr.overflow
      - mask reg
        - halt.mask
        - intr.mask
      - pending reg
        - intr.pending
      - ppost reg
        - intr.post
      - sstatus reg
        - intr.status
      - status reg
    - Lock Register
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      - lock_r
      - lock_set
      - lock_toggle
    - Paged Register
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      - page_rd_select
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    - RO, WO Pair Register
      - rwpair
    - Shadow Register
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      - shadow_reg
    - Reserved
      - is_rsv
      - undefined_rd_val
      - is_present
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    - Simple Register
      - buffer_trig
      - buffer_trig_read
      - buffer_trig_reg
    - Trigger Buffer(Atomic Write) Register
    - Multidimensional register
      - rtl_pack_array
    - fifo
      - fifo.width
      - fifo_depth
      - fifo.full
      - fifo.empty
      - fifo.almost_empty
      - fifo.almost_full
      - fifo.almost_full_val
      - fifo.almost_empty_val
    - Accumulator Register
      - accumulate
  - Types
    - SW (bus)
      - rw,wo,ro,w1c, ...
    - Access
    - HW (app logic)
      - rw, wo, ro, na
  - Memory
    - depth
    - maptlo_dprsram
    - contiguous address locations
    - Repeat on Memory
    - memory=rtl/uvm/all" with "repeat" on external reggroup
    - Multiple Interfaces on Memory
    - *wide_external_access*
  - Hierarchy
    - System
    - Board
    - Chip
    - Block
    - Section
    - *type=subblock*
  - General
    - spec_ver
    - alignment
    - inst_name_cppstyle
    - *refvariant*
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    - variant
    - size
    - type
    - external
    - *reg_default*
    - *byte_addressing*
    - *is_rsv*
    - *reg_hw*
    - *reg_sw*
    - *addr_sort*
    - *output_file_name*
    - unit
    - export
    - type
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    - stride
    - display_name
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    - override
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    - out_third_party
    - ispresent
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  - TCL Configuration APIs
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    - check
    - generate
    - ids_read
    - reset_config
    - set_config
    - set_inp
    - set_prop
    - set_switch
    - set_multi_out_file
    - set_vertical_reuse
    - set_traceability
    - set_outputs
  - IDS-Integrate
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      - system verilog
      - ipxact 2009/2014
      - verilog 1995/2001
    - outputs
    - IDS-Integrate
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        - at soc level
        - at block level
      - tie values
      - parameter overriding
      - support standard verilog and ipxact files
      - static and dynamic hireing
      - promoting selective ports
  - idsbatch -s <TCL script>
  - TCL APIs for scripts
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    - is_null
    - get_value_constraints
    - get_params_objects
    - get_tcl_api_version
    - get_block
    - get_reg_width
    - get_id
    - get_unit
    - get_variants
    - get_config
    - get_ids_version
    - get_hierarchy
    - get_objects
    - get_top
    - get_prop
    - get_type
    - get_defines
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    - get_chip
    - get_params
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    - get_board
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    - get_fields
    - get_objects_by_name
    - get_parent
    - get_default_value_enum
    - get_unique_name
    - is_equal
- IDS-Batch CLI
  - -top (for systemRDL input)
  - -variant
  - -fast
  - -sheet_name <sheet_name>
  - -cache_dir
  - -copyright
  - -top <top_elem_name>
  - -reg_width <8|16|32|64|128>
  - -unit <8|16|32|64|128>
  - -bus
    - i2c
    - wishbone
    - tilelink
    - proprietary
    - ocp
    - amba3ahblite
    - apb
    - amba
    - spi
    - axi
    - avalon
  - -chip_size <val>
  - -block_size <val>
  - -if
  - -force_out
  - -company
  - -traceability
  - -preserve
  - -dir <output_dir>
  - -template_file <csv_template_file>
  - -velocity "<list of velocity template files>"
  - -inp
  - -verbose
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    - ralf
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  - -verilog_dep
  - -uvm_dep
  - -deprecated_6_36
  - switches for systemC output
    - -if_sysc
  - switches for svheader output
    - -if_svheader
  - switches for UVM output
    - -auto_mirror
    - -if_uvm
    - -fast_uvm
  - -ctest
    - ctest_opt
  - switches for ipxact output
    - -if_ipxact
    - bus_comp
    - -ipxact_comp "<blockboards>"
  - switches for html outputs
    - if_html_section
    - -fast_html
    - -if_html
    - -no_formatting
    - -hide_htmlalt2_prop
  - switch for Word output
    - -doexclude <list_of_table>
    - -force
  - switches for RTL design
    - -in_third_party <d|m>
    - -low_power
    - -out_third_party <d>
  - switches for pdf output
    - -no_formatting
    - -lloc
    - -if_pif
  - switches for RDL input
    - -incdir
    - -rdl_version
    - -no_warn
    - -rdl
  - switches for Verilog output
    - -no_external_mask
    - -special_reg
    - -bus_port_case <upper|lower>
    - -default_reset <async|synch>
    - -rtl_no_error
    - -parity_widget
    - -no_lint_warn
    - -rtl_wire
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    - -if_verilog
    - -fast_verilog
    - -lowpower
  - switches for C header output
    - -c_opt
    - -vertical_reuse
    - -c_type <val>
    - -big_endian <true|false>
    - -c_tests
    - -c_api
    - -little_endian <true|false>
    - -if_header
    - -c_type_std
  - switches for vhdl
    - -out ooxsl
  - switch for Obfuscated output
    - -illegalbins
    - -hdlpath
    - -arv_coverage
    - -arv_constraint
    - -arv_assertion
    - -coverage
    - **-auto_mirror**
  - switches for ARV output in uvm
- -out
  - excel
  - rtl_sysc
  - html
  - custom csv
  - arv
  - htmlalt2
  - word2010
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  - ovm
  - ipxact1_4
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  - dita
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      - dummybyte
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      - cfg
      - txn
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        - AMBA AXI4LITE
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          - avalon_noburst
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      - *vhdl.entity*
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      - Buses
      - Integration logic
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        - clock
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        - Control & Signal
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          - rtl.hw_wt
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          - rtl.hw_wp
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          - singlepulse
          - sw
        - dynamic_empty_address
        - ext_signal
        - format
        - ext_byte_enb
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