**Release Notes**

**v7.12.0.0**

***(May******6th, 2021)***

**IDesignSpec™ (IDS)**

**RTL Enhancements**

1. “**hierarchical\_decode**” property has been enhanced to support decoding of block IPs in a multicast/broadcast manner within an address map. ([More Details](https://www.agnisys.com/release/docs/ids/HierarchicalDecode.html#Multicast))
2. **“tmr\_error”** property has been enhanced to take a third argument '*activehigh*' to make the tmr\_error signal as active high. ([More Details](https://www.agnisys.com/release/docs/ids/TMR.html#tmr_error_enh))
3. **“registered”** property has been enhanced with a new argument ‘*retain*’ (“registered=false:retain”), to retain the storage value for unregistered register/field. ([More Details](https://www.agnisys.com/release/docs/ids/UnregisteredFields.html#register_retain))
4. CDC feature is supported in the Tilelink bus interface. ([More Details](https://www.agnisys.com/release/docs/ids/ClockDomainCrossing.html))

**UVM Enhancements**

1. “**cross**” property has been supported with variants for UVM RAL output. ([More Details](https://www.agnisys.com/release/docs/ids/CrossCoverage.html#variant))
2. **“uvm.block\_class”** property has been introduced to extend the chip and block classes from the class specified as value of this property. ([More Details](https://www.agnisys.com/release/docs/ids/UVMClassNameExtension.html#uvm_block))
3. **“uvm.regfile\_class”** property is used to extend the regfile classes with the class mentioned as the value of this property.  ([More Details](https://www.agnisys.com/release/docs/ids/UVMClassNameExtension.html#uvm_regfile))

**General Enhancements**

1. “**rtl\_wrapper=true**” property is supported in Specta-AV and SV for chip level RTL. ([More Details](https://www.agnisys.com/release/docs/ids/RTLWrapper.html))
2. “**alignment**” property has been supported for alignment of all the components inside the associated chip, block and section. ([More Details](https://www.agnisys.com/release/docs/ids/Alignment1.html#Alignment))

Note :

1. If “**-no\_warn**” switch is used, then input file name should be given before the switch in the idsbatch command line, preferably switch should be applied at the end of the command line.
2. Variants have been enhanced to be case sensitive.

**Bug Fixes**

**RTL**

1. Fix for lint errors regarding operand bit-width mismatch in Verilog output.
2. Fix for read operation in case of page register when different selector registers are used from hardware and software side.
3. Fix for missing CDC ports instantiation in case of AMBA-AXI4Fullbus.
4. Fix in “counter.incr.ral = <signal\_value>” property to support the incr value of counter based upon the input signal pin.
5. Checks are added to depict that “lowpower” switch and “rtl.byte\_enable=false” are mutually exclusive.
6. Fix for null pointer issue in case of nested external sections for Verilog output.
7. Fix in Verilog output when the "-rtl\_wire" switch is used with chip-in-chip flow.

**SystemVerilog**

1. Fix for tmr error when there is repeat on register/section.
2. Fix for issue in chip-in-chip flow when an SV wrapper is missing.

**SystemRDL**

1. Fix for naming issue of iterator when dynamic reset array assignment is used in Verilog output.
2. Fix for SystemRDL Compiler 2.0 freeze issue when RDLFormatcode closing tag is missing.
3. Fix for SystemRDL Code Formatting issue for documentation output.
4. Fix for issue in SystemRDL compiler regarding the nested preprocessor directives.

**UVM**

1. Fix for callback registration order for pending register.
2. “Interrupt\_monitor” will only generate in case of “intr.overflow”.
3. Fix for issues in UVM output for "uvm\_class\_name\_inst=true" property when referring to an external block inside the chip in case of chip-in-chip flow.

**C Header**

1. Fix for naming issue in case of deep hierarchy of sections when “cheader.name\_format” property is applied on the top.
2. Fix for duplicate filler generation issue in C header output.
3. Fix for issue in C Header output for "cheader.name\_format" UDP in case of deep reggroup hierarchy.

**General**

1. Fix for “dir\_out\_specific” switch for misrac, uvm, xrsl and autoseq output.
2. Fix for all properties which takes variant as an argument to the value of property defined in the spec.
3. Following fixes have been done while importing an IP-XACT file :
4. Fix when register size is less than address unit
5. Fix for number format
6. Fix for field name
7. Fix for RW register pair
8. Fix for description issue for IDSExcel input when description has extra curl ({) braces.
9. Fix for markdown output to convert “\n”  into <br>.
10. Fix for PDF-Alt4 layout issue in case of register table.
11. Fix for IDSExcel export configuration issue in case of multiout.
12. Fix for address overlap issue in annotation check in case of chip-in-chip flow.
13. Improvement in generation of C-APIs using “-fast\_capi” switch.

**ISequenceSpec™ (ISS)**

**Enhancements**

1. Following enhancements have been made in ISS uvm and firmware output :

* 1. Loading Memory from a text file ([More Details](https://www.agnisys.com/release/docs/ids/Memory1.html#loading_memory))
  2. Arguments and variables can be defined as two dimensional arrays, and can be further used as [arguments](https://www.agnisys.com/release/docs/ids/arrayofarguments.html#2D_as_array)/[variables](https://www.agnisys.com/release/docs/ids/arrayofvariables.html#2D_as_variable) to function calls ([More Details](https://www.agnisys.com/release/docs/ids/CMSIS.html#CMSIS))

2. Two new outputs are supported in ISS :

 1. CMSIS : Users can specify ARM device drivers in ISS & can generate CMSIS driver packages which can be imported in Keil(R) software using “iss\_cmsis” switch. ([More Details](https://www.agnisys.com/release/docs/ids/CMSIS.html))

2. MISRA C : Users can [generate the MISRA C Compliant Firmware using “-iss\_misrac” switch.](https://docs.google.com/document/d/1_O6uGcllKd5OJ2jDCapaxM3qOLyOJ_dJP5geHRnIghg/edit#heading=h.yw5yc6fzmpqe)([More Details](https://www.agnisys.com/release/docs/ids/ISSFirmwareMISRACComplaince.html))

3. Chip inside Chip is supported in the ISS. ([More Details](https://www.agnisys.com/release/docs/ids/Chip-inside-ChipFlow.html#chip_inside_chip_ISS))

**Bug Fixes**

1. Fix for undefined variables that are created when reading registers in case of chip with repeated block and register.
2. Fix for one-dimensional arrays in case of function and argument.
3. Fix for part select of the argument in ISS firmware and ISS uvm output.

**ARV™**

**Enhancements**

1. “arv\_report” switch has been introduced to generate the HTML reports for the coverage in ARV-Sim.

**Specta-AV™**

**Enhancements**

1. Chip Level scenario is supported in Specta-AV. ([More Details](https://www.agnisys.com/release/docs/ids/RTLWrapper1.html))
2. Two Dimensional variables are supported in checkers. ([More Details](https://www.agnisys.com/release/docs/ids/Checker.html#2D_checker))

**Bug Fixes**

1. Fix for the register name in “tapper” interface file.

**IDS NextGen™ (IDS-NG)**

**Enhancements**

1. Supported RDLEditor 2.0 in IDS-NG. ([More Details](https://www.agnisys.com/release/docs/ids/SpecialFeatures.html#rdl2))

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