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| 1.1.1.311 | [CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET7](#1.1.1.311.0) | 0x00000000 | 0x3C0 |  |
| 1.1.1.312 | [RET\_ENC\_SUM\_ME0\_Y\_DIR\_LOWER](#1.1.1.312.0) | 0x00000000 | 0x3C0 |  |
| 1.1.1.314 | [RET\_ENC\_SUM\_ME0\_Y\_DIR\_HIGHER](#1.1.1.314.0) | 0x00000000 | 0x3C4 |  |
| 1.1.1.316 | [RET\_ENC\_SUM\_ME1\_X\_DIR\_LOWER](#1.1.1.316.0) | 0x00000000 | 0x3C8 |  |
| 1.1.1.318 | [RET\_DEC\_WARN\_INFO](#1.1.1.318.0) | 0x00000000 | 0x3CC |  |
| 1.1.1.319 | [RET\_ENC\_SUM\_ME1\_X\_DIR\_HIGHER](#1.1.1.319.0) | 0x00000000 | 0x3CC |  |
| 1.1.1.321 | [CMD\_SET\_FB\_ADDR\_LUMA\_BASE8](#1.1.1.321.0) | 0x00000000 | 0x3D0 |  |
| 1.1.1.322 | [RET\_DEC\_ERR\_INFO](#1.1.1.322.0) | 0x00000000 | 0x3D0 |  |
| 1.1.1.323 | [RET\_ENC\_SUM\_ME1\_Y\_DIR\_LOWER](#1.1.1.323.0) | 0x00000000 | 0x3D0 |  |
| 1.1.1.325 | [CMD\_SET\_FB\_ADDR\_CB\_BASE8](#1.1.1.325.0) | 0x00000000 | 0x3D4 |  |
| 1.1.1.326 | [RET\_DEC\_DECODING\_SUCCESS](#1.1.1.326.0) | 0x00000000 | 0x3D4 |  |
| 1.1.1.327 | [RET\_ENC\_SUM\_ME1\_Y\_DIR\_HIGHER](#1.1.1.327.0) | 0x00000000 | 0x3D4 |  |
| 1.1.1.329 | [CMD\_SET\_FB\_ADDR\_CR\_BASE8](#1.1.1.329.0) | 0x00000000 | 0x3D8 |  |
| 1.1.1.330 | [CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET8](#1.1.1.330.0) | 0x00000000 | 0x3D8 |  |
| 1.1.1.332 | [CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET8](#1.1.1.332.0) | 0x00000000 | 0x3DC |  |
| 1.1.1.334 | [CMD\_SET\_FB\_ADDR\_COL8](#1.1.1.334.0) | 0x00000000 | 0x3E0 |  |
| 1.1.1.336 | [CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE8](#1.1.1.336.0) | 0x00000000 | 0x3E4 |  |
| 1.1.1.338 | [CMD\_SET\_FB\_ADDR\_LUMA\_BASE9](#1.1.1.338.0) | 0x00000000 | 0x3E8 |  |
| 1.1.1.340 | [CMD\_SET\_FB\_ADDR\_CB\_BASE9](#1.1.1.340.0) | 0x00000000 | 0x3EC |  |
| 1.1.1.342 | [CMD\_SET\_FB\_ADDR\_CR\_BASE9](#1.1.1.342.0) | 0x00000000 | 0x3F0 |  |
| 1.1.1.343 | [CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET9](#1.1.1.343.0) | 0x00000000 | 0x3F0 |  |
| 1.1.1.345 | [CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET9](#1.1.1.345.0) | 0x00000000 | 0x3F4 |  |
| 1.1.1.347 | [CMD\_SET\_FB\_ADDR\_COL9](#1.1.1.347.0) | 0x00000000 | 0x3F8 |  |
| 1.1.1.348 | [RET\_ENC\_SRC\_DEBUG\_0](#1.1.1.348.0) | 0x00000000 | 0x3F8 |  |
| 1.1.1.350 | [CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE9](#1.1.1.350.0) | 0x00000000 | 0x3FC |  |
| 1.1.1.351 | [RET\_ENC\_SRC\_DEBUG\_1](#1.1.1.351.0) | 0x00000000 | 0x3FC |  |
| 1.1.1.353 | [CMD\_SET\_FB\_ADDR\_LUMA\_BASE10](#1.1.1.353.0) | 0x00000000 | 0x400 |  |
| 1.1.1.355 | [CMD\_SET\_FB\_ADDR\_CB\_BASE10](#1.1.1.355.0) | 0x00000000 | 0x404 |  |
| 1.1.1.357 | [CMD\_SET\_FB\_ADDR\_CR\_BASE10](#1.1.1.357.0) | 0x00000000 | 0x408 |  |
| 1.1.1.358 | [CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET10](#1.1.1.358.0) | 0x00000000 | 0x408 |  |
| 1.1.1.360 | [CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET10](#1.1.1.360.0) | 0x00000000 | 0x40C |  |
| 1.1.1.362 | [CMD\_SET\_FB\_ADDR\_COL10](#1.1.1.362.0) | 0x00000000 | 0x410 |  |
| 1.1.1.364 | [CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE10](#1.1.1.364.0) | 0x00000000 | 0x414 |  |
| 1.1.1.366 | [CMD\_SET\_FB\_ADDR\_LUMA\_BASE11](#1.1.1.366.0) | 0x00000000 | 0x418 |  |
| 1.1.1.368 | [CMD\_SET\_FB\_ADDR\_CB\_BASE11](#1.1.1.368.0) | 0x00000000 | 0x41C |  |
| 1.1.1.370 | [CMD\_SET\_FB\_ADDR\_CR\_BASE11](#1.1.1.370.0) | 0x00000000 | 0x420 |  |
| 1.1.1.371 | [CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET11](#1.1.1.371.0) | 0x00000000 | 0x420 |  |
| 1.1.1.373 | [CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET11](#1.1.1.373.0) | 0x00000000 | 0x424 |  |
| 1.1.1.375 | [CMD\_SET\_FB\_ADDR\_COL11](#1.1.1.375.0) | 0x00000000 | 0x428 |  |
| 1.1.1.377 | [CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE11](#1.1.1.377.0) | 0x00000000 | 0x42C |  |
| 1.1.1.379 | [CMD\_SET\_FB\_ADDR\_LUMA\_BASE12](#1.1.1.379.0) | 0x00000000 | 0x430 |  |
| 1.1.1.381 | [CMD\_SET\_FB\_ADDR\_CB\_BASE12](#1.1.1.381.0) | 0x00000000 | 0x434 |  |
| 1.1.1.383 | [CMD\_SET\_FB\_ADDR\_CR\_BASE12](#1.1.1.383.0) | 0x00000000 | 0x438 |  |
| 1.1.1.384 | [CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET12](#1.1.1.384.0) | 0x00000000 | 0x438 |  |
| 1.1.1.386 | [CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET12](#1.1.1.386.0) | 0x00000000 | 0x43C |  |
| 1.1.1.388 | [CMD\_SET\_FB\_ADDR\_COL12](#1.1.1.388.0) | 0x00000000 | 0x440 |  |
| 1.1.1.390 | [CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE12](#1.1.1.390.0) | 0x00000000 | 0x444 |  |
| 1.1.1.392 | [CMD\_SET\_FB\_ADDR\_LUMA\_BASE13](#1.1.1.392.0) | 0x00000000 | 0x448 |  |
| 1.1.1.394 | [CMD\_SET\_FB\_ADDR\_CB\_BASE13](#1.1.1.394.0) | 0x00000000 | 0x44C |  |
| 1.1.1.396 | [CMD\_SET\_FB\_ADDR\_CR\_BASE13](#1.1.1.396.0) | 0x00000000 | 0x450 |  |
| 1.1.1.397 | [CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET13](#1.1.1.397.0) | 0x00000000 | 0x450 |  |
| 1.1.1.399 | [CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET13](#1.1.1.399.0) | 0x00000000 | 0x454 |  |
| 1.1.1.401 | [CMD\_SET\_FB\_ADDR\_COL13](#1.1.1.401.0) | 0x00000000 | 0x458 |  |
| 1.1.1.403 | [CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE13](#1.1.1.403.0) | 0x00000000 | 0x45C |  |
| 1.1.1.405 | [CMD\_SET\_FB\_ADDR\_LUMA\_BASE14](#1.1.1.405.0) | 0x00000000 | 0x460 |  |
| 1.1.1.407 | [CMD\_SET\_FB\_ADDR\_CB\_BASE14](#1.1.1.407.0) | 0x00000000 | 0x464 |  |
| 1.1.1.409 | [CMD\_SET\_FB\_ADDR\_CR\_BASE14](#1.1.1.409.0) | 0x00000000 | 0x468 |  |
| 1.1.1.410 | [CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET14](#1.1.1.410.0) | 0x00000000 | 0x468 |  |
| 1.1.1.412 | [CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET14](#1.1.1.412.0) | 0x00000000 | 0x46C |  |
| 1.1.1.414 | [CMD\_SET\_FB\_ADDR\_COL14](#1.1.1.414.0) | 0x00000000 | 0x470 |  |
| 1.1.1.416 | [CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE14](#1.1.1.416.0) | 0x00000000 | 0x474 |  |
| 1.1.1.418 | [CMD\_SET\_FB\_ADDR\_LUMA\_BASE15](#1.1.1.418.0) | 0x00000000 | 0x478 |  |
| 1.1.1.420 | [CMD\_SET\_FB\_ADDR\_CB\_BASE15](#1.1.1.420.0) | 0x00000000 | 0x47C |  |
| 1.1.1.422 | [CMD\_SET\_FB\_ADDR\_CR\_BASE15](#1.1.1.422.0) | 0x00000000 | 0x480 |  |
| 1.1.1.423 | [CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET15](#1.1.1.423.0) | 0x00000000 | 0x480 |  |
| 1.1.1.425 | [CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET15](#1.1.1.425.0) | 0x00000000 | 0x484 |  |
| 1.1.1.427 | [CMD\_SET\_FB\_ADDR\_COL15](#1.1.1.427.0) | 0x00000000 | 0x488 |  |
| 1.1.1.429 | [CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE15](#1.1.1.429.0) | 0x00000000 | 0x48C |  |
| 1.1.1.432 | [CMD\_SET\_FB\_ADDR\_DEFAULT\_CDF](#1.1.1.432.0) | 0x00000000 | 0x494 |  |
| 1.1.1.434 | [CMD\_SET\_FB\_ADDR\_SEGMAP](#1.1.1.434.0) | 0x00000000 | 0x498 |  |
| 1.1.1.436 | [CMD\_SET\_FB\_DEC\_PP\_PVRIC\_CTRL](#1.1.1.436.0) | 0x00000000 | 0x49C |  |
| 1.1.1.439 | [CMD\_SET\_FB\_DEC\_PP\_SCL\_PARAM](#1.1.1.439.0) | 0x00000000 | 0x4A4 |  |
| 1.1.1.448 | [CMD\_SET\_FB\_DEC\_PP\_CROP\_POS](#1.1.1.448.0) | 0x00000000 | 0x4C4 |  |
| 1.1.1.450 | [CMD\_SET\_FB\_DEC\_PP\_CROP\_SIZE](#1.1.1.450.0) | 0x00000000 | 0x4C8 |  |
| 1.1.1.452 | [CMD\_SET\_FB\_DEC\_PP\_AFBC\_COMMON](#1.1.1.452.0) | 0x00000000 | 0x4CC |  |
| 1.1.1.457 | [CMD\_SET\_FB\_DEC\_ADDR\_COL\_DUAL](#1.1.1.457.0) | 0x00000000 | 0x4DC |  |
| 1.1.1.1 | [HOST\_GLOBAL\_WR](#1.1.1.1.0) | 0x00000000 | 0x000 |  |
| 1.1.1.2 | [VCPU\_CUR\_PC](#1.1.1.2.0) | 0x00000000 | 0x004 |  |
| 1.1.1.3 | [VCPU\_CUR\_LR](#1.1.1.3.0) | 0x00000000 | 0x008 |  |
| 1.1.1.4 | [DBG\_MSG\_17](#1.1.1.4.0) | 0x00000000 | 0x00C |  |
| 1.1.1.5 | [DBG\_MSG\_18](#1.1.1.5.0) | 0x00000000 | 0x010 |  |
| 1.1.1.6 | [DBG\_MSG\_19](#1.1.1.6.0) | 0x00000000 | 0x014 |  |
| 1.1.1.7 | [DBG\_MSG\_20](#1.1.1.7.0) | 0x00000000 | 0x018 |  |
| 1.1.1.8 | [DBG\_MSG\_21](#1.1.1.8.0) | 0x00000000 | 0x01C |  |
| 1.1.1.9 | [VPU\_FIO\_ADDR](#1.1.1.9.0) | 0x00000000 | 0x020 |  |
| 1.1.1.10 | [VPU\_FIO\_DATA](#1.1.1.10.0) | 0x00000000 | 0x024 |  |
| 1.1.1.11 | [DBG\_MSG\_0](#1.1.1.11.0) | 0x00000000 | 0x028 |  |
| 1.1.1.12 | [DBG\_MSG\_1](#1.1.1.12.0) | 0x00000000 | 0x02C |  |
| 1.1.1.13 | [DBG\_MSG\_22](#1.1.1.13.0) | 0x00000000 | 0x030 |  |
| 1.1.1.14 | [VPU\_VINT\_REASON\_CLR](#1.1.1.14.0) | 0x00000000 | 0x034 |  |
| 1.1.1.15 | [VPU\_HOST\_INT\_REQ](#1.1.1.15.0) | 0x00000000 | 0x038 |  |
| 1.1.1.16 | [VPU\_VINT\_CLEAR](#1.1.1.16.0) | 0x00000000 | 0x03C |  |
| 1.1.1.17 | [VPU\_HINT\_CLEAR](#1.1.1.17.0) | 0x00000000 | 0x040 |  |
| 1.1.1.18 | [VPU\_VPU\_INT\_STS](#1.1.1.18.0) | 0x00000000 | 0x044 |  |
| 1.1.1.19 | [VPU\_VINT\_ENABLE](#1.1.1.19.0) | 0x00000000 | 0x048 |  |
| 1.1.1.20 | [VPU\_VINT\_REASON](#1.1.1.20.0) | 0x00000000 | 0x04C |  |
| 1.1.1.22 | [VCPU\_RESTART](#1.1.1.22.0) | 0x00000000 | 0x058 |  |
| 1.1.1.24 | [VPU\_REMAP\_CTRL](#1.1.1.24.0) | 0x00000000 | 0x060 |  |
| 1.1.1.25 | [VPU\_REMAP\_VADDR](#1.1.1.25.0) | 0x00000000 | 0x064 |  |
| 1.1.1.26 | [VPU\_REMAP\_PADDR](#1.1.1.26.0) | 0x00000000 | 0x068 |  |
| 1.1.1.27 | [VPU\_REMAP\_CORE\_START](#1.1.1.27.0) | 0x00000000 | 0x06C |  |
| 1.1.1.28 | [VCPU\_CMD\_BUSY\_STATUS](#1.1.1.28.0) | 0x00000000 | 0x070 |  |
| 1.1.1.29 | [VPU\_HALT\_STATUS](#1.1.1.29.0) | 0x00000000 | 0x074 |  |
| 1.1.1.30 | [VPU\_VCPU\_STATUS](#1.1.1.30.0) | 0x00000000 | 0x078 |  |
| 1.1.1.31 | [VPU\_BUSY\_STATUS](#1.1.1.31.0) | 0x00000000 | 0x07C |  |
| 1.1.1.32 | [RET\_FIO\_STATUS](#1.1.1.32.0) | 0x00000000 | 0x080 |  |
| 1.1.1.33 | [DBG\_MSG\_3](#1.1.1.33.0) | 0x00000000 | 0x084 |  |
| 1.1.1.34 | [DBG\_MSG\_4](#1.1.1.34.0) | 0x00000000 | 0x088 |  |
| 1.1.1.35 | [DBG\_MSG\_5](#1.1.1.35.0) | 0x00000000 | 0x08C |  |
| 1.1.1.36 | [RET\_PRODUCT\_NAME](#1.1.1.36.0) | 0x00000000 | 0x090 |  |
| 1.1.1.37 | [RET\_PRODUCT\_VERSION](#1.1.1.37.0) | 0x00000000 | 0x094 |  |
| 1.1.1.38 | [RET\_VCPU\_CONFIG0](#1.1.1.38.0) | 0x00000000 | 0x098 |  |
| 1.1.1.39 | [RET\_VCPU\_CONFIG1](#1.1.1.39.0) | 0x00000000 | 0x09C |  |
| 1.1.1.40 | [RET\_CODEC\_STD](#1.1.1.40.0) | 0x00000000 | 0x0A0 |  |
| 1.1.1.41 | [RET\_CONF\_DATE](#1.1.1.41.0) | 0x00000000 | 0x0A4 |  |
| 1.1.1.42 | [RET\_CONF\_REVISION](#1.1.1.42.0) | 0x00000000 | 0x0A8 |  |
| 1.1.1.43 | [RET\_CONF\_TYPE](#1.1.1.43.0) | 0x00000000 | 0x0AC |  |
| 1.1.1.44 | [RET\_VCORE0\_CFG](#1.1.1.44.0) | 0x00000000 | 0x0B0 |  |
| 1.1.1.45 | [RET\_VCORE1\_CFG](#1.1.1.45.0) | 0x00000000 | 0x0B4 |  |
| 1.1.1.46 | [RET\_VCORE2\_CFG](#1.1.1.46.0) | 0x00000000 | 0x0B8 |  |
| 1.1.1.47 | [RET\_VCORE3\_CFG](#1.1.1.47.0) | 0x00000000 | 0x0BC |  |
| 1.1.1.48 | [VPU\_RET\_VCORE\_PRESENT](#1.1.1.48.0) | 0x00000000 | 0x0C0 |  |
| 1.1.1.49 | [DBG\_MSG\_6](#1.1.1.49.0) | 0x00000000 | 0x0C4 |  |
| 1.1.1.50 | [DBG\_MSG\_7](#1.1.1.50.0) | 0x00000000 | 0x0C8 |  |
| 1.1.1.51 | [DBG\_MSG\_8](#1.1.1.51.0) | 0x00000000 | 0x0CC |  |
| 1.1.1.52 | [DBG\_MSG\_9](#1.1.1.52.0) | 0x00000000 | 0x0D0 |  |
| 1.1.1.54 | [DBG\_MSG\_10](#1.1.1.54.0) | 0x00000000 | 0x0D8 |  |
| 1.1.1.55 | [DBG\_MSG\_11](#1.1.1.55.0) | 0x00000000 | 0x0DC |  |
| 1.1.1.56 | [DBG\_MSG\_12](#1.1.1.56.0) | 0x00000000 | 0x0E0 |  |
| 1.1.1.57 | [DBG\_MSG\_13](#1.1.1.57.0) | 0x00000000 | 0x0E4 |  |
| 1.1.1.58 | [DBG\_MSG\_14](#1.1.1.58.0) | 0x00000000 | 0x0E8 |  |
| 1.1.1.59 | [DBG\_MSG\_15](#1.1.1.59.0) | 0x00000000 | 0x0EC |  |
| 1.1.1.60 | [VPU\_DBG\_SW\_UART\_STATUS](#1.1.1.60.0) | 0x00000000 | 0x0F0 |  |
| 1.1.1.61 | [VPU\_DBG\_SW\_UART\_TX](#1.1.1.61.0) | 0x00000000 | 0x0F4 |  |
| 1.1.1.62 | [VPU\_DBG\_REG\_0](#1.1.1.62.0) | 0x00000000 | 0x0F8 |  |
| 1.1.1.63 | [VPU\_DBG\_REG\_1](#1.1.1.63.0) | 0x00000000 | 0x0FC |  |
| 1.1.1.65 | [VPU\_SUB\_FRAME\_SYNC\_CTRL](#1.1.1.65.0) | 0x00000000 | 0x11C |  |
| 1.1.1.67 | [COMMAND](#1.1.1.67.0) | 0x00000000 | 0x200 |  |
| 1.1.1.68 | [CMD\_DEC\_PIC\_OPTION](#1.1.1.68.0) | 0x00000000 | 0x204 |  |
| 1.1.1.73 | [RET\_SUCCESS](#1.1.1.73.0) | 0x00000000 | 0x208 |  |
| 1.1.1.74 | [RET\_FAIL\_REASON](#1.1.1.74.0) | 0x00000000 | 0x20C |  |
| 1.1.1.75 | [CMD\_INSTANCE\_INFO](#1.1.1.75.0) | 0x00000000 | 0x210 |  |
| 1.1.1.76 | [CMD\_QUE\_FULL\_IDC](#1.1.1.76.0) | 0x00000000 | 0x214 |  |
| 1.1.1.77 | [RET\_QUE\_EMPTY\_IDC](#1.1.1.77.0) | 0x00000000 | 0x218 |  |
| 1.1.1.78 | [CMD\_DONE\_INST\_IDC](#1.1.1.78.0) | 0x00000000 | 0x21C |  |
| 1.1.1.79 | [RET\_CREATE\_INSTANCE\_ID](#1.1.1.79.0) | 0x00000000 | 0x220 |  |
| 1.1.1.81 | [RET\_CMD\_CQ\_IN\_TICK](#1.1.1.81.0) | 0x00000000 | 0x23C |  |
| 1.1.1.82 | [RET\_CMD\_FW\_RUN\_TICK](#1.1.1.82.0) | 0x00000000 | 0x240 |  |
| 1.1.1.83 | [RET\_CMD\_HW\_RUN\_TICK](#1.1.1.83.0) | 0x00000000 | 0x244 |  |
| 1.1.1.84 | [RET\_CMD\_HW\_DONE\_TICK](#1.1.1.84.0) | 0x00000000 | 0x248 |  |
| 1.1.1.85 | [RET\_CMD\_FW\_DONE\_TICK](#1.1.1.85.0) | 0x00000000 | 0x24C |  |
| 1.1.1.86 | [RET\_CMD\_RQ\_OUT\_TICK](#1.1.1.86.0) | 0x00000000 | 0x250 |  |
| 1.1.1.87 | [RET\_CMD\_FW\_RRE\_RUN\_TICK](#1.1.1.87.0) | 0x00000000 | 0x254 |  |
| 1.1.1.88 | [RET\_CMD\_HW\_RRE\_RUN\_TICK](#1.1.1.88.0) | 0x00000000 | 0x258 |  |
| 1.1.1.89 | [RET\_CMD\_HW\_RRE\_DONE\_TICK](#1.1.1.89.0) | 0x00000000 | 0x25C |  |
| 1.1.1.90 | [RET\_CMD\_FW\_RRE\_DONE\_TICK](#1.1.1.90.0) | 0x00000000 | 0x260 |  |
| 1.1.1.92 | [CMD\_BS\_RD\_PTR](#1.1.1.92.0) | 0x00000000 | 0x300 |  |
| 1.1.1.102 | [CMD\_BS\_SIZE](#1.1.1.102.0) | 0x00000000 | 0x304 |  |
| 1.1.1.112 | [CMD\_BS\_OPTION](#1.1.1.112.0) | 0x00000000 | 0x308 |  |
| 1.1.1.118 | [CMD\_ENC\_SEQ\_PARAM](#1.1.1.118.0) | 0x00000000 | 0x30C |  |
| 1.1.1.124 | [CMD\_CREATE\_INST\_BS\_PARAM](#1.1.1.124.0) | 0x00000000 | 0x310 |  |
| 1.1.1.131 | [CMD\_DEC\_SEI\_MASK](#1.1.1.131.0) | 0x00000000 | 0x314 |  |
| 1.1.1.136 | [CMD\_CREATE\_ADDR\_EXT](#1.1.1.136.0) | 0x00000000 | 0x318 |  |
| 1.1.1.145 | [CMD\_DEC\_FORCE\_FB\_LATENCY\_PLUS1](#1.1.1.145.0) | 0x00000000 | 0x31C |  |
| 1.1.1.151 | [CMD\_ENC\_CUSTOM\_MAP\_OPTION\_PARAM](#1.1.1.151.0) | 0x00000000 | 0x320 |  |
| 1.1.1.156 | [CMD\_ENC\_CUSTOM\_MAP\_OPTION\_ADDR](#1.1.1.156.0) | 0x00000000 | 0x324 |  |
| 1.1.1.161 | [CMD\_ENC\_SEQ\_SLICE\_PARAM](#1.1.1.161.0) | 0x00000000 | 0x328 |  |
| 1.1.1.165 | [CMD\_ENC\_SEQ\_INTRA\_REFRESH](#1.1.1.165.0) | 0x00000000 | 0x32C |  |
| 1.1.1.170 | [CMD\_CREATE\_INST\_CORE\_INFO](#1.1.1.170.0) | 0x00000000 | 0x330 |  |
| 1.1.1.177 | [CMD\_CREATE\_INST\_PRIORITY](#1.1.1.177.0) | 0x00000000 | 0x334 |  |
| 1.1.1.183 | [CMD\_ENC\_SEQ\_RC\_TARGET\_RATE](#1.1.1.183.0) | 0x00000000 | 0x338 |  |
| 1.1.1.188 | [CMD\_ENC\_SEQ\_RC\_PARAM](#1.1.1.188.0) | 0x00000000 | 0x33C |  |
| 1.1.1.193 | [CMD\_ENC\_SEQ\_HVS\_PARAM](#1.1.1.193.0) | 0x00000000 | 0x340 |  |
| 1.1.1.198 | [CMD\_ENC\_SEQ\_RC\_MAX\_BITRATE](#1.1.1.198.0) | 0x00000000 | 0x344 |  |
| 1.1.1.202 | [CMD\_CREATE\_INST\_ADDR\_TEMP\_BASE](#1.1.1.202.0) | 0x00000000 | 0x348 |  |
| 1.1.1.209 | [CMD\_CREATE\_INST\_TEMP\_SIZE](#1.1.1.209.0) | 0x00000000 | 0x34C |  |
| 1.1.1.215 | [CMD\_CREATE\_INST\_ADDR\_SEC\_AXI](#1.1.1.215.0) | 0x00000000 | 0x350 |  |
| 1.1.1.221 | [CMD\_CREATE\_INST\_SEC\_AXI\_SIZE](#1.1.1.221.0) | 0x00000000 | 0x354 |  |
| 1.1.1.227 | [CMD\_CREATE\_INST\_ADDR\_AR\_TABLE](#1.1.1.227.0) | 0x00000000 | 0x358 |  |
| 1.1.1.233 | [CMD\_ENC\_PREFIX\_SEI\_INFO](#1.1.1.233.0) | 0x00000000 | 0x35C |  |
| 1.1.1.237 | [CMD\_ENC\_SUFFIX\_SEI\_NAL\_ADDR](#1.1.1.237.0) | 0x00000000 | 0x360 |  |
| 1.1.1.242 | [CMD\_ENC\_SUFFIX\_SEI\_INFO](#1.1.1.242.0) | 0x00000000 | 0x364 |  |
| 1.1.1.246 | [CMD\_SET\_FB\_ADDR\_COL3](#1.1.1.246.0) | 0x00000000 | 0x368 |  |
| 1.1.1.249 | [CMD\_ENC\_SEQ\_BG\_PARAM](#1.1.1.249.0) | 0x00000000 | 0x36C |  |
| 1.1.1.253 | [CMD\_ENC\_SEQ\_NON\_VCL\_PARAM](#1.1.1.253.0) | 0x00000000 | 0x370 |  |
| 1.1.1.257 | [CMD\_ENC\_CSC\_COEFF\_0](#1.1.1.257.0) | 0x00000000 | 0x374 |  |
| 1.1.1.261 | [CMD\_ENC\_CSC\_COEFF\_1](#1.1.1.261.0) | 0x00000000 | 0x378 |  |
| 1.1.1.266 | [CMD\_ENC\_CSC\_COEFF\_2](#1.1.1.266.0) | 0x00000000 | 0x37C |  |
| 1.1.1.269 | [CMD\_ENC\_CSC\_COEFF\_3](#1.1.1.269.0) | 0x00000000 | 0x380 |  |
| 1.1.1.273 | [CMD\_ENC\_SEQ\_QUANT\_PARAM\_0](#1.1.1.273.0) | 0x00000000 | 0x384 |  |
| 1.1.1.275 | [CMD\_ENC\_SEQ\_QUANT\_PARAM\_1](#1.1.1.275.0) | 0x00000000 | 0x388 |  |
| 1.1.1.277 | [CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PARAM](#1.1.1.277.0) | 0x00000000 | 0x38C |  |
| 1.1.1.279 | [CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_0](#1.1.1.279.0) | 0x00000000 | 0x390 |  |
| 1.1.1.282 | [CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_1](#1.1.1.282.0) | 0x00000000 | 0x394 |  |
| 1.1.1.285 | [CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_2](#1.1.1.285.0) | 0x00000000 | 0x398 |  |
| 1.1.1.287 | [CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_3](#1.1.1.287.0) | 0x00000000 | 0x39C |  |
| 1.1.1.289 | [CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_4](#1.1.1.289.0) | 0x00000000 | 0x3A0 |  |
| 1.1.1.292 | [CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_5](#1.1.1.292.0) | 0x00000000 | 0x3A4 |  |
| 1.1.1.295 | [CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_6](#1.1.1.295.0) | 0x00000000 | 0x3A8 |  |
| 1.1.1.299 | [CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_7](#1.1.1.299.0) | 0x00000000 | 0x3AC |  |
| 1.1.1.302 | [CMD\_SET\_FB\_ADDR\_COL6](#1.1.1.302.0) | 0x00000000 | 0x3B0 |  |
| 1.1.1.304 | [CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE6](#1.1.1.304.0) | 0x00000000 | 0x3B4 |  |
| 1.1.1.306 | [CMD\_SET\_FB\_ADDR\_LUMA\_BASE7](#1.1.1.306.0) | 0x00000000 | 0x3B8 |  |
| 1.1.1.308 | [CMD\_SET\_FB\_ADDR\_CB\_BASE7](#1.1.1.308.0) | 0x00000000 | 0x3BC |  |
| 1.1.1.310 | [CMD\_SET\_FB\_ADDR\_CR\_BASE7](#1.1.1.310.0) | 0x00000000 | 0x3C0 |  |
| 1.1.1.313 | [CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET7](#1.1.1.313.0) | 0x00000000 | 0x3C4 |  |
| 1.1.1.315 | [CMD\_SET\_FB\_ADDR\_COL7](#1.1.1.315.0) | 0x00000000 | 0x3C8 |  |
| 1.1.1.317 | [CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE7](#1.1.1.317.0) | 0x00000000 | 0x3CC |  |
| 1.1.1.320 | [CMD\_ENC\_SEQ\_TILE\_PARAM](#1.1.1.320.0) | 0x00000000 | 0x3D0 |  |
| 1.1.1.324 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_0](#1.1.1.324.0) | 0x00000000 | 0x3D4 |  |
| 1.1.1.328 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_1](#1.1.1.328.0) | 0x00000000 | 0x3D8 |  |
| 1.1.1.331 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_2](#1.1.1.331.0) | 0x00000000 | 0x3DC |  |
| 1.1.1.333 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_3](#1.1.1.333.0) | 0x00000000 | 0x3E0 |  |
| 1.1.1.335 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_4](#1.1.1.335.0) | 0x00000000 | 0x3E4 |  |
| 1.1.1.337 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_5](#1.1.1.337.0) | 0x00000000 | 0x3E8 |  |
| 1.1.1.339 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_6](#1.1.1.339.0) | 0x00000000 | 0x3EC |  |
| 1.1.1.341 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_7](#1.1.1.341.0) | 0x00000000 | 0x3F0 |  |
| 1.1.1.344 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_8](#1.1.1.344.0) | 0x00000000 | 0x3F4 |  |
| 1.1.1.346 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_9](#1.1.1.346.0) | 0x00000000 | 0x3F8 |  |
| 1.1.1.349 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_10](#1.1.1.349.0) | 0x00000000 | 0x3FC |  |
| 1.1.1.352 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_11](#1.1.1.352.0) | 0x00000000 | 0x400 |  |
| 1.1.1.354 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_12](#1.1.1.354.0) | 0x00000000 | 0x404 |  |
| 1.1.1.356 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_13](#1.1.1.356.0) | 0x00000000 | 0x408 |  |
| 1.1.1.359 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_14](#1.1.1.359.0) | 0x00000000 | 0x40C |  |
| 1.1.1.361 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_15](#1.1.1.361.0) | 0x00000000 | 0x410 |  |
| 1.1.1.363 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_16](#1.1.1.363.0) | 0x00000000 | 0x414 |  |
| 1.1.1.365 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_17](#1.1.1.365.0) | 0x00000000 | 0x418 |  |
| 1.1.1.367 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_18](#1.1.1.367.0) | 0x00000000 | 0x41C |  |
| 1.1.1.369 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_19](#1.1.1.369.0) | 0x00000000 | 0x420 |  |
| 1.1.1.372 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_20](#1.1.1.372.0) | 0x00000000 | 0x424 |  |
| 1.1.1.374 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_21](#1.1.1.374.0) | 0x00000000 | 0x428 |  |
| 1.1.1.376 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_22](#1.1.1.376.0) | 0x00000000 | 0x42C |  |
| 1.1.1.378 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_23](#1.1.1.378.0) | 0x00000000 | 0x430 |  |
| 1.1.1.380 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_24](#1.1.1.380.0) | 0x00000000 | 0x434 |  |
| 1.1.1.382 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_25](#1.1.1.382.0) | 0x00000000 | 0x438 |  |
| 1.1.1.385 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_26](#1.1.1.385.0) | 0x00000000 | 0x43C |  |
| 1.1.1.387 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_27](#1.1.1.387.0) | 0x00000000 | 0x440 |  |
| 1.1.1.389 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_28](#1.1.1.389.0) | 0x00000000 | 0x444 |  |
| 1.1.1.391 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_29](#1.1.1.391.0) | 0x00000000 | 0x448 |  |
| 1.1.1.393 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_30](#1.1.1.393.0) | 0x00000000 | 0x44C |  |
| 1.1.1.395 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_31](#1.1.1.395.0) | 0x00000000 | 0x450 |  |
| 1.1.1.398 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_32](#1.1.1.398.0) | 0x00000000 | 0x454 |  |
| 1.1.1.400 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_33](#1.1.1.400.0) | 0x00000000 | 0x458 |  |
| 1.1.1.402 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_34](#1.1.1.402.0) | 0x00000000 | 0x45C |  |
| 1.1.1.404 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_35](#1.1.1.404.0) | 0x00000000 | 0x460 |  |
| 1.1.1.406 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_36](#1.1.1.406.0) | 0x00000000 | 0x464 |  |
| 1.1.1.408 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_37](#1.1.1.408.0) | 0x00000000 | 0x468 |  |
| 1.1.1.411 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_38](#1.1.1.411.0) | 0x00000000 | 0x46C |  |
| 1.1.1.413 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_39](#1.1.1.413.0) | 0x00000000 | 0x470 |  |
| 1.1.1.415 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_40](#1.1.1.415.0) | 0x00000000 | 0x474 |  |
| 1.1.1.417 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_41](#1.1.1.417.0) | 0x00000000 | 0x478 |  |
| 1.1.1.419 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_42](#1.1.1.419.0) | 0x00000000 | 0x47C |  |
| 1.1.1.421 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_43](#1.1.1.421.0) | 0x00000000 | 0x480 |  |
| 1.1.1.424 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_44](#1.1.1.424.0) | 0x00000000 | 0x484 |  |
| 1.1.1.426 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_45](#1.1.1.426.0) | 0x00000000 | 0x488 |  |
| 1.1.1.428 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_46](#1.1.1.428.0) | 0x00000000 | 0x48C |  |
| 1.1.1.430 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_47](#1.1.1.430.0) | 0x00000000 | 0x490 |  |
| 1.1.1.431 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_48](#1.1.1.431.0) | 0x00000000 | 0x494 |  |
| 1.1.1.433 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_49](#1.1.1.433.0) | 0x00000000 | 0x498 |  |
| 1.1.1.435 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_50](#1.1.1.435.0) | 0x00000000 | 0x49C |  |
| 1.1.1.437 | [CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_51](#1.1.1.437.0) | 0x00000000 | 0x4A0 |  |
| 1.1.1.438 | [CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_0\_QP](#1.1.1.438.0) | 0x00000000 | 0x4A4 |  |
| 1.1.1.440 | [CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_1\_QP](#1.1.1.440.0) | 0x00000000 | 0x4A8 |  |
| 1.1.1.441 | [CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_2\_QP](#1.1.1.441.0) | 0x00000000 | 0x4AC |  |
| 1.1.1.442 | [CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_3\_QP](#1.1.1.442.0) | 0x00000000 | 0x4B0 |  |
| 1.1.1.443 | [CMD\_ENC\_SEQ\_SCL\_SRC\_SIZE](#1.1.1.443.0) | 0x00000000 | 0x4B4 |  |
| 1.1.1.444 | [CMD\_ENC\_SEQ\_SCL\_PARAM](#1.1.1.444.0) | 0x00000000 | 0x4B8 |  |
| 1.1.1.445 | [CMD\_ENC\_SEQ\_Y2Y\_PARAM](#1.1.1.445.0) | 0x00000000 | 0x4BC |  |
| 1.1.1.446 | [CMD\_SET\_FB\_DEC\_PP\_CROP\_PARAM](#1.1.1.446.0) | 0x00000000 | 0x4C0 |  |
| 1.1.1.447 | [CMD\_ENC\_SEQ\_SFS\_PARAM](#1.1.1.447.0) | 0x00000000 | 0x4C4 |  |
| 1.1.1.449 | [CMD\_ENC\_SEQ\_CROP\_ENABLE](#1.1.1.449.0) | 0x00000000 | 0x4C8 |  |
| 1.1.1.451 | [CMD\_ENC\_SEQ\_CROP\_START\_POS](#1.1.1.451.0) | 0x00000000 | 0x4CC |  |
| 1.1.1.453 | [CMD\_ENC\_SEQ\_CROP\_SRC\_SIZE](#1.1.1.453.0) | 0x00000000 | 0x4D0 |  |
| 1.1.1.455 | [CMD\_ENC\_SEQ\_Y2Y\_DATA\_0](#1.1.1.455.0) | 0x00000000 | 0x4D8 |  |
| 1.1.1.456 | [CMD\_ENC\_SEQ\_Y2Y\_DATA\_1](#1.1.1.456.0) | 0x00000000 | 0x4DC |  |
| 1.1.1.458 | [CMD\_ENC\_SEQ\_Y2Y\_DATA\_2](#1.1.1.458.0) | 0x00000000 | 0x4E0 |  |
| 1.1.1.459 | [CMD\_ENC\_SEQ\_INPUT\_RINGBUF](#1.1.1.459.0) | 0x00000000 | 0x4E4 |  |
| 1.1.1.461 | [VPU\_PDBG\_CTRL](#1.1.1.461.0) | 0x00000000 | 0x600 |  |
| 1.1.1.462 | [VPU\_PDBG\_IDX\_REG](#1.1.1.462.0) | 0x00000000 | 0x604 |  |
| 1.1.1.463 | [VPU\_PDBG\_WDATA\_REG](#1.1.1.463.0) | 0x00000000 | 0x608 |  |
| 1.1.1.464 | [VPU\_PDBG\_RDATA\_REG](#1.1.1.464.0) | 0x00000000 | 0x60C |  |
| 1.1.1.465 | [VPU\_PDBG\_STEP\_MASK](#1.1.1.465.0) | 0x00000000 | 0x610 |  |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 1.0 | | | WAVE677DV\_ARCH | | block | 0x000 |
| offset | 0 | external | |  | size | 2048 |
|  | | | | | | |
|  | | | | | | |
| {vendor=ChipsnMedia;library=ip;version=v1.0.0} | | | | | | |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 1.1.0 | | | signals | signal |  | |
|  | | | | | | |
|  | | | | | | |
|  | | | | | | |
| name | port type | description | | | | |
| CMD\_DEC\_PIC\_OPTION\_signal | in |  | | | |  |
| CMD\_BS\_RD\_PTR\_signal | in |  | | | |  |
| CMD\_BS\_SIZE\_signal | in |  | | | |  |
| CMD\_BS\_OPTION\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_PARAM\_signal | in |  | | | |  |
| CMD\_CREATE\_INST\_BS\_PARAM\_signal | in |  | | | |  |
| CMD\_DEC\_SEI\_MASK\_signal | in |  | | | |  |
| CMD\_CREATE\_ADDR\_EXT\_signal | in |  | | | |  |
| CMD\_DEC\_FORCE\_FB\_LATENCY\_PLUS1\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_MAP\_OPTION\_PARAM\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_MAP\_OPTION\_ADDR\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_SLICE\_PARAM\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_INTRA\_REFRESH\_signal | in |  | | | |  |
| CMD\_CREATE\_INST\_CORE\_INFO\_signal | in |  | | | |  |
| CMD\_CREATE\_INST\_PRIORITY\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_RC\_TARGET\_RATE\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_RC\_PARAM\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_HVS\_PARAM\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_RC\_MAX\_BITRATE\_signal | in |  | | | |  |
| CMD\_CREATE\_INST\_ADDR\_TEMP\_BASE\_signal | in |  | | | |  |
| CMD\_CREATE\_INST\_TEMP\_SIZE\_signal | in |  | | | |  |
| CMD\_CREATE\_INST\_ADDR\_SEC\_AXI\_signal | in |  | | | |  |
| CMD\_CREATE\_INST\_SEC\_AXI\_SIZE\_signal | in |  | | | |  |
| CMD\_CREATE\_INST\_ADDR\_AR\_TABLE\_signal | in |  | | | |  |
| CMD\_ENC\_PREFIX\_SEI\_INFO\_signal | in |  | | | |  |
| CMD\_ENC\_SUFFIX\_SEI\_NAL\_ADDR\_signal | in |  | | | |  |
| CMD\_ENC\_SUFFIX\_SEI\_INFO\_signal | in |  | | | |  |
| CMD\_SET\_FB\_ADDR\_COL3\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_BG\_PARAM\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_NON\_VCL\_PARAM\_signal | in |  | | | |  |
| CMD\_ENC\_CSC\_COEFF\_0\_signal | in |  | | | |  |
| CMD\_ENC\_CSC\_COEFF\_1\_signal | in |  | | | |  |
| CMD\_ENC\_CSC\_COEFF\_2\_signal | in |  | | | |  |
| CMD\_ENC\_CSC\_COEFF\_3\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_QUANT\_PARAM\_0\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_QUANT\_PARAM\_1\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PARAM\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_0\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_1\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_2\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_3\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_4\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_5\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_6\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_7\_signal | in |  | | | |  |
| CMD\_SET\_FB\_ADDR\_COL6\_signal | in |  | | | |  |
| CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE6\_signal | in |  | | | |  |
| CMD\_SET\_FB\_ADDR\_LUMA\_BASE7\_signal | in |  | | | |  |
| CMD\_SET\_FB\_ADDR\_CB\_BASE7\_signal | in |  | | | |  |
| CMD\_SET\_FB\_ADDR\_CR\_BASE7\_signal | in |  | | | |  |
| CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET7\_signal | in |  | | | |  |
| CMD\_SET\_FB\_ADDR\_COL7\_signal | in |  | | | |  |
| CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE7\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_TILE\_PARAM\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_0\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_1\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_2\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_3\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_4\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_5\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_6\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_7\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_8\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_9\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_10\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_11\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_12\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_13\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_14\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_15\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_16\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_17\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_18\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_19\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_20\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_21\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_22\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_23\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_24\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_25\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_26\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_27\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_28\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_29\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_30\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_31\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_32\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_33\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_34\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_35\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_36\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_37\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_38\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_39\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_40\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_41\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_42\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_43\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_44\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_45\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_46\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_48\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_49\_signal | in |  | | | |  |
| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_50\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_0\_QP\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_SFS\_PARAM\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_CROP\_ENABLE\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_CROP\_START\_POS\_signal | in |  | | | |  |
| CMD\_ENC\_SEQ\_Y2Y\_DATA\_1\_signal | in |  | | | |  |

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| 1.1.1.0 | | | | WAVE6\_HOST\_IF | | | section | | 0x000 | |
| offset | 0 | external |  | | repeat |  | | size | | 2048 |
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| 1.1.1.69.0 | | | | WAVE6\_HOST\_IF\_groups | | | section | | 0x000 | |
| offset | 0 | external |  | | repeat |  | | size | | 2048 |
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| NOTE: Basically, the reset values of command I/O interface are pseudo-values. But it can be initialized as 0x0 when the host run INIT\_VPU of ref\_sw and cleared it.{range=2048} | | | | | | | | | | |

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| 1.1.1.70.0 | | | | | | | | CMD\_INIT\_SEQ\_OPTION | | | | | reg32 | | 0x204 |
| offset | | 516 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Decode picture header option{alt\_mode=CMD\_DEC\_PIC\_OPTION\_signal=1;virtualpairUid=2022-09-0709:27:31T173acdd5-3dd6-4841-8584-d31cbbc63a2c;alternate\_reg=CMD\_DEC\_PIC\_OPTION} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 5:0 | INIT\_SEQ\_OPTION | | | rw | ro | | 0x0 | | | 0x01: INIT\_SEQ  0x11: INIT\_SEQ (w/ Thumbnail mode){has\_reset=0} | | | | | |

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| 1.1.1.71.0 | | | | | | | | CMD\_OPTION | | | | | reg32 | | 0x204 |
| offset | | 516 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Command option{alt\_mode=CMD\_DEC\_PIC\_OPTION\_signal=2;virtualpairUid=2022-09-0709:27:31T173acdd5-3dd6-4841-8584-d31cbbc63a2c;alternate\_reg=CMD\_DEC\_PIC\_OPTION} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | RSVD0 | | | rw | ro | | 0x0 | | | if COMMAND is QUERY, CMD\_OPTION is as follows.  2 : ENC\_GET\_RESULT, DEC\_GET\_RESULT  3 : ENC\_FW\_STATUS (for debugging purpose)  6 : GET\_WR\_PTR  otherwise, refer to description in the relevant command.{has\_reset=0} | | | | | |

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| 1.1.1.72.0 | | | | | | | | CMD\_SET\_FB\_OPTION | | | | | reg32 | | 0x204 |
| offset | | 516 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| CMD\_SET\_FB\_OPTION {alt\_mode=CMD\_DEC\_PIC\_OPTION\_signal=3;virtualpairUid=2022-09-0709:27:31T173acdd5-3dd6-4841-8584-d31cbbc63a2c;alternate\_reg=CMD\_DEC\_PIC\_OPTION} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:27 | RSVD0 | | | rw | ro | | 0x0 | | | RSVD{has\_reset=0} | | | | | |
| 26:26 | NON\_REF\_FBC\_WRITING | | | rw | ro | | 0x0 | | | 0: disable FBC writing for non-reference pictures. (default)  1: enable FBC writing for all pictures for verification.{has\_reset=0} | | | | | |
| 25:20 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 19:16 | FB\_ENDIAN | | | rw | ro | | 0x0 | | | Framebuffer endianness. This is applied to only decoder.{has\_reset=0} | | | | | |
| 4:4 | SETUP\_DONE | | | rw | ro | | 0x0 | | | Setup Done  Please set this flag as 1 when setup for frame buffer is done{has\_reset=0} | | | | | |
| 3:3 | FB\_GROUP\_INDICATOR | | | rw | ro | | 0x0 | | | shall be 1{has\_reset=0} | | | | | |
| 2:0 | SET\_FB\_MODE | | | rw | ro | | 0x0 | | | \*0: Set FB\*  1: Update FB{has\_reset=0} | | | | | |

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| 1.1.1.93.0 | | | | | | | | CMD\_SET\_PARAM\_OPTION | | | | | reg32 | | 0x204 |
| offset | | 516 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| CMD\_SET\_PARAM\_OPTION{alt\_mode=CMD\_DEC\_PIC\_OPTION\_signal=4;virtualpairUid=2022-09-0709:27:31T173acdd5-3dd6-4841-8584-d31cbbc63a2c;alternate\_reg=CMD\_DEC\_PIC\_OPTION} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:2 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 1:0 | SET\_PARAM\_OPTION | | | rw | ro | | 0x0 | | | ENC\_SET\_PARAM command option  \*0x0 : SET\_PARAM\*  0x1 : CHANGE\_PARAM{has\_reset=0} | | | | | |

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| 1.1.1.94.0 | | | | | | | | CMD\_BS\_RD\_PTR\_DEC\_PIC | | | | | reg32 | | 0x300 |
| offset | | 768 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| read pointer on Bitstream buffer{alt\_mode=CMD\_BS\_RD\_PTR\_signal=1;virtualpairUid=2022-09-0709:27:31T927ba960-7865-42b9-b066-08646b1e13ba;alternate\_reg=CMD\_BS\_RD\_PTR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | RD\_PTR | | | rw | ro | | 0x0 | | | Start address of bitstream buffer (in line buffer mode only){has\_reset=0} | | | | | |

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| 1.1.1.95.0 | | | | | | | | CMD\_BS\_START | | | | | reg32 | | 0x300 |
| offset | | 768 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Bitstream buffer start address{alt\_mode=CMD\_BS\_RD\_PTR\_signal=2;virtualpairUid=2022-09-0709:27:31T927ba960-7865-42b9-b066-08646b1e13ba;alternate\_reg=CMD\_BS\_RD\_PTR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | BS\_START\_ADDR | | | rw | ro | | 0x0 | | | Start address of bitstream buffer (in line buffer mode only)  It should be aligned in bus width (128bit/16 byte), but we highly recommend to be aligned in 4KB{has\_reset=0} | | | | | |

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| 1.1.1.96.0 | | | | | | | | CMD\_CREATE\_INST\_ADDR\_WORK\_BUF | | | | | reg32 | | 0x300 |
| offset | | 768 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Work buffer base address{alt\_mode=CMD\_BS\_RD\_PTR\_signal=3;virtualpairUid=2022-09-0709:27:31T927ba960-7865-42b9-b066-08646b1e13ba;alternate\_reg=CMD\_BS\_RD\_PTR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | WORK\_BUF\_BASE | | | rw | ro | | 0x0 | | | Base address of work buffer for each instance  This address should be aligned in 4KB boundary.{has\_reset=0} | | | | | |

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| 1.1.1.97.0 | | | | | | | | CMD\_ENC\_SEQ\_SET\_PARAM\_ENABLE | | | | | reg32 | | 0x300 |
| offset | | 768 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Enabling flags for parameter changing{alt\_mode=CMD\_BS\_RD\_PTR\_signal=4;virtualpairUid=2022-09-0709:27:31T927ba960-7865-42b9-b066-08646b1e13ba;alternate\_reg=CMD\_BS\_RD\_PTR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:28 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 27:27 | ENABLE\_SET\_QUANT\_PARAM | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_QUANT\_PARAM\_0 and CMD\_ENC\_SEQ\_QUANT\_PARAM\_1.{has\_reset=0} | | | | | |
| 26:26 | ENABLE\_SET\_QROUND\_OFFSET | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_QROUND\_OFFSET.{has\_reset=0} | | | | | |
| 25:23 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 22:22 | ENABLE\_SET\_BG\_PARAM | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_BG\_PARAM.{has\_reset=0} | | | | | |
| 21:21 | RSVD2 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:20 | ENABLE\_SET\_VUI\_HRD\_PARAM | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_NON\_VCL\_PARAM and CMD\_ENC\_SEQ\_VUI\_RBSP\_ADDR, CMD\_ENC\_SEQ\_HRD\_RBSP\_ADDR.{has\_reset=0} | | | | | |
| 19:15 | RSVD3 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 14:14 | ENABLE\_SET\_RC\_VBV\_BUFFER\_SIZE | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_RC\_VBV\_BUFFER\_SIZE.{has\_reset=0} | | | | | |
| 13:13 | ENABLE\_SET\_RC\_MAX\_BITRATE | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_RC\_MAX\_BITRATE.{has\_reset=0} | | | | | |
| 12:12 | ENABLE\_SET\_MIN\_MAX\_QP | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_INTRA\_MIN\_MAX\_QP and CMD\_ENC\_SEQ\_INTER\_MIN\_MAX\_QP.{has\_reset=0} | | | | | |
| 11:11 | ENABLE\_SET\_RC\_PARAM | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_RC\_PARAM.{has\_reset=0} | | | | | |
| 10:10 | ENABLE\_SET\_RC\_TARGET\_RATE | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_RC\_TARGET\_RATE.{has\_reset=0} | | | | | |
| 9:7 | RSVD4 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 6:6 | ENABLE\_SET\_SLICE\_PARAM | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_SLICE.{has\_reset=0} | | | | | |
| 5:5 | RSVD5 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 4:4 | ENABLE\_SET\_TEMPORAL\_QP\_PARAM | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_TEMPORAL\_QP\_PARAM.  - CODECAPI\_AVEncVideoEncodeQp  - CODECAPI\_AVEncVideoEncodeFrameTypeQp{has\_reset=0} | | | | | |
| 3:3 | RSVD6 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 2:2 | ENABLE\_SET\_INTRA\_PARAM | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_INTRA\_PARAM/CMD\_ENC\_SEQ\_INTRA\_PARAM\_AVC.{has\_reset=0} | | | | | |
| 1:1 | ENABLE\_SET\_TEMPORAL\_COUNT\_PARAM | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_TEMPORAL\_COUNT\_PARAM.  - CODECAPI\_AVTemporalLayerCount{has\_reset=0} | | | | | |
| 0:0 | ENABLE\_SET\_PPS\_PARAM | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_PPS\_PARAM.{has\_reset=0} | | | | | |

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| 1.1.1.98.0 | | | | | | | | CMD\_SET\_FB\_COMMON\_PIC\_INFO | | | | | reg32 | | 0x300 |
| offset | | 768 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| DPB information{alt\_mode=CMD\_BS\_RD\_PTR\_signal=5;virtualpairUid=2022-09-0709:27:31T927ba960-7865-42b9-b066-08646b1e13ba;alternate\_reg=CMD\_BS\_RD\_PTR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:31 | PVRIC\_ENABLE | | | rw | ro | | 0x0 | | | This field enables VPU to generate PVRIC format of decoded frames.  0: BWB format  1: PVRIC format  [NOTE] This is valid only if PVRIC hardware is included in the product.{has\_reset=0} | | | | | |
| 30:30 | AFBC\_ENABLE | | | rw | ro | | 0x0 | | | This field enables VPU to generate AFBC(Arm Frame Buffer Compression) format of decoded frames.  0: BWB format  1: AFBC format  [NOTE] This is valid only if AFBC hardware is included in the product.{has\_reset=0} | | | | | |
| 29:29 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 28:28 | BWB\_ENABLE | | | rw | ro | | 0x0 | | | This field indicates whether target frame buffers are used for uncompressed linear frame.  0: Target frame buffers are compressed frames.  1: Target frame buffers are uncompressed linear frames.{has\_reset=0} | | | | | |
| 27:27 | CSC\_ENABLE | | | rw | ro | | 0x0 | | | This field indicates whether to enable CSC (color space conversion) or not.  0 : disable CSC. (output: YCbCr)  1 : enable CSC. (output: RGB)  This field is valid only if BWB\_ENABLE is 1.  [NOTE] This is valid only if CSC hardware is included in the product.{has\_reset=0} | | | | | |
| 26:26 | ONE\_PLANE\_OUTPUT\_ENABLE | | | rw | ro | | 0x0 | | | This field indicates enable 1 plane output  0 : disalbe 1-plane output  1 : enable 1-plane output  [NOTE] YUV444 support 1 plane output.  This field is valid only if BWB\_ENABLE is 1.{has\_reset=0} | | | | | |
| 25:24 | PIXEL\_FORMAT | | | rw | ro | | 0x0 | | | This filed indicates pixel format of the bitstream  0 : YUV420  1 : YUV422  2 : YUV444  This field is valid only if BWB\_ENABLE is 1.{has\_reset=0} | | | | | |
| 23:23 | PIXEL\_ORDER\_MODE | | | rw | ro | | 0x0 | | | Pixel ordering in a bus word  0: decreasing ordering - pixel position is decreasing as byte address in a bus is increaing.  1: incrsing ordering - pixel position is increasing as byte address in a bus is increaing.  [NOTE] Pixel position is always increasing as word address is increasing.  This field is valid only if BWB\_ENABLE is 1.{has\_reset=0} | | | | | |
| 22:20 | PIXEL\_OUTPUT\_MODE | | | rw | ro | | 0x0 | | | [22]  0 : MSB justified pixel  1 : LSB justified pixel  [21:20]  0 : BWB output mode 0 (10bit/pixel -> 8bit/pixel)  1 : BWB output mode 1 (16bit/pixel)  2 : BWB output mode 2 (32bit/pixel)  PIXEL\_OUTPUT\_MODE cannot be 2 if Chroma Output Format (COMMON\_PIC\_INFO[18:16]) is set as packed mode (4~7)  Valid only if BWB\_ENABLE is 1.{has\_reset=0} | | | | | |
| 19:19 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 18:16 | CHROMA\_OUTPUT\_FORMAT | | | rw | ro | | 0x0 | | | BWB Chroma format  0 : Planar mode - YV12 when YCbCr420, YV16 when YCbCr422  1 : Semi-planar mode, Cb/Cr interleaved - NV12 when YCbCr420, NV16 when YCbCr422  3 : Semi-planar mode, Cb/Cr interleaved - NV21 when YCbCr420, NV61 when YCbCr422  Valid only if BWB\_ENABLE is 1.{has\_reset=0} | | | | | |
| 15:0 | FB\_STRIDE | | | rw | ro | | 0x0 | | | Stride for the storing alignment{has\_reset=0} | | | | | |

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| 1.1.1.99.0 | | | | | | | | RET\_DEC\_ADDR\_USERDATA\_BASE | | | | | reg32 | | 0x300 |
| offset | | 768 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| User Data Buffer Base Address{alt\_mode=CMD\_BS\_RD\_PTR\_signal=6;virtualpairUid=2022-09-0709:27:31T927ba960-7865-42b9-b066-08646b1e13ba;alternate\_reg=CMD\_BS\_RD\_PTR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | USER\_DATA\_BUF\_BASE | | | rw | ro | | 0x0 | | | \* support standard : H265/H264  Base address of user data buffer  User data buffer holds SEI, SPS, and VUI information. This address should be aligned in 4K boundary.  VPU reports user data of the decoded frame if user data exists in the decoded frame and the relevant user data report option is enabled. User data buffering/reordering is required to sync user data with display frame.{has\_reset=0} | | | | | |

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| 1.1.1.100.0 | | | | | | | | RET\_ENC\_RD\_PTR | | | | | reg32 | | 0x300 |
| offset | | 768 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| bitstream buffer read pointer{alt\_mode=CMD\_BS\_RD\_PTR\_signal=7;virtualpairUid=2022-09-0709:27:31T927ba960-7865-42b9-b066-08646b1e13ba;alternate\_reg=CMD\_BS\_RD\_PTR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | RD\_PTR | | | rw | ro | | 0x0 | | | The start address of CPB where bitstream reads{has\_reset=0} | | | | | |

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| 1.1.1.101.0 | | | | | | | | RET\_ENC\_RD\_PTR\_QUERY\_ENC\_FW\_STATUS | | | | | reg32 | | 0x300 |
| offset | | 768 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| bitstream buffer read pointer{alt\_mode=CMD\_BS\_RD\_PTR\_signal=8;virtualpairUid=2022-09-0709:27:31T927ba960-7865-42b9-b066-08646b1e13ba;alternate\_reg=CMD\_BS\_RD\_PTR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | RD\_PTR | | | rw | ro | | 0x0 | | | The start address of CPB where bitstream reads{has\_reset=0} | | | | | |

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| 1.1.1.103.0 | | | | | | | | RET\_QUERY\_ENC\_BS\_RD\_PTR | | | | | reg32 | | 0x300 |
| offset | | 768 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| {alt\_mode=CMD\_BS\_RD\_PTR\_signal=9;virtualpairUid=2022-09-0709:27:31T927ba960-7865-42b9-b066-08646b1e13ba;alternate\_reg=CMD\_BS\_RD\_PTR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | QUERY\_ENC\_BS\_RD\_PTR | | | ro | ro | | 0x0 | | | The start position of bistream buffer for the currnetly encoded picture.{has\_reset=0} | | | | | |

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| 1.1.1.104.0 | | | | | | | | CMD\_BS\_WR\_PTR | | | | | reg32 | | 0x304 |
| offset | | 772 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Bitstream buffer write pointer{alt\_mode=CMD\_BS\_SIZE\_signal=1;virtualpairUid=2022-09-0709:27:31T93109875-62e0-4860-bc83-f143828565a6;alternate\_reg=CMD\_BS\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | WR\_PTR | | | rw | ro | | 0x0 | | | End address of bitstream for handling current command  Host can update this register anytime. If a bitstream\_empty interrupt is asserted, host processor should do either feed more bitstream and update WR\_PTR or set EXPLICIT\_END to complete decoding anyhow.{has\_reset=0} | | | | | |

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| 1.1.1.105.0 | | | | | | | | CMD\_BS\_WR\_PTR\_DEC\_PIC | | | | | reg32 | | 0x304 |
| offset | | 772 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| write pointer on Bitstream buffer{alt\_mode=CMD\_BS\_SIZE\_signal=2;virtualpairUid=2022-09-0709:27:31T93109875-62e0-4860-bc83-f143828565a6;alternate\_reg=CMD\_BS\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | WR\_PTR | | | rw | ro | | 0x0 | | | WR\_PTR{has\_reset=0} | | | | | |

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| 1.1.1.106.0 | | | | | | | | CMD\_CREATE\_INST\_WORK\_BUF\_SIZE | | | | | reg32 | | 0x304 |
| offset | | 772 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Work buffer size{alt\_mode=CMD\_BS\_SIZE\_signal=3;virtualpairUid=2022-09-0709:27:31T93109875-62e0-4860-bc83-f143828565a6;alternate\_reg=CMD\_BS\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | WORK\_BUF\_SIZE | | | rw | ro | | 0x0 | | | Size of work buffer (4KB boundary)  The size of work buffer should be larger than required minimum work buffer size. This address should be aligned in 4KB boundary.{has\_reset=0} | | | | | |

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| 1.1.1.107.0 | | | | | | | | CMD\_ENC\_SEQ\_SRC\_SIZE | | | | | reg32 | | 0x304 |
| offset | | 772 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| A size of source picture (MANDATORY){alt\_mode=CMD\_BS\_SIZE\_signal=4;virtualpairUid=2022-09-0709:27:31T93109875-62e0-4860-bc83-f143828565a6;alternate\_reg=CMD\_BS\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | SRC\_HEIGHT | | | rw | ro | | 0x0 | | | A height of source picture in pixel (128 ~ 8192){has\_reset=0} | | | | | |
| 15:0 | SRC\_WIDTH | | | rw | ro | | 0x0 | | | A width of source picture in pixel (256 ~ 8192){has\_reset=0} | | | | | |

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| 1.1.1.108.0 | | | | | | | | CMD\_SET\_FB\_PIC\_SIZE | | | | | reg32 | | 0x304 |
| offset | | 772 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Decoded picture size{alt\_mode=CMD\_BS\_SIZE\_signal=5;virtualpairUid=2022-09-0709:27:31T93109875-62e0-4860-bc83-f143828565a6;alternate\_reg=CMD\_BS\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | PIC\_WIDTH | | | rw | ro | | 0x0 | | | Picture width of DPB  When SCL\_EN is 1 and BWB\_ENABLE is 1, following restrictions are applied  - output image width (support down scaler only 1- 1/8)  - size range :32 ~ 8192  - size must be 4 align{has\_reset=0} | | | | | |
| 15:0 | PIC\_HEIGHT | | | rw | ro | | 0x0 | | | Picture height of DPB  When SCL\_EN is 1 and BWB\_ENABLE is 1, following restrictions are applied  - output image height (support down scaler only 1- 1/8)  - size range :32 ~ 8192  - size must be 4 align{has\_reset=0} | | | | | |

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| 1.1.1.109.0 | | | | | | | | RET\_DEC\_USERDATA\_SIZE | | | | | reg32 | | 0x304 |
| offset | | 772 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| User Data Buffer Size{alt\_mode=CMD\_BS\_SIZE\_signal=6;virtualpairUid=2022-09-0709:27:31T93109875-62e0-4860-bc83-f143828565a6;alternate\_reg=CMD\_BS\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | USER\_DATA\_BUF\_SIZE | | | rw | ro | | 0x0 | | | \* support standard : H265/H264  Size of user data buffer{has\_reset=0} | | | | | |

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| 1.1.1.110.0 | | | | | | | | RET\_ENC\_WR\_PTR | | | | | reg32 | | 0x304 |
| offset | | 772 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| bitstream buffer write pointer{alt\_mode=CMD\_BS\_SIZE\_signal=7;virtualpairUid=2022-09-0709:27:31T93109875-62e0-4860-bc83-f143828565a6;alternate\_reg=CMD\_BS\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | WR\_PTR | | | rw | ro | | 0x0 | | | The end address of CPB where bitstream writes{has\_reset=0} | | | | | |

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| 1.1.1.111.0 | | | | | | | | RET\_ENC\_WR\_PTR\_QUERY\_ENC\_FW\_STATUS | | | | | reg32 | | 0x304 |
| offset | | 772 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| bitstream buffer write pointer{alt\_mode=CMD\_BS\_SIZE\_signal=8;virtualpairUid=2022-09-0709:27:31T93109875-62e0-4860-bc83-f143828565a6;alternate\_reg=CMD\_BS\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | WR\_PTR | | | rw | ro | | 0x0 | | | The end address of CPB where bitstream writes{has\_reset=0} | | | | | |

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| 1.1.1.113.0 | | | | | | | | RET\_QUERY\_ENC\_BS\_WR\_PTR | | | | | reg32 | | 0x304 |
| offset | | 772 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| {alt\_mode=CMD\_BS\_SIZE\_signal=9;virtualpairUid=2022-09-0709:27:31T93109875-62e0-4860-bc83-f143828565a6;alternate\_reg=CMD\_BS\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | QUERY\_ENC\_BS\_WR\_PTR | | | ro | ro | | 0x0 | | | The end position of bistream buffer for the currnetly encoded picture{has\_reset=0} | | | | | |

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| 1.1.1.114.0 | | | | | | | | CMD\_BS\_OPTIONS | | | | | reg32 | | 0x308 |
| offset | | 776 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| Bitstream buffer option{alt\_mode=CMD\_BS\_OPTION\_signal=1;virtualpairUid=2022-09-0709:27:31Tf65c537b-3e95-47ab-8050-d9673202e17e;alternate\_reg=CMD\_BS\_OPTION} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:4 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 3:2 | STREAM\_FORMAT | | | rw | ro | | 0x0 | | | Bitstream format (AV1)  0 : IVF  1 : OBU  2 : ANNEXB{has\_reset=0} | | | | | |
| 1:1 | STREAM\_END | | | rw | ro | | 0x0 | | | This field makes VPU assume Stream End when there is no stream to feed in the buffer.{has\_reset=0} | | | | | |
| 0:0 | EXPLICIT\_END | | | rw | ro | | 0x0 | | | Explicit End  When this field is set to 1, VPU assumes that bitstream buffer has at least one single frame and follows the tasks below.  # VPU decodes until the end of bitstream buffer (WR\_PTR) even if the last 3 bytes are all 0.  # VPU returns success if it has decoded a frame successfully.  If bitstream is insufficient to complete decoding a frame, VPU performs what it is supposed to do with the specified task in BS\_SHORTAGE\_OPTION of BS\_PARAM.  If this flag is 0,  # VPU decodes to the almost end of bitstream buffer (WR\_PTR), but not to some bytes (less than 3). It intentionally does not consume some a few bytes, because VPU is not sure if the last bytes are the start code of next NAL or they might not fill the offset in the CABAC.  # VPU returns success if it has decoded a frame successfully.  If bitstream is insufficient to complete decoding a frame, VPU stops decoding and waits for more bitstream to be filled. Then host processor can do either feed bitstream more or set EXPLICIT\_END to complete decoding anyhow.  BITSTREAM\_EMPTY interrupt is asserted when EXPLITCT\_END = 0 or  when bitstream buffer is near empty (not real empty) for seamless decoding.  CAUTION: Host processor can set this register any time, but cannot clear during command processing.{has\_reset=0} | | | | | |

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| 1.1.1.115.0 | | | | | | | | CMD\_BS\_OPTIONS\_ENC\_PIC | | | | | reg32 | | 0x308 |
| offset | | 776 | external | | |  | | | size | | 32 |  | |  | |
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| Bitstream buffer option{alt\_mode=CMD\_BS\_OPTION\_signal=2;virtualpairUid=2022-09-0709:27:31Tf65c537b-3e95-47ab-8050-d9673202e17e;alternate\_reg=CMD\_BS\_OPTION} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 5:4 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 3:0 | BS\_ENDIAN | | | rw | ro | | 0x0 | | | Endianness of bitstream buffer{has\_reset=0} | | | | | |

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| 1.1.1.116.0 | | | | | | | | CMD\_ENC\_SEQ\_CUSTOM\_MAP\_ENDIAN | | | | | reg32 | | 0x308 |
| offset | | 776 | external | | |  | | | size | | 32 |  | |  | |
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| Custom map endian (MANDATORY){alt\_mode=CMD\_BS\_OPTION\_signal=3;virtualpairUid=2022-09-0709:27:31Tf65c537b-3e95-47ab-8050-d9673202e17e;alternate\_reg=CMD\_BS\_OPTION} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CUSTOM\_MAP\_ENDIAN | | | rw | ro | | 0x0 | | | Endianness{has\_reset=0} | | | | | |

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| 1.1.1.117.0 | | | | | | | | CMD\_SET\_FB\_NUM\_FB | | | | | reg32 | | 0x308 |
| offset | | 776 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| The number of start/end frame buffer to set (max. 8 frame buffers can be set for one SET\_FB command{alt\_mode=CMD\_BS\_OPTION\_signal=4;virtualpairUid=2022-09-0709:27:31Tf65c537b-3e95-47ab-8050-d9673202e17e;alternate\_reg=CMD\_BS\_OPTION} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:29 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 28:24 | BWB\_FB\_START\_IDX | | | rw | ro | | 0x0 | | | The start frame buffer index to set{has\_reset=0} | | | | | |
| 20:16 | BWB\_FB\_END\_IDX | | | rw | ro | | 0x0 | | | The end frame buffer index to set{has\_reset=0} | | | | | |
| 15:10 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 9:5 | COL\_FB\_START\_IDX | | | rw | ro | | 0x0 | | | The start frame buffer index to set for Codec dedicated information buffer{has\_reset=0} | | | | | |
| 4:0 | COL\_FB\_END\_IDX | | | rw | ro | | 0x0 | | | The end frame buffer index to set for Codec dedicated information buffer{has\_reset=0} | | | | | |

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| 1.1.1.119.0 | | | | | | | | RET\_ENC\_NUM\_REQUIRED\_FB | | | | | reg32 | | 0x308 |
| offset | | 776 | external | | |  | | | size | | 32 |  | |  | |
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| Minimum number of reference frame buffer required for encoding{alt\_mode=CMD\_BS\_OPTION\_signal=5;virtualpairUid=2022-09-0709:27:31Tf65c537b-3e95-47ab-8050-d9673202e17e;alternate\_reg=CMD\_BS\_OPTION} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | RET\_MIN\_FB\_BUF\_NUM | | | rw | ro | | 0x0 | | | The minimum number of reference frame buffer for encoding (1 ~ 16){has\_reset=0} | | | | | |

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| 1.1.1.120.0 | | | | | | | | CMD\_SET\_FB\_FBC\_STRIDE | | | | | reg32 | | 0x30C |
| offset | | 780 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Frame buffer setting for compressed frame{alt\_mode=CMD\_ENC\_SEQ\_PARAM\_signal=1;virtualpairUid=2022-09-0709:27:31Ta8acfb72-9691-4023-9e43-d4626272c979;alternate\_reg=CMD\_ENC\_SEQ\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | FBC\_LUMA\_STRIDE | | | rw | ro | | 0x0 | | | A stride of FBC for luma component{has\_reset=0} | | | | | |
| 15:0 | FBC\_CHROMA\_STRIDE | | | rw | ro | | 0x0 | | | A stride of FBC for chroma component{has\_reset=0} | | | | | |

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| 1.1.1.121.0 | | | | | | | | CMD\_USE\_SEC\_AXI | | | | | reg32 | | 0x30C |
| offset | | 780 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Secondary AXI usage option{alt\_mode=CMD\_ENC\_SEQ\_PARAM\_signal=2;virtualpairUid=2022-09-0709:27:31Ta8acfb72-9691-4023-9e43-d4626272c979;alternate\_reg=CMD\_ENC\_SEQ\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 1:1 | SEC\_AXI\_LF\_ROW | | | rw | ro | | 0x0 | | | Use 2nd AXI temp buffer for Read channel of RDO row buffer.{has\_reset=0} | | | | | |
| 0:0 | SEC\_AXI\_RDO\_ENABLE | | | rw | ro | | 0x0 | | | Use 2nd AXI temp buffer for Read channel of LF row buffer.{has\_reset=0} | | | | | |

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| 1.1.1.122.0 | | | | | | | | CMD\_USE\_SEC\_AXI\_ENC\_PIC | | | | | reg32 | | 0x30C |
| offset | | 780 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Secondary AXI usage option{alt\_mode=CMD\_ENC\_SEQ\_PARAM\_signal=3;virtualpairUid=2022-09-0709:27:31Ta8acfb72-9691-4023-9e43-d4626272c979;alternate\_reg=CMD\_ENC\_SEQ\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 1:1 | SEC\_AXI\_RDO\_ENABLE | | | rw | ro | | 0x0 | | | Use 2nd AXI temp buffer for Read channel of RDO row buffer.{has\_reset=0} | | | | | |
| 0:0 | SEC\_AXI\_LF\_ROW | | | rw | ro | | 0x0 | | | Use 2nd AXI temp buffer for Read channel of LF row buffer.{has\_reset=0} | | | | | |

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| 1.1.1.123.0 | | | | | | | | RET\_DEC\_BS\_RD\_PTR | | | | | reg32 | | 0x30C |
| offset | | 780 | external | | |  | | | size | | 32 |  | |  | |
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| Bitstream buffer read pointer{alt\_mode=CMD\_ENC\_SEQ\_PARAM\_signal=4;virtualpairUid=2022-09-0709:27:31Ta8acfb72-9691-4023-9e43-d4626272c979;alternate\_reg=CMD\_ENC\_SEQ\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | BS\_RD\_PTR | | | rw | ro | | 0x0 | | | VPU read address in the CPB. Host can feed bitstream data up to this address.{has\_reset=0} | | | | | |

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| 1.1.1.125.0 | | | | | | | | RET\_MIN\_SRC\_BUF\_NUM | | | | | reg32 | | 0x30C |
| offset | | 780 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Minimum number of source frame buffer required for encoding{alt\_mode=CMD\_ENC\_SEQ\_PARAM\_signal=5;virtualpairUid=2022-09-0709:27:31Ta8acfb72-9691-4023-9e43-d4626272c979;alternate\_reg=CMD\_ENC\_SEQ\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | RET\_MIN\_SRC\_BUF\_NUM | | | rw | ro | | 0x0 | | | The minimum number of source frame buffer for encoding (1 ~ 16){has\_reset=0} | | | | | |

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| 1.1.1.126.0 | | | | | | | | CMD\_ENC\_REPORT\_PARAM | | | | | reg32 | | 0x310 |
| offset | | 784 | external | | |  | | | size | | 32 |  | |  | |
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| Report parameters{alt\_mode=CMD\_CREATE\_INST\_BS\_PARAM\_signal=1;virtualpairUid=2022-09-0709:27:32Te06ff2d0-7434-4684-be12-3c276b70f371;alternate\_reg=CMD\_CREATE\_INST\_BS\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:2 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 1:1 | ENABLE\_HISTO\_EN | | | rw | ro | | 0x0 | | | It eanbles to report MV histogram count.{has\_reset=0} | | | | | |
| 0:0 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |

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| 1.1.1.127.0 | | | | | | | | CMD\_ENC\_SEQ\_PPS\_PARAM | | | | | reg32 | | 0x310 |
| offset | | 784 | external | | |  | | | size | | 32 |  | |  | |
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| Encoder picture parameters (MANDATORY){alt\_mode=CMD\_CREATE\_INST\_BS\_PARAM\_signal=2;virtualpairUid=2022-09-0709:27:32Te06ff2d0-7434-4684-be12-3c276b70f371;alternate\_reg=CMD\_CREATE\_INST\_BS\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:31 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 30:30 | USE\_ENTROPY\_CODING\_MODE | | | rw | ro | | 0x0 | | | It enables CABAC. (AVC only)  0 : CAVLC is used for entropy coding  1 : CABAC is used for entropy coding{has\_reset=0} | | | | | |
| 29:29 | USE\_TRANSFORM\_8x8 | | | rw | ro | | 0x0 | | | It enables transform 8x8.{has\_reset=0} | | | | | |
| 28:24 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved  It should be 0.{has\_reset=0} | | | | | |
| 23:19 | CR\_QP\_OFFSET | | | rw | ro | | 0x0 | | | HEVC/AVC: QP offset for Cr color component{has\_reset=0} | | | | | |
| 18:14 | CB\_QP\_OFFSET | | | rw | ro | | 0x0 | | | HEVC/AVC: QP offset for Cb color component{has\_reset=0} | | | | | |
| 13:10 | TC\_OFFSET\_DIV2 | | | rw | ro | | 0x0 | | | HEVC/AVC: TcOffsetDiv2 for deblocking filter{has\_reset=0} | | | | | |
| 9:6 | BETA\_OFFSET\_DIV2 | | | rw | ro | | 0x0 | | | HEVC/AVC: BetaOffsetDiv2 for deblocking filter  AV1: LF sharpness{has\_reset=0} | | | | | |
| 5:5 | DISABLE\_DBK | | | rw | ro | | 0x0 | | | It disables the in-loop deblocking filter.{has\_reset=0} | | | | | |
| 4:3 | RSVD2 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 2:2 | USE\_LF\_CROSS\_SLICE\_BOUNDARY | | | rw | ro | | 0x0 | | | It enables the use of in-loop filtering across slice boundaries. (HEVC/AVC){has\_reset=0} | | | | | |
| 1:1 | CONSTRAINED\_INTRA\_PRED | | | rw | ro | | 0x0 | | | It enables constrained intra prediction. (HEVC/AVC){has\_reset=0} | | | | | |
| 0:0 | RSVD3 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |

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| 1.1.1.128.0 | | | | | | | | CMD\_SEQ\_CHANGE\_ENABLE\_FLAG | | | | | reg32 | | 0x310 |
| offset | | 784 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Sequence change enable flag  If any bit flag of SEQ\_CHANGE\_ENABLE\_FLAG is 1 and the syntax value corresponding the bit flag is changed with a newly activated SPS, VPU regards it as sequence change.  VPU reports sequence change to RET\_QUERY\_DEC\_NOTIFICATION register. Then VPU bumps out all of the pictures that remain in DPB and clears the reference flag. However, there is an exception. If RET\_QUERY\_DEC\_NOTIFICATION[17] is 1, VPU only reports the DPB index to be replaced wihtin the same sequence.{alt\_mode=CMD\_CREATE\_INST\_BS\_PARAM\_signal=3;virtualpairUid=2022-09-0709:27:32Te06ff2d0-7434-4684-be12-3c276b70f371;alternate\_reg=CMD\_CREATE\_INST\_BS\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:20 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 19:19 | DEC\_TEMP\_ID\_MODE | | | rw | ro | | 0x0 | | | A DPB count change enable flag{has\_reset=0} | | | | | |
| 18:18 | SEQ\_CHANGE\_ENABLE\_FLAG\_BITDEPTH | | | rw | ro | | 0x0 | | | A bit-depth change enable flag{has\_reset=0} | | | | | |
| 17:17 | SEQ\_CHANGE\_ENABLE\_FLAG\_INTER\_RES\_CHANGE | | | rw | ro | | 0x0 | | | An inter resolution change enable flag for VP9/AV1{has\_reset=0} | | | | | |
| 16:16 | SEQ\_CHANGE\_ENABLE\_FLAG\_SIZE | | | rw | ro | | 0x0 | | | A picture size change enable flag{has\_reset=0} | | | | | |
| 15:15 | SEQ\_CHANGE\_ENABLE\_FLAG\_CHROMA\_FORMAT | | | rw | ro | | 0x0 | | | A chroma format change enable flag{has\_reset=0} | | | | | |
| 14:6 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 5:5 | SEQ\_CHANGE\_ENABLE\_FLAG\_PROFILE | | | rw | ro | | 0x0 | | | A profile change enable flag{has\_reset=0} | | | | | |
| 4:0 | RSVD2 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |

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| 1.1.1.129.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_LUMA\_BASE0 | | | | | reg32 | | 0x310 |
| offset | | 784 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Luma base of index 0{alt\_mode=CMD\_CREATE\_INST\_BS\_PARAM\_signal=4;virtualpairUid=2022-09-0709:27:32Te06ff2d0-7434-4684-be12-3c276b70f371;alternate\_reg=CMD\_CREATE\_INST\_BS\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | LUMA\_BASE0 | | | rw | ro | | 0x0 | | | Luma base address of DPB index 0  Compressed Luma base address of DPB index 0{has\_reset=0} | | | | | |

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| 1.1.1.130.0 | | | | | | | | RET\_DEC\_SEQ\_PARAM | | | | | reg32 | | 0x310 |
| offset | | 784 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Bitstream sequence parameter information{alt\_mode=CMD\_CREATE\_INST\_BS\_PARAM\_signal=5;virtualpairUid=2022-09-0709:27:32Te06ff2d0-7434-4684-be12-3c276b70f371;alternate\_reg=CMD\_CREATE\_INST\_BS\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:30 | PROFILE\_SPACE | | | rw | ro | | 0x0 | | | H.265 : the value of general\_profile\_space of active SPS. See H.265 annex A for detail information.  AVS2 : the value of sample\_precision 8{has\_reset=0} | | | | | |
| 29:29 | PROFILE\_TIER\_FLAG | | | rw | ro | | 0x0 | | | H.265 : the value of general\_tire\_flag of active SPS{has\_reset=0} | | | | | |
| 28:24 | PROFILE\_IDC | | | rw | ro | | 0x0 | | | H.265/H.264 : the value of general\_profile\_idc of active SPS  VP9 : the value of a profile of VP9  AVS2: the value of profile\_id of active SPS  AV1 : the value of profile\_ of sequence header{has\_reset=0} | | | | | |
| 23:21 | SPS\_MAX\_SUB\_LAYER | | | rw | ro | | 0x0 | | | H.265/H.264 : the value of maximum number of temporal sub-layers, sps\_max\_sub\_layer\_minus1+1, of active SPS  AVS2 : the value of maximum number of temporal sub-layers if temporal\_id\_enable is 1. Then it returns 7. Otherwise, it is 0.{has\_reset=0} | | | | | |
| 20:20 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 19:12 | PROFILE\_COMPATIBILITY\_FLAG | | | rw | ro | | 0x0 | | | H.265 : the value of first 8 bits out of general\_profile\_compatiblity\_flag[32] of active SPS. PROFILE\_COMPATIBILITY\_FLAG[i] is equal to general\_profile\_compatiblity\_flag[i] with i = 0 to 7.{has\_reset=0} | | | | | |
| 11:11 | PROGRESS\_SOURCE\_FLAG | | | rw | ro | | 0x0 | | | H.265 : the value of general\_progressive\_source\_flag of active SPS  AVS2 : the value of progressive\_sequence of active SPS{has\_reset=0} | | | | | |
| 10:10 | INTERLACE\_SOURCE\_FLAG | | | rw | ro | | 0x0 | | | H.265 : the value of general\_interlaced\_source\_flag of active SPS  AVS2 : the value of field\_coded\_sequence of active SPS{has\_reset=0} | | | | | |
| 9:9 | NON\_PACKED\_CONSTRAINT\_FLAG | | | rw | ro | | 0x0 | | | H.256 : the value of general\_non\_packed\_constraint\_flag of active SPS{has\_reset=0} | | | | | |
| 8:8 | FRAME\_ONLY\_CONSTRAINT\_FLAG | | | rw | ro | | 0x0 | | | H.265 : the value of general\_frame\_only\_constraint\_flag of active SPS  AVS2 : the value of progressive\_sequence of active SPS{has\_reset=0} | | | | | |
| 7:0 | LEVEL\_IDC | | | rw | ro | | 0x0 | | | H.265/H.264 : the value of general\_level\_idc of active SPS  AVS2 : the value of level\_id of active SPS  AV1 : the value of level\_id of sequence header{has\_reset=0} | | | | | |

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| 1.1.1.132.0 | | | | | | | | RET\_ENC\_PIC\_TYPE | | | | | reg32 | | 0x310 |
| offset | | 784 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Encoded picture type{alt\_mode=CMD\_CREATE\_INST\_BS\_PARAM\_signal=6;virtualpairUid=2022-09-0709:27:32Te06ff2d0-7434-4684-be12-3c276b70f371;alternate\_reg=CMD\_CREATE\_INST\_BS\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 15:0 | PIC\_TYPE | | | rw | ro | | 0x0 | | | The encoded picture type  0 : I slice  1 : P slice  2 : B slice{has\_reset=0} | | | | | |

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| 1.1.1.133.0 | | | | | | | | CMD\_ENC\_SEQ\_GOP\_PARAM | | | | | reg32 | | 0x314 |
| offset | | 788 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| GOP structure designation (MANDATORY){alt\_mode=CMD\_DEC\_SEI\_MASK\_signal=1;virtualpairUid=2022-09-0709:27:32Tcbc23275-2bfa-4d9e-b933-c6d6fb79bb1e;alternate\_reg=CMD\_DEC\_SEI\_MASK} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:20 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 19:16 | TEMPORAL\_LAYER\_COUNT | | | rw | ro | | 0x0 | | | Temporal layer count ??number of temporal layer{has\_reset=0} | | | | | |
| 15:12 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 11:11 | EN\_TEMPORAL\_LAYER\_3\_QP | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_3\_QP.{has\_reset=0} | | | | | |
| 10:10 | EN\_TEMPORAL\_LAYER\_2\_QP | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_2\_QP.{has\_reset=0} | | | | | |
| 9:9 | EN\_TEMPORAL\_LAYER\_1\_QP | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_1\_QP.{has\_reset=0} | | | | | |
| 8:8 | EN\_TEMPORAL\_LAYER\_0\_QP | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_0\_QP.{has\_reset=0} | | | | | |
| 7:0 | GOP\_PRESET\_IDX | | | rw | ro | | 0x0 | | | A GOP structure option  0: Custom GOP  1 : I-I-I-I,..I (all intra, gop\_size=1)  2 : I-P-P-P,... P (consecutive P, gop\_size=1)  3 : I-B-B-B,...B (consecutive B, gop\_size=1)  4 : I-B-P-B-P,... (gop\_size=2)  5 : I-B-B-B-P,... (gop\_size=4)  6 : I-P-P-P-P,... (consecutive P, gop\_size=4)  7 : I-B-B-B-B,... (consecutive B, gop\_size=4)  8 : I-B-B-B-B-B-B-B-B,... (random access, gop\_size=8){has\_reset=0} | | | | | |

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| 1.1.1.134.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CB\_BASE0 | | | | | reg32 | | 0x314 |
| offset | | 788 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Cb base of index 0{alt\_mode=CMD\_DEC\_SEI\_MASK\_signal=2;virtualpairUid=2022-09-0709:27:32Tcbc23275-2bfa-4d9e-b933-c6d6fb79bb1e;alternate\_reg=CMD\_DEC\_SEI\_MASK} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CB\_BASE0 | | | rw | ro | | 0x0 | | | Cb base address of DPB index 0  Compressed Cb and Cr base address of DPB index 0{has\_reset=0} | | | | | |

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| 1.1.1.135.0 | | | | | | | | RET\_DEC\_COLOR\_SAMPLE\_INFO | | | | | reg32 | | 0x314 |
| offset | | 788 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Color Sample Information{alt\_mode=CMD\_DEC\_SEI\_MASK\_signal=3;virtualpairUid=2022-09-0709:27:32Tcbc23275-2bfa-4d9e-b933-c6d6fb79bb1e;alternate\_reg=CMD\_DEC\_SEI\_MASK} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 23:16 | ASPECT\_RATIO\_IDC | | | rw | ro | | 0x0 | | | H.265 : The value of aspect\_ratio\_idc of H.265. See Table E-1 of Annex E.2 of VUI of H.265 specification. If not decoded in the bitstream, the value of ASPECT\_RATIO\_IDC is equal to 0.  AVS2 : The value of aspect\_ratio of AVS2. See Table-39 of AVS2 specification.{has\_reset=0} | | | | | |
| 12:12 | LF\_PIC\_DBK\_DISABLE | | | rw | ro | | 0x0 | | | H.265 : 1 when both sao and loop filter are off. 0 otherwise.  VP9 : 1 when loop filter is off. 0 otherwise.{has\_reset=0} | | | | | |
| 11:8 | COLOR\_FORMAT\_IDC | | | rw | ro | | 0x0 | | | H.265/H.264 : Chroma sampling, chroma\_format\_idc. See H.265 spec clause 6.2 for more information  AVS2 : The chroma sampling chroma\_format\_idc. See Table-36 of AVS2 specification.{has\_reset=0} | | | | | |
| 7:4 | BIT\_DEPTH\_CHROMA | | | rw | ro | | 0x0 | | | Bit depth of chroma sample{has\_reset=0} | | | | | |
| 3:0 | BIT\_DEPTH\_LUMA | | | rw | ro | | 0x0 | | | Bit depth of luma sample{has\_reset=0} | | | | | |

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| 1.1.1.137.0 | | | | | | | | RET\_ENC\_PIC\_POC | | | | | reg32 | | 0x314 |
| offset | | 788 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| A POC value of encoded picture{alt\_mode=CMD\_DEC\_SEI\_MASK\_signal=4;virtualpairUid=2022-09-0709:27:32Tcbc23275-2bfa-4d9e-b933-c6d6fb79bb1e;alternate\_reg=CMD\_DEC\_SEI\_MASK} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | PIC\_POC | | | rw | ro | | 0x0 | | | A POC value of the currently encoded picture{has\_reset=0} | | | | | |

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| 1.1.1.138.0 | | | | | | | | CMD\_DEC\_TEMPORAL\_ID\_PLUS1 | | | | | reg32 | | 0x318 |
| offset | | 792 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Max Decode Temporal ID{alt\_mode=CMD\_CREATE\_ADDR\_EXT\_signal=1;virtualpairUid=2022-09-0709:27:32T38f35ffa-5d2c-443b-a1a3-7b811f6c6cdc;alternate\_reg=CMD\_CREATE\_ADDR\_EXT} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 11:9 | TARGET\_DEC\_SPATIAL\_ID\_PLUS1 | | | rw | ro | | 0x0 | | | Set an absolute target spatial ID (TARGET\_DEC\_SPATIAL\_ID\_PLUS1). (for AV1){has\_reset=0} | | | | | |
| 8:8 | DEC\_TEMP\_ID\_MODE | | | rw | ro | | 0x0 | | | Set the mode of temporal ID selection.  0: use the target temporal\_id as absolute value.  @\* TARGET\_DEC\_TEMP\_ID = TARGET\_DEC\_TEMP\_ID\_PLUS1 -1  @\* When use of absolute value for temporal target, decoder can keep the decoding layer ID. If the SPS\_MAX\_SUB\_LAYER is changed in the bitstream, the temporal skip ratio can be changed.  1: use the target temporal \_id as relative value.  @\* TARGET\_DEC\_TEMP\_ID = SPS\_MAX\_SUB\_LAYER - REL\_TARGET\_TEMP\_ID  @\* SPS\_MAX\_SUB\_LAYER is signalled from bitstream.  @\* When use of relatvie value, decoder can keep the skip(discard) ratio regardless the change of SPS\_MAX\_SUB\_LAYER in the bitstream{has\_reset=0} | | | | | |
| 7:0 | TARGET\_DEC\_TEMP\_ID\_PLUS1 | | | rw | ro | | 0x0 | | | If DEC\_TEMP\_ID\_MODE is 0, this field is used as an absolute target temporal ID (TARGET\_DEC\_TEMP\_ID\_PLUS1).  @\* TARGET\_DEC\_TEMP\_ID = TARGET\_DEC\_TEMP\_ID\_PLUS1 -1.  @\* Based on TARGET\_DEC\_TEMP\_ID,  @\*\* 0x0 : it decodes a picture of all ranges of temporal ID, which means temporal ID decoding constraint off.  @\*\* 0x1 ~ 0x6 : it decodes a picture if the temporal ID is less than or equal to TARGET\_DEC\_TEMP\_ID. It discards a picture when its temporal ID is greater than TARGET\_DEC\_TEMP\_ID.  If DEC\_TEMP\_ID\_MODE is 1, this field is used as a relative target temporal ID (REL\_TARGET\_TEMP\_ID).  @\* TARGET\_DEC\_TEMP\_ID = SPS\_MAX\_SUB\_LAYER - REL\_TARGET\_TEMP\_ID  @\* It discards a picture when its temporal ID is greater than TARGET\_DEC\_TEMP\_ID.{has\_reset=0} | | | | | |

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| 1.1.1.139.0 | | | | | | | | CMD\_ENC\_MV\_HISTO\_CLASS0 | | | | | reg32 | | 0x318 |
| offset | | 792 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| CMD\_ENC\_MV\_HISTO\_CLASS0{alt\_mode=CMD\_CREATE\_ADDR\_EXT\_signal=2;virtualpairUid=2022-09-0709:27:32T38f35ffa-5d2c-443b-a1a3-7b811f6c6cdc;alternate\_reg=CMD\_CREATE\_ADDR\_EXT} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | MV\_CLASS\_THRESHOLD\_0 | | | rw | ro | | 0x0 | | | MV threshold value for MV histogram class 0 (MV precison = 1/4-pel){has\_reset=0} | | | | | |
| 15:0 | MV\_CLASS\_THRESHOLD\_1 | | | rw | ro | | 0x0 | | | MV threshold value for MV histogram class 1 (MV precison = 1/4-pel){has\_reset=0} | | | | | |

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| 1.1.1.140.0 | | | | | | | | CMD\_ENC\_SEQ\_INTRA\_PARAM | | | | | reg32 | | 0x318 |
| offset | | 792 | external | | |  | | | size | | 32 |  | |  | |
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| Intra picture coding parameters for HEVC, AV1 (MANDATORY) {alt\_mode=CMD\_CREATE\_ADDR\_EXT\_signal=3;virtualpairUid=2022-09-0709:27:32T38f35ffa-5d2c-443b-a1a3-7b811f6c6cdc;alternate\_reg=CMD\_CREATE\_ADDR\_EXT} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | INTRA\_PERIOD | | | rw | ro | | 0x0 | | | A period of intra picture (0 ~ 1024)  0 - implies an infinite period{has\_reset=0} | | | | | |
| 15:11 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 10:9 | EN\_FORCED\_IDR\_HEADER | | | rw | ro | | 0x0 | | | 0 : ForcedIDRHeader off  1 : Add Header at every IDR frame  2 : Add Header at every I frame{has\_reset=0} | | | | | |
| 8:3 | INTRA\_QP | | | rw | ro | | 0x0 | | | A quantization parameter of intra picture (0 ~ 51){has\_reset=0} | | | | | |
| 2:0 | DECODING\_REFRESH\_TYPE | | | rw | ro | | 0x0 | | | A decoding refresh type of intra picture  0 : Non-IRAP  1 : CRA  2 : IDR  [NOTE] This parameter cannot be changed within the same sequence.�{has\_reset=0} | | | | | |

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| 1.1.1.141.0 | | | | | | | | CMD\_ENC\_SEQ\_INTRA\_PARAM\_AVC | | | | | reg32 | | 0x318 |
| offset | | 792 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Intra picture coding parameters for AVC (MANDATORY){alt\_mode=CMD\_CREATE\_ADDR\_EXT\_signal=4;virtualpairUid=2022-09-0709:27:32T38f35ffa-5d2c-443b-a1a3-7b811f6c6cdc;alternate\_reg=CMD\_CREATE\_ADDR\_EXT} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:30 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 29:28 | EN\_FORCED\_IDR\_HEADER | | | rw | ro | | 0x0 | | | 0: No forced header(SPS/PPS)  1: Forced header before IDR frame  2: Forced header before key frame{has\_reset=0} | | | | | |
| 27:17 | IDR\_PERIOD | | | rw | ro | | 0x0 | | | A period of IDR picture (0 ~ 2047)  0 - implies an infinite period  [NOTE] This parameter cannot be changed within the same sequence.{has\_reset=0} | | | | | |
| 16:6 | INTRA\_PERIOD | | | rw | ro | | 0x0 | | | A period of intra picture (0 ~ 2047)  0 - implies an infinite period  [NOTE] This parameter cannot be changed within the same sequence.{has\_reset=0} | | | | | |
| 5:0 | INTRA\_QP | | | rw | ro | | 0x0 | | | A quantization parameter of intra picture (0 ~ 51)  {has\_reset=0} | | | | | |

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| 1.1.1.142.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CR\_BASE0 | | | | | reg32 | | 0x318 |
| offset | | 792 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Cr base of index 0{alt\_mode=CMD\_CREATE\_ADDR\_EXT\_signal=5;virtualpairUid=2022-09-0709:27:32T38f35ffa-5d2c-443b-a1a3-7b811f6c6cdc;alternate\_reg=CMD\_CREATE\_ADDR\_EXT} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CR\_BASE0 | | | rw | ro | | 0x0 | | | Cr base address of DPB index 0{has\_reset=0} | | | | | |

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| 1.1.1.143.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET0 | | | | | reg32 | | 0x318 |
| offset | | 792 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| FBC luma offset base of index 0{alt\_mode=CMD\_CREATE\_ADDR\_EXT\_signal=6;virtualpairUid=2022-09-0709:27:32T38f35ffa-5d2c-443b-a1a3-7b811f6c6cdc;alternate\_reg=CMD\_CREATE\_ADDR\_EXT} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_LUMA\_OFFSET\_BASE0 | | | rw | ro | | 0x0 | | | Compressed Luma offset table base address of DPB index 0 when FBC is used{has\_reset=0} | | | | | |

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| 1.1.1.144.0 | | | | | | | | RET\_DEC\_ASPECT\_RATIO | | | | | reg32 | | 0x318 |
| offset | | 792 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Sample Aspect Ratio{alt\_mode=CMD\_CREATE\_ADDR\_EXT\_signal=7;virtualpairUid=2022-09-0709:27:32T38f35ffa-5d2c-443b-a1a3-7b811f6c6cdc;alternate\_reg=CMD\_CREATE\_ADDR\_EXT} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | SAR\_WIDTH | | | rw | ro | | 0x0 | | | H.265 : the horizontal size of the sample aspect ratio. If it is not decoded in bitstream (VUI in case of H.265), the value of SarWidth is equal to 0.  VP9 : N/A{has\_reset=0} | | | | | |
| 15:0 | SAR\_HEIGHT | | | rw | ro | | 0x0 | | | H.265 : the vertical size of the sample aspect ratio. If it is not decoded in bitstream(VUI in case of H.265), the value of SarHeight is equal to 0.{has\_reset=0} | | | | | |

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| 1.1.1.146.0 | | | | | | | | RET\_ENC\_PIC\_IDX | | | | | reg32 | | 0x318 |
| offset | | 792 | external | | |  | | | size | | 32 |  | |  | |
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| A frame buffer index of the encoded picture {alt\_mode=CMD\_CREATE\_ADDR\_EXT\_signal=8;virtualpairUid=2022-09-0709:27:32T38f35ffa-5d2c-443b-a1a3-7b811f6c6cdc;alternate\_reg=CMD\_CREATE\_ADDR\_EXT} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | PIC\_IDX | | | rw | ro | | 0x0 | | | Greater than or equal to 0 : encoded picture buffer index  -1 : encoding end  -2 : encoding delay (default)  -3 : header encoded only (no VCL)  -4 : change of encoding parameter{has\_reset=0} | | | | | |

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| 1.1.1.147.0 | | | | | | | | CMD\_ENC\_MV\_HISTO\_CLASS1 | | | | | reg32 | | 0x31C |
| offset | | 796 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_MV\_HISTO\_CLASS1{alt\_mode=CMD\_DEC\_FORCE\_FB\_LATENCY\_PLUS1\_signal=1;virtualpairUid=2022-09-0709:27:32T1b95734c-2e2e-4e4b-8df1-d6dcd5e28ac5;alternate\_reg=CMD\_DEC\_FORCE\_FB\_LATENCY\_PLUS1} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | MV\_CLASS\_THRESHOLD\_2 | | | rw | ro | | 0x0 | | | MV threshold value for MV histogram class 2 (MV precison = 1/4-pel){has\_reset=0} | | | | | |
| 15:0 | MV\_CLASS\_THRESHOLD\_3 | | | rw | ro | | 0x0 | | | tile\_y\_meta\_stride{has\_reset=0} | | | | | |

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| 1.1.1.148.0 | | | | | | | | CMD\_ENC\_SEQ\_CONF\_WIN\_TOP\_BOT | | | | | reg32 | | 0x31C |
| offset | | 796 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Top and bottom size for conformance window {alt\_mode=CMD\_DEC\_FORCE\_FB\_LATENCY\_PLUS1\_signal=2;virtualpairUid=2022-09-0709:27:32T1b95734c-2e2e-4e4b-8df1-d6dcd5e28ac5;alternate\_reg=CMD\_DEC\_FORCE\_FB\_LATENCY\_PLUS1} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | CONFORMACE\_WINDOW\_SIZE\_BOTTOM | | | rw | ro | | 0x0 | | | A conformance bottom window size (0 ~ 8192){has\_reset=0} | | | | | |
| 15:0 | CONFORMACE\_WINDOW\_SIZE\_TOP | | | rw | ro | | 0x0 | | | A conformance top window size (0 ~ 8192){has\_reset=0} | | | | | |

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| 1.1.1.149.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET0 | | | | | reg32 | | 0x31C |
| offset | | 796 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC chroma offset base of index 0{alt\_mode=CMD\_DEC\_FORCE\_FB\_LATENCY\_PLUS1\_signal=3;virtualpairUid=2022-09-0709:27:32T1b95734c-2e2e-4e4b-8df1-d6dcd5e28ac5;alternate\_reg=CMD\_DEC\_FORCE\_FB\_LATENCY\_PLUS1} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE0 | | | rw | ro | | 0x0 | | | If FBC is used, this is chroma offset base address of DPB index 0. Otherwise, it is ignored.{has\_reset=0} | | | | | |

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| 1.1.1.150.0 | | | | | | | | RET\_DEC\_BIT\_RATE | | | | | reg32 | | 0x31C |
| offset | | 796 | external | | |  | | | size | | 32 |  | |  | |
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| Maximum Bit Rate{alt\_mode=CMD\_DEC\_FORCE\_FB\_LATENCY\_PLUS1\_signal=4;virtualpairUid=2022-09-0709:27:32T1b95734c-2e2e-4e4b-8df1-d6dcd5e28ac5;alternate\_reg=CMD\_DEC\_FORCE\_FB\_LATENCY\_PLUS1} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | MAX\_BIT\_RATE | | | rw | ro | | 0x0 | | | The maximum input bit rate for maxNumSubLayer, as specified in sub layer HRD parameter of H.265.  The maximum input bit rate specified in active SPS of AVS2{has\_reset=0} | | | | | |

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| 1.1.1.152.0 | | | | | | | | RET\_ENC\_PIC\_SLICE\_NUM | | | | | reg32 | | 0x31C |
| offset | | 796 | external | | |  | | | size | | 32 |  | |  | |
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| Number of slice segments{alt\_mode=CMD\_DEC\_FORCE\_FB\_LATENCY\_PLUS1\_signal=5;virtualpairUid=2022-09-0709:27:32T1b95734c-2e2e-4e4b-8df1-d6dcd5e28ac5;alternate\_reg=CMD\_DEC\_FORCE\_FB\_LATENCY\_PLUS1} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | reserved | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 15:0 | PIC\_SLICE\_NUM | | | rw | ro | | 0x0 | | | The number of slices in the encoded picture{has\_reset=0} | | | | | |

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| 1.1.1.153.0 | | | | | | | | CMD\_ENC\_SEQ\_CONF\_WIN\_LEFT\_RIGHT | | | | | reg32 | | 0x320 |
| offset | | 800 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Left and right size for conformance window{alt\_mode=CMD\_ENC\_CUSTOM\_MAP\_OPTION\_PARAM\_signal=1;virtualpairUid=2022-09-0709:27:32Tfda4929d-ec37-4c3a-a063-12c2a1966d63;alternate\_reg=CMD\_ENC\_CUSTOM\_MAP\_OPTION\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | CONFORMANCE\_WINDOW\_SIZE\_RIGHT | | | rw | ro | | 0x0 | | | A conformance right window size (0 ~ 8192){has\_reset=0} | | | | | |
| 15:0 | CONFORMANCE\_WINDOW\_SIZE\_LFET | | | rw | ro | | 0x0 | | | A conformance left window size (0 ~ 8192){has\_reset=0} | | | | | |

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| 1.1.1.154.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_COL0 | | | | | reg32 | | 0x320 |
| offset | | 800 | external | | |  | | | size | | 32 |  | |  | |
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| Info base of index 0{alt\_mode=CMD\_ENC\_CUSTOM\_MAP\_OPTION\_PARAM\_signal=2;virtualpairUid=2022-09-0709:27:32Tfda4929d-ec37-4c3a-a063-12c2a1966d63;alternate\_reg=CMD\_ENC\_CUSTOM\_MAP\_OPTION\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | COL\_BASE0 | | | rw | ro | | 0x0 | | | Codec dedicated information buffer for encoding/decoding  HEVC/AVC: MV COL  AV1 : CDF{has\_reset=0} | | | | | |

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| 1.1.1.155.0 | | | | | | | | RET\_DEC\_FRAME\_RATE\_NR | | | | | reg32 | | 0x320 |
| offset | | 800 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Frame Rate Numerator{alt\_mode=CMD\_ENC\_CUSTOM\_MAP\_OPTION\_PARAM\_signal=3;virtualpairUid=2022-09-0709:27:32Tfda4929d-ec37-4c3a-a063-12c2a1966d63;alternate\_reg=CMD\_ENC\_CUSTOM\_MAP\_OPTION\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FRAME\_RATE\_NR | | | rw | ro | | 0x0 | | | It returns a frame rate numerator. This field is valid for H.265 and AVS2.  If frame rate syntax is not decoded in bitstream, the value of FrameRateNr is equal to -1.  If FRAME\_RATE\_NR and FRAME\_RATE\_DR are not-zero values, FrameRate is derived as follows.  FrameRate =FRAME\_RATE\_NR/FRAME\_RATE\_DR.  Otherwise if FRAME\_RATE\_NR or FRAME\_RATE\_DR are zero values, the value of FrameRate is invalid.{has\_reset=0} | | | | | |

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| 1.1.1.157.0 | | | | | | | | RET\_ENC\_PIC\_SKIP | | | | | reg32 | | 0x320 |
| offset | | 800 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| A picture skip flag {alt\_mode=CMD\_ENC\_CUSTOM\_MAP\_OPTION\_PARAM\_signal=4;virtualpairUid=2022-09-0709:27:32Tfda4929d-ec37-4c3a-a063-12c2a1966d63;alternate\_reg=CMD\_ENC\_CUSTOM\_MAP\_OPTION\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 7:1 | PIC\_SKIP | | | rw | ro | | 0x0 | | | A picture skip flag{has\_reset=0} | | | | | |

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| 1.1.1.158.0 | | | | | | | | CMD\_ENC\_SEQ\_RDO\_PARAM | | | | | reg32 | | 0x324 |
| offset | | 804 | external | | |  | | | size | | 32 |  | |  | |
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| RDO coding options (MANDATORY){alt\_mode=CMD\_ENC\_CUSTOM\_MAP\_OPTION\_ADDR\_signal=1;virtualpairUid=2022-09-0709:27:32Tce3f12d5-fc35-45e7-8b86-f1d2d4a4b6b3;alternate\_reg=CMD\_ENC\_CUSTOM\_MAP\_OPTION\_ADDR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:23 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 22:22 | USE\_CUSTOM\_LAMBDA | | | rw | ro | | 0x0 | | | It enables to change CMD\_ENC\_CUSTOM\_LAMBDA\_ADDR.{has\_reset=0} | | | | | |
| 21:21 | ME\_SEARCH\_CENTER | | | rw | ro | | 0x0 | | | It specifies a search center mode for motion estimation.  0 : the ME search center is fixed as (0, 0).  1 : the ME search center is decided by MVP (motion vertor prediction).{has\_reset=0} | | | | | |
| 20:20 | USE\_CUSTOM\_QP\_MAP | | | rw | ro | | 0x0 | | | It enables custom QP map.{has\_reset=0} | | | | | |
| 19:19 | USE\_CUSTOM\_MODE\_MAP | | | rw | ro | | 0x0 | | | It enables custom mode map.{has\_reset=0} | | | | | |
| 18:18 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 17:17 | USE\_CUSTOM\_QROUND\_OFFSET | | | rw | ro | | 0x0 | | | It enables custom QRoundIntra and QRoundInter{has\_reset=0} | | | | | |
| 16:10 | RSVD2 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 9:8 | INTRA\_NXN | | | rw | ro | | 0x0 | | | It enables intra NxN Pu mode{has\_reset=0} | | | | | |
| 7:5 | RSVD3 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 4:4 | DISABLE\_COEF\_CLEAR | | | rw | ro | | 0x0 | | | Disables the transform coefficient clearing algorithm in P or B picture  0 : All-zero coefficient block is evaluated additionally in RDO  1 : All-zero coefficient block is not evaluated in RDO{has\_reset=0} | | | | | |
| 3:3 | USE\_ADAPTIVE\_ROUNDING | | | rw | ro | | 0x0 | | | It enables adaptive rounding and ignore QRoundIntra and QRoundInter{has\_reset=0} | | | | | |
| 2:2 | EN\_HVS\_QP | | | rw | ro | | 0x0 | | | It enables CU QP adjustment for subjective quality enhancement.{has\_reset=0} | | | | | |
| 1:0 | RSVD4 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |

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| 1.1.1.159.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE0 | | | | | reg32 | | 0x324 |
| offset | | 804 | external | | |  | | | size | | 32 |  | |  | |
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| Base address of sub-sampled frame buffer for index 0{alt\_mode=CMD\_ENC\_CUSTOM\_MAP\_OPTION\_ADDR\_signal=2;virtualpairUid=2022-09-0709:27:32Tce3f12d5-fc35-45e7-8b86-f1d2d4a4b6b3;alternate\_reg=CMD\_ENC\_CUSTOM\_MAP\_OPTION\_ADDR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SUB\_SAMPLED\_FB\_BASE0 | | | rw | ro | | 0x0 | | | A base address of frame buffer for sub sampled decoded frame 0{has\_reset=0} | | | | | |

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| 1.1.1.160.0 | | | | | | | | RET\_DEC\_FRAME\_RATE\_DR | | | | | reg32 | | 0x324 |
| offset | | 804 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Frame Rate Denominator{alt\_mode=CMD\_ENC\_CUSTOM\_MAP\_OPTION\_ADDR\_signal=3;virtualpairUid=2022-09-0709:27:32Tce3f12d5-fc35-45e7-8b86-f1d2d4a4b6b3;alternate\_reg=CMD\_ENC\_CUSTOM\_MAP\_OPTION\_ADDR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FRAME\_RATE\_DR | | | rw | ro | | 0x0 | | | It returns a frame rate denominator. This field is valid for H.265 and AVS2.  If frame rate syntax is not decoded in bitstream, the value of FrameRateDr is equal to -1.{has\_reset=0} | | | | | |

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| 1.1.1.162.0 | | | | | | | | RET\_ENC\_PIC\_NUM\_INTRA | | | | | reg32 | | 0x324 |
| offset | | 804 | external | | |  | | | size | | 32 |  | |  | |
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| Number of intra block{alt\_mode=CMD\_ENC\_CUSTOM\_MAP\_OPTION\_ADDR\_signal=4;virtualpairUid=2022-09-0709:27:32Tce3f12d5-fc35-45e7-8b86-f1d2d4a4b6b3;alternate\_reg=CMD\_ENC\_CUSTOM\_MAP\_OPTION\_ADDR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | PIC\_NUM\_INTRA | | | rw | ro | | 0x0 | | | The number of intra block in 8x8{has\_reset=0} | | | | | |

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| 1.1.1.163.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_LUMA\_BASE1 | | | | | reg32 | | 0x328 |
| offset | | 808 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Luma base of index 1{alt\_mode=CMD\_ENC\_SEQ\_SLICE\_PARAM\_signal=1;virtualpairUid=2022-09-0709:27:32T82a2a29b-f5f5-412f-9f20-e6fc01c64e82;alternate\_reg=CMD\_ENC\_SEQ\_SLICE\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | LUMA\_BASE1 | | | rw | ro | | 0x0 | | | Luma base address of DPB index 1  Compressed Luma base address of DPB index 1{has\_reset=0} | | | | | |

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| 1.1.1.164.0 | | | | | | | | RET\_DEC\_NUM\_REQURED\_FB | | | | | reg32 | | 0x328 |
| offset | | 808 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Required Number of Minimum DPB {alt\_mode=CMD\_ENC\_SEQ\_SLICE\_PARAM\_signal=2;virtualpairUid=2022-09-0709:27:32T82a2a29b-f5f5-412f-9f20-e6fc01c64e82;alternate\_reg=CMD\_ENC\_SEQ\_SLICE\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 4:0 | MIN\_DPB\_NUM | | | rw | ro | | 0x0 | | | Required number of frame buffers for decoding sequence  {has\_reset=0} | | | | | |

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| 1.1.1.166.0 | | | | | | | | RET\_ENC\_PIC\_NUM\_MERGE | | | | | reg32 | | 0x328 |
| offset | | 808 | external | | |  | | | size | | 32 |  | |  | |
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| Number of merge block{alt\_mode=CMD\_ENC\_SEQ\_SLICE\_PARAM\_signal=3;virtualpairUid=2022-09-0709:27:32T82a2a29b-f5f5-412f-9f20-e6fc01c64e82;alternate\_reg=CMD\_ENC\_SEQ\_SLICE\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | PIC\_NUM\_MERGE | | | rw | ro | | 0x0 | | | The number of merge block in 8x8{has\_reset=0} | | | | | |

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| 1.1.1.167.0 | | | | | | | | CMD\_ENC\_SRC\_PIC\_IDX | | | | | reg32 | | 0x32C |
| offset | | 812 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| GOP structure designation (MANDATORY){alt\_mode=CMD\_ENC\_SEQ\_INTRA\_REFRESH\_signal=1;virtualpairUid=2022-09-0709:27:32T2fdf6ba9-44df-4557-9994-3046c65d5372;alternate\_reg=CMD\_ENC\_SEQ\_INTRA\_REFRESH} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SRC\_IDX | | | rw | ro | | 0x0 | | | A buffer index of a source picture (-2 : no more source picture){has\_reset=0} | | | | | |

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| 1.1.1.168.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CB\_BASE1 | | | | | reg32 | | 0x32C |
| offset | | 812 | external | | |  | | | size | | 32 |  | |  | |
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| Cb base of index1{alt\_mode=CMD\_ENC\_SEQ\_INTRA\_REFRESH\_signal=2;virtualpairUid=2022-09-0709:27:32T2fdf6ba9-44df-4557-9994-3046c65d5372;alternate\_reg=CMD\_ENC\_SEQ\_INTRA\_REFRESH} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CB\_BASE1 | | | rw | ro | | 0x0 | | | Cb base address of DPB index 1  Compressed Cb and Cr base address of DPB index 1{has\_reset=0} | | | | | |

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| 1.1.1.169.0 | | | | | | | | RET\_DEC\_NUM\_REORDER\_DELAY | | | | | reg32 | | 0x32C |
| offset | | 812 | external | | |  | | | size | | 32 |  | |  | |
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| Reorder frame number{alt\_mode=CMD\_ENC\_SEQ\_INTRA\_REFRESH\_signal=3;virtualpairUid=2022-09-0709:27:32T2fdf6ba9-44df-4557-9994-3046c65d5372;alternate\_reg=CMD\_ENC\_SEQ\_INTRA\_REFRESH} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 4:0 | REORDER\_DELAY\_NUM | | | rw | ro | | 0x0 | | | The value of REORDER\_DELAY\_NUM is reorder picture number of H.265.  No picture reordering in VP9.  The value of output\_reorder\_delay of active SPS of AVS2.  {has\_reset=0} | | | | | |

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| 1.1.1.171.0 | | | | | | | | RET\_ENC\_PIC\_NON\_REF\_PIC\_FLAG | | | | | reg32 | | 0x32C |
| offset | | 812 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Non reference picture flag{alt\_mode=CMD\_ENC\_SEQ\_INTRA\_REFRESH\_signal=4;virtualpairUid=2022-09-0709:27:32T2fdf6ba9-44df-4557-9994-3046c65d5372;alternate\_reg=CMD\_ENC\_SEQ\_INTRA\_REFRESH} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | PIC\_NON\_REF\_PIC\_FLAG | | | rw | ro | | 0x0 | | | Non reference picture flag  0 : reference picture  1 : non reference picture{has\_reset=0} | | | | | |

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| 1.1.1.172.0 | | | | | | | | CMD\_ENC\_SEQ\_INTRA\_MIN\_MAX\_QP | | | | | reg32 | | 0x330 |
| offset | | 816 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_INTRA\_MIN\_MAX\_QP{alt\_mode=CMD\_CREATE\_INST\_CORE\_INFO\_signal=1;virtualpairUid=2022-09-0709:27:32Te6ec9a82-4986-41ae-95c6-164a717fa1d4;alternate\_reg=CMD\_CREATE\_INST\_CORE\_INFO} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:12 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 11:6 | I\_MAX\_QP | | | rw | ro | | 0x0 | | | A maximum QP of I pictures. (0 ~ 51){has\_reset=0} | | | | | |
| 5:0 | I\_MIN\_QP | | | rw | ro | | 0x0 | | | A minimum QP of I pictures. (0 ~ 51){has\_reset=0} | | | | | |

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| 1.1.1.173.0 | | | | | | | | CMD\_ENC\_SRC\_ADDR\_Y | | | | | reg32 | | 0x330 |
| offset | | 816 | external | | |  | | | size | | 32 |  | |  | |
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| Y component source address {alt\_mode=CMD\_CREATE\_INST\_CORE\_INFO\_signal=2;virtualpairUid=2022-09-0709:27:32Te6ec9a82-4986-41ae-95c6-164a717fa1d4;alternate\_reg=CMD\_CREATE\_INST\_CORE\_INFO} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SRC\_ADDR\_Y | | | rw | ro | | 0x0 | | | An address of luma component of a source picture buffer  An address of luma compressed source buffer when PVRIC\_EN is 1{has\_reset=0} | | | | | |

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| 1.1.1.174.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CR\_BASE1 | | | | | reg32 | | 0x330 |
| offset | | 816 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Cr base of index 1{alt\_mode=CMD\_CREATE\_INST\_CORE\_INFO\_signal=3;virtualpairUid=2022-09-0709:27:32Te6ec9a82-4986-41ae-95c6-164a717fa1d4;alternate\_reg=CMD\_CREATE\_INST\_CORE\_INFO} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CR\_BASE1 | | | rw | ro | | 0x0 | | | Cr base address of DPB index 1{has\_reset=0} | | | | | |

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| 1.1.1.175.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET1 | | | | | reg32 | | 0x330 |
| offset | | 816 | external | | |  | | | size | | 32 |  | |  | |
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| FBC luma offset base of index 1{alt\_mode=CMD\_CREATE\_INST\_CORE\_INFO\_signal=4;virtualpairUid=2022-09-0709:27:32Te6ec9a82-4986-41ae-95c6-164a717fa1d4;alternate\_reg=CMD\_CREATE\_INST\_CORE\_INFO} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_LUMA\_OFFSET\_BASE1 | | | rw | ro | | 0x0 | | | Compressed Luma offset table base address of DPB index 1 when FBC is used{has\_reset=0} | | | | | |

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| 1.1.1.176.0 | | | | | | | | RET\_DEC\_SUB\_LAYER\_INFO | | | | | reg32 | | 0x330 |
| offset | | 816 | external | | |  | | | size | | 32 |  | |  | |
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| Sub-layer information{alt\_mode=CMD\_CREATE\_INST\_CORE\_INFO\_signal=5;virtualpairUid=2022-09-0709:27:32Te6ec9a82-4986-41ae-95c6-164a717fa1d4;alternate\_reg=CMD\_CREATE\_INST\_CORE\_INFO} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 25:24 | MAX\_SPATIAL\_ID | | | rw | ro | | 0x0 | | | Max spatial ID in current coded video sequence. (for AV1){has\_reset=0} | | | | | |
| 20:19 | SPATIAL\_ID | | | rw | ro | | 0x0 | | | Spatial ID of current picture. (for AV1){has\_reset=0} | | | | | |
| 18:18 | SPATIAL\_SVC\_LAYER | | | rw | ro | | 0x0 | | | Spatial SVC layer (SVAC decoder only)  0 : base layer picture  1 : enhance layer picture{has\_reset=0} | | | | | |
| 17:17 | SPATIAL\_SVC\_MODE | | | rw | ro | | 0x0 | | | Spatial SVC mode (SVAC decoder only)  0 : disable inter-layer prediction, simulcast.  1 : enable inter-layer prediction in which EL picture is predicted with motion vector information from the base layer picture.{has\_reset=0} | | | | | |
| 16:16 | SPATIAL\_SVC\_FLAG | | | rw | ro | | 0x0 | | | Spatial SVC flag (SVAC/AV1 decoder only){has\_reset=0} | | | | | |
| 15:8 | MAX\_TEMPORAL\_ID | | | rw | ro | | 0x0 | | | Max temporal ID (num\_of\_temporal\_level\_minus1 + 1)\_x000D\_  VP9 : N/A{has\_reset=0} | | | | | |
| 7:0 | TEMPORAL\_ID | | | rw | ro | | 0x0 | | | Temporal ID  VP9 : N/A{has\_reset=0} | | | | | |

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| 1.1.1.178.0 | | | | | | | | RET\_ENC\_PIC\_NUM\_SKIP | | | | | reg32 | | 0x330 |
| offset | | 816 | external | | |  | | | size | | 32 |  | |  | |
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| Number of skip block{alt\_mode=CMD\_CREATE\_INST\_CORE\_INFO\_signal=6;virtualpairUid=2022-09-0709:27:32Te6ec9a82-4986-41ae-95c6-164a717fa1d4;alternate\_reg=CMD\_CREATE\_INST\_CORE\_INFO} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | PIC\_NUM\_SKIP | | | rw | ro | | 0x0 | | | The number of skip block in 8x8{has\_reset=0} | | | | | |

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| 1.1.1.179.0 | | | | | | | | CMD\_ENC\_SEQ\_RC\_FRAME\_RATE | | | | | reg32 | | 0x334 |
| offset | | 820 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| CMD\_ENC\_SEQ\_RC\_FRAME\_RATE{alt\_mode=CMD\_CREATE\_INST\_PRIORITY\_signal=1;virtualpairUid=2022-09-0709:27:32T71f10ab9-3169-4b2d-86da-421bc28f21b1;alternate\_reg=CMD\_CREATE\_INST\_PRIORITY} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | RC\_FRAME\_RATE | | | rw | ro | | 0x0 | | | A frame rate indicator for rate control  For example, the value 30 of frameRateInfo represents 30 frames/sec.{has\_reset=0} | | | | | |

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| 1.1.1.180.0 | | | | | | | | CMD\_ENC\_SRC\_ADDR\_U | | | | | reg32 | | 0x334 |
| offset | | 820 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Cb component source address {alt\_mode=CMD\_CREATE\_INST\_PRIORITY\_signal=2;virtualpairUid=2022-09-0709:27:32T71f10ab9-3169-4b2d-86da-421bc28f21b1;alternate\_reg=CMD\_CREATE\_INST\_PRIORITY} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SRC\_ADDR\_U | | | rw | ro | | 0x0 | | | An address of Cb component of a source picture buffer  An address of Cb compressed source buffer when PVRIC\_EN is 1{has\_reset=0} | | | | | |

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| 1.1.1.181.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET1 | | | | | reg32 | | 0x334 |
| offset | | 820 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC chroma offset base of index 1{alt\_mode=CMD\_CREATE\_INST\_PRIORITY\_signal=3;virtualpairUid=2022-09-0709:27:32T71f10ab9-3169-4b2d-86da-421bc28f21b1;alternate\_reg=CMD\_CREATE\_INST\_PRIORITY} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE1 | | | rw | ro | | 0x0 | | | If FBC is used, this is chroma offset base address of DPB index 1. Otherwise, it is ignored.{has\_reset=0} | | | | | |

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| 1.1.1.182.0 | | | | | | | | RET\_DEC\_NOTIFICATION | | | | | reg32 | | 0x334 |
| offset | | 820 | external | | |  | | | size | | 32 |  | |  | |
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| Sequence change flag  If NOTI\_FLAG is equal to 1, VPU detects a new sequence. It may require different decoding resources such as DPB size, DPB number, and etc. Otherwise, VPU decodes the subsequent AU of the sequence.{alt\_mode=CMD\_CREATE\_INST\_PRIORITY\_signal=4;virtualpairUid=2022-09-0709:27:32T71f10ab9-3169-4b2d-86da-421bc28f21b1;alternate\_reg=CMD\_CREATE\_INST\_PRIORITY} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:20 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 19:19 | NOTI\_FLAG\_DPB\_COUNT | | | rw | ro | | 0x0 | | | If NOTI\_FLAG\_DPB\_COUNT is equal to 1, the current picture needs the different number of DPB.{has\_reset=0} | | | | | |
| 18:18 | NOTI\_FLAG\_BITDEPTH | | | rw | ro | | 0x0 | | | If NOTI\_FLAG\_BITDEPTH is equal to 1, the bitdepth of the currently decoded picture is different from the bitdepth of the previously decoded picture.{has\_reset=0} | | | | | |
| 17:17 | NOTI\_FLAG\_INTER\_RES\_CHANGE | | | rw | ro | | 0x0 | | | If NOTI\_FLAG\_INTER\_RES\_CHANGE is equal to 1, one DPB needs to be reallocated. (VP9/AV1 decoder only){has\_reset=0} | | | | | |
| 16:16 | NOTI\_FLAG\_SIZE | | | rw | ro | | 0x0 | | | If NOTI\_FLAG\_SIZE is equal to 1, the decoded size of the current picture is different from the size of the previously decoded picture. Otherwise, the decoded size of current picture is equal to the size of previously decoded picture.{has\_reset=0} | | | | | |
| 15:15 | NOTI\_FLAG\_CHROMA\_FORMAT\_CHANGE | | | rw | ro | | 0x0 | | | If it is equal to 1, the chroma format (4:2:0 etc.) is different from the chroma format of the previously decoded picture.{has\_reset=0} | | | | | |
| 14:6 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 5:5 | NOTI\_FLAG\_PROFILE | | | rw | ro | | 0x0 | | | If NOTI\_FLAG\_PROFILE is equal to 1, the profile of the current picture is different from the profile of the previously decoded picture. Otherwise, the profile of the current picture is equal to the profile of the previously decoded picture.{has\_reset=0} | | | | | |
| 4:0 | RSVD2 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |

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| 1.1.1.184.0 | | | | | | | | RET\_ENC\_PIC\_AVG\_CTU\_QP | | | | | reg32 | | 0x334 |
| offset | | 820 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| CTU QP on average{alt\_mode=CMD\_CREATE\_INST\_PRIORITY\_signal=5;virtualpairUid=2022-09-0709:27:32T71f10ab9-3169-4b2d-86da-421bc28f21b1;alternate\_reg=CMD\_CREATE\_INST\_PRIORITY} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | PIC\_AVG\_CTU\_QP | | | rw | ro | | 0x0 | | | An average value of CTU QPs{has\_reset=0} | | | | | |

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| 1.1.1.185.0 | | | | | | | | CMD\_ENC\_SRC\_ADDR\_V | | | | | reg32 | | 0x338 |
| offset | | 824 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Cr component source address {alt\_mode=CMD\_ENC\_SEQ\_RC\_TARGET\_RATE\_signal=1;virtualpairUid=2022-09-0709:27:32T5e2fe86d-1d70-4964-8c14-ec30876729a2;alternate\_reg=CMD\_ENC\_SEQ\_RC\_TARGET\_RATE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SRC\_ADDR\_V | | | rw | ro | | 0x0 | | | An address of Cr component of a source picture buffer  An address of Cr compressed source buffer when EN\_CFRAME50 is 1{has\_reset=0} | | | | | |

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| 1.1.1.186.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_COL1 | | | | | reg32 | | 0x338 |
| offset | | 824 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Info base of index 1{alt\_mode=CMD\_ENC\_SEQ\_RC\_TARGET\_RATE\_signal=2;virtualpairUid=2022-09-0709:27:32T5e2fe86d-1d70-4964-8c14-ec30876729a2;alternate\_reg=CMD\_ENC\_SEQ\_RC\_TARGET\_RATE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | COL\_BASE1 | | | rw | ro | | 0x0 | | | Codec dedicated information buffer for encoding/decoding  HEVC/AVC: MV COL  AV1 : CDF{has\_reset=0} | | | | | |

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| 1.1.1.187.0 | | | | | | | | RET\_DEC\_USERDATA\_IDC | | | | | reg32 | | 0x338 |
| offset | | 824 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Each bit field of USER\_DATA\_FLAG specifies the report result to USER\_DATA\_BUF\_BASE. (HEVC/AVC only){alt\_mode=CMD\_ENC\_SEQ\_RC\_TARGET\_RATE\_signal=3;virtualpairUid=2022-09-0709:27:32T5e2fe86d-1d70-4964-8c14-ec30876729a2;alternate\_reg=CMD\_ENC\_SEQ\_RC\_TARGET\_RATE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:31 | USERDATA\_FLAG0 | | | rw | ro | | 0x0 | | | A flag of the 3rd user\_data\_registered\_itu\_t\_t35 suffix sei{has\_reset=0} | | | | | |
| 30:30 | USERDATA\_FLAG1 | | | rw | ro | | 0x0 | | | A flag of the 2nd user\_data\_registered\_itu\_t\_t35 suffix sei{has\_reset=0} | | | | | |
| 29:29 | USERDATA\_FLAG2 | | | rw | ro | | 0x0 | | | A flag of the 3rd user\_data\_registered\_itu\_t\_t35 prefix sei{has\_reset=0} | | | | | |
| 28:28 | USERDATA\_FLAG3 | | | rw | ro | | 0x0 | | | A flag of the 2nd user\_data\_registered\_itu\_t\_t35 prefix sei{has\_reset=0} | | | | | |
| 27:17 | USERDATA\_FLAG4 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 16:16 | USERDATA\_FLAG5 | | | rw | ro | | 0x0 | | | A flag of colour\_remapping\_info prefix sei{has\_reset=0} | | | | | |
| 15:15 | USERDATA\_FLAG6 | | | rw | ro | | 0x0 | | | A flag of content\_light\_level\_info prefix sei{has\_reset=0} | | | | | |
| 14:14 | USERDATA\_FLAG7 | | | rw | ro | | 0x0 | | | A flag of film\_grain\_characteristics\_info prefix sei{has\_reset=0} | | | | | |
| 13:13 | USERDATA\_FLAG8 | | | rw | ro | | 0x0 | | | A flag of tone\_mapping\_info prefix sei{has\_reset=0} | | | | | |
| 12:12 | USERDATA\_FLAG9 | | | rw | ro | | 0x0 | | | A flag of knee\_function\_info sei{has\_reset=0} | | | | | |
| 11:11 | USERDATA\_FLAG10 | | | rw | ro | | 0x0 | | | A flag of chroma\_resampling\_filter\_hint prefix sei{has\_reset=0} | | | | | |
| 10:10 | USERDATA\_FLAG11 | | | rw | ro | | 0x0 | | | A flag of mastering\_display\_color\_volume prefix sei{has\_reset=0} | | | | | |
| 9:9 | RSVD12 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 8:8 | USERDATA\_FLAG13 | | | rw | ro | | 0x0 | | | A flag of user\_data\_unregistered suffix sei.{has\_reset=0} | | | | | |
| 7:7 | USERDATA\_FLAG14 | | | rw | ro | | 0x0 | | | A flag of the 1st user\_data\_registered\_itu\_t\_t35 suffix sei.{has\_reset=0} | | | | | |
| 6:6 | USERDATA\_FLAG15 | | | rw | ro | | 0x0 | | | A flag of user\_data\_unregistered prefix sei{has\_reset=0} | | | | | |
| 5:5 | USERDATA\_FLAG16 | | | rw | ro | | 0x0 | | | A flag of the 1st user\_data\_registered\_itu\_t\_t35 prefix sei{has\_reset=0} | | | | | |
| 4:4 | USERDATA\_FLAG17 | | | rw | ro | | 0x0 | | | A flag of pic\_timing sei{has\_reset=0} | | | | | |
| 3:3 | RSVD18 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 2:2 | USERDATA\_FLAG19 | | | rw | ro | | 0x0 | | | A flag of vui parameter.{has\_reset=0} | | | | | |
| 1:1 | USERDATA\_FLAG20 | | | rw | ro | | 0x0 | | | A flag of user data buffer full.  User data buffer full flag equal to 1 specifies that decoded frame has more user data size than VPU internal buffer. VPU only dumps the internal buffer size of user data to USER\_DATA\_BUF\_BASE buffer. In other words, VPU is unable to report the rest of the user data to USER\_DATA\_BUF\_BASE buffer after the internal buffer fullness happens.{has\_reset=0} | | | | | |
| 0:0 | RSVD21 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |

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| 1.1.1.189.0 | | | | | | | | RET\_ENC\_PIC\_BYTE | | | | | reg32 | | 0x338 |
| offset | | 824 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Byte size of encoded picture{alt\_mode=CMD\_ENC\_SEQ\_RC\_TARGET\_RATE\_signal=4;virtualpairUid=2022-09-0709:27:32T5e2fe86d-1d70-4964-8c14-ec30876729a2;alternate\_reg=CMD\_ENC\_SEQ\_RC\_TARGET\_RATE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | PIC\_BYTE | | | rw | ro | | 0x0 | | | The size of encoded picture in byte{has\_reset=0} | | | | | |

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| 1.1.1.190.0 | | | | | | | | CMD\_ENC\_SRC\_STRIDE | | | | | reg32 | | 0x33C |
| offset | | 828 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Stride of source picture{alt\_mode=CMD\_ENC\_SEQ\_RC\_PARAM\_signal=1;virtualpairUid=2022-09-0709:27:32T26638be9-8879-4a66-8008-fb3c88d6f9ab;alternate\_reg=CMD\_ENC\_SEQ\_RC\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | SRC\_Y\_STRIDE | | | rw | ro | | 0x0 | | | A luma stride of source picture in pixel{has\_reset=0} | | | | | |
| 15:0 | SRC\_C\_STRIDE | | | rw | ro | | 0x0 | | | A chroma stride of source picture in pixel. In case of FORMAT\_422, it should be doubled.{has\_reset=0} | | | | | |

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| 1.1.1.191.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE1 | | | | | reg32 | | 0x33C |
| offset | | 828 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Base address of sub-sampled frame buffer for index 1{alt\_mode=CMD\_ENC\_SEQ\_RC\_PARAM\_signal=2;virtualpairUid=2022-09-0709:27:32T26638be9-8879-4a66-8008-fb3c88d6f9ab;alternate\_reg=CMD\_ENC\_SEQ\_RC\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SUB\_SAMPLED\_FB\_BASE1 | | | rw | ro | | 0x0 | | | A base address of frame buffer for sub sampled decoded frames 1{has\_reset=0} | | | | | |

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| 1.1.1.192.0 | | | | | | | | RET\_DEC\_PIC\_SIZE | | | | | reg32 | | 0x33C |
| offset | | 828 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Decoded Picture Size{alt\_mode=CMD\_ENC\_SEQ\_RC\_PARAM\_signal=3;virtualpairUid=2022-09-0709:27:32T26638be9-8879-4a66-8008-fb3c88d6f9ab;alternate\_reg=CMD\_ENC\_SEQ\_RC\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | DECODED\_PIC\_WIDTH | | | rw | ro | | 0x0 | | | Decoded Picture Width  The value of DECODED\_PIC\_WIDTH is eqaul to the value of pic\_width\_in\_luma\_samples in H.265 active SPS.  The value of horizontal\_size in AVS2 active SPS.{has\_reset=0} | | | | | |
| 15:0 | DECODED\_PIC\_HEIGHT | | | rw | ro | | 0x0 | | | Decoded Picture Height  The value of DECODED\_PIC\_HEIGHT is eqaul to the value of pic\_height\_in\_luma\_samples in H.265 active SPS.  The value of vertical\_size in AVS2 active SPS.{has\_reset=0} | | | | | |

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| 1.1.1.194.0 | | | | | | | | RET\_ENC\_GOP\_PIC\_IDX | | | | | reg32 | | 0x33C |
| offset | | 828 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| A picture index in GOP {alt\_mode=CMD\_ENC\_SEQ\_RC\_PARAM\_signal=4;virtualpairUid=2022-09-0709:27:32T26638be9-8879-4a66-8008-fb3c88d6f9ab;alternate\_reg=CMD\_ENC\_SEQ\_RC\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | GOP\_PIC\_IDX | | | rw | ro | | 0x0 | | | A picture index in GOP{has\_reset=0} | | | | | |

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| 1.1.1.195.0 | | | | | | | | CMD\_ENC\_SRC\_FORMAT | | | | | reg32 | | 0x340 |
| offset | | 832 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Format of source picture{alt\_mode=CMD\_ENC\_SEQ\_HVS\_PARAM\_signal=1;virtualpairUid=2022-09-0709:27:32T94a5ed0e-4d23-40d5-b894-8376d608dea1;alternate\_reg=CMD\_ENC\_SEQ\_HVS\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:25 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 15:12 | src\_endian | | | rw | ro | | 0x0 | | | Endianness of source picture{has\_reset=0} | | | | | |
| 11:8 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 6:6 | src\_sample\_left\_aligned | | | rw | ro | | 0x0 | | | (Only for 10bit)  0 : source data bits located MSB  1 : source data bits located LSB{has\_reset=0} | | | | | |
| 5:5 | src\_sample\_special\_flag | | | rw | ro | | 0x0 | | | (Only for 10bit)  0 : 1 pixels packing in 2-byte  1 : 3 pixels packing in 4-byte{has\_reset=0} | | | | | |
| 4:4 | src\_sample\_10bit | | | rw | ro | | 0x0 | | | 0 : 8bit  1 : 10bit{has\_reset=0} | | | | | |
| 3:3 | src\_plane\_special\_flag | | | rw | ro | | 0x0 | | | When source is 1-plane,  0 : YUYV, YVYU  1 : UYUV, VYUY{has\_reset=0} | | | | | |
| 2:2 | src\_plane\_cr\_first | | | rw | ro | | 0x0 | | | For 1-plane,  0 : YUYV  1 : YVYU  For 2-plane,  0 : NV12, NV16  1 : NV21, NV61  For 3-plane, there is no effect because cb\_base and cr\_base have a seperated register.{has\_reset=0} | | | | | |
| 1:0 | src\_plane\_num | | | rw | ro | | 0x0 | | | 0 : prohibited but hardware retrieves it as 3 plane.  1 : 1-plane (Packed - only for YUV422)  2 : 2-plane (one of NV12/21/16/61)  0, 3 : 3-plane (Planar){has\_reset=0} | | | | | |

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| 1.1.1.196.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_LUMA\_BASE2 | | | | | reg32 | | 0x340 |
| offset | | 832 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Luma base of index 2{alt\_mode=CMD\_ENC\_SEQ\_HVS\_PARAM\_signal=2;virtualpairUid=2022-09-0709:27:32T94a5ed0e-4d23-40d5-b894-8376d608dea1;alternate\_reg=CMD\_ENC\_SEQ\_HVS\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | LUMA\_BASE2 | | | rw | ro | | 0x0 | | | Luma base address of DPB index 2  Compressed Luma base address of DPB index 2{has\_reset=0} | | | | | |

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| 1.1.1.197.0 | | | | | | | | RET\_DEC\_CROP\_TOP\_BOTTOM | | | | | reg32 | | 0x340 |
| offset | | 832 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Display Crop Offset Top/Bottom{alt\_mode=CMD\_ENC\_SEQ\_HVS\_PARAM\_signal=3;virtualpairUid=2022-09-0709:27:32T94a5ed0e-4d23-40d5-b894-8376d608dea1;alternate\_reg=CMD\_ENC\_SEQ\_HVS\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | DISPLAY\_TOP\_OFFSET | | | rw | ro | | 0x0 | | | Display top offset  DISPLAY\_TOP\_OFFSET is equal to leftOffset.  topOffset = conf\_win\_top\_offset + def\_disp\_win\_top\_offset.  See Annex E.3 of H.265 specification for more information.{has\_reset=0} | | | | | |
| 15:0 | DISPLAY\_BOTTOM\_OFFSET | | | rw | ro | | 0x0 | | | Display bottom offset  DISPLAY\_BOTTOM\_OFFSET is equal to bottomOffset.  bottomOffset = conf\_win\_bottom\_offset + def\_disp\_win\_bottom\_offset{has\_reset=0} | | | | | |

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| 1.1.1.199.0 | | | | | | | | RET\_ENC\_USED\_SRC\_IDX | | | | | reg32 | | 0x340 |
| offset | | 832 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Buffer index of source picture that is used for encoding{alt\_mode=CMD\_ENC\_SEQ\_HVS\_PARAM\_signal=4;virtualpairUid=2022-09-0709:27:32T94a5ed0e-4d23-40d5-b894-8376d608dea1;alternate\_reg=CMD\_ENC\_SEQ\_HVS\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | USED\_SRC\_PIC\_IDX | | | rw | ro | | 0x0 | | | A source buffer index of the encoded picture (-2 : encoding delay){has\_reset=0} | | | | | |

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| 1.1.1.200.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CB\_BASE2 | | | | | reg32 | | 0x344 |
| offset | | 836 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Cb base of index 2{alt\_mode=CMD\_ENC\_SEQ\_RC\_MAX\_BITRATE\_signal=1;virtualpairUid=2022-09-0709:27:32T5e4acd37-0329-4cfc-bdcf-6ae569421836;alternate\_reg=CMD\_ENC\_SEQ\_RC\_MAX\_BITRATE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CB\_BASE2 | | | rw | ro | | 0x0 | | | Cb base address of DPB index 2  Compressed Cb and Cr base address of DPB index 2{has\_reset=0} | | | | | |

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| 1.1.1.201.0 | | | | | | | | RET\_DEC\_CROP\_LEFT\_RIGHT | | | | | reg32 | | 0x344 |
| offset | | 836 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Display Crop Offset Left/Right{alt\_mode=CMD\_ENC\_SEQ\_RC\_MAX\_BITRATE\_signal=2;virtualpairUid=2022-09-0709:27:32T5e4acd37-0329-4cfc-bdcf-6ae569421836;alternate\_reg=CMD\_ENC\_SEQ\_RC\_MAX\_BITRATE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | DISPLAY\_LEFT\_OFFSET | | | rw | ro | | 0x0 | | | Display left offset  DISPLAY\_LEFT\_OFFSET is equal to leftOffset.  leftOffset = conf\_win\_left\_offset + def\_disp\_win\_left\_offset{has\_reset=0} | | | | | |
| 15:0 | DISPLAY\_RIGHT\_OFFSET | | | rw | ro | | 0x0 | | | Display right offset  DISPLAY\_RIGHT\_OFFSET is equal to rightOffset.  rightOffset = conf\_win\_right\_offset + def\_disp\_win\_right\_offset{has\_reset=0} | | | | | |

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| 1.1.1.203.0 | | | | | | | | RET\_ENC\_PIC\_NUM | | | | | reg32 | | 0x344 |
| offset | | 836 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Encoded picture number{alt\_mode=CMD\_ENC\_SEQ\_RC\_MAX\_BITRATE\_signal=3;virtualpairUid=2022-09-0709:27:32T5e4acd37-0329-4cfc-bdcf-6ae569421836;alternate\_reg=CMD\_ENC\_SEQ\_RC\_MAX\_BITRATE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | PIC\_NUM | | | rw | ro | | 0x0 | | | The encoded picture number{has\_reset=0} | | | | | |

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| 1.1.1.204.0 | | | | | | | | CMD\_ENC\_SEQ\_RC\_VBV\_BUFFER\_SIZE | | | | | reg32 | | 0x348 |
| offset | | 840 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| CMD\_ENC\_SEQ\_RC\_VBV\_BUFFER\_SIZE{alt\_mode=CMD\_CREATE\_INST\_ADDR\_TEMP\_BASE\_signal=1;virtualpairUid=2022-09-0709:27:32Te4120e6d-9df2-4cb6-b629-7530429bdc0d;alternate\_reg=CMD\_CREATE\_INST\_ADDR\_TEMP\_BASE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | RC\_VBV\_BUFFER\_SIZE | | | rw | ro | | 0x0 | | | VBV buffer size in msec{has\_reset=0} | | | | | |

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| 1.1.1.205.0 | | | | | | | | CMD\_ENC\_SRC\_AXI\_SEL | | | | | reg32 | | 0x348 |
| offset | | 840 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Selection of AXI port to load source pictures {alt\_mode=CMD\_CREATE\_INST\_ADDR\_TEMP\_BASE\_signal=2;virtualpairUid=2022-09-0709:27:32Te4120e6d-9df2-4cb6-b629-7530429bdc0d;alternate\_reg=CMD\_CREATE\_INST\_ADDR\_TEMP\_BASE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 0:0 | PRP\_GDI\_SEL | | | rw | ro | | 0x0 | | | 0 : PRP port (default)  1 : Primary port{has\_reset=0} | | | | | |

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| 1.1.1.206.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CR\_BASE2 | | | | | reg32 | | 0x348 |
| offset | | 840 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Cr base of index 2{alt\_mode=CMD\_CREATE\_INST\_ADDR\_TEMP\_BASE\_signal=3;virtualpairUid=2022-09-0709:27:32Te4120e6d-9df2-4cb6-b629-7530429bdc0d;alternate\_reg=CMD\_CREATE\_INST\_ADDR\_TEMP\_BASE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CR\_BASE2 | | | rw | ro | | 0x0 | | | Cr base address of DPB index 2{has\_reset=0} | | | | | |

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| 1.1.1.207.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET2 | | | | | reg32 | | 0x348 |
| offset | | 840 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC luma offset base of index 2{alt\_mode=CMD\_CREATE\_INST\_ADDR\_TEMP\_BASE\_signal=4;virtualpairUid=2022-09-0709:27:32Te4120e6d-9df2-4cb6-b629-7530429bdc0d;alternate\_reg=CMD\_CREATE\_INST\_ADDR\_TEMP\_BASE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_LUMA\_OFFSET\_BASE2 | | | rw | ro | | 0x0 | | | Compressed Luma offset table base address of DPB index 2 when FBC is used{has\_reset=0} | | | | | |

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| 1.1.1.208.0 | | | | | | | | RET\_DEC\_AU\_START\_POS | | | | | reg32 | | 0x348 |
| offset | | 840 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| AU Bitstream Start Position{alt\_mode=CMD\_CREATE\_INST\_ADDR\_TEMP\_BASE\_signal=5;virtualpairUid=2022-09-0709:27:32Te4120e6d-9df2-4cb6-b629-7530429bdc0d;alternate\_reg=CMD\_CREATE\_INST\_ADDR\_TEMP\_BASE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | AU\_START\_POS | | | rw | ro | | 0x0 | | | Access unit(AU) bitstream start position{has\_reset=0} | | | | | |

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| 1.1.1.210.0 | | | | | | | | RET\_ENC\_VCL\_NUT | | | | | reg32 | | 0x348 |
| offset | | 840 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Encoded NAL unit type of VCL{alt\_mode=CMD\_CREATE\_INST\_ADDR\_TEMP\_BASE\_signal=6;virtualpairUid=2022-09-0709:27:32Te4120e6d-9df2-4cb6-b629-7530429bdc0d;alternate\_reg=CMD\_CREATE\_INST\_ADDR\_TEMP\_BASE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | VCL\_NUT | | | rw | ro | | 0x0 | | | The type of the VCL NAL unit which has been encoded for the current command{has\_reset=0} | | | | | |

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| 1.1.1.211.0 | | | | | | | | CMD\_ENC\_CODE\_OPTION | | | | | reg32 | | 0x34C |
| offset | | 844 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| CMD\_ENC\_CODE\_OPTION{alt\_mode=CMD\_CREATE\_INST\_TEMP\_SIZE\_signal=1;virtualpairUid=2022-09-0709:27:32T534f9b1f-97aa-4d7b-8dfb-a0eb35e0a9ee;alternate\_reg=CMD\_CREATE\_INST\_TEMP\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:8 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 7:7 | EOB | | | rw | ro | | 0x0 | | | A flag to encode EOB nal unit explicitly (HEVC, AVC).{has\_reset=0} | | | | | |
| 6:6 | EOS | | | rw | ro | | 0x0 | | | A flag to encode EOS nal unit explicitly (HEVC, AVC).{has\_reset=0} | | | | | |
| 5:5 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 4:4 | PPS | | | rw | ro | | 0x0 | | | A flag to encode PPS nal unit explicitly (HEVC, AVC).  A flag to encode FRAME\_HEADER\_OBU explicitly (AV1).{has\_reset=0} | | | | | |
| 3:3 | SPS | | | rw | ro | | 0x0 | | | A flag to encode SPS nal unit explicitly (HEVC, AVC).  A flag to encode SEQ\_HEADER\_OBU explicitly (AV1).{has\_reset=0} | | | | | |
| 2:2 | VPS | | | rw | ro | | 0x0 | | | A flag to encode VPS nal unit explicitly (HEVC only){has\_reset=0} | | | | | |
| 1:1 | VCL | | | rw | ro | | 0x0 | | | A flag to encode VCL nal unit explicitly (HEVC, AVC).  A flag to encode TILE\_GROUP\_OBU explicitly (AV1).{has\_reset=0} | | | | | |
| 0:0 | IMPLICITLY\_HEADER\_ENCODE | | | rw | ro | | 0x0 | | | A flag to enable to encode a header or headers (SPS, PPS) implicitly for generating bitstreams conforming to specification{has\_reset=0} | | | | | |

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| 1.1.1.212.0 | | | | | | | | CMD\_ENC\_SEQ\_INTER\_MIN\_MAX\_QP | | | | | reg32 | | 0x34C |
| offset | | 844 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| CMD\_ENC\_SEQ\_INTER\_MIN\_MAX\_QP{alt\_mode=CMD\_CREATE\_INST\_TEMP\_SIZE\_signal=2;virtualpairUid=2022-09-0709:27:32T534f9b1f-97aa-4d7b-8dfb-a0eb35e0a9ee;alternate\_reg=CMD\_CREATE\_INST\_TEMP\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:24 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 23:18 | B\_MAX\_QP | | | rw | ro | | 0x0 | | | A maximum QP of B pictures. (0 ~ 51){has\_reset=0} | | | | | |
| 17:12 | B\_MIN\_QP | | | rw | ro | | 0x0 | | | A minimum QP of B pictures. (0 ~ 51){has\_reset=0} | | | | | |
| 11:6 | P\_MAX\_QP | | | rw | ro | | 0x0 | | | A maximum QP of P pictures. (0 ~ 51){has\_reset=0} | | | | | |
| 5:0 | P\_MIN\_QP | | | rw | ro | | 0x0 | | | A minimum QP of P pictures. (0 ~ 51){has\_reset=0} | | | | | |

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| 1.1.1.213.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET2 | | | | | reg32 | | 0x34C |
| offset | | 844 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC chroma offset base of index 2{alt\_mode=CMD\_CREATE\_INST\_TEMP\_SIZE\_signal=3;virtualpairUid=2022-09-0709:27:32T534f9b1f-97aa-4d7b-8dfb-a0eb35e0a9ee;alternate\_reg=CMD\_CREATE\_INST\_TEMP\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE2 | | | rw | ro | | 0x0 | | | If FBC is used, this is chroma offset base address of DPB index 2. Otherwise, it is ignored.{has\_reset=0} | | | | | |

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| 1.1.1.214.0 | | | | | | | | RET\_DEC\_AU\_END\_POS | | | | | reg32 | | 0x34C |
| offset | | 844 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| AU Bitstream End Position{alt\_mode=CMD\_CREATE\_INST\_TEMP\_SIZE\_signal=4;virtualpairUid=2022-09-0709:27:32T534f9b1f-97aa-4d7b-8dfb-a0eb35e0a9ee;alternate\_reg=CMD\_CREATE\_INST\_TEMP\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | AU\_END\_POS | | | rw | ro | | 0x0 | | | Access unit(AU) bitstream end position{has\_reset=0} | | | | | |

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| 1.1.1.216.0 | | | | | | | | RET\_ENC\_PIC\_PADD\_BYTE | | | | | reg32 | | 0x34C |
| offset | | 844 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Encoded NAL padding byte num{alt\_mode=CMD\_CREATE\_INST\_TEMP\_SIZE\_signal=5;virtualpairUid=2022-09-0709:27:32T534f9b1f-97aa-4d7b-8dfb-a0eb35e0a9ee;alternate\_reg=CMD\_CREATE\_INST\_TEMP\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | PADD\_BYTE | | | rw | ro | | 0x0 | | | The size of encoded picture padd in NAL byte{has\_reset=0} | | | | | |

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| 1.1.1.217.0 | | | | | | | | CMD\_ENC\_PIC\_PARAM | | | | | reg32 | | 0x350 |
| offset | | 848 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Picture level encoding parameters {alt\_mode=CMD\_CREATE\_INST\_ADDR\_SEC\_AXI\_signal=1;virtualpairUid=2022-09-0709:27:32Tb40b4091-1660-4f6f-91eb-7ba45d239368;alternate\_reg=CMD\_CREATE\_INST\_ADDR\_SEC\_AXI} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:24 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 23:21 | FORCE\_PIC\_TYPE | | | rw | ro | | 0x0 | | | A force picture type (I, P, IDR) or an irap type  0 : I picture (non-IRAP picture)  1 : P picture (valid if original picture type is not an I picture)  2 : reserved  3 : IDR picture{has\_reset=0} | | | | | |
| 20:20 | USE\_FORCE\_PIC\_TYPE | | | rw | ro | | 0x0 | | | A flag whether to use a force picture type or an irap type{has\_reset=0} | | | | | |
| 19:14 | FORCE\_PIC\_QP\_B | | | rw | ro | | 0x0 | | | A force picture quantization parameter for B picture (0 ~ 51){has\_reset=0} | | | | | |
| 13:8 | FORCE\_PIC\_QP\_P | | | rw | ro | | 0x0 | | | A force picture quantization parameter for P picture (0 ~ 51){has\_reset=0} | | | | | |
| 7:2 | FORCE\_PIC\_QP\_I | | | rw | ro | | 0x0 | | | A force picture quantization parameter for I picture (0 ~ 51){has\_reset=0} | | | | | |
| 1:1 | USE\_FORCE\_PIC\_QP | | | rw | ro | | 0x0 | | | A flag to use a force picture quantization parameter{has\_reset=0} | | | | | |
| 0:0 | PIC\_SKIP\_FLAG | | | rw | ro | | 0x0 | | | A flag to skip the current picture{has\_reset=0} | | | | | |

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| 1.1.1.218.0 | | | | | | | | CMD\_ENC\_SEQ\_ROT\_PARAM | | | | | reg32 | | 0x350 |
| offset | | 848 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| CMD\_ENC\_SEQ\_ROT\_PARAM{alt\_mode=CMD\_CREATE\_INST\_ADDR\_SEC\_AXI\_signal=2;virtualpairUid=2022-09-0709:27:32Tb40b4091-1660-4f6f-91eb-7ba45d239368;alternate\_reg=CMD\_CREATE\_INST\_ADDR\_SEC\_AXI} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:5 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 4:1 | ROTATE\_MODE | | | rw | ro | | 0x0 | | | [3] - horizontal mirror  [2] - vertical mirror  [1:0] - 90 degree left rotate  1=90'  2=180'  3=270'{has\_reset=0} | | | | | |
| 0:0 | ROTATE\_ENABLE | | | rw | ro | | 0x0 | | | It enables or disables rotation.{has\_reset=0} | | | | | |

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| 1.1.1.219.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_COL2 | | | | | reg32 | | 0x350 |
| offset | | 848 | external | | |  | | | size | | 32 |  | |  | |
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| Info base of index 2{alt\_mode=CMD\_CREATE\_INST\_ADDR\_SEC\_AXI\_signal=3;virtualpairUid=2022-09-0709:27:32Tb40b4091-1660-4f6f-91eb-7ba45d239368;alternate\_reg=CMD\_CREATE\_INST\_ADDR\_SEC\_AXI} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | COL\_BASE2 | | | rw | ro | | 0x0 | | | Codec dedicated information buffer for encoding/decoding  HEVC/AVC: MV COL  AV1 : CDF{has\_reset=0} | | | | | |

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| 1.1.1.220.0 | | | | | | | | RET\_DEC\_PIC\_TYPE | | | | | reg32 | | 0x350 |
| offset | | 848 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Decoded picture type{alt\_mode=CMD\_CREATE\_INST\_ADDR\_SEC\_AXI\_signal=4;virtualpairUid=2022-09-0709:27:32Tb40b4091-1660-4f6f-91eb-7ba45d239368;alternate\_reg=CMD\_CREATE\_INST\_ADDR\_SEC\_AXI} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:31 | OUTPUT\_FLAG | | | rw | ro | | 0x0 | | | H.265/H.264 : a picture output flag  VP9 : show\_frame  If OUTPUT\_FLAG is 0, the current decoded picture is not output for display.  If OUTPUT\_FLAG is 1, the current decoded picture is (will be) output for display.  AVS2 : 0 if decoded picture is GB. 1 for other picture types{has\_reset=0} | | | | | |
| 30:30 | REF\_PIC\_FLAG | | | rw | ro | | 0x0 | | | H.264  0 : non reference picture  1 : reference picture{has\_reset=0} | | | | | |
| 11:10 | CTU\_SIZE | | | rw | ro | | 0x0 | | | CTU size  0 : 16x16  1 : 32x32  2 : 64x64{has\_reset=0} | | | | | |
| 9:4 | VCL\_NAL\_UNIT\_TYPE | | | rw | ro | | 0x0 | | | VCL NAL unit type{has\_reset=0} | | | | | |
| 3:3 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 2:0 | PIC\_TYPE | | | rw | ro | | 0x0 | | | H.265/H.264  Each field shows the decoded slices for the picture.  If more than one B slice are decoded, it returns 4 with the value of B\_SLICE\_DECODED[2] equal to 1. If there are all types of slices in a decoded picture, it returns 7.  [2] B\_SLICE\_DECODED  [1] P\_SLICE\_DECODED  [0] I\_SLICE\_DECODED  VP9,  1 : I picture  2 : P picture  AV1  0: KEY FRAME  1: INTER FRAME  2 : INTRA ONLY FRAME  3: SWITCH FRAME  AVS2,  0 : I picture  1 : P picture  2 : B picture  3 : F picture  4 : S picture  5 : G picture  6 : GB picture{has\_reset=0} | | | | | |

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| 1.1.1.222.0 | | | | | | | | RET\_ENC\_PIC\_DIST\_LOW | | | | | reg32 | | 0x350 |
| offset | | 848 | external | | |  | | | size | | 32 |  | |  | |
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| Low 32bit SSD {alt\_mode=CMD\_CREATE\_INST\_ADDR\_SEC\_AXI\_signal=5;virtualpairUid=2022-09-0709:27:32Tb40b4091-1660-4f6f-91eb-7ba45d239368;alternate\_reg=CMD\_CREATE\_INST\_ADDR\_SEC\_AXI} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DIST\_Y\_LOW | | | rw | ro | | 0x0 | | | Low 32bit SSD between source Y picture and reconstructed Y picture{has\_reset=0} | | | | | |

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| 1.1.1.223.0 | | | | | | | | CMD\_ENC\_LONGTERM\_PIC | | | | | reg32 | | 0x354 |
| offset | | 852 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Longterm picture setting{alt\_mode=CMD\_CREATE\_INST\_SEC\_AXI\_SIZE\_signal=1;virtualpairUid=2022-09-0709:27:32T73f57c14-4c40-49da-89f4-dba854a53f83;alternate\_reg=CMD\_CREATE\_INST\_SEC\_AXI\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:2 | RESERVED0 | | | rw | ro | | 0x0 | | | RESERVED{has\_reset=0} | | | | | |
| 1:1 | cmd\_enc\_longterm\_pic | | | rw | ro | | 0x0 | | | A flag to use a longterm reference picture in DPB when encoding the current picture{has\_reset=0} | | | | | |
| 0:0 | USE\_SRC\_LONGTERM\_PIC | | | rw | ro | | 0x0 | | | A flag for the current picture to be used as a longterm reference picture later when other picture's encoding{has\_reset=0} | | | | | |

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| 1.1.1.224.0 | | | | | | | | CMD\_ENC\_SEQ\_NUM\_UNITS\_IN\_TICK | | | | | reg32 | | 0x354 |
| offset | | 852 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| CMD\_ENC\_SEQ\_NUM\_UNITS\_IN\_TICK{alt\_mode=CMD\_CREATE\_INST\_SEC\_AXI\_SIZE\_signal=2;virtualpairUid=2022-09-0709:27:32T73f57c14-4c40-49da-89f4-dba854a53f83;alternate\_reg=CMD\_CREATE\_INST\_SEC\_AXI\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | NUM\_UNITS\_IN\_TICK | | | rw | ro | | 0x0 | | | It specifies the number of time units of a clock operating at the frequency time\_scale Hz.{has\_reset=0} | | | | | |

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| 1.1.1.225.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE2 | | | | | reg32 | | 0x354 |
| offset | | 852 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Base address of sub-sampled frame buffer for index 2{alt\_mode=CMD\_CREATE\_INST\_SEC\_AXI\_SIZE\_signal=3;virtualpairUid=2022-09-0709:27:32T73f57c14-4c40-49da-89f4-dba854a53f83;alternate\_reg=CMD\_CREATE\_INST\_SEC\_AXI\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SUB\_SAMPLED\_FB\_BASE2 | | | rw | ro | | 0x0 | | | A base address of frame buffer for sub sampled decoded frame 2{has\_reset=0} | | | | | |

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| 1.1.1.226.0 | | | | | | | | RET\_DEC\_PIC\_POC | | | | | reg32 | | 0x354 |
| offset | | 852 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Picture Order Count{alt\_mode=CMD\_CREATE\_INST\_SEC\_AXI\_SIZE\_signal=4;virtualpairUid=2022-09-0709:27:32T73f57c14-4c40-49da-89f4-dba854a53f83;alternate\_reg=CMD\_CREATE\_INST\_SEC\_AXI\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | PIC\_ORDER\_COUNT | | | rw | ro | | 0x0 | | | H.265 : picture order count  VP9: N/A  AVS2 : display order index (POI)  POI = DOI + PictureOutputDelay - OutputReorderDelay{has\_reset=0} | | | | | |

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| 1.1.1.228.0 | | | | | | | | RET\_ENC\_PIC\_DIST\_HIGH | | | | | reg32 | | 0x354 |
| offset | | 852 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| High 32bit SSD {alt\_mode=CMD\_CREATE\_INST\_SEC\_AXI\_SIZE\_signal=5;virtualpairUid=2022-09-0709:27:32T73f57c14-4c40-49da-89f4-dba854a53f83;alternate\_reg=CMD\_CREATE\_INST\_SEC\_AXI\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DIST\_Y\_HIGH | | | rw | ro | | 0x0 | | | High 32bit SSD between source Y picture and reconstructed Y picture{has\_reset=0} | | | | | |

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| 1.1.1.229.0 | | | | | | | | CMD\_ENC\_PREFIX\_SEI\_NAL\_ADDR | | | | | reg32 | | 0x358 |
| offset | | 856 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| CMD\_ENC\_PREFIX\_SEI\_NAL\_ADDR{alt\_mode=CMD\_CREATE\_INST\_ADDR\_AR\_TABLE\_signal=1;virtualpairUid=2022-09-0709:27:32T36fca6a2-39fb-4b16-a005-358f3ef7c941;alternate\_reg=CMD\_CREATE\_INST\_ADDR\_AR\_TABLE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | PREFIX\_SEI\_NAL\_DATA\_ADDR | | | rw | ro | | 0x0 | | | The base address of the PREFIX SEI NAL buffer (Big endian){has\_reset=0} | | | | | |

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| 1.1.1.230.0 | | | | | | | | CMD\_ENC\_SEQ\_TIME\_SCALE | | | | | reg32 | | 0x358 |
| offset | | 856 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| CMD\_ENC\_SEQ\_TIME\_SCALE{alt\_mode=CMD\_CREATE\_INST\_ADDR\_AR\_TABLE\_signal=2;virtualpairUid=2022-09-0709:27:32T36fca6a2-39fb-4b16-a005-358f3ef7c941;alternate\_reg=CMD\_CREATE\_INST\_ADDR\_AR\_TABLE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | TIME\_SCALE | | | rw | ro | | 0x0 | | | It specifies the number of time units that pass in one second.{has\_reset=0} | | | | | |

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| 1.1.1.231.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_LUMA\_BASE3 | | | | | reg32 | | 0x358 |
| offset | | 856 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Luma base of index 3{alt\_mode=CMD\_CREATE\_INST\_ADDR\_AR\_TABLE\_signal=3;virtualpairUid=2022-09-0709:27:32T36fca6a2-39fb-4b16-a005-358f3ef7c941;alternate\_reg=CMD\_CREATE\_INST\_ADDR\_AR\_TABLE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | LUMA\_BASE3 | | | rw | ro | | 0x0 | | | Luma base address of DPB index 3  Compressed Luma base address of DPB index 3{has\_reset=0} | | | | | |

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| 1.1.1.232.0 | | | | | | | | RET\_DEC\_RECOVERY\_POINT | | | | | reg32 | | 0x358 |
| offset | | 856 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Recovery point of H.265{alt\_mode=CMD\_CREATE\_INST\_ADDR\_AR\_TABLE\_signal=4;virtualpairUid=2022-09-0709:27:32T36fca6a2-39fb-4b16-a005-358f3ef7c941;alternate\_reg=CMD\_CREATE\_INST\_ADDR\_AR\_TABLE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 18:18 | EXIST\_FLAG | | | rw | ro | | 0x0 | | | exist\_flag{has\_reset=0} | | | | | |
| 17:17 | BROKEN\_LINK\_FLAG | | | rw | ro | | 0x0 | | | broken\_link\_flag{has\_reset=0} | | | | | |
| 16:16 | EXACT\_MATCH\_FLAG | | | rw | ro | | 0x0 | | | exact\_match\_flag{has\_reset=0} | | | | | |
| 15:0 | SIGNED\_RECOVERY\_POC\_CNT | | | rw | ro | | 0x0 | | | signed recovery\_poc\_cnt{has\_reset=0} | | | | | |

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| 1.1.1.234.0 | | | | | | | | RET\_ENC\_MAX\_LATENCY\_PICTURES | | | | | reg32 | | 0x358 |
| offset | | 856 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| The number of latency picture{alt\_mode=CMD\_CREATE\_INST\_ADDR\_AR\_TABLE\_signal=5;virtualpairUid=2022-09-0709:27:32T36fca6a2-39fb-4b16-a005-358f3ef7c941;alternate\_reg=CMD\_CREATE\_INST\_ADDR\_AR\_TABLE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | MAX\_LATENCY\_PIC | | | rw | ro | | 0x0 | | | The number of picture delayed from reordering{has\_reset=0} | | | | | |

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| 1.1.1.235.0 | | | | | | | | CMD\_ENC\_SEQ\_NUM\_TICKS\_POC\_DIFF\_ONE | | | | | reg32 | | 0x35C |
| offset | | 860 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| CMD\_ENC\_SEQ\_NUM\_TICKS\_POC\_DIFF\_ONE{alt\_mode=CMD\_ENC\_PREFIX\_SEI\_INFO\_signal=1;virtualpairUid=2022-09-0709:27:32Tb96a9ca9-6897-498c-9eb4-f12e9b1b6422;alternate\_reg=CMD\_ENC\_PREFIX\_SEI\_INFO} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | NUM\_TICKS\_POC\_DIFF\_ONE | | | rw | ro | | 0x0 | | | It specifies the number of clock ticks corresponding to a difference of picture order count values equal to 1.{has\_reset=0} | | | | | |

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| 1.1.1.236.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CB\_BASE3 | | | | | reg32 | | 0x35C |
| offset | | 860 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Cb base of index 3{alt\_mode=CMD\_ENC\_PREFIX\_SEI\_INFO\_signal=2;virtualpairUid=2022-09-0709:27:32Tb96a9ca9-6897-498c-9eb4-f12e9b1b6422;alternate\_reg=CMD\_ENC\_PREFIX\_SEI\_INFO} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CB\_BASE3 | | | rw | ro | | 0x0 | | | Cb base address of DPB index 3  Compressed Cb and Cr base address of DPB index 3{has\_reset=0} | | | | | |

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| 1.1.1.238.0 | | | | | | | | RET\_DEC\_DEBUG\_INDEX | | | | | reg32 | | 0x35C |
| offset | | 860 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC and BWB frame buffer index for internal use{alt\_mode=CMD\_ENC\_PREFIX\_SEI\_INFO\_signal=3;virtualpairUid=2022-09-0709:27:32Tb96a9ca9-6897-498c-9eb4-f12e9b1b6422;alternate\_reg=CMD\_ENC\_PREFIX\_SEI\_INFO} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 16:16 | DEC\_AV1\_INTRA\_BC\_FLAG | | | rw | ro | | 0x0 | | | intra BC flag for AV1  Used for FBD model on VPU sim. env.{has\_reset=0} | | | | | |
| 15:8 | DEC\_FBC\_FB\_INDEX | | | rw | ro | | 0x0 | | | FBC frame buffer index{has\_reset=0} | | | | | |
| 7:0 | DEC\_BWB\_FB\_INDEX | | | rw | ro | | 0x0 | | | Linear frame buffer index{has\_reset=0} | | | | | |

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| 1.1.1.239.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CR\_BASE3 | | | | | reg32 | | 0x360 |
| offset | | 864 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Cr base of index 3{alt\_mode=CMD\_ENC\_SUFFIX\_SEI\_NAL\_ADDR\_signal=1;virtualpairUid=2022-09-0709:27:32T9262c75b-7010-417e-9ba5-4282b881ec88;alternate\_reg=CMD\_ENC\_SUFFIX\_SEI\_NAL\_ADDR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CR\_BASE3 | | | rw | ro | | 0x0 | | | Cr base address of DPB index 3{has\_reset=0} | | | | | |

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| 1.1.1.240.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET3 | | | | | reg32 | | 0x360 |
| offset | | 864 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC luma offset base of index 3{alt\_mode=CMD\_ENC\_SUFFIX\_SEI\_NAL\_ADDR\_signal=2;virtualpairUid=2022-09-0709:27:32T9262c75b-7010-417e-9ba5-4282b881ec88;alternate\_reg=CMD\_ENC\_SUFFIX\_SEI\_NAL\_ADDR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_LUMA\_OFFSET\_BASE3 | | | rw | ro | | 0x0 | | | Compressed Luma offset table base address of DPB index 3 when FBC is used{has\_reset=0} | | | | | |

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| 1.1.1.241.0 | | | | | | | | RET\_DEC\_DECODED\_INDEX | | | | | reg32 | | 0x360 |
| offset | | 864 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Decoded picture index of DPB{alt\_mode=CMD\_ENC\_SUFFIX\_SEI\_NAL\_ADDR\_signal=3;virtualpairUid=2022-09-0709:27:32T9262c75b-7010-417e-9ba5-4282b881ec88;alternate\_reg=CMD\_ENC\_SUFFIX\_SEI\_NAL\_ADDR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 4:0 | DEC\_PIC\_INDEX | | | rw | ro | | 0x0 | | | Decoded Picture Index for FBC buffer{has\_reset=0} | | | | | |

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| 1.1.1.243.0 | | | | | | | | RET\_ENC\_HISTO\_CNT\_0 | | | | | reg32 | | 0x360 |
| offset | | 864 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| MV histogram count{alt\_mode=CMD\_ENC\_SUFFIX\_SEI\_NAL\_ADDR\_signal=4;virtualpairUid=2022-09-0709:27:32T9262c75b-7010-417e-9ba5-4282b881ec88;alternate\_reg=CMD\_ENC\_SUFFIX\_SEI\_NAL\_ADDR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | HISTO\_CNT\_0 | | | rw | ro | | 0x0 | | | The count number of MV histogram accumulated for class 0{has\_reset=0} | | | | | |

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| 1.1.1.244.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET3 | | | | | reg32 | | 0x364 |
| offset | | 868 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC chroma offset base of index3{alt\_mode=CMD\_ENC\_SUFFIX\_SEI\_INFO\_signal=1;virtualpairUid=2022-09-0709:27:32T97daa0b5-21a7-400d-99a6-c3ba0833176a;alternate\_reg=CMD\_ENC\_SUFFIX\_SEI\_INFO} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE3 | | | rw | ro | | 0x0 | | | If FBC is used, this is chroma offset base address of DPB index 3. Otherwise, it is ignored.{has\_reset=0} | | | | | |

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| 1.1.1.245.0 | | | | | | | | RET\_DEC\_DISPLAY\_INDEX | | | | | reg32 | | 0x364 |
| offset | | 868 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Display picture index of DPB{alt\_mode=CMD\_ENC\_SUFFIX\_SEI\_INFO\_signal=2;virtualpairUid=2022-09-0709:27:32T97daa0b5-21a7-400d-99a6-c3ba0833176a;alternate\_reg=CMD\_ENC\_SUFFIX\_SEI\_INFO} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 4:0 | DISPLAY\_PIC\_INDEX | | | rw | ro | | 0x0 | | | Display Picture Index for FBC buffer (by reordering){has\_reset=0} | | | | | |

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| 1.1.1.247.0 | | | | | | | | RET\_ENC\_HISTO\_CNT\_1 | | | | | reg32 | | 0x364 |
| offset | | 868 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| MV histogram count{alt\_mode=CMD\_ENC\_SUFFIX\_SEI\_INFO\_signal=3;virtualpairUid=2022-09-0709:27:32T97daa0b5-21a7-400d-99a6-c3ba0833176a;alternate\_reg=CMD\_ENC\_SUFFIX\_SEI\_INFO} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | HISTO\_CNT\_1 | | | rw | ro | | 0x0 | | | The count number of MV histogram accumulated for class 1{has\_reset=0} | | | | | |

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| 1.1.1.248.0 | | | | | | | | RET\_DEC\_REALLOC\_INDEX | | | | | reg32 | | 0x368 |
| offset | | 872 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Display picture index of DPB{alt\_mode=CMD\_SET\_FB\_ADDR\_COL3\_signal=1;virtualpairUid=2022-09-0709:27:32Ta5312b75-e4e6-431c-a8f5-df5f19ff91fd;alternate\_reg=CMD\_SET\_FB\_ADDR\_COL3} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 4:0 | DISPLAY\_PIC\_INDEX | | | rw | ro | | 0x0 | | | Display Picture Index for FBC buffer (by reordering){has\_reset=0} | | | | | |

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| 1.1.1.250.0 | | | | | | | | RET\_ENC\_HISTO\_CNT\_2 | | | | | reg32 | | 0x368 |
| offset | | 872 | external | | |  | | | size | | 32 |  | |  | |
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| MV histogram count{alt\_mode=CMD\_SET\_FB\_ADDR\_COL3\_signal=2;virtualpairUid=2022-09-0709:27:32Ta5312b75-e4e6-431c-a8f5-df5f19ff91fd;alternate\_reg=CMD\_SET\_FB\_ADDR\_COL3} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | HISTO\_CNT\_2 | | | rw | ro | | 0x0 | | | The count number of MV histogram accumulated for class 2{has\_reset=0} | | | | | |

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| 1.1.1.251.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE3 | | | | | reg32 | | 0x36C |
| offset | | 876 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Base address of sub-sampled frame buffer for index 3{alt\_mode=CMD\_ENC\_SEQ\_BG\_PARAM\_signal=1;virtualpairUid=2022-09-0709:27:32T93327c5a-5874-4032-aa29-7b96dc4b6e24;alternate\_reg=CMD\_ENC\_SEQ\_BG\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SUB\_SAMPLED\_FB\_BASE3 | | | rw | ro | | 0x0 | | | A base address of frame buffer for sub sampled decoded frame 3{has\_reset=0} | | | | | |

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| 1.1.1.252.0 | | | | | | | | RET\_DEC\_DISP\_IDC | | | | | reg32 | | 0x36C |
| offset | | 876 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| RET\_DEC\_DISP\_IDC{alt\_mode=CMD\_ENC\_SEQ\_BG\_PARAM\_signal=2;virtualpairUid=2022-09-0709:27:32T93327c5a-5874-4032-aa29-7b96dc4b6e24;alternate\_reg=CMD\_ENC\_SEQ\_BG\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DISPLAY\_FLAG | | | rw | ro | | 0x0 | | | Display frame buffer flag.{has\_reset=0} | | | | | |

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| 1.1.1.254.0 | | | | | | | | RET\_ENC\_HISTO\_CNT\_3 | | | | | reg32 | | 0x36C |
| offset | | 876 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| MV histogram count{alt\_mode=CMD\_ENC\_SEQ\_BG\_PARAM\_signal=3;virtualpairUid=2022-09-0709:27:32T93327c5a-5874-4032-aa29-7b96dc4b6e24;alternate\_reg=CMD\_ENC\_SEQ\_BG\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | HISTO\_CNT\_3 | | | rw | ro | | 0x0 | | | The count number of MV histogram accumulated for class 3{has\_reset=0} | | | | | |

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| 1.1.1.255.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_LUMA\_BASE4 | | | | | reg32 | | 0x370 |
| offset | | 880 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Luma base of index 4{alt\_mode=CMD\_ENC\_SEQ\_NON\_VCL\_PARAM\_signal=1;virtualpairUid=2022-09-0709:27:32Tf64295e9-0696-44ae-812b-68fab558ac08;alternate\_reg=CMD\_ENC\_SEQ\_NON\_VCL\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | LUMA\_BASE4 | | | rw | ro | | 0x0 | | | Luma base address of DPB index 4  Compressed Luma base address of DPB index 4{has\_reset=0} | | | | | |

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| 1.1.1.256.0 | | | | | | | | RET\_DEC\_NUM\_ERR\_CTB | | | | | reg32 | | 0x370 |
| offset | | 880 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Number of error CTU{alt\_mode=CMD\_ENC\_SEQ\_NON\_VCL\_PARAM\_signal=2;virtualpairUid=2022-09-0709:27:32Tf64295e9-0696-44ae-812b-68fab558ac08;alternate\_reg=CMD\_ENC\_SEQ\_NON\_VCL\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | ERROR\_CTU\_NUMBER | | | rw | ro | | 0x0 | | | H.265 : error number of CTU  VP9 : error number of SB  SVAC : error number of CTU  AVS2 : error number of LCU  Otherwise : error number of macroblock{has\_reset=0} | | | | | |

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| 1.1.1.258.0 | | | | | | | | RET\_ENC\_HISTO\_CNT\_4 | | | | | reg32 | | 0x370 |
| offset | | 880 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| MV histogram count{alt\_mode=CMD\_ENC\_SEQ\_NON\_VCL\_PARAM\_signal=3;virtualpairUid=2022-09-0709:27:32Tf64295e9-0696-44ae-812b-68fab558ac08;alternate\_reg=CMD\_ENC\_SEQ\_NON\_VCL\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | HISTO\_CNT\_4 | | | rw | ro | | 0x0 | | | The count number of MV histogram accumulated for class 4{has\_reset=0} | | | | | |

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| 1.1.1.259.0 | | | | | | | | CMD\_ENC\_SEQ\_VUI\_RBSP\_ADDR | | | | | reg32 | | 0x374 |
| offset | | 884 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| CMD\_ENC\_SEQ\_VUI\_RBSP\_ADDR{alt\_mode=CMD\_ENC\_CSC\_COEFF\_0\_signal=1;virtualpairUid=2022-09-0709:27:32T4a4fcd77-14e7-4db5-baa2-b8cf0e96ed75;alternate\_reg=CMD\_ENC\_CSC\_COEFF\_0} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | VUI\_RBSP\_ADDR | | | rw | ro | | 0x0 | | | It specifies the address of VUI RBSP buffer. (Little endian){has\_reset=0} | | | | | |

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| 1.1.1.260.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CB\_BASE4 | | | | | reg32 | | 0x374 |
| offset | | 884 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Cb base of index 4{alt\_mode=CMD\_ENC\_CSC\_COEFF\_0\_signal=2;virtualpairUid=2022-09-0709:27:32T4a4fcd77-14e7-4db5-baa2-b8cf0e96ed75;alternate\_reg=CMD\_ENC\_CSC\_COEFF\_0} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CB\_BASE4 | | | rw | ro | | 0x0 | | | Cb base address of DPB index 4  Compressed Cb and Cr base address of DPB index 4{has\_reset=0} | | | | | |

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| 1.1.1.262.0 | | | | | | | | RET\_ENC\_NUM\_TILE\_COL | | | | | reg32 | | 0x374 |
| offset | | 884 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Number of tile columns{alt\_mode=CMD\_ENC\_CSC\_COEFF\_0\_signal=3;virtualpairUid=2022-09-0709:27:32T4a4fcd77-14e7-4db5-baa2-b8cf0e96ed75;alternate\_reg=CMD\_ENC\_CSC\_COEFF\_0} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | NUMBER\_OF\_TILE\_COLUMNS | | | rw | ro | | 0x0 | | | The number of tile columns considering tile constraints (both AV1 spec. and hardware) and rotation. (In case of 90 degree rotation, the number of tiles input from CMD\_ENC\_SEQ\_TILE\_PARAM need to be adjusted to consider the rotated size. the host can identify the actual number of tiles from this register.){has\_reset=0} | | | | | |

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| 1.1.1.263.0 | | | | | | | | CMD\_ENC\_SEQ\_HRD\_RBSP\_ADDR | | | | | reg32 | | 0x378 |
| offset | | 888 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_HRD\_RBSP\_ADDR{alt\_mode=CMD\_ENC\_CSC\_COEFF\_1\_signal=1;virtualpairUid=2022-09-0709:27:32T2c095cb0-c07c-4846-947f-160ee65aa5df;alternate\_reg=CMD\_ENC\_CSC\_COEFF\_1} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | HRD\_RBSP\_ADDR | | | rw | ro | | 0x0 | | | It specifies the address of HRD RBSP buffer. (Little endian){has\_reset=0} | | | | | |

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| 1.1.1.264.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CR\_BASE4 | | | | | reg32 | | 0x378 |
| offset | | 888 | external | | |  | | | size | | 32 |  | |  | |
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| Cr base of index 4{alt\_mode=CMD\_ENC\_CSC\_COEFF\_1\_signal=2;virtualpairUid=2022-09-0709:27:32T2c095cb0-c07c-4846-947f-160ee65aa5df;alternate\_reg=CMD\_ENC\_CSC\_COEFF\_1} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CR\_BASE4 | | | rw | ro | | 0x0 | | | Cr base address of DPB index 4{has\_reset=0} | | | | | |

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| 1.1.1.265.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET4 | | | | | reg32 | | 0x378 |
| offset | | 888 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| FBC luma offset base of index 4{alt\_mode=CMD\_ENC\_CSC\_COEFF\_1\_signal=3;virtualpairUid=2022-09-0709:27:32T2c095cb0-c07c-4846-947f-160ee65aa5df;alternate\_reg=CMD\_ENC\_CSC\_COEFF\_1} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_LUMA\_OFFSET\_BASE4 | | | rw | ro | | 0x0 | | | Compressed Luma offset table base address of DPB index 4 when FBC is used{has\_reset=0} | | | | | |

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| 1.1.1.267.0 | | | | | | | | RET\_ENC\_NUM\_TILE\_ROW | | | | | reg32 | | 0x378 |
| offset | | 888 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Number of tile rows{alt\_mode=CMD\_ENC\_CSC\_COEFF\_1\_signal=4;virtualpairUid=2022-09-0709:27:32T2c095cb0-c07c-4846-947f-160ee65aa5df;alternate\_reg=CMD\_ENC\_CSC\_COEFF\_1} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | NUMBER\_OF\_TILE\_ROWS | | | rw | ro | | 0x0 | | | The number of tile rows considering tile constraints (both AV1 spec. and hardware) and rotation.(In case of 90 degree rotation, the number of tiles input from CMD\_ENC\_SEQ\_TILE\_PARAM need to be adjusted to consider the rotated size. the host can identify the actual number of tiles from this register.){has\_reset=0} | | | | | |

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| 1.1.1.268.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET4 | | | | | reg32 | | 0x37C |
| offset | | 892 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC chroma offset base of index4{alt\_mode=CMD\_ENC\_CSC\_COEFF\_2\_signal=1;virtualpairUid=2022-09-0709:27:32T56c98a85-4560-481d-817d-28e3cf094f89;alternate\_reg=CMD\_ENC\_CSC\_COEFF\_2} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE4 | | | rw | ro | | 0x0 | | | If FBC is used, this is chroma offset base address of DPB index 4. Otherwise, it is ignored.{has\_reset=0} | | | | | |

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| 1.1.1.270.0 | | | | | | | | RET\_ENC\_PIC\_WIDTH | | | | | reg32 | | 0x37C |
| offset | | 892 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Encoded picture width{alt\_mode=CMD\_ENC\_CSC\_COEFF\_2\_signal=2;virtualpairUid=2022-09-0709:27:32T56c98a85-4560-481d-817d-28e3cf094f89;alternate\_reg=CMD\_ENC\_CSC\_COEFF\_2} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | ENCODED\_PICTURE\_WIDTH | | | rw | ro | | 0x0 | | | Encoded picture width considering rotation and padding by mirror and standard constraints. (For example, in case of AVC ENC, both picture width and height should be aligned with 16 pixels. So, the host can identiy the actual encoded picture size from this register.){has\_reset=0} | | | | | |

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| 1.1.1.271.0 | | | | | | | | CMD\_ENC\_SEQ\_QROUND\_OFFSET | | | | | reg32 | | 0x380 |
| offset | | 896 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| CMD\_ENC\_SEQ\_QROUND\_OFFSET{alt\_mode=CMD\_ENC\_CSC\_COEFF\_3\_signal=1;virtualpairUid=2022-09-0709:27:32T571dcddb-3bfc-4a2f-8025-676627200403;alternate\_reg=CMD\_ENC\_CSC\_COEFF\_3} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:24 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 23:13 | CUSTOM\_QROUND\_OFFSET\_INTER | | | rw | ro | | 0x0 | | | It specifies a customized quantization rounding offset for inter pictures. (0 ~ 255){has\_reset=0} | | | | | |
| 12:2 | CUSTOM\_QROUND\_OFFSET\_INTRA | | | rw | ro | | 0x0 | | | It specifies a customized quantization rounding offset for intra pictures(0 ~ 255){has\_reset=0} | | | | | |
| 1:0 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |

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| 1.1.1.272.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_COL4 | | | | | reg32 | | 0x380 |
| offset | | 896 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Info base of index 4{alt\_mode=CMD\_ENC\_CSC\_COEFF\_3\_signal=2;virtualpairUid=2022-09-0709:27:32T571dcddb-3bfc-4a2f-8025-676627200403;alternate\_reg=CMD\_ENC\_CSC\_COEFF\_3} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | COL\_BASE4 | | | rw | ro | | 0x0 | | | Codec dedicated information buffer for encoding/decoding  HEVC/AVC: MV COL  AV1 : CDF{has\_reset=0} | | | | | |

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| 1.1.1.274.0 | | | | | | | | ENC\_PIC\_HEIGHT | | | | | reg32 | | 0x380 |
| offset | | 896 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Encoded picture height{alt\_mode=CMD\_ENC\_CSC\_COEFF\_3\_signal=3;virtualpairUid=2022-09-0709:27:32T571dcddb-3bfc-4a2f-8025-676627200403;alternate\_reg=CMD\_ENC\_CSC\_COEFF\_3} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | ENCODED\_PICTURE\_HEIGHT | | | rw | ro | | 0x0 | | | Encoded picture height considering rotation and padding by mirror and standard constraints. (For example, in case of AVC ENC, both picture width and height should be aligned with 16 pixels. So, the host can identiy the actual encoded picture size from this register.){has\_reset=0} | | | | | |

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| 1.1.1.276.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE4 | | | | | reg32 | | 0x384 |
| offset | | 900 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| Base address of sub-sampled frame buffer for index 4{alt\_mode=CMD\_ENC\_SEQ\_QUANT\_PARAM\_0\_signal=1;virtualpairUid=2022-09-0709:27:32Td61867a9-5387-48c3-a20c-5b69b5cabd1a;alternate\_reg=CMD\_ENC\_SEQ\_QUANT\_PARAM\_0} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SUB\_SAMPLED\_FB\_BASE4 | | | rw | ro | | 0x0 | | | A base address of frame buffer for sub sampled decoded frame 4{has\_reset=0} | | | | | |

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| 1.1.1.278.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_LUMA\_BASE5 | | | | | reg32 | | 0x388 |
| offset | | 904 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Luma base of index 5{alt\_mode=CMD\_ENC\_SEQ\_QUANT\_PARAM\_1\_signal=1;virtualpairUid=2022-09-0709:27:32Tf1eb521d-8068-43d7-a3f5-b52be4a5ee7b;alternate\_reg=CMD\_ENC\_SEQ\_QUANT\_PARAM\_1} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | LUMA\_BASE5 | | | rw | ro | | 0x0 | | | Luma base address of DPB index 5  Compressed Luma base address of DPB index 5{has\_reset=0} | | | | | |

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| 1.1.1.280.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CB\_BASE5 | | | | | reg32 | | 0x38C |
| offset | | 908 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Cb base of index 5{alt\_mode=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PARAM\_signal=1;virtualpairUid=2022-09-0709:27:32Tbf081025-f0a8-42c7-8027-c2b1ab839db4;alternate\_reg=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CB\_BASE5 | | | rw | ro | | 0x0 | | | Cb base address of DPB index 5  Compressed Cb and Cr base address of DPB index 5{has\_reset=0} | | | | | |

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| 1.1.1.281.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CR\_BASE5 | | | | | reg32 | | 0x390 |
| offset | | 912 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Cr base of index 5{alt\_mode=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_0\_signal=1;virtualpairUid=2022-09-0709:27:32T2b814b5e-12f6-4131-82b2-f42cd8b451a4;alternate\_reg=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_0} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CR\_BASE5 | | | rw | ro | | 0x0 | | | Cr base address of DPB index 5{has\_reset=0} | | | | | |

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| 1.1.1.283.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET5 | | | | | reg32 | | 0x390 |
| offset | | 912 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| FBC luma offset base of index 5{alt\_mode=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_0\_signal=2;virtualpairUid=2022-09-0709:27:32T2b814b5e-12f6-4131-82b2-f42cd8b451a4;alternate\_reg=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_0} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_LUMA\_OFFSET\_BASE5 | | | rw | ro | | 0x0 | | | Compressed Luma offset table base address of DPB index 5 when FBC is used{has\_reset=0} | | | | | |

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| 1.1.1.284.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET5 | | | | | reg32 | | 0x394 |
| offset | | 916 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC chroma offset base of index 5{alt\_mode=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_1\_signal=1;virtualpairUid=2022-09-0709:27:32Teb77e763-fc47-434a-b2e8-d0bd11504ae9;alternate\_reg=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_1} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE5 | | | rw | ro | | 0x0 | | | If FBC is used, this is chroma offset base address of DPB index 5. Otherwise, it is ignored.{has\_reset=0} | | | | | |

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| 1.1.1.286.0 | | | | | | | | RET\_DEC\_NUM\_REQURED\_COL\_FB | | | | | reg32 | | 0x394 |
| offset | | 916 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Required Number of Minimum Col FB {alt\_mode=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_1\_signal=2;virtualpairUid=2022-09-0709:27:32Teb77e763-fc47-434a-b2e8-d0bd11504ae9;alternate\_reg=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_1} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 4:0 | MIN\_COL\_DPB\_NUM | | | rw | ro | | 0x0 | | | Required number of frame buffers for decoding sequence  {has\_reset=0} | | | | | |

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| 1.1.1.288.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_COL5 | | | | | reg32 | | 0x398 |
| offset | | 920 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Info base of index5{alt\_mode=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_2\_signal=1;virtualpairUid=2022-09-0709:27:32Tea98b471-70f1-4681-af54-11d5f181bdee;alternate\_reg=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_2} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | COL\_BASE5 | | | rw | ro | | 0x0 | | | Codec dedicated information buffer for encoding/decoding  HEVC/AVC: MV COL  AV1 : CDF{has\_reset=0} | | | | | |

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| 1.1.1.290.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE5 | | | | | reg32 | | 0x39C |
| offset | | 924 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Base address of sub-sampled frame buffer for index 5{alt\_mode=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_3\_signal=1;virtualpairUid=2022-09-0709:27:32Tca0b004e-8982-41fe-a4c6-0878e69809e3;alternate\_reg=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_3} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SUB\_SAMPLED\_FB\_BASE5 | | | rw | ro | | 0x0 | | | A base address of frame buffer for sub sampled decoded frame 5{has\_reset=0} | | | | | |

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| 1.1.1.291.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_LUMA\_BASE6 | | | | | reg32 | | 0x3A0 |
| offset | | 928 | external | | |  | | | size | | 32 |  | |  | |
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| Luma base of index 6{alt\_mode=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_4\_signal=1;virtualpairUid=2022-09-0709:27:32T3bc4aa26-bc06-4c40-8c58-616390cd8a31;alternate\_reg=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_4} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | LUMA\_BASE6 | | | rw | ro | | 0x0 | | | Luma base address of DPB index 6  Compressed Luma base address of DPB index 6{has\_reset=0} | | | | | |

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| 1.1.1.293.0 | | | | | | | | RET\_CORE\_IDC | | | | | reg32 | | 0x3A0 |
| offset | | 928 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| RET\_CORE\_IDC{alt\_mode=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_4\_signal=2;virtualpairUid=2022-09-0709:27:32T3bc4aa26-bc06-4c40-8c58-616390cd8a31;alternate\_reg=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_4} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 15:12 | STAGE3\_CORE\_IDC | | | rw | ro | | 0x0 | | | Allocated core idc for stage #3 (package-encoding){has\_reset=0} | | | | | |
| 11:8 | STAGE2\_CORE\_IDC | | | rw | ro | | 0x0 | | | Allocated core idc for stage #2 (vcore){has\_reset=0} | | | | | |
| 7:4 | STAGE1\_CORE\_IDC | | | rw | ro | | 0x0 | | | Allocated core idc for stage #1 (prescan-decoding){has\_reset=0} | | | | | |
| 3:0 | STAGE0\_CORE\_IDC | | | rw | ro | | 0x0 | | | Allocated core idc for stage #0 (seek/prepare){has\_reset=0} | | | | | |

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| 1.1.1.294.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CB\_BASE6 | | | | | reg32 | | 0x3A4 |
| offset | | 932 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Cb base of index 6{alt\_mode=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_5\_signal=1;virtualpairUid=2022-09-0709:27:32T49c312b9-cbdc-4bf2-9b9e-3a7c259357c2;alternate\_reg=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_5} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CB\_BASE6 | | | rw | ro | | 0x0 | | | Cb base address of DPB index 6  Compressed Cb and Cr base address of DPB index 6{has\_reset=0} | | | | | |

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| 1.1.1.296.0 | | | | | | | | RET\_DEC\_PIC\_PARAM | | | | | reg32 | | 0x3A4 |
| offset | | 932 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Bitstream sequence/picture parameter information{alt\_mode=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_5\_signal=2;virtualpairUid=2022-09-0709:27:32T49c312b9-cbdc-4bf2-9b9e-3a7c259357c2;alternate\_reg=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_5} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:2 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 1:1 | ENABLE\_SCREEN\_CONT\_TOOLS | | | rw | ro | | 0x0 | | | AV1: screen contents tools enable{has\_reset=0} | | | | | |
| 0:0 | ENABLE\_INTRABC | | | rw | ro | | 0x0 | | | AV1: intrabc tool enable{has\_reset=0} | | | | | |

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| 1.1.1.297.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CR\_BASE6 | | | | | reg32 | | 0x3A8 |
| offset | | 936 | external | | |  | | | size | | 32 |  | |  | |
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| Cr base of index 6{alt\_mode=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_6\_signal=1;virtualpairUid=2022-09-0709:27:32T5d80a5d3-1a3b-47c1-99a2-8d18f5271e82;alternate\_reg=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_6} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CR\_BASE6 | | | rw | ro | | 0x0 | | | Cr base address of DPB index 6{has\_reset=0} | | | | | |

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| 1.1.1.298.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET6 | | | | | reg32 | | 0x3A8 |
| offset | | 936 | external | | |  | | | size | | 32 |  | |  | |
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| FBC luma offset base of index 6{alt\_mode=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_6\_signal=2;virtualpairUid=2022-09-0709:27:32T5d80a5d3-1a3b-47c1-99a2-8d18f5271e82;alternate\_reg=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_6} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_LUMA\_OFFSET\_BASE6 | | | rw | ro | | 0x0 | | | Compressed Luma offset table base address of DPB index 6 when FBC is used{has\_reset=0} | | | | | |

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| 1.1.1.300.0 | | | | | | | | RET\_ENC\_CORE\_IDC | | | | | reg32 | | 0x3A8 |
| offset | | 936 | external | | |  | | | size | | 32 |  | |  | |
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| Used core id{alt\_mode=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_6\_signal=3;virtualpairUid=2022-09-0709:27:32T5d80a5d3-1a3b-47c1-99a2-8d18f5271e82;alternate\_reg=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_6} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:4 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 3:0 | ENC\_CORE\_IDC | | | rw | ro | | 0x0 | | | 0x0 : HW not used  0x1 : Core 0  0x2 : Core 1{has\_reset=0} | | | | | |

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| 1.1.1.301.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET6 | | | | | reg32 | | 0x3AC |
| offset | | 940 | external | | |  | | | size | | 32 |  | |  | |
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| FBC chroma offset base of index6{alt\_mode=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_7\_signal=1;virtualpairUid=2022-09-0709:27:32Tb195cde3-469e-4e9d-8393-4049759dd807;alternate\_reg=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_7} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE6 | | | rw | ro | | 0x0 | | | If FBC is used, this is chroma offset base address of DPB index 6. Otherwise, it is ignored.{has\_reset=0} | | | | | |

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| 1.1.1.303.0 | | | | | | | | RET\_HOST\_CMD\_WARN\_INFO | | | | | reg32 | | 0x3AC |
| offset | | 940 | external | | |  | | | size | | 32 |  | |  | |
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| Warning Info{alt\_mode=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_7\_signal=2;virtualpairUid=2022-09-0709:27:32Tb195cde3-469e-4e9d-8393-4049759dd807;alternate\_reg=CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_7} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | ret\_host\_cmd\_warn\_info | | | rw | ro | | 0x0 | | | ret\_host\_cmd\_warn\_info{has\_reset=0} | | | | | |

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| 1.1.1.305.0 | | | | | | | | RET\_HOST\_CMD\_ERR\_INFO | | | | | reg32 | | 0x3B0 |
| offset | | 944 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Error Info{alt\_mode=CMD\_SET\_FB\_ADDR\_COL6\_signal=1;virtualpairUid=2022-09-0709:27:32Tfe313fbe-fbb7-4c8d-b582-265b423d0846;alternate\_reg=CMD\_SET\_FB\_ADDR\_COL6} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | ret\_host\_cmd\_err\_info | | | rw | ro | | 0x0 | | | ret\_host\_cmd\_err\_info{has\_reset=0} | | | | | |

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| 1.1.1.307.0 | | | | | | | | RET\_HOST\_CMD\_SUCCESS | | | | | reg32 | | 0x3B4 |
| offset | | 948 | external | | |  | | | size | | 32 |  | |  | |
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| Host command Reture Value{alt\_mode=CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE6\_signal=1;virtualpairUid=2022-09-0709:27:32T02a09861-a1e4-4112-b489-2444406c2ac4;alternate\_reg=CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE6} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | ret\_host\_cmd\_success | | | rw | ro | | 0x0 | | | ret\_host\_cmd\_success{has\_reset=0} | | | | | |

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| 1.1.1.309.0 | | | | | | | | RET\_ENC\_SUM\_ME0\_X\_DIR\_LOWER | | | | | reg32 | | 0x3B8 |
| offset | | 952 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| mv x sum lower{alt\_mode=CMD\_SET\_FB\_ADDR\_LUMA\_BASE7\_signal=1;virtualpairUid=2022-09-0709:27:32Tc0be92c1-8a02-43a7-939b-e429b687379a;alternate\_reg=CMD\_SET\_FB\_ADDR\_LUMA\_BASE7} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | L0\_MV\_X\_SUIM\_LOWER | | | rw | ro | | 0x0 | | | L0 FME 32x32 mv\_x sum lower{has\_reset=0} | | | | | |

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| 1.1.1.311.0 | | | | | | | | RET\_ENC\_SUM\_ME0\_X\_DIR\_HIGHER | | | | | reg32 | | 0x3BC |
| offset | | 956 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| mv x sum higher{alt\_mode=CMD\_SET\_FB\_ADDR\_CB\_BASE7\_signal=1;virtualpairUid=2022-09-0709:27:32T28ee4502-bbf8-412a-a375-8f11be486f94;alternate\_reg=CMD\_SET\_FB\_ADDR\_CB\_BASE7} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | L0\_MV\_X\_SUIM\_HIGHER | | | rw | ro | | 0x0 | | | L0 FME 32x32 mv\_x sum higher{has\_reset=0} | | | | | |

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| 1.1.1.312.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET7 | | | | | reg32 | | 0x3C0 |
| offset | | 960 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| FBC luma offset base of index 7{alt\_mode=CMD\_SET\_FB\_ADDR\_CR\_BASE7\_signal=1;virtualpairUid=2022-09-0709:27:32T42dd8c3f-a630-4581-8b36-c772020616eb;alternate\_reg=CMD\_SET\_FB\_ADDR\_CR\_BASE7} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_LUMA\_OFFSET\_BASE7 | | | rw | ro | | 0x0 | | | Compressed Luma offset table base address of DPB index 7 when FBC is used{has\_reset=0} | | | | | |

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| 1.1.1.314.0 | | | | | | | | RET\_ENC\_SUM\_ME0\_Y\_DIR\_LOWER | | | | | reg32 | | 0x3C0 |
| offset | | 960 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| mv y sum lower{alt\_mode=CMD\_SET\_FB\_ADDR\_CR\_BASE7\_signal=2;virtualpairUid=2022-09-0709:27:32T42dd8c3f-a630-4581-8b36-c772020616eb;alternate\_reg=CMD\_SET\_FB\_ADDR\_CR\_BASE7} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | L0\_MV\_Y\_SUIM\_LOWER | | | rw | ro | | 0x0 | | | L0 FME 32x32 mv\_y sum lower{has\_reset=0} | | | | | |

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| 1.1.1.316.0 | | | | | | | | RET\_ENC\_SUM\_ME0\_Y\_DIR\_HIGHER | | | | | reg32 | | 0x3C4 |
| offset | | 964 | external | | |  | | | size | | 32 |  | |  | |
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| mv y sum higher{alt\_mode=CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET7\_signal=1;virtualpairUid=2022-09-0709:27:32Te1263344-d0d7-4e61-b4a7-be63dec0fe16;alternate\_reg=CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET7} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | L0\_MV\_Y\_SUIM\_HIGHER | | | rw | ro | | 0x0 | | | L0 FME 32x32 mv\_y sum higher{has\_reset=0} | | | | | |

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| 1.1.1.318.0 | | | | | | | | RET\_ENC\_SUM\_ME1\_X\_DIR\_LOWER | | | | | reg32 | | 0x3C8 |
| offset | | 968 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| mv x sum lower{alt\_mode=CMD\_SET\_FB\_ADDR\_COL7\_signal=1;virtualpairUid=2022-09-0709:27:32T2ff3cdd7-515f-4c23-8dc7-5683463332d1;alternate\_reg=CMD\_SET\_FB\_ADDR\_COL7} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | L1\_MV\_X\_SUIM\_LOWER | | | rw | ro | | 0x0 | | | L1 FME 32x32 mv\_x sum lower{has\_reset=0} | | | | | |

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| 1.1.1.319.0 | | | | | | | | RET\_DEC\_WARN\_INFO | | | | | reg32 | | 0x3CC |
| offset | | 972 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Warning Information {alt\_mode=CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE7\_signal=1;virtualpairUid=2022-09-0709:27:32T52484437-14f9-4dae-acc7-7d9e0fe981dc;alternate\_reg=CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE7} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DEC\_WARN\_INFO | | | rw | ro | | 0x0 | | | Please refer to <<wave6\_error\_info>> defining warnings that VPU might have.{has\_reset=0} | | | | | |

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| 1.1.1.321.0 | | | | | | | | RET\_ENC\_SUM\_ME1\_X\_DIR\_HIGHER | | | | | reg32 | | 0x3CC |
| offset | | 972 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| mv x sum higher{alt\_mode=CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE7\_signal=2;virtualpairUid=2022-09-0709:27:32T52484437-14f9-4dae-acc7-7d9e0fe981dc;alternate\_reg=CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE7} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | L1\_MV\_X\_SUIM\_HIGHER | | | rw | ro | | 0x0 | | | L1 FME 32x32 mv\_x sum higher{has\_reset=0} | | | | | |

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| 1.1.1.322.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_LUMA\_BASE8 | | | | | reg32 | | 0x3D0 |
| offset | | 976 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Luma base of index 8{alt\_mode=CMD\_ENC\_SEQ\_TILE\_PARAM\_signal=1;virtualpairUid=2022-09-0709:27:32T1360298c-6df3-414b-9155-fba07f445ad4;alternate\_reg=CMD\_ENC\_SEQ\_TILE\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | LUMA\_BASE8 | | | rw | ro | | 0x0 | | | Luma base address of DPB index 8  Compressed Luma base address of DPB index 8{has\_reset=0} | | | | | |

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| 1.1.1.323.0 | | | | | | | | RET\_DEC\_ERR\_INFO | | | | | reg32 | | 0x3D0 |
| offset | | 976 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Error Information {alt\_mode=CMD\_ENC\_SEQ\_TILE\_PARAM\_signal=2;virtualpairUid=2022-09-0709:27:32T1360298c-6df3-414b-9155-fba07f445ad4;alternate\_reg=CMD\_ENC\_SEQ\_TILE\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | ERROR\_INFO | | | rw | ro | | 0x0 | | | Please refer to <<wave6\_error\_info>> defining errors that VPU might have.{has\_reset=0} | | | | | |

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| 1.1.1.325.0 | | | | | | | | RET\_ENC\_SUM\_ME1\_Y\_DIR\_LOWER | | | | | reg32 | | 0x3D0 |
| offset | | 976 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| mv y sum lower{alt\_mode=CMD\_ENC\_SEQ\_TILE\_PARAM\_signal=3;virtualpairUid=2022-09-0709:27:32T1360298c-6df3-414b-9155-fba07f445ad4;alternate\_reg=CMD\_ENC\_SEQ\_TILE\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | L1\_MV\_Y\_SUIM\_LOWER | | | rw | ro | | 0x0 | | | L1 FME 32x32 mv\_y sum lower{has\_reset=0} | | | | | |

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| 1.1.1.326.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CB\_BASE8 | | | | | reg32 | | 0x3D4 |
| offset | | 980 | external | | |  | | | size | | 32 |  | |  | |
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| Cb base of index 8{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_0\_signal=1;virtualpairUid=2022-09-0709:27:32Td46888d7-6650-456d-8787-a10863e9e32d;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_0} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CB\_BASE8 | | | rw | ro | | 0x0 | | | Cb base address of DPB index 8  Compressed Cb and Cr base address of DPB index 8{has\_reset=0} | | | | | |

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| 1.1.1.327.0 | | | | | | | | RET\_DEC\_DECODING\_SUCCESS | | | | | reg32 | | 0x3D4 |
| offset | | 980 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| RET\_DEC\_DECODING\_SUCCESS{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_0\_signal=2;virtualpairUid=2022-09-0709:27:32Td46888d7-6650-456d-8787-a10863e9e32d;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_0} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 1:0 | QUERY\_DEC\_SUCCESS | | | rw | ro | | 0x0 | | | It indicates that decoding result for enqueued decode command(INIT\_SEQ or DEC\_PIC)  00: FAIL  If the value is not "zero", it means "SUCCESS"  01: SUCCESS  10: SUCCESS\_WITH\_WARNING (success but there exist some warning)  If it returns FAIL, please refer to RET\_QUERY\_DEC\_ERR\_INFO.  If it returns SUCCESS\_WITH\_WARNING, please refer to RET\_QUERY\_DEC\_WARN\_INFO{has\_reset=0} | | | | | |

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| 1.1.1.329.0 | | | | | | | | RET\_ENC\_SUM\_ME1\_Y\_DIR\_HIGHER | | | | | reg32 | | 0x3D4 |
| offset | | 980 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| mv y sum higher{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_0\_signal=3;virtualpairUid=2022-09-0709:27:32Td46888d7-6650-456d-8787-a10863e9e32d;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_0} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | L1\_MV\_Y\_SUIM\_HIGHER | | | rw | ro | | 0x0 | | | L1 FME 32x32 mv\_y sum higher{has\_reset=0} | | | | | |

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| 1.1.1.330.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CR\_BASE8 | | | | | reg32 | | 0x3D8 |
| offset | | 984 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Cr base of index 8{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_1\_signal=1;virtualpairUid=2022-09-0709:27:32Td86760b6-c0dc-4f1f-aefc-7038b01b76b1;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_1} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CR\_BASE8 | | | rw | ro | | 0x0 | | | Cr base address of DPB index 8{has\_reset=0} | | | | | |

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| 1.1.1.332.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET8 | | | | | reg32 | | 0x3D8 |
| offset | | 984 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC luma offset base of index 8{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_1\_signal=2;virtualpairUid=2022-09-0709:27:32Td86760b6-c0dc-4f1f-aefc-7038b01b76b1;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_1} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_LUMA\_OFFSET\_BASE8 | | | rw | ro | | 0x0 | | | Compressed Luma offset table base address of DPB index 8 when FBC is used{has\_reset=0} | | | | | |

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| 1.1.1.334.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET8 | | | | | reg32 | | 0x3DC |
| offset | | 988 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC chroma offset base of index 8{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_2\_signal=1;virtualpairUid=2022-09-0709:27:32T7f98f243-8e2e-4e3b-9990-86eb3e75b33a;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_2} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE8 | | | rw | ro | | 0x0 | | | If FBC is used, this is chroma offset base address of DPB index 8. Otherwise, it is ignored.{has\_reset=0} | | | | | |

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| 1.1.1.336.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_COL8 | | | | | reg32 | | 0x3E0 |
| offset | | 992 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Info base of index 8{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_3\_signal=1;virtualpairUid=2022-09-0709:27:32T11538bb0-2fe5-4eb3-b027-4cc5140cea15;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_3} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | COL\_BASE8 | | | rw | ro | | 0x0 | | | Codec dedicated information buffer for encoding/decoding  HEVC/AVC: MV COL  AV1 : CDF{has\_reset=0} | | | | | |

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| 1.1.1.338.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE8 | | | | | reg32 | | 0x3E4 |
| offset | | 996 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Base address of sub-sampled frame buffer for index 8{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_4\_signal=1;virtualpairUid=2022-09-0709:27:32T40f79e2d-57ec-4b30-ba4e-cce3ba4bbd4d;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_4} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SUB\_SAMPLED\_FB\_BASE8 | | | rw | ro | | 0x0 | | | A base address of frame buffer for sub sampled decoded frame 8{has\_reset=0} | | | | | |

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| 1.1.1.340.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_LUMA\_BASE9 | | | | | reg32 | | 0x3E8 |
| offset | | 1000 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Luma base of index 9{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_5\_signal=1;virtualpairUid=2022-09-0709:27:32T17a8747d-0285-45dd-adf6-7acc49d8e24d;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_5} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | LUMA\_BASE9 | | | rw | ro | | 0x0 | | | Luma base address of DPB index 9  Compressed Luma base address of DPB index 9{has\_reset=0} | | | | | |

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| 1.1.1.342.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CB\_BASE9 | | | | | reg32 | | 0x3EC |
| offset | | 1004 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Cb base of index 9{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_6\_signal=1;virtualpairUid=2022-09-0709:27:32Tdb096d4d-3be3-4b6d-be07-946b70b7fdba;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_6} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CB\_BASE9 | | | rw | ro | | 0x0 | | | Cb base address of DPB index 9  Compressed Cb and Cr base address of DPB index 9{has\_reset=0} | | | | | |

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| 1.1.1.343.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CR\_BASE9 | | | | | reg32 | | 0x3F0 |
| offset | | 1008 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Cr base of index 9{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_7\_signal=1;virtualpairUid=2022-09-0709:27:32T047fa116-47bf-4b86-a2de-c192c60f2b4c;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_7} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CR\_BASE9 | | | rw | ro | | 0x0 | | | Cr base address of DPB index 9{has\_reset=0} | | | | | |

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| 1.1.1.345.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET9 | | | | | reg32 | | 0x3F0 |
| offset | | 1008 | external | | |  | | | size | | 32 |  | |  | |
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| FBC luma offset base of index 9{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_7\_signal=2;virtualpairUid=2022-09-0709:27:32T047fa116-47bf-4b86-a2de-c192c60f2b4c;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_7} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_LUMA\_OFFSET\_BASE9 | | | rw | ro | | 0x0 | | | Compressed Luma offset table base address of DPB index 9 when FBC is used{has\_reset=0} | | | | | |

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| 1.1.1.347.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET9 | | | | | reg32 | | 0x3F4 |
| offset | | 1012 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC chroma offset base of index 9{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_8\_signal=1;virtualpairUid=2022-09-0709:27:32Tf9c54489-5ed4-4c4b-a906-db3835ab0db2;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_8} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE9 | | | rw | ro | | 0x0 | | | If FBC is used, this is chroma offset base address of DPB index 9. Otherwise, it is ignored.{has\_reset=0} | | | | | |

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| 1.1.1.348.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_COL9 | | | | | reg32 | | 0x3F8 |
| offset | | 1016 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Info base of index 9{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_9\_signal=1;virtualpairUid=2022-09-0709:27:32Td4fcad5b-2f06-423a-9745-3760a5a27909;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_9} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | COL\_BASE9 | | | rw | ro | | 0x0 | | | Codec dedicated information buffer for encoding/decoding  HEVC/AVC: MV COL  AV1 : CDF{has\_reset=0} | | | | | |

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| 1.1.1.350.0 | | | | | | | | RET\_ENC\_SRC\_DEBUG\_0 | | | | | reg32 | | 0x3F8 |
| offset | | 1016 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| ret\_enc\_src\_debug\_0{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_9\_signal=2;virtualpairUid=2022-09-0709:27:32Td4fcad5b-2f06-423a-9745-3760a5a27909;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_9} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SFS\_DEBUG\_INFO | | | rw | ro | | 0x0 | | | SFS debugging info - will be removed{has\_reset=0} | | | | | |

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| 1.1.1.351.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE9 | | | | | reg32 | | 0x3FC |
| offset | | 1020 | external | | |  | | | size | | 32 |  | |  | |
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| Base address of sub-sampled frame buffer for index 9{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_10\_signal=1;virtualpairUid=2022-09-0709:27:32T9a1cbb1e-be5c-44c1-a571-7de4cda9e2d4;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_10} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SUB\_SAMPLED\_FB\_BASE9 | | | rw | ro | | 0x0 | | | A base address of frame buffer for sub sampled decoded frame 9{has\_reset=0} | | | | | |

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| 1.1.1.353.0 | | | | | | | | RET\_ENC\_SRC\_DEBUG\_1 | | | | | reg32 | | 0x3FC |
| offset | | 1020 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| ret\_enc\_src\_debug\_1{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_10\_signal=2;virtualpairUid=2022-09-0709:27:32T9a1cbb1e-be5c-44c1-a571-7de4cda9e2d4;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_10} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SFS\_DEBUG\_INFO | | | rw | ro | | 0x0 | | | SFS debugging info - will be removed{has\_reset=0} | | | | | |

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| 1.1.1.355.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_LUMA\_BASE10 | | | | | reg32 | | 0x400 |
| offset | | 1024 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Luma base of index 10{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_11\_signal=1;virtualpairUid=2022-09-0709:27:32T10f2c046-67ea-4d24-9c78-8bdd34539237;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_11} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | LUMA\_BASE10 | | | rw | ro | | 0x0 | | | Luma base address of DPB index 10  Compressed Luma base address of DPB index 10{has\_reset=0} | | | | | |

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| 1.1.1.357.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CB\_BASE10 | | | | | reg32 | | 0x404 |
| offset | | 1028 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Cb base of index 10{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_12\_signal=1;virtualpairUid=2022-09-0709:27:32T90d70f0c-260d-4cb3-b1b2-426e79bb0d87;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_12} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CB\_BASE10 | | | rw | ro | | 0x0 | | | Cb base address of DPB index 10  Compressed Cb and Cr base address of DPB index 10{has\_reset=0} | | | | | |

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| 1.1.1.358.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CR\_BASE10 | | | | | reg32 | | 0x408 |
| offset | | 1032 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Cr base of index 10{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_13\_signal=1;virtualpairUid=2022-09-0709:27:32T12fe2b7b-ff36-48f4-86c1-a87fa5de5654;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_13} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CR\_BASE10 | | | rw | ro | | 0x0 | | | Cr base address of DPB index 10{has\_reset=0} | | | | | |

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| 1.1.1.360.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET10 | | | | | reg32 | | 0x408 |
| offset | | 1032 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC luma offset base of index 10{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_13\_signal=2;virtualpairUid=2022-09-0709:27:32T12fe2b7b-ff36-48f4-86c1-a87fa5de5654;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_13} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_LUMA\_OFFSET\_BASE10 | | | rw | ro | | 0x0 | | | Compressed Luma offset table base address of DPB index 10 when FBC is used{has\_reset=0} | | | | | |

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| 1.1.1.362.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET10 | | | | | reg32 | | 0x40C |
| offset | | 1036 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC chroma offset base of index 10{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_14\_signal=1;virtualpairUid=2022-09-0709:27:32Td28f0dd7-eb0d-4178-925c-990c0a6f5fcb;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_14} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE10 | | | rw | ro | | 0x0 | | | If FBC is used, this is chroma offset base address of DPB index 10. Otherwise, it is ignored.{has\_reset=0} | | | | | |

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| 1.1.1.364.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_COL10 | | | | | reg32 | | 0x410 |
| offset | | 1040 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| Info base of index 10{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_15\_signal=1;virtualpairUid=2022-09-0709:27:32T87b02600-3ef8-43e4-ba03-f0c4790825eb;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_15} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | COL\_BASE10 | | | rw | ro | | 0x0 | | | Codec dedicated information buffer for encoding/decoding  HEVC/AVC: MV COL  AV1 : CDF{has\_reset=0} | | | | | |

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| 1.1.1.366.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE10 | | | | | reg32 | | 0x414 |
| offset | | 1044 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Base address of sub-sampled frame buffer for index 10{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_16\_signal=1;virtualpairUid=2022-09-0709:27:32T769c4fc8-23ff-4381-9642-8fcf771bb334;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_16} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE10 | | | rw | ro | | 0x0 | | | A base address of frame buffer for sub sampled decoded frame 10{has\_reset=0} | | | | | |

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| 1.1.1.368.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_LUMA\_BASE11 | | | | | reg32 | | 0x418 |
| offset | | 1048 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| Luma base of index 11{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_17\_signal=1;virtualpairUid=2022-09-0709:27:32T09dfcbcf-7f7b-4c7a-9def-5bdce41c5daf;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_17} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | LUMA\_BASE11 | | | rw | ro | | 0x0 | | | Luma base address of DPB index 11  Compressed Luma base address of DPB index 11{has\_reset=0} | | | | | |

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| 1.1.1.370.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CB\_BASE11 | | | | | reg32 | | 0x41C |
| offset | | 1052 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| Cb base of index 11{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_18\_signal=1;virtualpairUid=2022-09-0709:27:32T2c52bbb2-3f0f-4c14-89bb-0ca202764cc9;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_18} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CB\_BASE11 | | | rw | ro | | 0x0 | | | Cb base address of DPB index 11  Compressed Cb and Cr base address of DPB index 11{has\_reset=0} | | | | | |

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| 1.1.1.371.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CR\_BASE11 | | | | | reg32 | | 0x420 |
| offset | | 1056 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| Cr base of index 11{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_19\_signal=1;virtualpairUid=2022-09-0709:27:32Tbc968102-0e96-48e5-9104-32bcf0ef806d;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_19} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CR\_BASE11 | | | rw | ro | | 0x0 | | | Cr base address of DPB index 11{has\_reset=0} | | | | | |

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| 1.1.1.373.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET11 | | | | | reg32 | | 0x420 |
| offset | | 1056 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC luma offset base of index 11{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_19\_signal=2;virtualpairUid=2022-09-0709:27:32Tbc968102-0e96-48e5-9104-32bcf0ef806d;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_19} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_LUMA\_OFFSET\_BASE11 | | | rw | ro | | 0x0 | | | Compressed Luma offset table base address of DPB 11 index when FBC is used{has\_reset=0} | | | | | |

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| 1.1.1.375.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET11 | | | | | reg32 | | 0x424 |
| offset | | 1060 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC chroma offset base of index 11{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_20\_signal=1;virtualpairUid=2022-09-0709:27:32T86eeee10-b7f7-44f6-940c-8f5cda97760e;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_20} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE11 | | | rw | ro | | 0x0 | | | If FBC is used, this is chroma offset base address of DPB index 11. Otherwise, it is ignored.{has\_reset=0} | | | | | |

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| 1.1.1.377.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_COL11 | | | | | reg32 | | 0x428 |
| offset | | 1064 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| Info base of index 11{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_21\_signal=1;virtualpairUid=2022-09-0709:27:32T0090317e-67e6-4cfb-a923-9cf4e9946280;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_21} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | COL\_BASE11 | | | rw | ro | | 0x0 | | | Codec dedicated information buffer for encoding/decoding  HEVC/AVC: MV COL  AV1 : CDF{has\_reset=0} | | | | | |

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| 1.1.1.379.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE11 | | | | | reg32 | | 0x42C |
| offset | | 1068 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Base address of sub-sampled frame buffer for index 11{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_22\_signal=1;virtualpairUid=2022-09-0709:27:32T0e6243ad-6259-48b7-ae99-1c8547af8ac8;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_22} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE11 | | | rw | ro | | 0x0 | | | A base address of frame buffer for sub sampled decoded frame 11{has\_reset=0} | | | | | |

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| 1.1.1.381.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_LUMA\_BASE12 | | | | | reg32 | | 0x430 |
| offset | | 1072 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Luma base of index 12{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_23\_signal=1;virtualpairUid=2022-09-0709:27:32T7921316b-dd7e-4994-8406-27b62aa19cc7;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_23} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | LUMA\_BASE12 | | | rw | ro | | 0x0 | | | Luma base address of DPB index 12  Compressed Luma base address of DPB index 12{has\_reset=0} | | | | | |

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| 1.1.1.383.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CB\_BASE12 | | | | | reg32 | | 0x434 |
| offset | | 1076 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Cb base of index 12{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_24\_signal=1;virtualpairUid=2022-09-0709:27:32T066bab4d-aec7-4629-8032-d7df6e3301fe;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_24} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CB\_BASE12 | | | rw | ro | | 0x0 | | | Cb base address of DPB index 12  Compressed Cb and Cr base address of DPB index 12{has\_reset=0} | | | | | |

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| 1.1.1.384.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CR\_BASE12 | | | | | reg32 | | 0x438 |
| offset | | 1080 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Cr base of index 12{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_25\_signal=1;virtualpairUid=2022-09-0709:27:32Tab553a80-0cf7-4457-b3fb-de6b34b5d9be;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_25} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CR\_BASE12 | | | rw | ro | | 0x0 | | | Cr base address of DPB index 12{has\_reset=0} | | | | | |

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| 1.1.1.386.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET12 | | | | | reg32 | | 0x438 |
| offset | | 1080 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC luma offset base of index 12{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_25\_signal=2;virtualpairUid=2022-09-0709:27:32Tab553a80-0cf7-4457-b3fb-de6b34b5d9be;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_25} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_LUMA\_OFFSET\_BASE12 | | | rw | ro | | 0x0 | | | Compressed Luma offset table base address of DPB index 12 when FBC is used{has\_reset=0} | | | | | |

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| 1.1.1.388.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET12 | | | | | reg32 | | 0x43C |
| offset | | 1084 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| FBC chroma offset base of index 12{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_26\_signal=1;virtualpairUid=2022-09-0709:27:32T257cb468-b340-48e7-9db0-f6e8f23a2967;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_26} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE12 | | | rw | ro | | 0x0 | | | If FBC is used, this is chroma offset base address of DPB index 12. Otherwise, it is ignored.{has\_reset=0} | | | | | |

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| 1.1.1.390.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_COL12 | | | | | reg32 | | 0x440 |
| offset | | 1088 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| Info base of index 12{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_27\_signal=1;virtualpairUid=2022-09-0709:27:32T4edac029-23e9-426f-9633-5afabe5deb23;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_27} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | COL\_BASE12 | | | rw | ro | | 0x0 | | | Codec dedicated information buffer for encoding/decoding  HEVC/AVC: MV COL  AV1 : CDF{has\_reset=0} | | | | | |

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| 1.1.1.392.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE12 | | | | | reg32 | | 0x444 |
| offset | | 1092 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Base address of sub-sampled frame buffer for index 12{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_28\_signal=1;virtualpairUid=2022-09-0709:27:32T6014bd8c-5c14-4197-8d92-8372f5024b4f;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_28} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE12 | | | rw | ro | | 0x0 | | | A base address of frame buffer for sub sampled decoded frame 12{has\_reset=0} | | | | | |

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| 1.1.1.394.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_LUMA\_BASE13 | | | | | reg32 | | 0x448 |
| offset | | 1096 | external | | |  | | | size | | 32 |  | |  | |
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| Luma base of index 13{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_29\_signal=1;virtualpairUid=2022-09-0709:27:32Tfc71c8cc-02c7-44e0-87ae-dd8fc89f6574;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_29} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | LUMA\_BASE13 | | | rw | ro | | 0x0 | | | Luma base address of DPB index 13  Compressed Luma base address of DPB index 13{has\_reset=0} | | | | | |

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| 1.1.1.396.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CB\_BASE13 | | | | | reg32 | | 0x44C |
| offset | | 1100 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| Cb base of index 13{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_30\_signal=1;virtualpairUid=2022-09-0709:27:32T437bfe73-b8e9-4e66-a6f3-3625e58b004c;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_30} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CB\_BASE13 | | | rw | ro | | 0x0 | | | Cb base address of DPB index 13  Compressed Cb and Cr base address of DPB index 13{has\_reset=0} | | | | | |

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| 1.1.1.397.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CR\_BASE13 | | | | | reg32 | | 0x450 |
| offset | | 1104 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| Cr base of index 13{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_31\_signal=1;virtualpairUid=2022-09-0709:27:32T9cb53884-0469-44dd-b18e-5d2f73df6875;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_31} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CR\_BASE13 | | | rw | ro | | 0x0 | | | Cr base address of DPB index 13{has\_reset=0} | | | | | |

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| 1.1.1.399.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET13 | | | | | reg32 | | 0x450 |
| offset | | 1104 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| FBC luma offset base of index 13{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_31\_signal=2;virtualpairUid=2022-09-0709:27:32T9cb53884-0469-44dd-b18e-5d2f73df6875;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_31} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_LUMA\_OFFSET\_BASE13 | | | rw | ro | | 0x0 | | | Compressed Luma offset table base address of DPB index 13 when FBC is used{has\_reset=0} | | | | | |

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| 1.1.1.401.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET13 | | | | | reg32 | | 0x454 |
| offset | | 1108 | external | | |  | | | size | | 32 |  | |  | |
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| FBC chroma offset base of index 13{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_32\_signal=1;virtualpairUid=2022-09-0709:27:32T049b1faf-986e-4889-8677-63060f19ffb4;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_32} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE13 | | | rw | ro | | 0x0 | | | If FBC is used, this is chroma offset base address of DPB index 13. Otherwise, it is ignored.{has\_reset=0} | | | | | |

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| 1.1.1.403.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_COL13 | | | | | reg32 | | 0x458 |
| offset | | 1112 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| Info base of index 13{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_33\_signal=1;virtualpairUid=2022-09-0709:27:32Tb428ec4d-ca90-4fb5-80a5-96d2e3fa9cc4;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_33} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | COL\_BASE13 | | | rw | ro | | 0x0 | | | Codec dedicated information buffer for encoding/decoding  HEVC/AVC: MV COL  AV1 : CDF{has\_reset=0} | | | | | |

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| 1.1.1.405.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE13 | | | | | reg32 | | 0x45C |
| offset | | 1116 | external | | |  | | | size | | 32 |  | |  | |
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| Base address of sub-sampled frame buffer for index 13{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_34\_signal=1;virtualpairUid=2022-09-0709:27:32Tbed604b2-82ee-46a5-a5d1-169eb283106e;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_34} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE13 | | | rw | ro | | 0x0 | | | A base address of frame buffer for sub sampled decoded frame 13{has\_reset=0} | | | | | |

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| 1.1.1.407.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_LUMA\_BASE14 | | | | | reg32 | | 0x460 |
| offset | | 1120 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| Luma base of index 14{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_35\_signal=1;virtualpairUid=2022-09-0709:27:32T7d9aea98-bc2e-4938-bdd2-6b9dcbd1e477;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_35} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | LUMA\_BASE14 | | | rw | ro | | 0x0 | | | Luma base address of DPB index 14  Compressed Luma base address of DPB index 14{has\_reset=0} | | | | | |

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| 1.1.1.409.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CB\_BASE14 | | | | | reg32 | | 0x464 |
| offset | | 1124 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| Cb base of index 14{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_36\_signal=1;virtualpairUid=2022-09-0709:27:32T5d82eed9-66bd-44a1-b006-3b2724d9125d;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_36} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CB\_BASE14 | | | rw | ro | | 0x0 | | | Cb base address of DPB index 14  Compressed Cb and Cr base address of DPB index 14{has\_reset=0} | | | | | |

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| 1.1.1.410.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CR\_BASE14 | | | | | reg32 | | 0x468 |
| offset | | 1128 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| Cr base of index 14{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_37\_signal=1;virtualpairUid=2022-09-0709:27:32T569896bc-be1f-45f2-815e-4ac4c43feeec;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_37} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CR\_BASE14 | | | rw | ro | | 0x0 | | | Cr base address of DPB index 14{has\_reset=0} | | | | | |

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| 1.1.1.412.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET14 | | | | | reg32 | | 0x468 |
| offset | | 1128 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| FBC luma offset base of index 14{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_37\_signal=2;virtualpairUid=2022-09-0709:27:32T569896bc-be1f-45f2-815e-4ac4c43feeec;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_37} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_LUMA\_OFFSET\_BASE14 | | | rw | ro | | 0x0 | | | Compressed Luma offset table base address of DPB index 14 when FBC is used{has\_reset=0} | | | | | |

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| 1.1.1.414.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET14 | | | | | reg32 | | 0x46C |
| offset | | 1132 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC chroma offset base of index 14{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_38\_signal=1;virtualpairUid=2022-09-0709:27:32T6c48ea0c-cb01-4495-970d-e777b6a99cd2;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_38} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE14 | | | rw | ro | | 0x0 | | | If FBC is used, this is chroma offset base address of DPB index 14. Otherwise, it is ignored.{has\_reset=0} | | | | | |

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| 1.1.1.416.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_COL14 | | | | | reg32 | | 0x470 |
| offset | | 1136 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| Info base of index 14{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_39\_signal=1;virtualpairUid=2022-09-0709:27:32Tbc1bccac-84b1-4dcb-a5dd-5345bba52a7b;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_39} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | COL\_BASE14 | | | rw | ro | | 0x0 | | | Codec dedicated information buffer for encoding/decoding  HEVC/AVC: MV COL  AV1 : CDF{has\_reset=0} | | | | | |

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| 1.1.1.418.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE14 | | | | | reg32 | | 0x474 |
| offset | | 1140 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Base address of sub-sampled frame buffer for index 14{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_40\_signal=1;virtualpairUid=2022-09-0709:27:32T204ca053-81fe-457e-b0c7-904ad9458dec;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_40} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE14 | | | rw | ro | | 0x0 | | | A base address of frame buffer for sub sampled decoded frame 14{has\_reset=0} | | | | | |

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| 1.1.1.420.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_LUMA\_BASE15 | | | | | reg32 | | 0x478 |
| offset | | 1144 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Luma base of index 15{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_41\_signal=1;virtualpairUid=2022-09-0709:27:32T69b791c3-4190-4171-9698-d434faaead23;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_41} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | LUMA\_BASE15 | | | rw | ro | | 0x0 | | | Luma base address of DPB index 15  Compressed Luma base address of DPB index 15{has\_reset=0} | | | | | |

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| 1.1.1.422.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CB\_BASE15 | | | | | reg32 | | 0x47C |
| offset | | 1148 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Cb base of index 15{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_42\_signal=1;virtualpairUid=2022-09-0709:27:32T0d8e743e-08a4-4b35-a3aa-993499b4ac8c;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_42} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CB\_BASE15 | | | rw | ro | | 0x0 | | | Cb base address of DPB index 15  Compressed Cb and Cr base address of DPB index 15{has\_reset=0} | | | | | |

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| 1.1.1.423.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CR\_BASE15 | | | | | reg32 | | 0x480 |
| offset | | 1152 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Cr base of index 15{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_43\_signal=1;virtualpairUid=2022-09-0709:27:32Tc9a6cf0a-3d81-40f8-9953-57f71605f9b5;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_43} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CR\_BASE15 | | | rw | ro | | 0x0 | | | Cr base address of DPB index 15{has\_reset=0} | | | | | |

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| 1.1.1.425.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET15 | | | | | reg32 | | 0x480 |
| offset | | 1152 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC luma offset base of index 15{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_43\_signal=2;virtualpairUid=2022-09-0709:27:32Tc9a6cf0a-3d81-40f8-9953-57f71605f9b5;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_43} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_LUMA\_OFFSET\_BASE15 | | | rw | ro | | 0x0 | | | Compressed Luma offset table base address of DPB index 15 when FBC is used{has\_reset=0} | | | | | |

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| 1.1.1.427.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET15 | | | | | reg32 | | 0x484 |
| offset | | 1156 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FBC chroma offset base of index 15{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_44\_signal=1;virtualpairUid=2022-09-0709:27:32T7f0ca812-969c-426f-a8d4-7c827c1970eb;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_44} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE15 | | | rw | ro | | 0x0 | | | If FBC is used, this is chroma offset base address of DPB index 15. Otherwise, it is ignored.{has\_reset=0} | | | | | |

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| 1.1.1.429.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_COL15 | | | | | reg32 | | 0x488 |
| offset | | 1160 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Info base of index 15{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_45\_signal=1;virtualpairUid=2022-09-0709:27:32T3e8e4988-7ce4-4be3-8095-4e4d25377299;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_45} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | COL\_BASE15 | | | rw | ro | | 0x0 | | | Codec dedicated information buffer for encoding/decoding  HEVC/AVC: MV COL  AV1 : CDF{has\_reset=0} | | | | | |

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| 1.1.1.432.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE15 | | | | | reg32 | | 0x48C |
| offset | | 1164 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Base address of sub-sampled frame buffer for index 15 {alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_46\_signal=1;virtualpairUid=2022-09-0709:27:32Tc41719ba-8f58-4d16-905c-4c5dfec84feb;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_46} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE15 | | | rw | ro | | 0x0 | | | A base address of frame buffer for sub sampled decoded frame 15{has\_reset=0} | | | | | |

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| 1.1.1.434.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_DEFAULT\_CDF | | | | | reg32 | | 0x494 |
| offset | | 1172 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_SET\_FB\_ADDR\_DEFAULT\_CDF{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_48\_signal=1;virtualpairUid=2022-09-0709:27:32T9c5754e0-c4a0-46d6-b4b2-d6268ad29c2c;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_48} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DEFAULT\_CDF\_BASE | | | rw | ro | | 0x0 | | | Start Address of default cdf table  AV1 encoder/decoder only{has\_reset=0} | | | | | |

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| 1.1.1.436.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_SEGMAP | | | | | reg32 | | 0x498 |
| offset | | 1176 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| CMD\_SET\_FB\_ADDR\_SEGMAP{alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_49\_signal=1;virtualpairUid=2022-09-0709:27:32T16080eee-d963-4ecb-a898-fcde367152c7;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_49} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SEGMAP\_BUF\_BASE | | | rw | ro | | 0x0 | | | Start Address of segmap buffer  VP9 decoder only{has\_reset=0} | | | | | |

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| 1.1.1.439.0 | | | | | | | | CMD\_SET\_FB\_DEC\_PP\_PVRIC\_CTRL | | | | | reg32 | | 0x49C |
| offset | | 1180 | external | | |  | | | size | | 32 |  | |  | |
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| PVRIC control resigster (Post processing){alt\_mode=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_50\_signal=1;virtualpairUid=2022-09-0709:27:32T785cc35c-8aa3-4efd-a5a3-1c0143febd40;alternate\_reg=CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_50} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:10 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 9:9 | PVRIC\_REQ\_LOSSY | | | rw | ro | | 0x0 | | | pvric lossy  0: off  1: on{has\_reset=0} | | | | | |
| 8:7 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 6:0 | PVRIC\_REQ\_FMT | | | rw | ro | | 0x0 | | | pvric format  0x37 : YVU420, 8bit  0x65: YVU420, 10bit{has\_reset=0} | | | | | |

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| 1.1.1.448.0 | | | | | | | | CMD\_SET\_FB\_DEC\_PP\_SCL\_PARAM | | | | | reg32 | | 0x4A4 |
| offset | | 1188 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Scaler control paramter (Post processing){alt\_mode=CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_0\_QP\_signal=1;virtualpairUid=2022-09-0709:27:32T7a94c0e2-7a19-4ed8-a199-49f70b83944c;alternate\_reg=CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_0\_QP} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:5 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 4:3 | SCL\_CHR\_FORMAT | | | rw | ro | | 0x0 | | | Output chroma format  0 : 420  1 : 422  2 : 444  This field is valid only if SCL\_EN is 1.{has\_reset=0} | | | | | |
| 2:1 | SCL\_COEF\_MODE | | | rw | ro | | 0x0 | | | Scaler interpolation mode  0 : bicubic 0.5  1 : bicubic 1.0  2 : bicubic 1.5  3 : lanczos  This field is valid only if SCL\_EN is 1.{has\_reset=0} | | | | | |
| 0:0 | SCL\_EN | | | rw | ro | | 0x0 | | | This field indicates whether output scaling is enabled or not.  0: Scaling disable  1: Scaling enable  This field is valid only if BWB\_ENABLE is 1.  [NOTE] This is valid only if scaler hardware is included in the product.{has\_reset=0} | | | | | |

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| 1.1.1.450.0 | | | | | | | | CMD\_SET\_FB\_DEC\_PP\_CROP\_POS | | | | | reg32 | | 0x4C4 |
| offset | | 1220 | external | | |  | | | size | | 32 |  | |  | |
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| Crop start position (Post processing){alt\_mode=CMD\_ENC\_SEQ\_SFS\_PARAM\_signal=1;virtualpairUid=2022-09-0709:27:32Te268da9d-9d30-4380-9920-5097e1165065;alternate\_reg=CMD\_ENC\_SEQ\_SFS\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | CROP\_START\_POS\_X | | | rw | ro | | 0x0 | | | Crop start x position  - position must be 16 align{has\_reset=0} | | | | | |
| 15:0 | CROP\_START\_POS\_Y | | | rw | ro | | 0x0 | | | Crop start y position  - position must be 16 align{has\_reset=0} | | | | | |

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| 1.1.1.452.0 | | | | | | | | CMD\_SET\_FB\_DEC\_PP\_CROP\_SIZE | | | | | reg32 | | 0x4C8 |
| offset | | 1224 | external | | |  | | | size | | 32 |  | |  | |
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| Crop size (Post processing){alt\_mode=CMD\_ENC\_SEQ\_CROP\_ENABLE\_signal=1;virtualpairUid=2022-09-0709:27:32T92b71e80-e251-49e3-bc64-026b3fa4ac42;alternate\_reg=CMD\_ENC\_SEQ\_CROP\_ENABLE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | CROP\_WIDTH | | | rw | ro | | 0x0 | | | Crop width  - size must be 16 align{has\_reset=0} | | | | | |
| 15:0 | CROP\_HEIGHT | | | rw | ro | | 0x0 | | | Crop height  - size must be 16 align{has\_reset=0} | | | | | |

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| 1.1.1.457.0 | | | | | | | | CMD\_SET\_FB\_DEC\_PP\_AFBC\_COMMON | | | | | reg32 | | 0x4CC |
| offset | | 1228 | external | | |  | | | size | | 32 |  | |  | |
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| AFBC control paramter (Post processing){alt\_mode=CMD\_ENC\_SEQ\_CROP\_START\_POS\_signal=1;virtualpairUid=2022-09-0709:27:32T5e862428-201b-4a4e-80db-a7edfdd47190;alternate\_reg=CMD\_ENC\_SEQ\_CROP\_START\_POS} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:17 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 16:16 | AFBC\_TZMP\_ERR | | | rw | ro | | 0x0 | | | AFBC core master setting value{has\_reset=0} | | | | | |
| 15:15 | AFBC\_SINGLE\_ID | | | rw | ro | | 0x0 | | | AFBC core master setting value{has\_reset=0} | | | | | |
| 14:12 | AFBC\_OUTSTANDING | | | rw | ro | | 0x0 | | | AFBC core master setting value{has\_reset=0} | | | | | |
| 11:9 | AFBC\_MAX\_LEN | | | rw | ro | | 0x0 | | | AFBC core master setting value{has\_reset=0} | | | | | |
| 8:8 | AFBC\_AFBC\_DATA\_128B | | | rw | ro | | 0x0 | | | AFBC core master setting value{has\_reset=0} | | | | | |
| 7:7 | AFBC\_AWWIDE\_SB | | | rw | ro | | 0x0 | | | AFBC sb\_mode{has\_reset=0} | | | | | |
| 6:6 | AFBC\_AWHALF\_SB | | | rw | ro | | 0x0 | | | AFBC split mode{has\_reset=0} | | | | | |
| 5:1 | AFBC\_FORMAT\_IDX | | | rw | ro | | 0x0 | | | AFBC superblock format index{has\_reset=0} | | | | | |
| 0:0 | AFBC\_SOLID\_COLOR | | | rw | ro | | 0x0 | | | AFBC solid color{has\_reset=0} | | | | | |

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| 1.1.1.1.0 | | | | | | | | CMD\_SET\_FB\_DEC\_ADDR\_COL\_DUAL | | | | | reg32 | | 0x4DC |
| offset | | 1244 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| {alt\_mode=CMD\_ENC\_SEQ\_Y2Y\_DATA\_1\_signal=1;virtualpairUid=2022-09-0709:27:32T93ccfa6e-bf06-4cd1-a09c-df81a8f984dc;alternate\_reg=CMD\_ENC\_SEQ\_Y2Y\_DATA\_1} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | ADDR\_DUAL\_COL | | | rw | ro | | 0x0 | | | Required only for vp9 dual and av1 dual{has\_reset=0} | | | | | |

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| 1.1.1.2.0 | | | | | | | | HOST\_GLOBAL\_WR | | | | | reg32 | | 0x000 |
| offset | | 0 | external | | |  | | | size | | 32 |  | |  | |
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| Host can read and write this register but this register does not affect any VPU operation. VPU has internally single register for all 4 VMs instead of each regsiter for each VM. So, reading/writing from/to this register through any VM accesses the same regsiter value.  The purpose of this register is that host controls VM using mutex such as test\_and\_set operation. | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | HOST\_GLOBAL\_WR | | | rw | ro | | 0x0 | | | host data | | | | | |

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| 1.1.1.3.0 | | | | | | | | VCPU\_CUR\_PC | | | | | reg32 | | 0x004 |
| offset | | 4 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Current program counter value of V-CPU | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CUR\_PC | | | ro | ro | | 0x0 | | | [DEBUG]  PC value represents the address of instruction which is executed in V-CPU | | | | | |

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| 1.1.1.4.0 | | | | | | | | VCPU\_CUR\_LR | | | | | reg32 | | 0x008 |
| offset | | 8 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Current LR (for debugger only) | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CUR\_LR | | | ro | ro | | 0x0 | | | [DEBUG]  Current LR (Link Register) to find out caller address | | | | | |

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| 1.1.1.5.0 | | | | | | | | DBG\_MSG\_17 | | | | | reg32 | | 0x00C |
| offset | | 12 | external | | |  | | | size | | 32 |  | |  | |
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| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.6.0 | | | | | | | | DBG\_MSG\_18 | | | | | reg32 | | 0x010 |
| offset | | 16 | external | | |  | | | size | | 32 |  | |  | |
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| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.7.0 | | | | | | | | DBG\_MSG\_19 | | | | | reg32 | | 0x014 |
| offset | | 20 | external | | |  | | | size | | 32 |  | |  | |
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| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.8.0 | | | | | | | | DBG\_MSG\_20 | | | | | reg32 | | 0x018 |
| offset | | 24 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.1.9.0 | | | | | | | | DBG\_MSG\_21 | | | | | reg32 | | 0x01C |
| offset | | 28 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.10.0 | | | | | | | | VPU\_FIO\_ADDR | | | | | reg32 | | 0x020 |
| offset | | 32 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FIO CRTL, READY, and Address for accessing FIO (FastIO) which is an internal peripheral bus in VPU.  By accessing FIO, user can check the internal status of some accelerators in VPU for debugging purpose in some cases.  FIO transaction is carried out when host writes this register.  CAUTON: Accessing FIO can make unwanted behavior in VPU, please access it using API only. | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:31 | READY | | | rw | ro | | 0x0 | | | Ready for the transaction  When writing, it should be 0. | | | | | |
| 16:16 | RW\_FLAG | | | wo | ro | | 0x0 | | | Read/Write transaction control  0: read  1: write | | | | | |
| 15:0 | FIO\_ADDR | | | wo | ro | | 0x0 | | | FIO Address | | | | | |

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| 1.1.1.11.0 | | | | | | | | VPU\_FIO\_DATA | | | | | reg32 | | 0x024 |
| offset | | 36 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| FIO data | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FIO\_DATA | | | rw | ro | | 0x0 | | | When writing, FIO data should be written to this register firstly.  When reading,  # Write data to this register.  # Check whether READY flag of VPU\_FIO\_CTRL\_ADDR register is 1.  # When READY flag is asserted, VPU reads data from this VPU\_FIO\_DATA. | | | | | |

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| 1.1.1.12.0 | | | | | | | | DBG\_MSG\_0 | | | | | reg32 | | 0x028 |
| offset | | 40 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.13.0 | | | | | | | | DBG\_MSG\_1 | | | | | reg32 | | 0x02C |
| offset | | 44 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.14.0 | | | | | | | | DBG\_MSG\_22 | | | | | reg32 | | 0x030 |
| offset | | 48 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.15.0 | | | | | | | | VPU\_VINT\_REASON\_CLR | | | | | reg32 | | 0x034 |
| offset | | 52 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Interrupt Reason Clear  This register clears the interrupt reason in ISR when host processor catchs an interrupt. It is to notify that host processor has received the interrupt. If host processor wants to get task done interrupts or so from VPU, they should set the fields of VPU\_VINT\_ENABLE register as they wish. And when they recieve any of the command done interrupt from VPU (VPU\_VINT\_REASON\_CLR is not zero), host processor should check the interrupt and do the following sequence for safe interrupt clear.  1. Clear the interrupt by setting the relevant bit of this VPU\_VINT\_REASON\_CLR.  2. Set VPU\_VINT\_CLEAR to 1, which drops the interrupt signal.  Then VPU\_VPU\_INT\_STS is automatically cleared.  In above sequence, 1 should be done first than 2 because VPU\_VINT\_CLEAR without VPU\_VINT\_REASON\_CLR leads to interrupt reassurtion. | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 15:15 | BSEMPTY\_CLR | | | wo | ro | | 0x0 | | | Bitstream empty (bitstream feeding request) interrupt clear | | | | | |
| 14:14 | RSVD0 | | | wo | ro | | 0x0 | | | Reserved | | | | | |
| 13:13 | RSVD1 | | | wo | ro | | 0x0 | | | Reserved | | | | | |
| 12:12 | RSVD2 | | | wo | ro | | 0x0 | | | Reserved | | | | | |
| 11:11 | RSVD3 | | | wo | ro | | 0x0 | | | Reserved | | | | | |
| 10:10 | RSVD4 | | | wo | ro | | 0x0 | | | Reserved | | | | | |
| 9:9 | CMD9\_CLR | | | wo | ro | | 0x0 | | | ENC\_SET\_PARAM command done interrupt clear | | | | | |
| 8:8 | CMD8\_CLR | | | wo | ro | | 0x0 | | | DEC\_PIC/ENC\_PIC command done interrupt clear | | | | | |
| 7:7 | CMD7\_CLR | | | wo | ro | | 0x0 | | | SET\_FRAMEBUFFER command done interrupt clear | | | | | |
| 6:6 | CMD6\_CLR | | | wo | ro | | 0x0 | | | INIT\_SEQ command done interrupt clear | | | | | |
| 5:5 | CMD5\_CLR | | | wo | ro | | 0x0 | | | DESTROY\_INSTANCE command done interrupt clear | | | | | |
| 4:4 | CMD4\_CLR | | | wo | ro | | 0x0 | | | FLSUH\_INSTANCE command done interrupt clear | | | | | |
| 3:3 | CMD3\_CLR | | | wo | ro | | 0x0 | | | CREATE\_INSTANCE command done interrupt clear | | | | | |
| 2:2 | CMD2\_CLR | | | wo | ro | | 0x0 | | | SLEEP\_VPU command done interrupt clear | | | | | |
| 1:1 | CMD1\_CLR | | | wo | ro | | 0x0 | | | WAKE\_VPU command done interrupt clear | | | | | |
| 0:0 | CMD0\_CLR | | | wo | ro | | 0x0 | | | INIT\_VPU command done interrupt clear | | | | | |

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| 1.1.1.16.0 | | | | | | | | VPU\_HOST\_INT\_REQ | | | | | reg32 | | 0x038 |
| offset | | 56 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Interrupt request sent from host processor to VPU for the command and so on. | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 0:0 | HINTREQ | | | wo | ro | | 0x0 | | | If this is set to 1, an interrupt named HOST interrupt is sent to VPU. | | | | | |

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| 1.1.1.17.0 | | | | | | | | VPU\_VINT\_CLEAR | | | | | reg32 | | 0x03C |
| offset | | 60 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Clear VPU interrupt.  Host processor can clear the VPU interrupt which has been pending through this register. As mentioned in VPU\_VINT\_REASON\_CLR, this register setting definetely come after VPU\_INT\_REASON setting. Also, setting this VPU\_VINT\_CLEAR to 1 forces VPU\_VPU\_INT\_STS INT\_STS to be cleared automatically. | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 0:0 | VINTCLR | | | wo | ro | | 0x0 | | | Clear VPU interrupt. | | | | | |

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| 1.1.1.18.0 | | | | | | | | VPU\_HINT\_CLEAR | | | | | reg32 | | 0x040 |
| offset | | 64 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Check Host Command Interrupt is cleared.  From host side, this register is not used or checked.  VPU can clear the host interrupt which has been pending through this register. When VPU operation for the host interrupt is done, VPU sets this reigster to clear the host interrupt. | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 0:0 | HINTCLR | | | wo | ro | | 0x0 | | | Check Host Command Interrupt is cleared. | | | | | |

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| 1.1.1.19.0 | | | | | | | | VPU\_VPU\_INT\_STS | | | | | reg32 | | 0x044 |
| offset | | 68 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Interrupt Status.  This has the same value as interrupt output signal from VPU. This is a way of interrupt check by register polling. | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 0:0 | VPU\_VPU\_INT\_STS | | | ro | ro | | 0x0 | | | Interrupt Status | | | | | |

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| 1.1.1.20.0 | | | | | | | | VPU\_VINT\_ENABLE | | | | | reg32 | | 0x048 |
| offset | | 72 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Interrupt Enable for each interrupt reason(source)  Interrupt in LSB position shall be handled with higher priority. | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 15:15 | BSEMPTY\_EN | | | rw | ro | | 0x0 | | | Bitstream empty (bitstream feeding request) interrupt clear | | | | | |
| 14:14 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved | | | | | |
| 13:13 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved | | | | | |
| 12:12 | RSVD2 | | | rw | ro | | 0x0 | | | Reserved | | | | | |
| 11:11 | RSVD3 | | | rw | ro | | 0x0 | | | Reserved | | | | | |
| 10:10 | RSVD4 | | | rw | ro | | 0x0 | | | Reserved | | | | | |
| 9:9 | CMD9\_EN | | | rw | ro | | 0x0 | | | ENC\_SET\_PARAM command done interrupt enable | | | | | |
| 8:8 | CMD8\_EN | | | rw | ro | | 0x0 | | | DEC\_PIC/ENC\_PIC command done interrupt enable | | | | | |
| 7:7 | CMD7\_EN | | | rw | ro | | 0x0 | | | SET\_FRAMEBUFFER command done interrupt enable | | | | | |
| 6:6 | CMD6\_EN | | | rw | ro | | 0x0 | | | INIT\_SEQ command done interrupt enable | | | | | |
| 5:5 | CMD5\_EN | | | rw | ro | | 0x0 | | | DESTROY\_INSTANCE command done interrupt enable | | | | | |
| 4:4 | CMD4\_EN | | | rw | ro | | 0x0 | | | FLSUH\_INSTANCE command done interrupt enable | | | | | |
| 3:3 | CMD3\_EN | | | rw | ro | | 0x0 | | | CREATE\_INSTANCE command done interrupt enable | | | | | |
| 2:2 | CMD2\_EN | | | rw | ro | | 0x0 | | | SLEEP\_VPU command done interrupt enable | | | | | |
| 1:1 | CMD1\_EN | | | rw | ro | | 0x0 | | | WAKE\_VPU command done interrupt enable | | | | | |
| 0:0 | CMD0\_EN | | | rw | ro | | 0x0 | | | INIT\_VPU command done interrupt enable | | | | | |

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| 1.1.1.22.0 | | | | | | | | VPU\_VINT\_REASON | | | | | reg32 | | 0x04C |
| offset | | 76 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| VPU interrupt reason  This register Interrupt reasons are almost the same with the command. Interrupt in LSB position shall be handled with higher priority. | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 15:15 | BSEMPTY\_INTR | | | rw | ro | | 0x0 | | | Bitstream empty (bitstream feeding request) | | | | | |
| 14:14 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved | | | | | |
| 13:13 | CMDD\_INTR | | | rw | ro | | 0x0 | | | Low latency interrupt | | | | | |
| 12:12 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved | | | | | |
| 11:11 | RSVD2 | | | rw | ro | | 0x0 | | | Reserved | | | | | |
| 10:10 | RSVD3 | | | rw | ro | | 0x0 | | | Reserved | | | | | |
| 9:9 | CMD9\_INTR | | | rw | ro | | 0x0 | | | ENC\_SET\_PARAM command done interrupt | | | | | |
| 8:8 | CMD8\_INTR | | | rw | ro | | 0x0 | | | DEC\_PIC/ENC\_PIC command done interrupt | | | | | |
| 7:7 | CMD7\_INTR | | | rw | ro | | 0x0 | | | SET\_FRAMEBUFFER command done interrupt | | | | | |
| 6:6 | CMD6\_INTR | | | rw | ro | | 0x0 | | | INIT\_SEQ command done interrupt | | | | | |
| 5:5 | CMD5\_INTR | | | rw | ro | | 0x0 | | | DESTROY\_INSTANCE command done interrupt | | | | | |
| 4:4 | CMD4\_INTR | | | rw | ro | | 0x0 | | | FLSUH\_INSTANCE command done interrupt | | | | | |
| 3:3 | CMD3\_INTR | | | rw | ro | | 0x0 | | | CREATE\_INSTANCE command done interrupt | | | | | |
| 2:2 | CMD2\_INTR | | | rw | ro | | 0x0 | | | SLEEP\_VPU command done interrupt | | | | | |
| 1:1 | CMD1\_INTR | | | rw | ro | | 0x0 | | | WAKE\_VPU command done interrupt | | | | | |
| 0:0 | CMD0\_INTR | | | rw | ro | | 0x0 | | | INIT\_VPU command done interrupt | | | | | |

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| 1.1.1.24.0 | | | | | | | | VCPU\_RESTART | | | | | reg32 | | 0x058 |
| offset | | 88 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| V-CPU restart request | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 0:0 | VCPU\_RESTART | | | wo | ro | | 0x0 | | | This register restarts V-CPU from the reset vector without clearing H/W logic.  0: DO NOTHING  1: RESTART REQUEST | | | | | |

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| 1.1.1.25.0 | | | | | | | | VPU\_REMAP\_CTRL | | | | | reg32 | | 0x060 |
| offset | | 96 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Remap control register (REMAP REG ADDR / ATTR / SIZE)  VPU remaps addresses VCPU uses between the physical memory and virtual memory for efficient address management. VPU works with the virtual memory addresses that are translated to the phsyical addresses. Host processor needs to assign V-CPU code buffer to VPU\_REMAP\_PADDR and VPU\_REMAP\_VADDR to 0, so that VPU can start by reading from VPU\_REMAP\_PADDR considering it is its the base address 0. This register has the configuration fields for remapping. | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:31 | REMAP\_GLOBEN | | | rw | ro | | 0x0 | | | Set 1 if you want to change the [30:12] part of this register  Default to be 0 | | | | | |
| 30:20 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved | | | | | |
| 19:16 | ENDIAN | | | rw | ro | | 0x0 | | | Endianness for memory access  Endian control of memory transactions from processor core | | | | | |
| 15:12 | REMAP\_IDX | | | rw | ro | | 0x0 | | | Remap index  Only 0 to 3 are valid. | | | | | |
| 11:11 | REMAP\_PAGE\_SIZE\_EN | | | rw | ro | | 0x0 | | | Set 1 if you want to change the REMAP\_PSIZE field  Default to be 0 | | | | | |
| 10:9 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved | | | | | |
| 8:0 | REMAP\_PSIZE | | | rw | ro | | 0x0 | | | Remap Page Size (page base should be aligned in 4KB boundary)  0x001: 4K  0x002: 8K  0x004: 16K  0x008: 32K  0x010 : 64K  0x020 : 128K  0x040 : 256K  0x080: 512K  0x100: 1M | | | | | |

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| 1.1.1.26.0 | | | | | | | | VPU\_REMAP\_VADDR | | | | | reg32 | | 0x064 |
| offset | | 100 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Remap region base address in virtual address space  Virtual address space is an address generated by V-CPU.  To setup Remap region, keep the sequence below.  # set remap index using REMAP\_IDX in VPU\_REMAP\_CTRL. While setting up, other information should be the same as the previous value  # set virtual address using VPU\_REMAP\_VADDR  # set physical address using VPU\_REMAP\_PADDR  CAUTION: In case of CODE section (which has REMAP IDX 0), virtual address should be 0x0, since V-CPU always start booting up from virtual address 0. If not, VPU can not boot-up. | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:12 | VPU\_REMAP\_VADDR | | | rw | ro | | 0x0 | | | Remap region base address in virtual address space.  The address should be aligned to 4KB boundary. | | | | | |

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| 1.1.1.27.0 | | | | | | | | VPU\_REMAP\_PADDR | | | | | reg32 | | 0x068 |
| offset | | 104 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Remap region base address in physical address space | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:12 | VPU\_REMAP\_PADDR | | | rw | ro | | 0x0 | | | Real address(physical address) as a pair of virtual address.  It should aligned to 4KB boundary. | | | | | |

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| 1.1.1.28.0 | | | | | | | | VPU\_REMAP\_CORE\_START | | | | | reg32 | | 0x06C |
| offset | | 108 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| VPU Start Request | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 0:0 | VPU\_REMAP\_CORE\_START | | | rw | ro | | 0x0 | | | It starts VPU after initial setting has been done.  After setting up remap or initial configuartion, host should set this register to init VPU. | | | | | |

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| 1.1.1.29.0 | | | | | | | | VCPU\_CMD\_BUSY\_STATUS | | | | | reg32 | | 0x070 |
| offset | | 112 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| V-CPU Busy Status | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 0:0 | VPU\_BUSY\_STATUS | | | rw | ro | | 0x0 | | | Command Reentrance Check [0]  0: Host processor has the ownership for access to host interface.  1: VPU has the ownership for access to host interface.  - host should set this flag just before trying to send a command into command-queue  - firmware clears this flag when a command is queueued for processing.  - for the case of clock\_gating or power\_down, please use VPU\_VCPU\_STATUS register to check the status of VPU. | | | | | |

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| 1.1.1.30.0 | | | | | | | | VPU\_HALT\_STATUS | | | | | reg32 | | 0x074 |
| offset | | 116 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| For power control, status checking of V-CPU | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 4:4 | VPU\_HALT\_STATUS | | | ro | ro | | 0x0 | | | 1: V-CPU is on the HALT status | | | | | |
| 3:0 | VPU\_HALT\_STATUS\_DEBUG | | | ro | ro | | 0x0 | | | for debugging  - Eventhough V-CPU is on HALT status, for the clock gating or power down, VPU\_VCPU\_STATUS should be checked to check pending bus operations. | | | | | |

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| 1.1.1.31.0 | | | | | | | | VPU\_VCPU\_STATUS | | | | | reg32 | | 0x078 |
| offset | | 120 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| V-CPU bus busy and V-CPU status | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 14:0 | VPU\_VCPU\_STATUS | | | ro | ro | | 0x0 | | | If [31:16] is 0x0000, there is no more bus transaction on V-CPU.  If [15:0] is 0x0040, V-CPU is on the halt status.  Thus, the value returns 0x40, power for VPU can be turnned-off | | | | | |

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| 1.1.1.32.0 | | | | | | | | VPU\_BUSY\_STATUS | | | | | reg32 | | 0x07C |
| offset | | 124 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| VPU Busy Status | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 0:0 | VPU\_BUSY\_STATUS | | | ro | ro | | 0x0 | | | 0 : VPU is idle. Host processor can gate the clock of VPU.  1 : VPU is busy. | | | | | |

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| 1.1.1.33.0 | | | | | | | | RET\_FIO\_STATUS | | | | | reg32 | | 0x080 |
| offset | | 128 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Reserved | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | RSVD0 | | | ro | ro | | 0x0 | | | Reserved | | | | | |

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| 1.1.1.34.0 | | | | | | | | DBG\_MSG\_3 | | | | | reg32 | | 0x084 |
| offset | | 132 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.35.0 | | | | | | | | DBG\_MSG\_4 | | | | | reg32 | | 0x088 |
| offset | | 136 | external | | |  | | | size | | 32 |  | |  | |
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| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.36.0 | | | | | | | | DBG\_MSG\_5 | | | | | reg32 | | 0x08C |
| offset | | 140 | external | | |  | | | size | | 32 |  | |  | |
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| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.37.0 | | | | | | | | RET\_PRODUCT\_NAME | | | | | reg32 | | 0x090 |
| offset | | 144 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| VPU hardware product name | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 3:0 | HW\_NAME | | | ro | ro | | 0x0 | | | It always returns "WAVE" for WAVE6 series IP product. | | | | | |

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| 1.1.1.38.0 | | | | | | | | RET\_PRODUCT\_VERSION | | | | | reg32 | | 0x094 |
| offset | | 148 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| VPU hardware product version information.  [NOTE] The list is just examples of version code. Version code can be varied without notice | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 3:0 | PRODUCT\_NUMBER | | | ro | ro | | 0x0 | | | It returns as follows: 0x6270 for WAVE627 | | | | | |

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| 1.1.1.39.0 | | | | | | | | RET\_VCPU\_CONFIG0 | | | | | reg32 | | 0x098 |
| offset | | 152 | external | | |  | | | size | | 32 |  | |  | |
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| Reserved for Configuration Information | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | RSVD0 | | | ro | ro | | 0x0 | | | Configuration Information #0 (internal use only) | | | | | |

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| 1.1.1.40.0 | | | | | | | | RET\_VCPU\_CONFIG1 | | | | | reg32 | | 0x09C |
| offset | | 156 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Reserved for Configuration Information | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | RSVD0 | | | ro | ro | | 0x0 | | | Configuration Information #1 (internal use only) | | | | | |

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| 1.1.1.41.0 | | | | | | | | RET\_CODEC\_STD | | | | | reg32 | | 0x0A0 |
| offset | | 160 | external | | |  | | | size | | 32 |  | |  | |
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| Reserved for Configuration Information | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CODEC\_STD | | | ro | ro | | 0x0 | | | General Configuration Information (internal use only) | | | | | |

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| 1.1.1.42.0 | | | | | | | | RET\_CONF\_DATE | | | | | reg32 | | 0x0A4 |
| offset | | 164 | external | | |  | | | size | | 32 |  | |  | |
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| Reserved for Configuration Information | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | HW\_DATE | | | ro | ro | | 0x0 | | | The date that the hardware has been configured in YYYYmmdd in digit (internal use only) | | | | | |

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| 1.1.1.43.0 | | | | | | | | RET\_CONF\_REVISION | | | | | reg32 | | 0x0A8 |
| offset | | 168 | external | | |  | | | size | | 32 |  | |  | |
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| Reserved for Configuration Information | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | HW\_REVISION | | | ro | ro | | 0x0 | | | The revision number when the hardware has been configured (internal use only) | | | | | |

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| 1.1.1.44.0 | | | | | | | | RET\_CONF\_TYPE | | | | | reg32 | | 0x0AC |
| offset | | 172 | external | | |  | | | size | | 32 |  | |  | |
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| Reserved for Configuration Information | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | HW\_TYPE | | | ro | ro | | 0x0 | | | The define value used in hardware configuration (internal use only) | | | | | |

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| 1.1.1.45.0 | | | | | | | | RET\_VCORE0\_CFG | | | | | reg32 | | 0x0B0 |
| offset | | 176 | external | | |  | | | size | | 32 |  | |  | |
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| Reserved for Configuration Information | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CONFIG\_VORE0 | | | ro | ro | | 0x0 | | | The VCORE0 Configuration Information (internal use only) | | | | | |

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| 1.1.1.46.0 | | | | | | | | RET\_VCORE1\_CFG | | | | | reg32 | | 0x0B4 |
| offset | | 180 | external | | |  | | | size | | 32 |  | |  | |
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| Reserved for Configuration Information | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CONFIG\_VORE1 | | | ro | ro | | 0x0 | | | The VCORE1 Configuration Information (internal use only) | | | | | |

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| 1.1.1.47.0 | | | | | | | | RET\_VCORE2\_CFG | | | | | reg32 | | 0x0B8 |
| offset | | 184 | external | | |  | | | size | | 32 |  | |  | |
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| Reserved for Configuration Information | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CONFIG\_VORE2 | | | ro | ro | | 0x0 | | | The VCORE2 Configuration Information (internal use only) | | | | | |

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| 1.1.1.48.0 | | | | | | | | RET\_VCORE3\_CFG | | | | | reg32 | | 0x0BC |
| offset | | 188 | external | | |  | | | size | | 32 |  | |  | |
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| Reserved for Configuration Information | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CONFIG\_VORE3 | | | ro | ro | | 0x0 | | | The VCORE3 Configuration Information (internal use only) | | | | | |

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| 1.1.1.49.0 | | | | | | | | VPU\_RET\_VCORE\_PRESENT | | | | | reg32 | | 0x0C0 |
| offset | | 192 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Number of VCOREs present (turn on cores) | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 3:0 | VCORE\_PRESENT | | | ro | ro | | 0x0 | | | Each bit represnets turn-on VCORE  [0]: VCORE0  [1]: VCORE1  [2]: VCORE2  [3]: VCORE3 | | | | | |

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| 1.1.1.50.0 | | | | | | | | DBG\_MSG\_6 | | | | | reg32 | | 0x0C4 |
| offset | | 196 | external | | |  | | | size | | 32 |  | |  | |
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| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.51.0 | | | | | | | | DBG\_MSG\_7 | | | | | reg32 | | 0x0C8 |
| offset | | 200 | external | | |  | | | size | | 32 |  | |  | |
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| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.52.0 | | | | | | | | DBG\_MSG\_8 | | | | | reg32 | | 0x0CC |
| offset | | 204 | external | | |  | | | size | | 32 |  | |  | |
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| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.54.0 | | | | | | | | DBG\_MSG\_9 | | | | | reg32 | | 0x0D0 |
| offset | | 208 | external | | |  | | | size | | 32 |  | |  | |
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| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.55.0 | | | | | | | | DBG\_MSG\_10 | | | | | reg32 | | 0x0D8 |
| offset | | 216 | external | | |  | | | size | | 32 |  | |  | |
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| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.56.0 | | | | | | | | DBG\_MSG\_11 | | | | | reg32 | | 0x0DC |
| offset | | 220 | external | | |  | | | size | | 32 |  | |  | |
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| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.57.0 | | | | | | | | DBG\_MSG\_12 | | | | | reg32 | | 0x0E0 |
| offset | | 224 | external | | |  | | | size | | 32 |  | |  | |
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| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.58.0 | | | | | | | | DBG\_MSG\_13 | | | | | reg32 | | 0x0E4 |
| offset | | 228 | external | | |  | | | size | | 32 |  | |  | |
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|  | | | | | | | | | | | | | | | |
| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.59.0 | | | | | | | | DBG\_MSG\_14 | | | | | reg32 | | 0x0E8 |
| offset | | 232 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.60.0 | | | | | | | | DBG\_MSG\_15 | | | | | reg32 | | 0x0EC |
| offset | | 236 | external | | |  | | | size | | 32 |  | |  | |
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| Debugging message for HOST | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DBG\_MSG | | | ro | ro | | 0x0 | | | Debugging message | | | | | |

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| 1.1.1.61.0 | | | | | | | | VPU\_DBG\_SW\_UART\_STATUS | | | | | reg32 | | 0x0F0 |
| offset | | 240 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| VPU\_DBG\_SW\_UART\_STATUS | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:4 | RSVD0 | | | ro | ro | | 0x0 | | | Reserved | | | | | |
| 3:0 | VPU\_DBG\_SW\_UART\_STATUS | | | ro | ro | | 0x0 | | | the status of VPU SW\_UART | | | | | |

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| 1.1.1.62.0 | | | | | | | | VPU\_DBG\_SW\_UART\_TX | | | | | reg32 | | 0x0F4 |
| offset | | 244 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| VPU\_DBG\_SW\_UART\_TX | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:4 | RSVD0 | | | ro | ro | | 0x0 | | | Reserved | | | | | |
| 3:0 | VPU\_DBG\_SW\_UART\_TX | | | ro | ro | | 0x0 | | | TX of VPU SW\_UART | | | | | |

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| 1.1.1.63.0 | | | | | | | | VPU\_DBG\_REG\_0 | | | | | reg32 | | 0x0F8 |
| offset | | 248 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| VPU\_DBG\_REG\_0 | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:4 | RSVD0 | | | ro | ro | | 0x0 | | | Reserved | | | | | |
| 3:0 | VPU\_DBG\_REG\_0 | | | ro | ro | | 0x0 | | | Debug register 0 | | | | | |

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| 1.1.1.65.0 | | | | | | | | VPU\_DBG\_REG\_1 | | | | | reg32 | | 0x0FC |
| offset | | 252 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| VPU\_DBG\_REG\_1 | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:4 | RSVD0 | | | ro | ro | | 0x0 | | | Reserved | | | | | |
| 3:0 | VPU\_DBG\_REG\_1 | | | ro | ro | | 0x0 | | | Debug register 1 | | | | | |

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| 1.1.1.67.0 | | | | | | | | VPU\_SUB\_FRAME\_SYNC\_CTRL | | | | | reg32 | | 0x11C |
| offset | | 284 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | ipu\_frame\_row\_cnt | | | ro | ro | | 0x0 | | | Read valid source buffer count (for debugging) | | | | | |
| 15:15 | ipu\_frame\_row\_valid | | | ro | ro | | 0x0 | | | Read valid source buffer validation (for debugging) | | | | | |
| 14:7 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved | | | | | |
| 6:2 | current\_buffer | | | rw | ro | | 0x0 | | | Change current source buffer  Valid only if SUB\_FRAME\_SYNC\_TYPE is 1. | | | | | |
| 1:1 | new\_frame | | | rw | ro | | 0x0 | | | Toggle when new frame start.  Valid only if SUB\_FRAME\_SYNC\_TYPE is 1. | | | | | |
| 0:0 | end\_of\_row | | | rw | ro | | 0x0 | | | Toggle at end of line  Valid only if SUB\_FRAME\_SYNC\_TYPE is 1. | | | | | |

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| 1.1.1.68.0 | | | | | | | | COMMAND | | | | | reg32 | | 0x200 |
| offset | | 512 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Command to run VPU  Depending on the value of command, host interface registers from 0x210 mean different things. | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | COMMAND | | | rw | ro | | 0x0 | | | 0x0001 : INIT\_VPU  0x0002 : WAKE\_VPU  0x0004 : SLEEP\_VPU  0x0008 : CREATE\_INST  0x0010 : FLUSH\_INST  0x0020 : DESTROY\_INST  0x0040 : INIT\_SEQ  0x0080 : SET\_FB  0x0100 : ENC\_PIC / DEC\_PIC  0x0200 : ENC\_SET\_PARAM  0x4000 : QUERY  0x8000 : UPDATE\_BS{has\_reset=0} | | | | | |

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| 1.1.1.73.0 | | | | | | | | CMD\_DEC\_PIC\_OPTION | | | | | reg32 | | 0x204 |
| offset | | 516 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| CMD\_DEC\_PIC\_OPTION{alt\_reg=CMD\_INIT\_SEQ\_OPTION,CMD\_OPTION,CMD\_SET\_FB\_OPTION,CMD\_SET\_PARAM\_OPTION} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:7 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 6:6 | FORCE\_FILM\_GRAIN\_OFF | | | rw | ro | | 0x0 | | | AV1 DEC only  0x0: film grain is not applied to BWB output regardless of syntax  value named "apply\_grain"  0x1: film grain is applied or not to BWB output in accordance  with syntax value named "apply\_grain"{has\_reset=0} | | | | | |
| 5:0 | SKIP\_MODE | | | rw | ro | | 0x0 | | | [HEVC DEC]  0x00: normal DEC\_PIC  0x10: thumbnail mode. It skips non-IRAP pictures w/o registering  reference DPB.  0x11: skip non-IRAP.  0x13: skip non-reference picture.  0x20: handle CRA picture as BLA. It skips RASL pictures followd  by CRA pictures.  [AVC DEC]  0x00: normal DEC\_PIC  0x10: thumbnail mode. It skips non-IRAP pictures w/o registering  reference DPB.  0x11: skip non-IRAP.  0x13: skip non-reference picture.  [VP9 DEC]  0x00: normal DEC\_PIC  0x10: thumbnail mode. It skips non-IRAP pictures w/o registering  reference DPB.  0x11: skip non-key frame.  [AV1 DEC]  0x00: normal DEC\_PIC  0x10: thumbnail mode. It skips non-IRAP pictures w/o registering  reference DPB.  0x11: skip non-key frame.{has\_reset=0} | | | | | |

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| 1.1.1.74.0 | | | | | | | | RET\_SUCCESS | | | | | reg32 | | 0x208 |
| offset | | 520 | external | | |  | | | size | | 32 |  | |  | |
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| Result of the command  If the value is not 0x1, check the reason. | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 1:0 | RUN\_CMD\_STATUS | | | rw | ro | | 0x0 | | | 00: FAIL  01: SUCCESS  10: SUCCESS\_WITH\_WARNING{has\_reset=0} | | | | | |

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| 1.1.1.75.0 | | | | | | | | RET\_FAIL\_REASON | | | | | reg32 | | 0x20C |
| offset | | 524 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Fail reason of the run command | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FAIL\_REASON | | | rw | ro | | 0x0 | | | Please refer to <<wave6\_sys\_error>> which provides error code description.{has\_reset=0} | | | | | |

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| 1.1.1.76.0 | | | | | | | | CMD\_INSTANCE\_INFO | | | | | reg32 | | 0x210 |
| offset | | 528 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Instance information | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | CODEC\_STD | | | rw | ro | | 0x0 | | | Codec standard to run  STD\_HEVC\_DEC = 0x00  STD\_HEVC\_ENC = 0x01  STD\_AVC\_DEC = 0x02  STD\_AVC\_ENC = 0x03  STD\_VP9\_DEC = 0x16  STD\_AV1\_DEC = 0x1A  STD\_AV1\_ENC = 0x1B  {has\_reset=0} | | | | | |
| 15:0 | INST\_ID | | | rw | ro | | 0x0 | | | Instance ID  CREATE\_INSTANCE command returns instance ID through RET\_CREATE\_INSTANCE\_ID register. Then the following commands for this instance uses the intance ID as input.  VPU can encode or decode more than one instance simultaneously. If multiple instances are running, each instance must have its own process index that is assigned by this register. For example, two instances are running simultaneously, the first instance has the process index 0, the second instance has the process index 1. Instance index shall be in the range of 0 to 31, inclusive.{has\_reset=0} | | | | | |

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| 1.1.1.77.0 | | | | | | | | CMD\_QUE\_FULL\_IDC | | | | | reg32 | | 0x214 |
| offset | | 532 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Indicator for which command queue is full. Host can can read this register at any time. Because the reading of this register does not involve interrupt to VCPU, it does not cause any VCPU performance drop. Only valid for CQ FW | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CMD\_QUEUE\_FULLNESS | | | rw | ro | | 0x0 | | | For each bit position i,  - '1' means the command queue for instance i is full.  - '0' means the command queue for instance i is not full.{has\_reset=0} | | | | | |

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| 1.1.1.78.0 | | | | | | | | RET\_QUE\_EMPTY\_IDC | | | | | reg32 | | 0x218 |
| offset | | 536 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Indicator for which command queue is full. Host can can read this register at any time. Because the reading of this register does not involve interrupt to VCPU, it does not cause any VCPU performance drop. Only valid for CQ FW | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | RET\_QUEUE\_EMPTY | | | rw | ro | | 0x0 | | | For each bit position i,  - '1' means the command queue for instance i is empty.  - '0' means the command queue for instance i is not empty.{has\_reset=0} | | | | | |

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| 1.1.1.79.0 | | | | | | | | CMD\_DONE\_INST\_IDC | | | | | reg32 | | 0x21C |
| offset | | 540 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Done interrupt instance idc. Only valid for CQ FW | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | DONE\_INST\_IDC | | | rw | ro | | 0x0 | | | done instance idc for que command{has\_reset=0} | | | | | |

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| 1.1.1.81.0 | | | | | | | | RET\_CREATE\_INSTANCE\_ID | | | | | reg32 | | 0x220 |
| offset | | 544 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| return instance id | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | INSTANCE\_ID | | | rw | ro | | 0x0 | | | return allocation instance id (Valid after create\_instance command){has\_reset=0} | | | | | |

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| 1.1.1.82.0 | | | | | | | | RET\_CMD\_CQ\_IN\_TICK | | | | | reg32 | | 0x23C |
| offset | | 572 | external | | |  | | | size | | 32 |  | |  | |
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| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CMD\_CQ\_IN\_TICK | | | rw | ro | | 0x0 | | | Tick when CMD enters CQ{has\_reset=0} | | | | | |

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| 1.1.1.83.0 | | | | | | | | RET\_CMD\_FW\_RUN\_TICK | | | | | reg32 | | 0x240 |
| offset | | 576 | external | | |  | | | size | | 32 |  | |  | |
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| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CMD\_FW\_RUN\_TICK | | | rw | ro | | 0x0 | | | Tick when CMD comes out of CQ (De-queue){has\_reset=0} | | | | | |

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| 1.1.1.84.0 | | | | | | | | RET\_CMD\_HW\_RUN\_TICK | | | | | reg32 | | 0x244 |
| offset | | 580 | external | | |  | | | size | | 32 |  | |  | |
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| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CMD\_HW\_RUN\_TICK | | | rw | ro | | 0x0 | | | Tick when giving pic\_run from FW to HW{has\_reset=0} | | | | | |

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| 1.1.1.85.0 | | | | | | | | RET\_CMD\_HW\_DONE\_TICK | | | | | reg32 | | 0x248 |
| offset | | 584 | external | | |  | | | size | | 32 |  | |  | |
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| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CMD\_HW\_DONE\_TICK | | | rw | ro | | 0x0 | | | Tick when receiving pic\_done from HW to FW{has\_reset=0} | | | | | |

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| 1.1.1.86.0 | | | | | | | | RET\_CMD\_FW\_DONE\_TICK | | | | | reg32 | | 0x24C |
| offset | | 588 | external | | |  | | | size | | 32 |  | |  | |
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| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CMD\_FW\_DONE\_TICK | | | rw | ro | | 0x0 | | | Tick when report enters RQ{has\_reset=0} | | | | | |

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| 1.1.1.87.0 | | | | | | | | RET\_CMD\_RQ\_OUT\_TICK | | | | | reg32 | | 0x250 |
| offset | | 592 | external | | |  | | | size | | 32 |  | |  | |
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| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CMD\_RQ\_OUT\_TICK | | | rw | ro | | 0x0 | | | Tick when report comes out of RQ{has\_reset=0} | | | | | |

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| 1.1.1.88.0 | | | | | | | | RET\_CMD\_FW\_RRE\_RUN\_TICK | | | | | reg32 | | 0x254 |
| offset | | 596 | external | | |  | | | size | | 32 |  | |  | |
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| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CMD\_FW\_PRE\_RUN\_TICK | | | rw | ro | | 0x0 | | | Tick when CMD comes out of CQ (De-queue){has\_reset=0} | | | | | |

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| 1.1.1.89.0 | | | | | | | | RET\_CMD\_HW\_RRE\_RUN\_TICK | | | | | reg32 | | 0x258 |
| offset | | 600 | external | | |  | | | size | | 32 |  | |  | |
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| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CMD\_HW\_PRE\_RUN\_TICK | | | rw | ro | | 0x0 | | | Tick when giving pre\_run from FW to HW{has\_reset=0} | | | | | |

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| 1.1.1.90.0 | | | | | | | | RET\_CMD\_HW\_RRE\_DONE\_TICK | | | | | reg32 | | 0x25C |
| offset | | 604 | external | | |  | | | size | | 32 |  | |  | |
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| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CMD\_HW\_RRE\_DONE\_TICK | | | rw | ro | | 0x0 | | | Tick when receiving pre\_run done from HW to FW{has\_reset=0} | | | | | |

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| 1.1.1.92.0 | | | | | | | | RET\_CMD\_FW\_RRE\_DONE\_TICK | | | | | reg32 | | 0x260 |
| offset | | 608 | external | | |  | | | size | | 32 |  | |  | |
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| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CMD\_FW\_PRE\_DONE\_TICK | | | rw | ro | | 0x0 | | | Tick when giving pic\_run from FW to Pre HW{has\_reset=0} | | | | | |

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| 1.1.1.102.0 | | | | | | | | CMD\_BS\_RD\_PTR | | | | | reg32 | | 0x300 |
| offset | | 768 | external | | |  | | | size | | 32 |  | |  | |
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| Bitstream buffer read pointer{alt\_reg=CMD\_BS\_RD\_PTR\_DEC\_PIC,CMD\_BS\_START,CMD\_CREATE\_INST\_ADDR\_WORK\_BUF,CMD\_ENC\_SEQ\_SET\_PARAM\_ENABLE,CMD\_SET\_FB\_COMMON\_PIC\_INFO,RET\_DEC\_ADDR\_USERDATA\_BASE,RET\_ENC\_RD\_PTR,RET\_ENC\_RD\_PTR\_QUERY\_ENC\_FW\_STATUS,RET\_QUERY\_ENC\_BS\_RD\_PTR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | RD\_PTR | | | rw | ro | | 0x0 | | | Start address of bitstream for handling current command  Host processor cannot update this register in the middle of decoding. It is only allowed to update this before decoding has started.  VPU also updates this (RET\_ADDR\_BS\_RD\_PTR) with end address of a NAL, when a NAL is decoded.{has\_reset=0} | | | | | |

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| 1.1.1.112.0 | | | | | | | | CMD\_BS\_SIZE | | | | | reg32 | | 0x304 |
| offset | | 772 | external | | |  | | | size | | 32 |  | |  | |
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| Bitstream buffer size{alt\_reg=CMD\_BS\_WR\_PTR,CMD\_BS\_WR\_PTR\_DEC\_PIC,CMD\_CREATE\_INST\_WORK\_BUF\_SIZE,CMD\_ENC\_SEQ\_SRC\_SIZE,CMD\_SET\_FB\_PIC\_SIZE,RET\_DEC\_USERDATA\_SIZE,RET\_ENC\_WR\_PTR,RET\_ENC\_WR\_PTR\_QUERY\_ENC\_FW\_STATUS,RET\_QUERY\_ENC\_BS\_WR\_PTR} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | BS\_BUF\_SIZE | | | rw | ro | | 0x0 | | | Size of bitstream buffer  It should be aligned in bus width (128bit/16 byte), but we highly recommend to be aligned in 4KB{has\_reset=0} | | | | | |

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| 1.1.1.118.0 | | | | | | | | CMD\_BS\_OPTION | | | | | reg32 | | 0x308 |
| offset | | 776 | external | | |  | | | size | | 32 |  | |  | |
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| Bitstream buffer option{alt\_reg=CMD\_BS\_OPTIONS,CMD\_BS\_OPTIONS\_ENC\_PIC,CMD\_ENC\_SEQ\_CUSTOM\_MAP\_ENDIAN,CMD\_SET\_FB\_NUM\_FB,RET\_ENC\_NUM\_REQUIRED\_FB} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:8 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 7:6 | STREAM\_FORMAT | | | rw | ro | | 0x0 | | | Refer. to STREAM\_FORMAT on INIT\_SEQ{has\_reset=0} | | | | | |
| 5:5 | STREAM\_END | | | rw | ro | | 0x0 | | | Refer. to STREAM\_END on INIT\_SEQ{has\_reset=0} | | | | | |
| 4:4 | EXPLICIT\_END | | | rw | ro | | 0x0 | | | Refer. to EXPLICIT\_END on INIT\_SEQ{has\_reset=0} | | | | | |
| 3:0 | BS\_ENDIAN | | | rw | ro | | 0x0 | | | Endianness of bitstream buffer{has\_reset=0} | | | | | |

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| 1.1.1.124.0 | | | | | | | | CMD\_ENC\_SEQ\_PARAM | | | | | reg32 | | 0x30C |
| offset | | 780 | external | | |  | | | size | | 32 |  | |  | |
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| Encoder sequence parameters (MANDATORY){alt\_reg=CMD\_SET\_FB\_FBC\_STRIDE,CMD\_USE\_SEC\_AXI,CMD\_USE\_SEC\_AXI\_ENC\_PIC,RET\_DEC\_BS\_RD\_PTR,RET\_MIN\_SRC\_BUF\_NUM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:31 | USE\_DEFAULT\_SCALING\_LIST | | | rw | ro | | 0x0 | | | It enables to apply default scaling list.{has\_reset=0} | | | | | |
| 30:30 | STILL\_PICTURE | | | rw | ro | | 0x0 | | | Still\_profile indicator (HEVC)  0 : disable still\_profile encoding (default)  1 : enable main/main10\_still\_profile encoding according to bit\_depth{has\_reset=0} | | | | | |
| 29:28 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved  {has\_reset=0} | | | | | |
| 27:27 | USE\_STRONG\_INTRA | | | rw | ro | | 0x0 | | | It enables strong intra smoothing.{has\_reset=0} | | | | | |
| 26:25 | USE\_INTRA\_TRANS\_SKIP | | | rw | ro | | 0x0 | | | It enables transform skip for intra CU.{has\_reset=0} | | | | | |
| 24:24 | USE\_SAO | | | rw | ro | | 0x0 | | | It enables sample adaptive offset. (HEVC)  It enables wiener. (AV1){has\_reset=0} | | | | | |
| 23:23 | USE\_TMVP | | | rw | ro | | 0x0 | | | It enables temporal motion vector prediction. (HEVC)  It enables CDEF. (AV1){has\_reset=0} | | | | | |
| 22:22 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 21:21 | USE\_LONG\_TERM | | | rw | ro | | 0x0 | | | It enables to use longterm reference frame.{has\_reset=0} | | | | | |
| 20:19 | RSVD2 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 18:14 | BIT\_DEPTH | | | rw | ro | | 0x0 | | | Bit depth (8 or 10){has\_reset=0} | | | | | |
| 13:12 | TIER\_IDC | | | rw | ro | | 0x0 | | | A tier indicator (HEVC only)  0 : main  1 : high{has\_reset=0} | | | | | |
| 11:3 | LEVEL\_IDC | | | rw | ro | | 0x0 | | | 0 : VPU decides a proper level value.  Non-0 :host input value determines a level value as below:  For AVC, host inputs the level value 10.  For HEVC, host inputs the level value 30.  e.g.) If you want for the level value to be set as 5, for AVC, input 5\*10 = 50 as host level value. for HEVC, input 5\*30 = 150 as host level value{has\_reset=0} | | | | | |
| 2:0 | PROFILE\_IDC | | | rw | ro | | 0x0 | | | Profile indicator (HEVC only)  0 : VPU decides whether the profile is main or main10 according to bit\_depth.  1 : main  2 : main10  3 : main still picture  (In case of AV1, the profile is always "main". In case of AVC, the profile is decided by VPU according to "USE\_ENTROPY\_CODING\_MODE" and "USE\_TRANSFORM\_8x8"){has\_reset=0} | | | | | |

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| 1.1.1.131.0 | | | | | | | | CMD\_CREATE\_INST\_BS\_PARAM | | | | | reg32 | | 0x310 |
| offset | | 784 | external | | |  | | | size | | 32 |  | |  | |
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| Bitstream buffer option{alt\_reg=CMD\_ENC\_REPORT\_PARAM,CMD\_ENC\_SEQ\_PPS\_PARAM,CMD\_SEQ\_CHANGE\_ENABLE\_FLAG,CMD\_SET\_FB\_ADDR\_LUMA\_BASE0,RET\_DEC\_SEQ\_PARAM,RET\_ENC\_PIC\_TYPE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:6 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 5:4 | BS\_MODE | | | rw | ro | | 0x0 | | | 0x0: Line buffer mode{has\_reset=0} | | | | | |
| 3:0 | BS\_ENDIAN | | | rw | ro | | 0x0 | | | Endianness of bitstream buffer{has\_reset=0} | | | | | |

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| 1.1.1.136.0 | | | | | | | | CMD\_DEC\_SEI\_MASK | | | | | reg32 | | 0x314 |
| offset | | 788 | external | | |  | | | size | | 32 |  | |  | |
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| User data dump option{alt\_reg=CMD\_ENC\_SEQ\_GOP\_PARAM,CMD\_SET\_FB\_ADDR\_CB\_BASE0,RET\_DEC\_COLOR\_SAMPLE\_INFO,RET\_ENC\_PIC\_POC} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:17 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 16:16 | SUFFIX\_SEI\_COLOUR\_REAMPPING\_INFO | | | rw | ro | | 0x0 | | | HEVC : Enable to report colour\_remapping\_ info( ) PREFIX\_SEI message.  AVC : Enable to report colour\_remapping\_ info( ) SEI message.{has\_reset=0} | | | | | |
| 15:15 | PREFIX\_SEI\_CONTENT\_LIGHT\_LEVEL\_INFO | | | rw | ro | | 0x0 | | | HEVC : Enable to report content\_light\_level\_ info( ) PREFIX\_SEI message.  AVC : Reserved{has\_reset=0} | | | | | |
| 14:14 | PREFIX\_SEI\_FILM\_GRAIN\_CHARACTERISTICS\_INFO | | | rw | ro | | 0x0 | | | HEVC : Enable to report film\_grain\_ characteristics\_ info() message.  AVC : Enable to report film\_grain\_ characteristics\_ info() message.{has\_reset=0} | | | | | |
| 13:13 | PREFIX\_SEI\_TONE\_MAPPING\_INFO | | | rw | ro | | 0x0 | | | HEVC : Enable to report tone\_mapping\_info PREFIX\_SEI message.  AVC : Enable to report tone\_mapping\_info SEI message.{has\_reset=0} | | | | | |
| 12:12 | PREFIX\_SEI\_KNEE\_FUNCTION\_INFO | | | rw | ro | | 0x0 | | | HEVC : Enable to report knee\_function\_ info( ) PREFIX\_SEI message.  AVC : Reserved{has\_reset=0} | | | | | |
| 11:11 | PREFIX\_SEI\_CHROMA\_RESAMPLING\_FILTER\_HINT | | | rw | ro | | 0x0 | | | HEVC : Enable to report chroma\_ resampling\_filter\_ hint( ) PREFIX\_SEI message.  AVC : Reserved{has\_reset=0} | | | | | |
| 10:10 | PREFIX\_SEI\_MASTERING\_DISPLAY\_COLOUR\_VOLUME | | | rw | ro | | 0x0 | | | HEVC : Enable to report mastering\_display\_ colour\_volume( ) PREFIX\_SEI message.  AVC : Reserved{has\_reset=0} | | | | | |
| 9:9 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 8:8 | SUFFIX\_SEI\_USER\_DATA\_UNREGISTERED | | | rw | ro | | 0x0 | | | HEVC : Enable to report user\_data\_ unregistered( ) SUFFIX\_SEI message.  AVC : Reserved{has\_reset=0} | | | | | |
| 7:7 | SUFFIX\_SEI\_USER\_DATA\_REGISTERED\_ITU\_T\_T35\_0 | | | rw | ro | | 0x0 | | | HEVC : Enable to report the 1st user\_data\_ registered\_itu\_t\_ t35( ) SUFFIX\_SEI message.  AVC : Reserved{has\_reset=0} | | | | | |
| 6:6 | PREFIX\_SEI\_USER\_DATA\_UNREGISTERED | | | rw | ro | | 0x0 | | | HEVC : Enable to report user\_data\_ unregistered( ) PREFIX\_SEI message.  AVC : Enable to report user\_data\_unregistered() SEI message{has\_reset=0} | | | | | |
| 5:5 | PREFIX\_SEI\_USER\_DATA\_REGISTERED\_ITU\_T\_T35\_0 | | | rw | ro | | 0x0 | | | HEVC : Enable to report the 1st user\_data\_ registered\_itu\_t\_ t35( ) PREFIX\_SEI message.  AVC : Enable to report the user\_data\_registered\_itu\_t\_t35() SEI message{has\_reset=0} | | | | | |
| 4:4 | PREFIX\_SEI\_PIC\_TIMING | | | rw | ro | | 0x0 | | | HEVC : Enable to report pic\_timing( ) PREFIX\_SEI message.  AVC : Enable to report pic\_timing( ) SEI message.{has\_reset=0} | | | | | |
| 3:3 | RSVD2 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 2:2 | REPORT\_VUI | | | rw | ro | | 0x0 | | | HEVC : Enable to report VUI.  AVC : Enable to report VUI{has\_reset=0} | | | | | |
| 1:0 | RSVD3 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |

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| 1.1.1.145.0 | | | | | | | | CMD\_CREATE\_ADDR\_EXT | | | | | reg32 | | 0x318 |
| offset | | 792 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_CREATE\_ADDR\_EXT{alt\_reg=CMD\_DEC\_TEMPORAL\_ID\_PLUS1,CMD\_ENC\_MV\_HISTO\_CLASS0,CMD\_ENC\_SEQ\_INTRA\_PARAM,CMD\_ENC\_SEQ\_INTRA\_PARAM\_AVC,CMD\_SET\_FB\_ADDR\_CR\_BASE0,CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET0,RET\_DEC\_ASPECT\_RATIO,RET\_ENC\_PIC\_IDX} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:8 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 7:0 | EXT\_ADDR | | | rw | ro | | 0x0 | | | Primary AXI address extension{has\_reset=0} | | | | | |

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| 1.1.1.151.0 | | | | | | | | CMD\_DEC\_FORCE\_FB\_LATENCY\_PLUS1 | | | | | reg32 | | 0x31C |
| offset | | 796 | external | | |  | | | size | | 32 |  | |  | |
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| User define display latency{alt\_reg=CMD\_ENC\_MV\_HISTO\_CLASS1,CMD\_ENC\_SEQ\_CONF\_WIN\_TOP\_BOT,CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET0,RET\_DEC\_BIT\_RATE,RET\_ENC\_PIC\_SLICE\_NUM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 4:0 | USER\_DEF\_DISP\_LATENCY\_PLUS1 | | | rw | ro | | 0x0 | | | Change frame buffer display latency by force.  0x0 : not used  0x1~0x1f : latency + 1 (if this is set to 1, that means latency is 0 - immediate out){has\_reset=0} | | | | | |

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| 1.1.1.156.0 | | | | | | | | CMD\_ENC\_CUSTOM\_MAP\_OPTION\_PARAM | | | | | reg32 | | 0x320 |
| offset | | 800 | external | | |  | | | size | | 32 |  | |  | |
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| Custom map parameters{alt\_reg=CMD\_ENC\_SEQ\_CONF\_WIN\_LEFT\_RIGHT,CMD\_SET\_FB\_ADDR\_COL0,RET\_DEC\_FRAME\_RATE\_NR,RET\_ENC\_PIC\_SKIP} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:2 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 1:1 | USE\_CTU\_FORCE\_MODE\_FLAG | | | rw | ro | | 0x0 | | | It enables to force intra or, force skip in block unit.{has\_reset=0} | | | | | |
| 0:0 | USE\_QP\_MAP\_FLAG | | | rw | ro | | 0x0 | | | It enables to use QP map.{has\_reset=0} | | | | | |

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| 1.1.1.161.0 | | | | | | | | CMD\_ENC\_CUSTOM\_MAP\_OPTION\_ADDR | | | | | reg32 | | 0x324 |
| offset | | 804 | external | | |  | | | size | | 32 |  | |  | |
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| Custom map address{alt\_reg=CMD\_ENC\_SEQ\_RDO\_PARAM,CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE0,RET\_DEC\_FRAME\_RATE\_DR,RET\_ENC\_PIC\_NUM\_INTRA} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CUSTOM\_MAP\_OPTION\_ADDR | | | rw | ro | | 0x0 | | | Address of custom map{has\_reset=0} | | | | | |

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| 1.1.1.165.0 | | | | | | | | CMD\_ENC\_SEQ\_SLICE\_PARAM | | | | | reg32 | | 0x328 |
| offset | | 808 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Slice parameters{alt\_reg=CMD\_SET\_FB\_ADDR\_LUMA\_BASE1,RET\_DEC\_NUM\_REQURED\_FB,RET\_ENC\_PIC\_NUM\_MERGE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:3 | ARGUMENT | | | rw | ro | | 0x0 | | | It specifies a size of slice (2^29 - 1)  The number of CTU in case of SLICE\_MODE = 1{has\_reset=0} | | | | | |
| 2:0 | SLICE\_MODE | | | rw | ro | | 0x0 | | | A slice mode  0 - Single slice  1 - CTU based slice  2 - ROW based Slice{has\_reset=0} | | | | | |

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| 1.1.1.170.0 | | | | | | | | CMD\_ENC\_SEQ\_INTRA\_REFRESH | | | | | reg32 | | 0x32C |
| offset | | 812 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Intra refresh mode{alt\_reg=CMD\_ENC\_SRC\_PIC\_IDX,CMD\_SET\_FB\_ADDR\_CB\_BASE1,RET\_DEC\_NUM\_REORDER\_DELAY,RET\_ENC\_PIC\_NON\_REF\_PIC\_FLAG} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | INTRA\_REFRESH\_ARGUMENT | | | rw | ro | | 0x0 | | | It specifies an intra CTU refresh interval. Depending on intraRefreshMode, it can mean one of the followings:  The number of consecutive CTU rows for IntraCtuRefreshMode of 1  The number of consecutive CTU columns for IntraCtuRefreshMode of 2  A step size in CTU for IntraCtuRefreshMode of 3  The number of Intra CTUs to be encoded in a picture for IntraCtuRefreshMode of 4{has\_reset=0} | | | | | |
| 15:3 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 2:0 | INTRA\_REFRESH\_MODE | | | rw | ro | | 0x0 | | | An intra refresh mode  0 : No intra refresh  1 : Row  2 : Column  3 : A step size in CTU{has\_reset=0} | | | | | |

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| 1.1.1.177.0 | | | | | | | | CMD\_CREATE\_INST\_CORE\_INFO | | | | | reg32 | | 0x330 |
| offset | | 816 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| CMD\_CREATE\_INST\_CORE\_INFO{alt\_reg=CMD\_ENC\_SEQ\_INTRA\_MIN\_MAX\_QP,CMD\_ENC\_SRC\_ADDR\_Y,CMD\_SET\_FB\_ADDR\_CR\_BASE1,CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET1,RET\_DEC\_SUB\_LAYER\_INFO,RET\_ENC\_PIC\_NUM\_SKIP} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:11 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 10:8 | SET\_CQ\_DEPTH | | | rw | ro | | 0x0 | | | Set command queue depth  Minimum : 1  Maximim : 6  Default : 4{has\_reset=0} | | | | | |
| 7:4 | CORE\_IDC | | | rw | ro | | 0x0 | | | Core indicator to be used for the instance.  0 : Firmware allocates a core idc for the instance. (default)  1 : Core 0 is used for the instance when NUM\_CORE is 1. (only valid for dual core products)  2 : Core 1 is used for the instance when NUM\_CORE is 1. (only valid for dual core products){has\_reset=0} | | | | | |
| 3:0 | NUM\_CORE | | | rw | ro | | 0x0 | | | Number of cores to be used for the instance.  0 : N/A  1 : Use single-core.  2 : Use dual-cores (a frame parallel processing is used.){has\_reset=0} | | | | | |

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| 1.1.1.183.0 | | | | | | | | CMD\_CREATE\_INST\_PRIORITY | | | | | reg32 | | 0x334 |
| offset | | 820 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| CMD\_CREATE\_INST\_PRIORITY{alt\_reg=CMD\_ENC\_SEQ\_RC\_FRAME\_RATE,CMD\_ENC\_SRC\_ADDR\_U,CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET1,RET\_DEC\_NOTIFICATION,RET\_ENC\_PIC\_AVG\_CTU\_QP} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:9 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 8:8 | SECURITY\_FLAG | | | rw | ro | | 0x0 | | | security flag (0: non-secure instance / 1: secure instance) - AXI AxProt[1] bit is set to an inverted value.{has\_reset=0} | | | | | |
| 7:5 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 4:0 | PRIORITY\_VALUE | | | rw | ro | | 0x0 | | | priority value (low priority 0~31 high priority){has\_reset=0} | | | | | |

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| 1.1.1.188.0 | | | | | | | | CMD\_ENC\_SEQ\_RC\_TARGET\_RATE | | | | | reg32 | | 0x338 |
| offset | | 824 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_RC\_TARGET\_RATE{alt\_reg=CMD\_ENC\_SRC\_ADDR\_V,CMD\_SET\_FB\_ADDR\_COL1,RET\_DEC\_USERDATA\_IDC,RET\_ENC\_PIC\_BYTE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | RC\_TARGET\_RATE | | | rw | ro | | 0x0 | | | A target bitrate for for rate control{has\_reset=0} | | | | | |

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| 1.1.1.193.0 | | | | | | | | CMD\_ENC\_SEQ\_RC\_PARAM | | | | | reg32 | | 0x33C |
| offset | | 828 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| CMD\_ENC\_SEQ\_RC\_PARAM{alt\_reg=CMD\_ENC\_SRC\_STRIDE,CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE1,RET\_DEC\_PIC\_SIZE,RET\_ENC\_GOP\_PIC\_IDX} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:24 | RC\_UPDATE\_SPEED | | | rw | ro | | 0x0 | | | rc update speed{has\_reset=0} | | | | | |
| 23:20 | RC\_INITIAL\_LEVEL | | | rw | ro | | 0x0 | | | initial rc buffer level{has\_reset=0} | | | | | |
| 19:14 | RC\_INITIAL\_QP | | | rw | ro | | 0x0 | | | An initial QP  If this value is smaller than 0 or larger than 51, firmware decides the initial QP.  [NOTE] This parameter cannot be changed within the same sequence.�{has\_reset=0} | | | | | |
| 13:13 | RC\_MODE | | | rw | ro | | 0x0 | | | Rate control mode  0 : VBR  1 : CBR{has\_reset=0} | | | | | |
| 12:7 | PIC\_RC\_MAX\_DELTA\_QP | | | rw | ro | | 0x0 | | | Max delta QP for picture level RC{has\_reset=0} | | | | | |
| 6:2 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 1:1 | EN\_CU\_LEVEL\_RC | | | rw | ro | | 0x0 | | | It enables CU level rate control.  [NOTE] This parameter cannot be changed within the same sequence.{has\_reset=0} | | | | | |
| 0:0 | EN\_RATE\_CONTROL | | | rw | ro | | 0x0 | | | It enables rate control.  [NOTE] This parameter cannot be changed within the same sequence.{has\_reset=0} | | | | | |

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| 1.1.1.198.0 | | | | | | | | CMD\_ENC\_SEQ\_HVS\_PARAM | | | | | reg32 | | 0x340 |
| offset | | 832 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_HVS\_PARAM{alt\_reg=CMD\_ENC\_SRC\_FORMAT,CMD\_SET\_FB\_ADDR\_LUMA\_BASE2,RET\_DEC\_CROP\_TOP\_BOTTOM,RET\_ENC\_USED\_SRC\_IDX} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:18 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 17:12 | HVS\_MAX\_DELTA\_QP | | | rw | ro | | 0x0 | | | Specifies maximum delta QP from CTU QP. (only valid when CULevelRateControl is 1.) (0 ~ 12){has\_reset=0} | | | | | |
| 11:4 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 3:0 | HVS\_QP\_SCALE | | | rw | ro | | 0x0 | | | Specifies the scale for CU QP derivation. Only available when EnHvsQp is 1. (1 ~ 4){has\_reset=0} | | | | | |

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| 1.1.1.202.0 | | | | | | | | CMD\_ENC\_SEQ\_RC\_MAX\_BITRATE | | | | | reg32 | | 0x344 |
| offset | | 836 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_RC\_MAX\_BITRATE{alt\_reg=CMD\_SET\_FB\_ADDR\_CB\_BASE2,RET\_DEC\_CROP\_LEFT\_RIGHT,RET\_ENC\_PIC\_NUM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | RC\_MAX\_BITRATE | | | rw | ro | | 0x0 | | | A maximum bitrate for for rate control{has\_reset=0} | | | | | |

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| 1.1.1.209.0 | | | | | | | | CMD\_CREATE\_INST\_ADDR\_TEMP\_BASE | | | | | reg32 | | 0x348 |
| offset | | 840 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
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| Temporal buffer base address{alt\_reg=CMD\_ENC\_SEQ\_RC\_VBV\_BUFFER\_SIZE,CMD\_ENC\_SRC\_AXI\_SEL,CMD\_SET\_FB\_ADDR\_CR\_BASE2,CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET2,RET\_DEC\_AU\_START\_POS,RET\_ENC\_VCL\_NUT} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | TEMP\_BUF\_BASE | | | rw | ro | | 0x0 | | | Base address of temporal buffer for this frame  [NOTE] Each V-CORE should set this field for its own temporal buffer.{has\_reset=0} | | | | | |

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| 1.1.1.215.0 | | | | | | | | CMD\_CREATE\_INST\_TEMP\_SIZE | | | | | reg32 | | 0x34C |
| offset | | 844 | external | | |  | | | size | | 32 |  | |  | |
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| Temporal buffer size{alt\_reg=CMD\_ENC\_CODE\_OPTION,CMD\_ENC\_SEQ\_INTER\_MIN\_MAX\_QP,CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET2,RET\_DEC\_AU\_END\_POS,RET\_ENC\_PIC\_PADD\_BYTE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | TEMP\_BUF\_SIZE | | | rw | ro | | 0x0 | | | Temporal buffer size for a frame{has\_reset=0} | | | | | |

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| 1.1.1.221.0 | | | | | | | | CMD\_CREATE\_INST\_ADDR\_SEC\_AXI | | | | | reg32 | | 0x350 |
| offset | | 848 | external | | |  | | | size | | 32 |  | |  | |
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| Secondary AXI base address  It is valid when USE\_SEC\_AXI is not 0. {alt\_reg=CMD\_ENC\_PIC\_PARAM,CMD\_ENC\_SEQ\_ROT\_PARAM,CMD\_SET\_FB\_ADDR\_COL2,RET\_DEC\_PIC\_TYPE,RET\_ENC\_PIC\_DIST\_LOW} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SEC\_AXI\_BASE | | | rw | ro | | 0x0 | | | The base address of secondary AXI memory{has\_reset=0} | | | | | |

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| 1.1.1.227.0 | | | | | | | | CMD\_CREATE\_INST\_SEC\_AXI\_SIZE | | | | | reg32 | | 0x354 |
| offset | | 852 | external | | |  | | | size | | 32 |  | |  | |
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| Seconary AXI memory size  It is valid when USE\_SEC\_AXI is not 0. {alt\_reg=CMD\_ENC\_LONGTERM\_PIC,CMD\_ENC\_SEQ\_NUM\_UNITS\_IN\_TICK,CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE2,RET\_DEC\_PIC\_POC,RET\_ENC\_PIC\_DIST\_HIGH} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SEC\_AXI\_MEM\_SIZE | | | rw | ro | | 0x0 | | | The size of secondary AXI temporal buffer{has\_reset=0} | | | | | |

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| 1.1.1.233.0 | | | | | | | | CMD\_CREATE\_INST\_ADDR\_AR\_TABLE | | | | | reg32 | | 0x358 |
| offset | | 856 | external | | |  | | | size | | 32 |  | |  | |
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| adaptive roud base address{alt\_reg=CMD\_ENC\_PREFIX\_SEI\_NAL\_ADDR,CMD\_ENC\_SEQ\_TIME\_SCALE,CMD\_SET\_FB\_ADDR\_LUMA\_BASE3,RET\_DEC\_RECOVERY\_POINT,RET\_ENC\_MAX\_LATENCY\_PICTURES} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | AR\_TABLE\_BASE | | | rw | ro | | 0x0 | | | The base address of adaptive round table{has\_reset=0} | | | | | |

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| 1.1.1.237.0 | | | | | | | | CMD\_ENC\_PREFIX\_SEI\_INFO | | | | | reg32 | | 0x35C |
| offset | | 860 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_PREFIX\_SEI\_INFO{alt\_reg=CMD\_ENC\_SEQ\_NUM\_TICKS\_POC\_DIFF\_ONE,CMD\_SET\_FB\_ADDR\_CB\_BASE3,RET\_DEC\_DEBUG\_INDEX} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | NAL\_SIZE | | | rw | ro | | 0x0 | | | The total byte size of the prefix SEI (Max. size = 4096){has\_reset=0} | | | | | |
| 15:1 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 0:0 | NAL\_ENABLE | | | rw | ro | | 0x0 | | | It enables to encode the prefix SEI NAL which is given by host.  HEVC: prefix sei  AVC: sei  AV1: metadata{has\_reset=0} | | | | | |

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| 1.1.1.242.0 | | | | | | | | CMD\_ENC\_SUFFIX\_SEI\_NAL\_ADDR | | | | | reg32 | | 0x360 |
| offset | | 864 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SUFFIX\_SEI\_NAL\_ADDR{alt\_reg=CMD\_SET\_FB\_ADDR\_CR\_BASE3,CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET3,RET\_DEC\_DECODED\_INDEX,RET\_ENC\_HISTO\_CNT\_0} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SUFFIX\_SEI\_NAL\_ADDR | | | rw | ro | | 0x0 | | | The base address of the SUFFIX SEI NAL buffer (Big endian){has\_reset=0} | | | | | |

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| 1.1.1.246.0 | | | | | | | | CMD\_ENC\_SUFFIX\_SEI\_INFO | | | | | reg32 | | 0x364 |
| offset | | 868 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SUFFIX\_SEI\_INFO{alt\_reg=CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET3,RET\_DEC\_DISPLAY\_INDEX,RET\_ENC\_HISTO\_CNT\_1} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | NAL\_SIZE | | | rw | ro | | 0x0 | | | The total byte size of the suffix SEI (Max. size = 4096){has\_reset=0} | | | | | |
| 15:1 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 0:0 | NAL\_ENABLE | | | rw | ro | | 0x0 | | | It enables to encode the suffix SEI NAL which is given by host. (HEVC - suffix sei){has\_reset=0} | | | | | |

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| 1.1.1.249.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_COL3 | | | | | reg32 | | 0x368 |
| offset | | 872 | external | | |  | | | size | | 32 |  | |  | |
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| Info base of index 3{alt\_reg=RET\_DEC\_REALLOC\_INDEX,RET\_ENC\_HISTO\_CNT\_2} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | COL\_BASE3 | | | rw | ro | | 0x0 | | | Codec dedicated information buffer for encoding/decoding  HEVC/AVC: MV COL  AV1 : CDF{has\_reset=0} | | | | | |

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| 1.1.1.253.0 | | | | | | | | CMD\_ENC\_SEQ\_BG\_PARAM | | | | | reg32 | | 0x36C |
| offset | | 876 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_BG\_PARAM{alt\_reg=CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE3,RET\_DEC\_DISP\_IDC,RET\_ENC\_HISTO\_CNT\_3} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:30 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 29:24 | BG\_DELTA\_QP | | | rw | ro | | 0x0 | | | It specifies the difference between the lambda QP value of background and the lambda QP value of foreground. (-16 ~ 15){has\_reset=0} | | | | | |
| 23:18 | RSVD1 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 17:10 | BG\_TH\_MEAN\_DIFF | | | rw | ro | | 0x0 | | | It specifies the threshold of mean difference that is used in s2me block. It is valid when background detection is on. (0 ~ 255){has\_reset=0} | | | | | |
| 9:1 | BG\_TH\_MAX\_DIFF | | | rw | ro | | 0x0 | | | It specifies the threshold of max difference that is used in s2me block. It is valid when background detection is on. (0 ~ 255){has\_reset=0} | | | | | |
| 0:0 | EN\_BG\_DETECT | | | rw | ro | | 0x0 | | | It enables background detection.{has\_reset=0} | | | | | |

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| 1.1.1.257.0 | | | | | | | | CMD\_ENC\_SEQ\_NON\_VCL\_PARAM | | | | | reg32 | | 0x370 |
| offset | | 880 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_NON\_VCL\_PARAM{alt\_reg=CMD\_SET\_FB\_ADDR\_LUMA\_BASE4,RET\_DEC\_NUM\_ERR\_CTB,RET\_ENC\_HISTO\_CNT\_4} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:18 | HRD\_RBSP\_SIZE | | | rw | ro | | 0x0 | | | The bit length of HRD RBSP data (Big endian) (HEVC) (Max size=4096){has\_reset=0} | | | | | |
| 17:4 | VUI\_RBSP\_SIZE | | | rw | ro | | 0x0 | | | The bit length of VUI RBSP data (Big endian) (HEVC, AVC) (Max size=4096){has\_reset=0} | | | | | |
| 3:3 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 2:2 | ENCODE\_HRD\_RBSP | | | rw | ro | | 0x0 | | | A flag to encode the HRD syntax RBSP which is given by host into VPS{has\_reset=0} | | | | | |
| 1:1 | ENCODE\_VUI\_RBSP | | | rw | ro | | 0x0 | | | A flag to encode the VUI syntax RBSP which is given by host{has\_reset=0} | | | | | |
| 0:0 | ENCODE\_AUD | | | rw | ro | | 0x0 | | | A flag to encode the AUD NAL (HEVC, AVC){has\_reset=0} | | | | | |

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| 1.1.1.261.0 | | | | | | | | CMD\_ENC\_CSC\_COEFF\_0 | | | | | reg32 | | 0x374 |
| offset | | 884 | external | | |  | | | size | | 32 |  | |  | |
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| RGB to YUV color space conversion coefficient register  Coef and offset values can be freely set through the registers below.  However, we guarantee only for the 4 format mentioned below.  Y = ry\_coef\*R + gy\_coef\*G + by\_coef\*B + y offset  Cb = rcb\_coef\*R + rcb\_coef\*G + gcb\_coef\*B + cb offset  Cr = rcr\_coef\*R + gcr\_coef\*G + bcr\_coef\*B + cr offset  {alt\_reg=CMD\_ENC\_SEQ\_VUI\_RBSP\_ADDR,CMD\_SET\_FB\_ADDR\_CB\_BASE4,RET\_ENC\_NUM\_TILE\_COL} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:30 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 29:20 | CSC\_Coeff\_RY | | | rw | ro | | 0x0 | | | range : -512 ~511  examples:  BT.601 : 10'h0x99  BT.601 Studio Swing : 10'h0x84  BT.709 : 10'h0x6d  BT.2020 : 10'h0x87{has\_reset=0} | | | | | |
| 19:10 | CSC\_Coeff\_GY | | | rw | ro | | 0x0 | | | range : -512 ~511  examples:  BT.601 : 10'h0x12d  BT.601 Studio Swing : 10'h0x102  BT.709 : 10'h0x16e  BT.2020 : 10'h0x15b{has\_reset=0} | | | | | |
| 9:0 | CSC\_Coeff\_BY | | | rw | ro | | 0x0 | | | range : -512 ~511  examples:  BT.601 : 10'h0x3A  BT.601 Studio Swing : 10'h0x32  BT.709 : 10'h0x25  BT.2020 : 10'h0x1e{has\_reset=0} | | | | | |

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| 1.1.1.266.0 | | | | | | | | CMD\_ENC\_CSC\_COEFF\_1 | | | | | reg32 | | 0x378 |
| offset | | 888 | external | | |  | | | size | | 32 |  | |  | |
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| RGB to YUV color space conversion coefficient register  {alt\_reg=CMD\_ENC\_SEQ\_HRD\_RBSP\_ADDR,CMD\_SET\_FB\_ADDR\_CR\_BASE4,CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET4,RET\_ENC\_NUM\_TILE\_ROW} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:30 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 29:20 | CSC\_Coeff\_RCB | | | rw | ro | | 0x0 | | | range : -512 ~511  examples:  BT.601 : 10'h0x3aa  BT.601 Studio Swing : 10'h0x3b4  BT.709 : 10'h0x3c5  BT.2020 : 10'h0x3b9{has\_reset=0} | | | | | |
| 19:10 | CSC\_Coeff\_GCB | | | rw | ro | | 0x0 | | | range : -512 ~511  examples:  BT.601 : 10'h0x356  BT.601 Studio Swing : 10'h0x36c  BT.709 : 10'h0x33b  BT.2020 : 10'h0x347{has\_reset=0} | | | | | |
| 9:0 | CSC\_Coeff\_BCB | | | rw | ro | | 0x0 | | | range : -512 ~511  examples:  BT.601 : 10'h0x100  BT.601 Studio Swing : 10'h0x0e0  BT.709 : 10'h0x100  BT.2020 : 10'h0x100{has\_reset=0} | | | | | |

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| 1.1.1.269.0 | | | | | | | | CMD\_ENC\_CSC\_COEFF\_2 | | | | | reg32 | | 0x37C |
| offset | | 892 | external | | |  | | | size | | 32 |  | |  | |
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| RGB to YUV color space conversion coefficient register  {alt\_reg=CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET4,RET\_ENC\_PIC\_WIDTH} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:30 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 29:20 | CSC\_Coeff\_RCR | | | rw | ro | | 0x0 | | | range : -512 ~511  examples:  BT.601 : 10'h0x100  BT.601 Studio Swing : 10'h0x0e0  BT.709 : 10'h0x100  BT.2020 : 10'h0x100{has\_reset=0} | | | | | |
| 19:10 | CSC\_Coeff\_GCR | | | rw | ro | | 0x0 | | | range : -512 ~511  examples:  BT.601 : 10'h0x32a  BT.601 Studio Swing : 10'h0x344  BT.709 : 10'h0x317  BT.2020 : 10'h0x315{has\_reset=0} | | | | | |
| 9:0 | CSC\_Coeff\_BCR | | | rw | ro | | 0x0 | | | range : -512 ~511  examples:  BT.601 : 10'h0x3d6  BT.601 Studio Swing : 10'h0x3dc  BT.709 : 10'h0x3e9  BT.2020 : 10'h0x3eb{has\_reset=0} | | | | | |

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| 1.1.1.273.0 | | | | | | | | CMD\_ENC\_CSC\_COEFF\_3 | | | | | reg32 | | 0x380 |
| offset | | 896 | external | | |  | | | size | | 32 |  | |  | |
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| RGB to YUV color space conversion coefficient register{alt\_reg=CMD\_ENC\_SEQ\_QROUND\_OFFSET,CMD\_SET\_FB\_ADDR\_COL4,ENC\_PIC\_HEIGHT} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:30 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 29:20 | CSC\_Offset\_Y | | | rw | ro | | 0x0 | | | range: 0 ~ 1023  examples:  BT.601 : 10'h0x0  BT.601 Studio Swing : (bit\_depth != 8) ? 10'h0x40 : 10'h0x10  BT.709 : 10'h0x0  BT.2020 : 10'h0x0{has\_reset=0} | | | | | |
| 19:10 | CSC\_Offset\_Cb | | | rw | ro | | 0x0 | | | range: 0 ~ 1023  examples:  BT.601 : (bit\_depth != 8) ? 10'h0x200 : 10'h0x80  BT.601 Studio Swing : (bit\_depth != 8) ? 10'h0x200 : 10'h0x80  BT.709 : (bit\_depth != 8) ? 10'h0x200 : 10'h0x80  BT.2020 : (bit\_depth != 8) ? 10'h0x200 : 10'h0x80{has\_reset=0} | | | | | |
| 9:0 | CSC\_Offset\_Cr | | | rw | ro | | 0x0 | | | range: 0 ~ 1023  examples:  BT.601 : (bit\_depth != 8) ? 10'h0x200 : 10'h0x80  BT.601 Studio Swing : (bit\_depth != 8) ? 10'h0x200 : 10'h0x80  BT.709 : (bit\_depth != 8) ? 10'h0x200 : 10'h0x80  BT.2020 : (bit\_depth != 8) ? 10'h0x200 : 10'h0x80{has\_reset=0} | | | | | |

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| 1.1.1.275.0 | | | | | | | | CMD\_ENC\_SEQ\_QUANT\_PARAM\_0 | | | | | reg32 | | 0x384 |
| offset | | 900 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_QUANT\_PARAM\_0{alt\_reg=CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE4} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:24 | DELTA\_QP\_U\_DC | | | rw | ro | | 0x0 | | | It specifies the AV1 Qindex offset for DC of Cb component. (-64 ~ 63){has\_reset=0} | | | | | |
| 23:16 | DELTA\_QP\_V\_DC | | | rw | ro | | 0x0 | | | It specifies the AV1 Qindex offset for DC of Cr component. (-64 ~ 63){has\_reset=0} | | | | | |
| 15:8 | DELTA\_QP\_U\_AC | | | rw | ro | | 0x0 | | | It specifies the AV1 Qindex offset for AC of Cb component. (-64 ~ 63){has\_reset=0} | | | | | |
| 7:0 | DELTA\_QP\_V\_AC | | | rw | ro | | 0x0 | | | It specifies the AV1 Qindex offset for AC of Cr component. (-64 ~ 63){has\_reset=0} | | | | | |

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| 1.1.1.277.0 | | | | | | | | CMD\_ENC\_SEQ\_QUANT\_PARAM\_1 | | | | | reg32 | | 0x388 |
| offset | | 904 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_QUANT\_PARAM\_1{alt\_reg=CMD\_SET\_FB\_ADDR\_LUMA\_BASE5} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:20 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 19:14 | LAMBDA\_DELTA\_QP\_INTER | | | rw | ro | | 0x0 | | | It specifies a lambda delta QP for inter pictures. (-32 ~ 31){has\_reset=0} | | | | | |
| 13:8 | LAMBDA\_DELTA\_QP\_INTRA | | | rw | ro | | 0x0 | | | It specifies a lambda delta QP for intra pictures. (-32 ~ 31){has\_reset=0} | | | | | |
| 7:0 | DELTA\_QP\_Y\_DC | | | rw | ro | | 0x0 | | | It specifies the AV1 Qindex offset for Luma DC. (-64 ~ 63){has\_reset=0} | | | | | |

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| 1.1.1.279.0 | | | | | | | | CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PARAM | | | | | reg32 | | 0x38C |
| offset | | 908 | external | | |  | | | size | | 32 |  | |  | |
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| Size of source pictures of custom GOP{alt\_reg=CMD\_SET\_FB\_ADDR\_CB\_BASE5} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:5 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 4:0 | CUSTOM\_GOP\_SIZE | | | rw | ro | | 0x0 | | | The size of cyclic GOP (1 ~ 8)  This should be the same as the number of CUSTOM\_GOP\_PIC\_PARAM set by host{has\_reset=0} | | | | | |

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| 1.1.1.282.0 | | | | | | | | CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_0 | | | | | reg32 | | 0x390 |
| offset | | 912 | external | | |  | | | size | | 32 |  | |  | |
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| Parameters for the 0th picture of custom GOP (MANDATORY with CUSTOM\_GOP\_SIZE){alt\_reg=CMD\_SET\_FB\_ADDR\_CR\_BASE5,CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET5} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:30 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 29:26 | TEMPORAL\_ID | | | rw | ro | | 0x0 | | | A temporal ID of 0th picture in the custom GOP{has\_reset=0} | | | | | |
| 25:20 | REF0\_POC | | | rw | ro | | 0x0 | | | A poc offset of reference L0 of 0th picture in the custom GOP{has\_reset=0} | | | | | |
| 19:14 | REF1\_POC | | | rw | ro | | 0x0 | | | A poc offset of reference L1 of 0th picture in the custom GOP{has\_reset=0} | | | | | |
| 13:13 | USE\_MULTI\_REF\_P | | | rw | ro | | 0x0 | | | Flag to use multi reference picture for P picture  It is valid only if PIC\_TYPE is P{has\_reset=0} | | | | | |
| 12:7 | PIC\_QP | | | rw | ro | | 0x0 | | | A quantization parameter of 0th picture in the custom GOP{has\_reset=0} | | | | | |
| 6:2 | POC\_OFFSET | | | rw | ro | | 0x0 | | | A poc offset of 0th picture in the custom GOP{has\_reset=0} | | | | | |
| 1:0 | PIC\_TYPE | | | rw | ro | | 0x0 | | | A picture type of 0th picture in the custom GOP  1 : P picture  2 : B picture{has\_reset=0} | | | | | |

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| 1.1.1.285.0 | | | | | | | | CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_1 | | | | | reg32 | | 0x394 |
| offset | | 916 | external | | |  | | | size | | 32 |  | |  | |
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| Parameters for the 1st picture of custom GOP (MANDATORY with CUSTOM\_GOP\_SIZE){alt\_reg=CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET5,RET\_DEC\_NUM\_REQURED\_COL\_FB} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:30 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 29:26 | TEMPORAL\_ID | | | rw | ro | | 0x0 | | | A temporal ID of 1st picture in the custom GOP{has\_reset=0} | | | | | |
| 25:20 | REF0\_POC | | | rw | ro | | 0x0 | | | A poc offset of reference L0 of 1st picture in the custom GOP{has\_reset=0} | | | | | |
| 19:14 | REF1\_POC | | | rw | ro | | 0x0 | | | A poc offset of reference L1 of 1st picture in the custom GOP{has\_reset=0} | | | | | |
| 13:13 | USE\_MULTI\_REF\_P | | | rw | ro | | 0x0 | | | Flag to use multi reference picture for P picture  It is valid only if PIC\_TYPE is P{has\_reset=0} | | | | | |
| 12:7 | PIC\_QP | | | rw | ro | | 0x0 | | | A quantization parameter of 1st picture in the custom GOP{has\_reset=0} | | | | | |
| 6:2 | POC\_OFFSET | | | rw | ro | | 0x0 | | | A poc offset of 1st picture in the custom GOP{has\_reset=0} | | | | | |
| 1:0 | PIC\_TYPE | | | rw | ro | | 0x0 | | | A picture type of 0th picture in the custom GOP  1 : P picture  2 : B picture{has\_reset=0} | | | | | |

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| 1.1.1.287.0 | | | | | | | | CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_2 | | | | | reg32 | | 0x398 |
| offset | | 920 | external | | |  | | | size | | 32 |  | |  | |
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| Parameters for the 2nd picture of custom GOP (MANDATORY with CUSTOM\_GOP\_SIZE){alt\_reg=CMD\_SET\_FB\_ADDR\_COL5} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:30 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 29:26 | TEMPORAL\_ID | | | rw | ro | | 0x0 | | | A temporal ID of 2nd picture in the custom GOP{has\_reset=0} | | | | | |
| 25:20 | REF0\_POC | | | rw | ro | | 0x0 | | | A poc offset of reference L0 of 2nd picture in the custom GOP{has\_reset=0} | | | | | |
| 19:14 | REF1\_POC | | | rw | ro | | 0x0 | | | A poc offset of reference L1 of 2nd picture in the custom GOP{has\_reset=0} | | | | | |
| 13:13 | USE\_MULTI\_REF\_P | | | rw | ro | | 0x0 | | | Flag to use multi reference picture for P picture  It is valid only if PIC\_TYPE is P{has\_reset=0} | | | | | |
| 12:7 | PIC\_QP | | | rw | ro | | 0x0 | | | A quantization parameter of 2nd picture in the custom GOP{has\_reset=0} | | | | | |
| 6:2 | POC\_OFFSET | | | rw | ro | | 0x0 | | | A poc offset of 2nd picture in the custom GOP{has\_reset=0} | | | | | |
| 1:0 | PIC\_TYPE | | | rw | ro | | 0x0 | | | A picture type of 0th picture in the custom GOP  1 : P picture  2 : B picture{has\_reset=0} | | | | | |

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| 1.1.1.289.0 | | | | | | | | CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_3 | | | | | reg32 | | 0x39C |
| offset | | 924 | external | | |  | | | size | | 32 |  | |  | |
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| Parameters for the 3rd picture of custom GOP (MANDATORY with CUSTOM\_GOP\_SIZE){alt\_reg=CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE5} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:30 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 29:26 | TEMPORAL\_ID | | | rw | ro | | 0x0 | | | A temporal ID of 3rd picture in the custom GOP{has\_reset=0} | | | | | |
| 25:20 | REF0\_POC | | | rw | ro | | 0x0 | | | A poc offset of reference L0 of 3rd picture in the custom GOP{has\_reset=0} | | | | | |
| 19:14 | REF1\_POC | | | rw | ro | | 0x0 | | | A poc offset of reference L1 of 3rd picture in the custom GOP{has\_reset=0} | | | | | |
| 13:13 | USE\_MULTI\_REF\_P | | | rw | ro | | 0x0 | | | Flag to use multi reference picture for P picture  It is valid only if PIC\_TYPE is P{has\_reset=0} | | | | | |
| 12:7 | PIC\_QP | | | rw | ro | | 0x0 | | | A quantization parameter of 3rd picture in the custom GOP{has\_reset=0} | | | | | |
| 6:2 | POC\_OFFSET | | | rw | ro | | 0x0 | | | A poc offset of 3rd picture in the custom GOP{has\_reset=0} | | | | | |
| 1:0 | PIC\_TYPE | | | rw | ro | | 0x0 | | | A picture type of 0th picture in the custom GOP  1 : P picture  2 : B picture{has\_reset=0} | | | | | |

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| 1.1.1.292.0 | | | | | | | | CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_4 | | | | | reg32 | | 0x3A0 |
| offset | | 928 | external | | |  | | | size | | 32 |  | |  | |
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| Parameters for the 4th picture of custom GOP (MANDATORY with CUSTOM\_GOP\_SIZE){alt\_reg=CMD\_SET\_FB\_ADDR\_LUMA\_BASE6,RET\_CORE\_IDC} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:30 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 29:26 | TEMPORAL\_ID | | | rw | ro | | 0x0 | | | A temporal ID of 4th picture in the custom GOP{has\_reset=0} | | | | | |
| 25:20 | REF0\_POC | | | rw | ro | | 0x0 | | | A poc offset of reference L0 of 4th picture in the custom GOP{has\_reset=0} | | | | | |
| 19:14 | REF1\_POC | | | rw | ro | | 0x0 | | | A poc offset of reference L1 of 4th picture in the custom GOP{has\_reset=0} | | | | | |
| 13:13 | USE\_MULTI\_REF\_P | | | rw | ro | | 0x0 | | | Flag to use multi reference picture for P picture  It is valid only if PIC\_TYPE is P{has\_reset=0} | | | | | |
| 12:7 | PIC\_QP | | | rw | ro | | 0x0 | | | A quantization parameter of 4th picture in the custom GOP{has\_reset=0} | | | | | |
| 6:2 | POC\_OFFSET | | | rw | ro | | 0x0 | | | A poc offset of 4th picture in the custom GOP{has\_reset=0} | | | | | |
| 1:0 | PIC\_TYPE | | | rw | ro | | 0x0 | | | A picture type of 0th picture in the custom GOP  1 : P picture  2 : B picture{has\_reset=0} | | | | | |

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| 1.1.1.295.0 | | | | | | | | CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_5 | | | | | reg32 | | 0x3A4 |
| offset | | 932 | external | | |  | | | size | | 32 |  | |  | |
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| Parameters for the 5th picture of custom GOP (MANDATORY with CUSTOM\_GOP\_SIZE){alt\_reg=CMD\_SET\_FB\_ADDR\_CB\_BASE6,RET\_DEC\_PIC\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:30 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 29:26 | TEMPORAL\_ID | | | rw | ro | | 0x0 | | | A temporal ID of 5th picture in the custom GOP{has\_reset=0} | | | | | |
| 25:20 | REF0\_POC | | | rw | ro | | 0x0 | | | A poc offset of reference L0 of 5th picture in the custom GOP{has\_reset=0} | | | | | |
| 19:14 | REF1\_POC | | | rw | ro | | 0x0 | | | A poc offset of reference L1 of 5th picture in the custom GOP{has\_reset=0} | | | | | |
| 13:13 | USE\_MULTI\_REF\_P | | | rw | ro | | 0x0 | | | Flag to use multi reference picture for P picture  It is valid only if PIC\_TYPE is P{has\_reset=0} | | | | | |
| 12:7 | PIC\_QP | | | rw | ro | | 0x0 | | | A quantization parameter of 5th picture in the custom GOP{has\_reset=0} | | | | | |
| 6:2 | POC\_OFFSET | | | rw | ro | | 0x0 | | | A poc offset of 5th picture in the custom GOP{has\_reset=0} | | | | | |
| 1:0 | PIC\_TYPE | | | rw | ro | | 0x0 | | | A picture type of 0th picture in the custom GOP  1 : P picture  2 : B picture{has\_reset=0} | | | | | |

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| 1.1.1.299.0 | | | | | | | | CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_6 | | | | | reg32 | | 0x3A8 |
| offset | | 936 | external | | |  | | | size | | 32 |  | |  | |
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| Parameters for the 6th picture of custom GOP (MANDATORY with CUSTOM\_GOP\_SIZE){alt\_reg=CMD\_SET\_FB\_ADDR\_CR\_BASE6,CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET6,RET\_ENC\_CORE\_IDC} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:30 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 29:26 | TEMPORAL\_ID | | | rw | ro | | 0x0 | | | A temporal ID of 6th picture in the custom GOP{has\_reset=0} | | | | | |
| 25:20 | REF0\_POC | | | rw | ro | | 0x0 | | | A poc offset of reference L0 of 6th picture in the custom GOP{has\_reset=0} | | | | | |
| 19:14 | REF1\_POC | | | rw | ro | | 0x0 | | | A poc offset of reference L1 of 6th picture in the custom GOP{has\_reset=0} | | | | | |
| 13:13 | USE\_MULTI\_REF\_P | | | rw | ro | | 0x0 | | | Flag to use multi reference picture for P picture  It is valid only if PIC\_TYPE is P{has\_reset=0} | | | | | |
| 12:7 | PIC\_QP | | | rw | ro | | 0x0 | | | A quantization parameter of 6th picture in the custom GOP{has\_reset=0} | | | | | |
| 6:2 | POC\_OFFSET | | | rw | ro | | 0x0 | | | A poc offset of 6th picture in the custom GOP{has\_reset=0} | | | | | |
| 1:0 | PIC\_TYPE | | | rw | ro | | 0x0 | | | A picture type of 0th picture in the custom GOP  1 : P picture  2 : B picture{has\_reset=0} | | | | | |

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| 1.1.1.302.0 | | | | | | | | CMD\_ENC\_SEQ\_CUSTOM\_GOP\_PIC\_PARAM\_7 | | | | | reg32 | | 0x3AC |
| offset | | 940 | external | | |  | | | size | | 32 |  | |  | |
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| Parameters for the 7th picture of custom GOP (MANDATORY with CUSTOM\_GOP\_SIZE){alt\_reg=CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET6,RET\_HOST\_CMD\_WARN\_INFO} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:30 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 29:26 | TEMPORAL\_ID | | | rw | ro | | 0x0 | | | A temporal ID of 7th picture in the custom GOP{has\_reset=0} | | | | | |
| 25:20 | REF0\_POC | | | rw | ro | | 0x0 | | | A poc offset of reference L0 of 7th picture in the custom GOP{has\_reset=0} | | | | | |
| 19:14 | REF1\_POC | | | rw | ro | | 0x0 | | | A poc offset of reference L1 of 7th picture in the custom GOP{has\_reset=0} | | | | | |
| 13:13 | USE\_MULTI\_REF\_P | | | rw | ro | | 0x0 | | | Flag to use multi reference picture for P picture  It is valid only if PIC\_TYPE is P{has\_reset=0} | | | | | |
| 12:7 | PIC\_QP | | | rw | ro | | 0x0 | | | A quantization parameter of 7th picture in the custom GOP{has\_reset=0} | | | | | |
| 6:2 | POC\_OFFSET | | | rw | ro | | 0x0 | | | A poc offset of 7th picture in the custom GOP{has\_reset=0} | | | | | |
| 1:0 | PIC\_TYPE | | | rw | ro | | 0x0 | | | A picture type of 0th picture in the custom GOP  1 : P picture  2 : B picture{has\_reset=0} | | | | | |

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| 1.1.1.304.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_COL6 | | | | | reg32 | | 0x3B0 |
| offset | | 944 | external | | |  | | | size | | 32 |  | |  | |
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| Info base of index 6{alt\_reg=RET\_HOST\_CMD\_ERR\_INFO} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | COL\_BASE6 | | | rw | ro | | 0x0 | | | Codec dedicated information buffer for encoding/decoding  HEVC/AVC: MV COL  AV1 : CDF{has\_reset=0} | | | | | |

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| 1.1.1.306.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE6 | | | | | reg32 | | 0x3B4 |
| offset | | 948 | external | | |  | | | size | | 32 |  | |  | |
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| Base address of sub-sampled frame buffer for index 6{alt\_reg=RET\_HOST\_CMD\_SUCCESS} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SUB\_SAMPLED\_FB\_BASE6 | | | rw | ro | | 0x0 | | | A base address of frame buffer for sub sampled decoded frame 6{has\_reset=0} | | | | | |

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| 1.1.1.308.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_LUMA\_BASE7 | | | | | reg32 | | 0x3B8 |
| offset | | 952 | external | | |  | | | size | | 32 |  | |  | |
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| Luma base of index 7{alt\_reg=RET\_ENC\_SUM\_ME0\_X\_DIR\_LOWER} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | LUMA\_BASE7 | | | rw | ro | | 0x0 | | | Luma base address of DPB index 7  Compressed Luma base address of DPB index 7{has\_reset=0} | | | | | |

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| 1.1.1.310.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CB\_BASE7 | | | | | reg32 | | 0x3BC |
| offset | | 956 | external | | |  | | | size | | 32 |  | |  | |
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| Cb base of index7{alt\_reg=RET\_ENC\_SUM\_ME0\_X\_DIR\_HIGHER} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CB\_BASE7 | | | rw | ro | | 0x0 | | | Cb base address of DPB index 7  Compressed Cb and Cr base address of DPB index 7{has\_reset=0} | | | | | |

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| 1.1.1.313.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_CR\_BASE7 | | | | | reg32 | | 0x3C0 |
| offset | | 960 | external | | |  | | | size | | 32 |  | |  | |
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| Cr base of index 7{alt\_reg=CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET7,RET\_ENC\_SUM\_ME0\_Y\_DIR\_LOWER} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | CR\_BASE7 | | | rw | ro | | 0x0 | | | Cr base address of DPB index 7{has\_reset=0} | | | | | |

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| 1.1.1.315.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET7 | | | | | reg32 | | 0x3C4 |
| offset | | 964 | external | | |  | | | size | | 32 |  | |  | |
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| FBC chroma offset base of index 7{alt\_reg=RET\_ENC\_SUM\_ME0\_Y\_DIR\_HIGHER} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | FBC\_CHROMA\_OFFSET\_BASE7 | | | rw | ro | | 0x0 | | | If FBC is used, this is chroma offset base address of DPB index 7. Otherwise, it is ignored.{has\_reset=0} | | | | | |

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| 1.1.1.317.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_COL7 | | | | | reg32 | | 0x3C8 |
| offset | | 968 | external | | |  | | | size | | 32 |  | |  | |
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| Info base of index 7{alt\_reg=RET\_ENC\_SUM\_ME1\_X\_DIR\_LOWER} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | COL\_BASE7 | | | rw | ro | | 0x0 | | | Codec dedicated information buffer for encoding/decoding  HEVC/AVC: MV COL  AV1 : CDF{has\_reset=0} | | | | | |

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| 1.1.1.320.0 | | | | | | | | CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE7 | | | | | reg32 | | 0x3CC |
| offset | | 972 | external | | |  | | | size | | 32 |  | |  | |
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| Base address of sub-sampled frame buffer for index 7{alt\_reg=RET\_DEC\_WARN\_INFO,RET\_ENC\_SUM\_ME1\_X\_DIR\_HIGHER} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | SUB\_SAMPLED\_FB\_BASE7 | | | rw | ro | | 0x0 | | | A base address of frame buffer for sub sampled decoded frame 7{has\_reset=0} | | | | | |

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| 1.1.1.324.0 | | | | | | | | CMD\_ENC\_SEQ\_TILE\_PARAM | | | | | reg32 | | 0x3D0 |
| offset | | 976 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_TILE\_PARAM{alt\_reg=CMD\_SET\_FB\_ADDR\_LUMA\_BASE8,RET\_DEC\_ERR\_INFO,RET\_ENC\_SUM\_ME1\_Y\_DIR\_LOWER} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:8 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 7:4 | TILE\_NUM\_IN\_ROW\_M1 | | | rw | ro | | 0x0 | | | It specifies the number of tile rows minus 1. (0 ~ 15){has\_reset=0} | | | | | |
| 3:0 | TILE\_NUM\_IN\_COL\_M1 | | | rw | ro | | 0x0 | | | It specifies the number of tile columns minus 1. (0 ~ 15){has\_reset=0} | | | | | |

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| 1.1.1.328.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_0 | | | | | reg32 | | 0x3D4 |
| offset | | 980 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_0{alt\_reg=CMD\_SET\_FB\_ADDR\_CB\_BASE8,RET\_DEC\_DECODING\_SUCCESS,RET\_ENC\_SUM\_ME1\_Y\_DIR\_HIGHER} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.331.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_1 | | | | | reg32 | | 0x3D8 |
| offset | | 984 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_1{alt\_reg=CMD\_SET\_FB\_ADDR\_CR\_BASE8,CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET8} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.333.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_2 | | | | | reg32 | | 0x3DC |
| offset | | 988 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_2{alt\_reg=CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET8} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.335.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_3 | | | | | reg32 | | 0x3E0 |
| offset | | 992 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_3{alt\_reg=CMD\_SET\_FB\_ADDR\_COL8} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.337.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_4 | | | | | reg32 | | 0x3E4 |
| offset | | 996 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_4{alt\_reg=CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE8} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.339.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_5 | | | | | reg32 | | 0x3E8 |
| offset | | 1000 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_5{alt\_reg=CMD\_SET\_FB\_ADDR\_LUMA\_BASE9} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.341.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_6 | | | | | reg32 | | 0x3EC |
| offset | | 1004 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_6{alt\_reg=CMD\_SET\_FB\_ADDR\_CB\_BASE9} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.344.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_7 | | | | | reg32 | | 0x3F0 |
| offset | | 1008 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_7{alt\_reg=CMD\_SET\_FB\_ADDR\_CR\_BASE9,CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET9} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.346.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_8 | | | | | reg32 | | 0x3F4 |
| offset | | 1012 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_8{alt\_reg=CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET9} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.349.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_9 | | | | | reg32 | | 0x3F8 |
| offset | | 1016 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_9{alt\_reg=CMD\_SET\_FB\_ADDR\_COL9,RET\_ENC\_SRC\_DEBUG\_0} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.352.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_10 | | | | | reg32 | | 0x3FC |
| offset | | 1020 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_10{alt\_reg=CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE9,RET\_ENC\_SRC\_DEBUG\_1} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.354.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_11 | | | | | reg32 | | 0x400 |
| offset | | 1024 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_11{alt\_reg=CMD\_SET\_FB\_ADDR\_LUMA\_BASE10} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.356.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_12 | | | | | reg32 | | 0x404 |
| offset | | 1028 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_12{alt\_reg=CMD\_SET\_FB\_ADDR\_CB\_BASE10} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.359.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_13 | | | | | reg32 | | 0x408 |
| offset | | 1032 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_13{alt\_reg=CMD\_SET\_FB\_ADDR\_CR\_BASE10,CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET10} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.361.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_14 | | | | | reg32 | | 0x40C |
| offset | | 1036 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_14{alt\_reg=CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET10} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.363.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_15 | | | | | reg32 | | 0x410 |
| offset | | 1040 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_15{alt\_reg=CMD\_SET\_FB\_ADDR\_COL10} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.365.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_16 | | | | | reg32 | | 0x414 |
| offset | | 1044 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_16{alt\_reg=CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE10} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.367.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_17 | | | | | reg32 | | 0x418 |
| offset | | 1048 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_17{alt\_reg=CMD\_SET\_FB\_ADDR\_LUMA\_BASE11} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.369.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_18 | | | | | reg32 | | 0x41C |
| offset | | 1052 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_18{alt\_reg=CMD\_SET\_FB\_ADDR\_CB\_BASE11} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
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| 1.1.1.372.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_19 | | | | | reg32 | | 0x420 |
| offset | | 1056 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_19{alt\_reg=CMD\_SET\_FB\_ADDR\_CR\_BASE11,CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET11} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
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| 1.1.1.374.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_20 | | | | | reg32 | | 0x424 |
| offset | | 1060 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_20{alt\_reg=CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET11} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
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| 1.1.1.376.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_21 | | | | | reg32 | | 0x428 |
| offset | | 1064 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_21{alt\_reg=CMD\_SET\_FB\_ADDR\_COL11} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.378.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_22 | | | | | reg32 | | 0x42C |
| offset | | 1068 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_22{alt\_reg=CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE11} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.380.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_23 | | | | | reg32 | | 0x430 |
| offset | | 1072 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_23{alt\_reg=CMD\_SET\_FB\_ADDR\_LUMA\_BASE12} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.382.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_24 | | | | | reg32 | | 0x434 |
| offset | | 1076 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_24{alt\_reg=CMD\_SET\_FB\_ADDR\_CB\_BASE12} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.385.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_25 | | | | | reg32 | | 0x438 |
| offset | | 1080 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_25{alt\_reg=CMD\_SET\_FB\_ADDR\_CR\_BASE12,CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET12} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.387.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_26 | | | | | reg32 | | 0x43C |
| offset | | 1084 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_26{alt\_reg=CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET12} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.389.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_27 | | | | | reg32 | | 0x440 |
| offset | | 1088 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_27{alt\_reg=CMD\_SET\_FB\_ADDR\_COL12} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.391.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_28 | | | | | reg32 | | 0x444 |
| offset | | 1092 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_28{alt\_reg=CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE12} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.393.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_29 | | | | | reg32 | | 0x448 |
| offset | | 1096 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_29{alt\_reg=CMD\_SET\_FB\_ADDR\_LUMA\_BASE13} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.395.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_30 | | | | | reg32 | | 0x44C |
| offset | | 1100 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_30{alt\_reg=CMD\_SET\_FB\_ADDR\_CB\_BASE13} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.398.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_31 | | | | | reg32 | | 0x450 |
| offset | | 1104 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_31{alt\_reg=CMD\_SET\_FB\_ADDR\_CR\_BASE13,CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET13} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.400.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_32 | | | | | reg32 | | 0x454 |
| offset | | 1108 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_32{alt\_reg=CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET13} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.402.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_33 | | | | | reg32 | | 0x458 |
| offset | | 1112 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_33{alt\_reg=CMD\_SET\_FB\_ADDR\_COL13} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.404.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_34 | | | | | reg32 | | 0x45C |
| offset | | 1116 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_34{alt\_reg=CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE13} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.406.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_35 | | | | | reg32 | | 0x460 |
| offset | | 1120 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_35{alt\_reg=CMD\_SET\_FB\_ADDR\_LUMA\_BASE14} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.408.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_36 | | | | | reg32 | | 0x464 |
| offset | | 1124 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_36{alt\_reg=CMD\_SET\_FB\_ADDR\_CB\_BASE14} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.411.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_37 | | | | | reg32 | | 0x468 |
| offset | | 1128 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_37{alt\_reg=CMD\_SET\_FB\_ADDR\_CR\_BASE14,CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET14} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.413.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_38 | | | | | reg32 | | 0x46C |
| offset | | 1132 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_38{alt\_reg=CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET14} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
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| 1.1.1.415.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_39 | | | | | reg32 | | 0x470 |
| offset | | 1136 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_39{alt\_reg=CMD\_SET\_FB\_ADDR\_COL14} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.417.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_40 | | | | | reg32 | | 0x474 |
| offset | | 1140 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_40{alt\_reg=CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE14} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.419.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_41 | | | | | reg32 | | 0x478 |
| offset | | 1144 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_41{alt\_reg=CMD\_SET\_FB\_ADDR\_LUMA\_BASE15} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.421.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_42 | | | | | reg32 | | 0x47C |
| offset | | 1148 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_42{alt\_reg=CMD\_SET\_FB\_ADDR\_CB\_BASE15} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.424.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_43 | | | | | reg32 | | 0x480 |
| offset | | 1152 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_43{alt\_reg=CMD\_SET\_FB\_ADDR\_CR\_BASE15,CMD\_SET\_FB\_ADDR\_FBC\_Y\_OFFSET15} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.426.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_44 | | | | | reg32 | | 0x484 |
| offset | | 1156 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_44{alt\_reg=CMD\_SET\_FB\_ADDR\_FBC\_C\_OFFSET15} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.428.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_45 | | | | | reg32 | | 0x488 |
| offset | | 1160 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_45{alt\_reg=CMD\_SET\_FB\_ADDR\_COL15} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.430.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_46 | | | | | reg32 | | 0x48C |
| offset | | 1164 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_46{alt\_reg=CMD\_SET\_FB\_ADDR\_SUB\_SAMPLED\_FB\_BASE15} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.431.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_47 | | | | | reg32 | | 0x490 |
| offset | | 1168 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_47 | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.433.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_48 | | | | | reg32 | | 0x494 |
| offset | | 1172 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_48{alt\_reg=CMD\_SET\_FB\_ADDR\_DEFAULT\_CDF} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.435.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_49 | | | | | reg32 | | 0x498 |
| offset | | 1176 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_49{alt\_reg=CMD\_SET\_FB\_ADDR\_SEGMAP} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.437.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_50 | | | | | reg32 | | 0x49C |
| offset | | 1180 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_50{alt\_reg=CMD\_SET\_FB\_DEC\_PP\_PVRIC\_CTRL} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.438.0 | | | | | | | | CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_51 | | | | | reg32 | | 0x4A0 |
| offset | | 1184 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_CUSTOM\_LAMBDA\_DATA\_51 | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:21 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 20:7 | LAMBDA\_SSD | | | rw | ro | | 0x0 | | | lambda\_ssd data{has\_reset=0} | | | | | |
| 6:0 | LAMBDA\_SAD | | | rw | ro | | 0x0 | | | lambda\_sad data{has\_reset=0} | | | | | |

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| 1.1.1.440.0 | | | | | | | | CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_0\_QP | | | | | reg32 | | 0x4A4 |
| offset | | 1188 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_0\_QP{alt\_reg=CMD\_SET\_FB\_DEC\_PP\_SCL\_PARAM} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:18 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 17:12 | B\_QP | | | rw | ro | | 0x0 | | | A QP value of B Pictures{has\_reset=0} | | | | | |
| 11:6 | P\_QP | | | rw | ro | | 0x0 | | | A QP value of P Pictures{has\_reset=0} | | | | | |
| 5:0 | I\_QP | | | rw | ro | | 0x0 | | | A QP value of I Pictures{has\_reset=0} | | | | | |

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| 1.1.1.441.0 | | | | | | | | CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_1\_QP | | | | | reg32 | | 0x4A8 |
| offset | | 1192 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_1\_QP | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:18 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 17:12 | B\_QP | | | rw | ro | | 0x0 | | | A QP value of B Pictures{has\_reset=0} | | | | | |
| 11:6 | P\_QP | | | rw | ro | | 0x0 | | | A QP value of P Pictures{has\_reset=0} | | | | | |
| 5:0 | I\_QP | | | rw | ro | | 0x0 | | | A QP value of I Pictures{has\_reset=0} | | | | | |

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| 1.1.1.442.0 | | | | | | | | CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_2\_QP | | | | | reg32 | | 0x4AC |
| offset | | 1196 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_2\_QP | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:18 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 17:12 | B\_QP | | | rw | ro | | 0x0 | | | A QP value of B Pictures{has\_reset=0} | | | | | |
| 11:6 | P\_QP | | | rw | ro | | 0x0 | | | A QP value of P Pictures{has\_reset=0} | | | | | |
| 5:0 | I\_QP | | | rw | ro | | 0x0 | | | A QP value of I Pictures{has\_reset=0} | | | | | |

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| 1.1.1.443.0 | | | | | | | | CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_3\_QP | | | | | reg32 | | 0x4B0 |
| offset | | 1200 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_TEMPORAL\_LAYER\_3\_QP | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:18 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 17:12 | B\_QP | | | rw | ro | | 0x0 | | | A QP value of B Pictures{has\_reset=0} | | | | | |
| 11:6 | P\_QP | | | rw | ro | | 0x0 | | | A QP value of P Pictures{has\_reset=0} | | | | | |
| 5:0 | I\_QP | | | rw | ro | | 0x0 | | | A QP value of I Pictures{has\_reset=0} | | | | | |

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| 1.1.1.444.0 | | | | | | | | CMD\_ENC\_SEQ\_SCL\_SRC\_SIZE | | | | | reg32 | | 0x4B4 |
| offset | | 1204 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_SCL\_SRC\_SIZE | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | PIC\_HEIGHT | | | rw | ro | | 0x0 | | | A height of picture in pixel (128 ~ 8192) (before scaler){has\_reset=0} | | | | | |
| 15:0 | PIC\_WIDTH | | | rw | ro | | 0x0 | | | A width of picture in pixel (256 ~ 8192) (before scaler){has\_reset=0} | | | | | |

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| 1.1.1.445.0 | | | | | | | | CMD\_ENC\_SEQ\_SCL\_PARAM | | | | | reg32 | | 0x4B8 |
| offset | | 1208 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_SCL\_PARAM | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:3 | RSVD0 | | | rw | ro | | 0x0 | | | RSVD{has\_reset=0} | | | | | |
| 2:1 | SCL\_COEF\_MODE | | | rw | ro | | 0x0 | | | Scaler coeff mode  0:bicubic 0.5  1:bicubic 1.0  2:bicubic 1.5  3:lanczos{has\_reset=0} | | | | | |
| 0:0 | SCL\_EN | | | rw | ro | | 0x0 | | | Scaler enable flag (0 : off, 1: on){has\_reset=0} | | | | | |

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| 1.1.1.446.0 | | | | | | | | CMD\_ENC\_SEQ\_Y2Y\_PARAM | | | | | reg32 | | 0x4BC |
| offset | | 1212 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_Y2Y\_PARAM | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:2 | RSVD0 | | | rw | ro | | 0x0 | | | RSVD{has\_reset=0} | | | | | |
| 1:0 | Y2Y\_MODE | | | rw | ro | | 0x0 | | | Y2Y mode  0: off  1: Y only  2: Chroma only  3: Y/Chorma{has\_reset=0} | | | | | |

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| 1.1.1.447.0 | | | | | | | | CMD\_SET\_FB\_DEC\_PP\_CROP\_PARAM | | | | | reg32 | | 0x4C0 |
| offset | | 1216 | external | | |  | | | size | | 32 |  | |  | |
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| Crop control parameter (Post processing) | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:1 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 0:0 | CROP\_EN | | | rw | ro | | 0x0 | | | Crop enable flag  0 : disable  1 : enable{has\_reset=0} | | | | | |

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| 1.1.1.449.0 | | | | | | | | CMD\_ENC\_SEQ\_SFS\_PARAM | | | | | reg32 | | 0x4C4 |
| offset | | 1220 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_SFS\_PARAM{alt\_reg=CMD\_SET\_FB\_DEC\_PP\_CROP\_POS} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:2 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 1:1 | SUB\_FRAME\_SYNC\_TYPE | | | rw | ro | | 0x0 | | | 0 : signal(wired) based, 1: register based{has\_reset=0} | | | | | |
| 0:0 | SUB\_FRAME\_SYNC\_ON | | | rw | ro | | 0x0 | | | 0 : off, 1: on{has\_reset=0} | | | | | |

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| 1.1.1.451.0 | | | | | | | | CMD\_ENC\_SEQ\_CROP\_ENABLE | | | | | reg32 | | 0x4C8 |
| offset | | 1224 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_CROP\_ENABLE{alt\_reg=CMD\_SET\_FB\_DEC\_PP\_CROP\_SIZE} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:1 | RSVD0 | | | rw | ro | | 0x0 | | | reserved{has\_reset=0} | | | | | |
| 0:0 | CROP\_EN | | | rw | ro | | 0x0 | | | Crop enable flag (0 : off, 1: on){has\_reset=0} | | | | | |

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| 1.1.1.453.0 | | | | | | | | CMD\_ENC\_SEQ\_CROP\_START\_POS | | | | | reg32 | | 0x4CC |
| offset | | 1228 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_CROP\_START\_POS{alt\_reg=CMD\_SET\_FB\_DEC\_PP\_AFBC\_COMMON} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | CROP\_START\_X | | | rw | ro | | 0x0 | | | start X position for crop (AFBCD or Crop ){has\_reset=0} | | | | | |
| 15:0 | CROP\_START\_Y | | | rw | ro | | 0x0 | | | start Y position for crop (AFBCD or Crop ){has\_reset=0} | | | | | |

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| 1.1.1.455.0 | | | | | | | | CMD\_ENC\_SEQ\_CROP\_SRC\_SIZE | | | | | reg32 | | 0x4D0 |
| offset | | 1232 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_CROP\_SRC\_SIZE | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | PIC\_HEIGHT | | | rw | ro | | 0x0 | | | A height of picture in pixel (128 ~ 8192) (before crop){has\_reset=0} | | | | | |
| 15:0 | PIC\_WIDTH | | | rw | ro | | 0x0 | | | A width of picture in pixel (256 ~ 8192) (before crop){has\_reset=0} | | | | | |

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| 1.1.1.456.0 | | | | | | | | CMD\_ENC\_SEQ\_Y2Y\_DATA\_0 | | | | | reg32 | | 0x4D8 |
| offset | | 1240 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_Y2Y\_DATA\_0 | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:30 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 29:20 | LUMA\_OUT\_MIN | | | rw | ro | | 0x0 | | | Y2Y luma output min value  8bit: 0 ~ 255  10 bit : 0 ~ 1023{has\_reset=0} | | | | | |
| 19:10 | LUMA\_IN\_MAX | | | rw | ro | | 0x0 | | | Y2Y luma input max value  8bit: 0 ~ 255  10 bit : 0 ~ 1023{has\_reset=0} | | | | | |
| 9:0 | LUMA\_IN\_MIN | | | rw | ro | | 0x0 | | | Y2Y luma input min value  8bit: 0 ~ 255  10 bit : 0 ~ 1023{has\_reset=0} | | | | | |

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| 1.1.1.458.0 | | | | | | | | CMD\_ENC\_SEQ\_Y2Y\_DATA\_1 | | | | | reg32 | | 0x4DC |
| offset | | 1244 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_Y2Y\_DATA\_1{alt\_reg=CMD\_SET\_FB\_DEC\_ADDR\_COL\_DUAL} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:30 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 29:20 | CHR\_IN\_MAX | | | rw | ro | | 0x0 | | | Y2Y Chroma input max value  8bit: 0 ~ 255  10 bit : 0 ~ 1023{has\_reset=0} | | | | | |
| 19:10 | CHR\_IN\_MIN | | | rw | ro | | 0x0 | | | Y2Y Chroma input min value  8bit: 0 ~ 255  10 bit : 0 ~ 1023{has\_reset=0} | | | | | |
| 9:0 | LUMA\_OUT\_MAX | | | rw | ro | | 0x0 | | | Y2Y luma output max value  8bit: 0 ~ 255  10 bit : 0 ~ 1023{has\_reset=0} | | | | | |

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| 1.1.1.459.0 | | | | | | | | CMD\_ENC\_SEQ\_Y2Y\_DATA\_2 | | | | | reg32 | | 0x4E0 |
| offset | | 1248 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_Y2Y\_DATA\_2 | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:20 | RESERVED0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 19:10 | CHR\_OUT\_MAX | | | rw | ro | | 0x0 | | | Y2Y Chroma output max value  8bit: 0 ~ 255  10 bit : 0 ~ 1023{has\_reset=0} | | | | | |
| 9:0 | CHR\_OUT\_MIN | | | rw | ro | | 0x0 | | | Y2Y Chroma output min value  8bit: 0 ~ 255  10 bit : 0 ~ 1023{has\_reset=0} | | | | | |

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| 1.1.1.461.0 | | | | | | | | CMD\_ENC\_SEQ\_INPUT\_RINGBUF | | | | | reg32 | | 0x4E4 |
| offset | | 1252 | external | | |  | | | size | | 32 |  | |  | |
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| CMD\_ENC\_SEQ\_INPUT\_RINGBUF | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 0:0 | INPUT\_RINGBUF\_EN | | | rw | ro | | 0x0 | | | 0 : off, 1 : on{has\_reset=0} | | | | | |

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| 1.1.1.462.0 | | | | | | | | VPU\_PDBG\_CTRL | | | | | reg32 | | 0x600 |
| offset | | 1536 | external | | |  | | | size | | 32 |  | |  | |
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| Debugger control  (for debugger only) | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:4 | RSVD0 | | | wo | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 3:3 | IMMBRK | | | wo | ro | | 0x0 | | | Immediate break  It forces to stop V-CPU and enter in a debug mode to analyze hang-up situation.  V-CPU cannot resume from the break point.{has\_reset=0} | | | | | |
| 2:2 | STABLEBRK | | | wo | ro | | 0x0 | | | Stable break  It is an external break request when V-CPU is in stable (breakable) status.{has\_reset=0} | | | | | |
| 1:1 | RESUME | | | wo | ro | | 0x0 | | | Resume  It resumes from the breakpoint.{has\_reset=0} | | | | | |
| 0:0 | STEP | | | wo | ro | | 0x0 | | | Step  It runs V-CPU in step instruction mode.{has\_reset=0} | | | | | |

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| 1.1.1.463.0 | | | | | | | | VPU\_PDBG\_IDX\_REG | | | | | reg32 | | 0x604 |
| offset | | 1540 | external | | |  | | | size | | 32 |  | |  | |
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| V-CPU debugger index register  (For debugger only) | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:10 | RSVD0 | | | wo | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 9:9 | RDDBG | | | wo | ro | | 0x0 | | | Read Operation Request  RDDBG and WRDBG cannot be 1 at the same time.{has\_reset=0} | | | | | |
| 8:8 | WRDBG | | | wo | ro | | 0x0 | | | Write Operation Request  RDDBG and WRDBG cannot be 1 at the same time.{has\_reset=0} | | | | | |
| 7:0 | DBGIDX | | | wo | ro | | 0x0 | | | Debug Index  Debugger Register Index{has\_reset=0} | | | | | |

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| 1.1.1.464.0 | | | | | | | | VPU\_PDBG\_WDATA\_REG | | | | | reg32 | | 0x608 |
| offset | | 1544 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| V-CPU debugger write data register  (For debugger only) | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | VPU\_PDBG\_WDATA\_REG | | | wo | ro | | 0x0 | | | To write data to the debugger,  # Write some data to this register.  # Write VCPU\_PDBG\_IDX\_REG with WRDBG as 1 and DBGIDX as this register address.  # After writing is completed, VPU\_PDBG\_WDATA\_REG will be cleared.{has\_reset=0} | | | | | |

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| 1.1.1.465.0 | | | | | | | | VPU\_PDBG\_RDATA\_REG | | | | | reg32 | | 0x60C |
| offset | | 1548 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| V-CPU debugger read data register  (For debugger only) | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | VPU\_PDBG\_RDATA\_REG | | | ro | ro | | 0x0 | | | To read data to the debugger,  # Write VCPU\_PDBG\_IDX\_REG with RDDBG as 1 and DBGIDX as the register address to be read.  # Read from the specified register to this register.{has\_reset=0} | | | | | |

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|  | | | | | | | | VPU\_PDBG\_STEP\_MASK | | | | | reg32 | | 0x610 |
| offset | | 1552 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Debugger control  (for debugger only) | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:1 | RSVD0 | | | rw | ro | | 0x0 | | | Reserved{has\_reset=0} | | | | | |
| 0:0 | STEP\_MASK\_ENABLE | | | rw | ro | | 0x0 | | | Interrupt Disable at step for debugger{has\_reset=0} | | | | | |

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| End RegGroup |

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| End RegGroup |