ECE335 Introduction to Electronic Devices

Project 1
Simulation of a PN junction

Report Submission Date

18th November 2023

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Introduction

A P-N junction, also known as a semiconductor junction, is a fundamental component in electronics and semiconductor devices. It is formed by joining a P-type semiconductor material which is in excess of positively charged holes with a N-type semiconductor material which holds an excess of negatively charged electrons. The combination of the above two semiconductor materials creates the P-N junction.

For this project we are making use of the TCAD software Sentaurus by Synopsys in order to simulate our very own PN junction and produce the necessary outputs for the given questions.

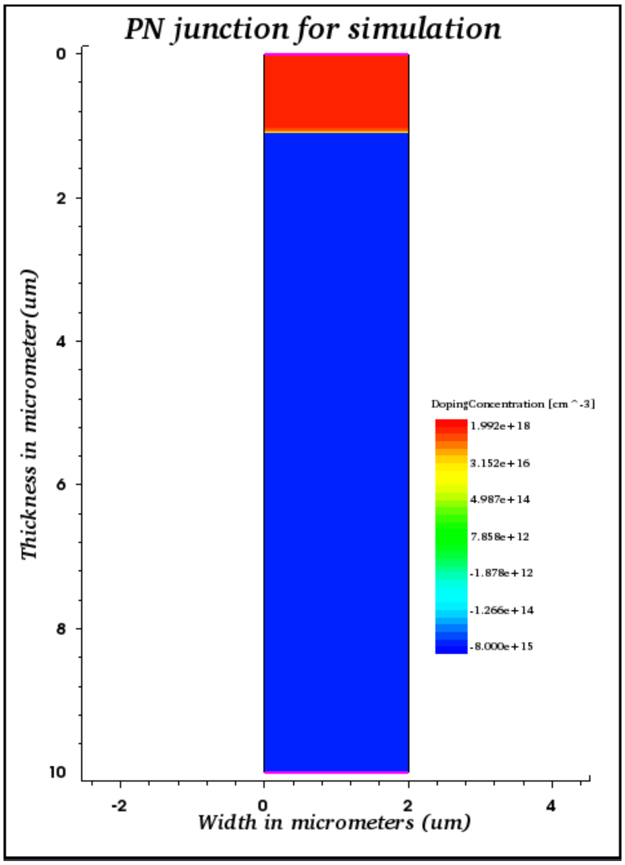


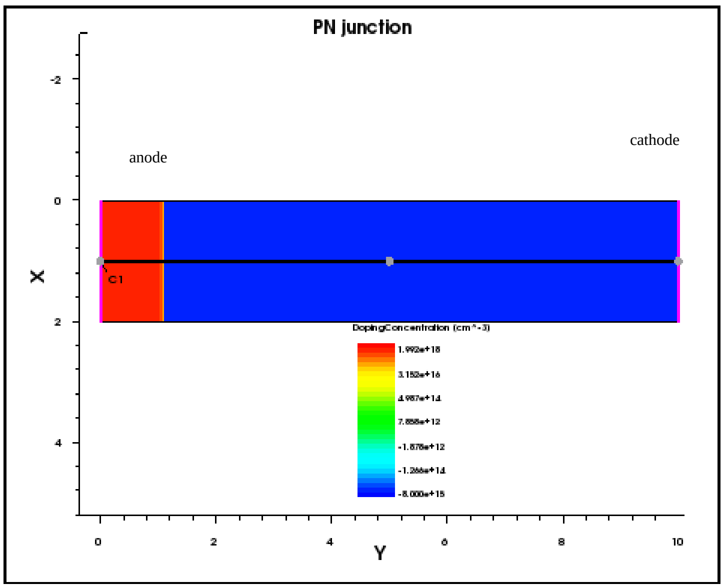
Figure 1: PN junction simulation in Sentaurus with N+(red region) and P(blue region)

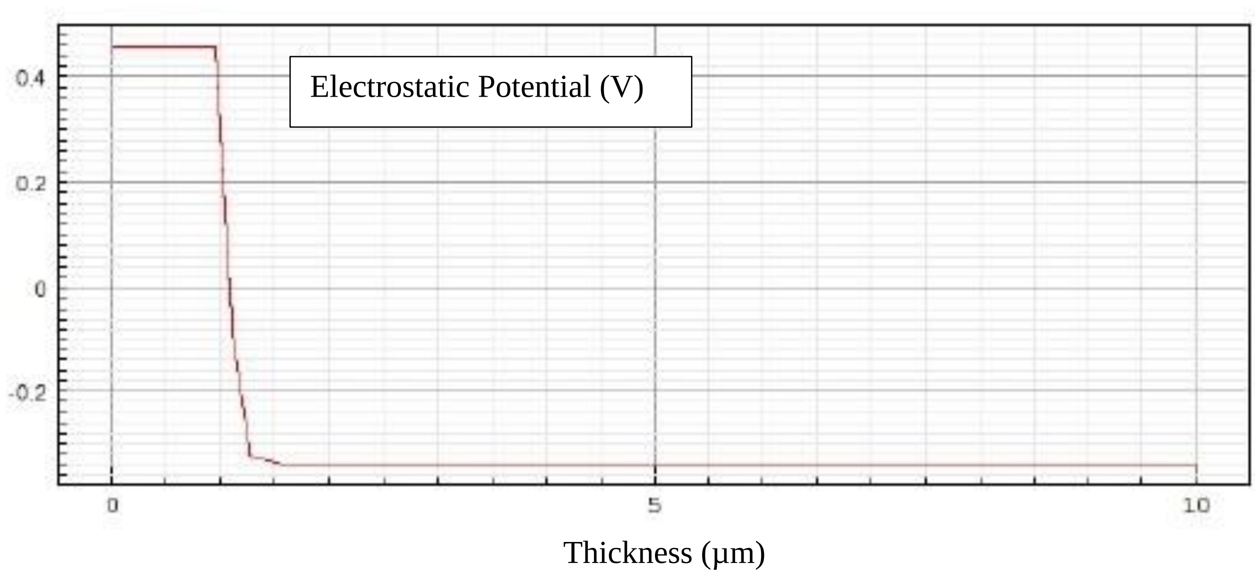
The above simulation of the PN junction consists of the N+ region having a concentration $N_d = 2 \times 10^{18}$ cm^{-3} and the P region having a concentration $N_a = 8 \times 10^{18}$ cm^{-3}. The total device depth is 10 µm while the junction depth is 1 µm.

1.Zero Bias Uniform Doping Profile

1.1)1D Electrostatic Potential Plot

The following graphs have been simulated by making an X-cut through the middle of the above PN junction with the built-in tool in the Sentaurus simulation window.





When observed closely the potential is 0.47 – (-0.32) = 0.79V.

The depletion width is 1.3 – 0.95 = 0.35µm.

1.2)Calculation for Built-in Potential and W_{dep}

The built-in potential and the depletion regions can be calculated by using the following equations where W is the depletion region width an V_{bi} is the built-in potential.

$$W = \sqrt{\frac{2\varepsilon_S(V_{bi} + V_R)}{q}\frac{N_A + N_D}{N_A N_D}} \qquad\qquad V_{bi} = \frac{kT}{q} ln\left(\frac{N_A\, N_D}{n_i^2}\right)$$

For V_{bi} we use the following values:

$$0.029 \times \ln\left(\frac{2\ \times 10^{18}\,.\ 8\ \times 10^{15}}{(1\ \times 10^{10})^2}\right)$$

and get theoretical V_{bi}= 0.95V

For W we use the same values used for the above and the V_{bi} value calculated and get the theoretical W = 0.393µm.

The built-in potential from the graph is less than the theoretical calculation for the built-in potential as the junction may not exactly be split in the middle and also, we assume no limit to the junction length when calculating the theoretical value. There is a sizeable difference in the depletion width which may occur due to errors in exactly pinpointing the points on the graph itself.

2.Reverse Bias

2.1)IV Plot

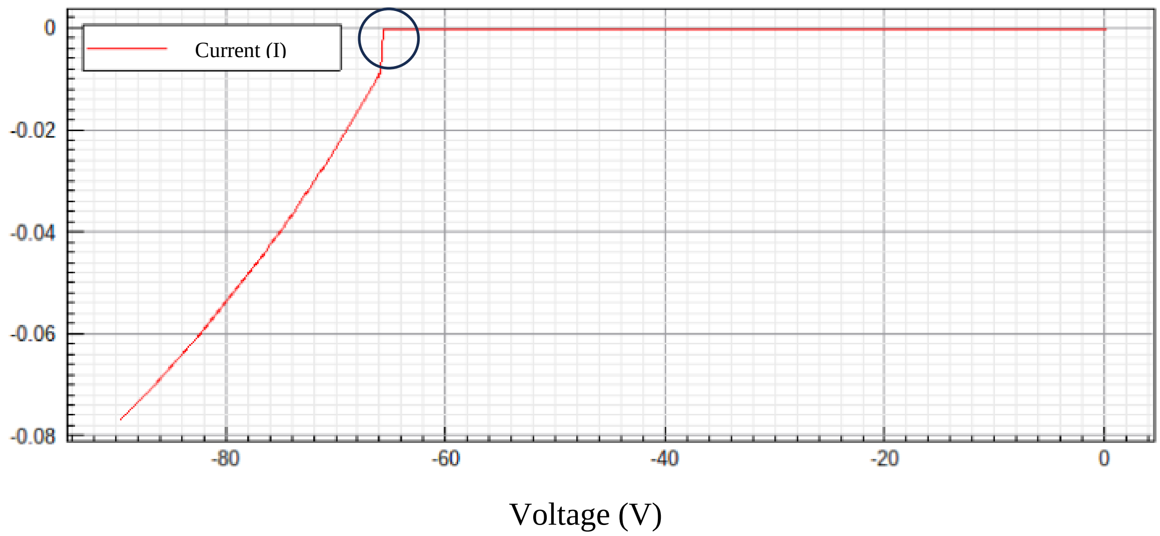


Figure 2.1.1:The above diagram shows the I-V plot for the reverse bias simulation.

When looking at the graph it is evident that the breakdown voltage starts at around -75V as highlighted above.(Negative value due to reverse bias).

Now let's compare the value obtained with the graph below.

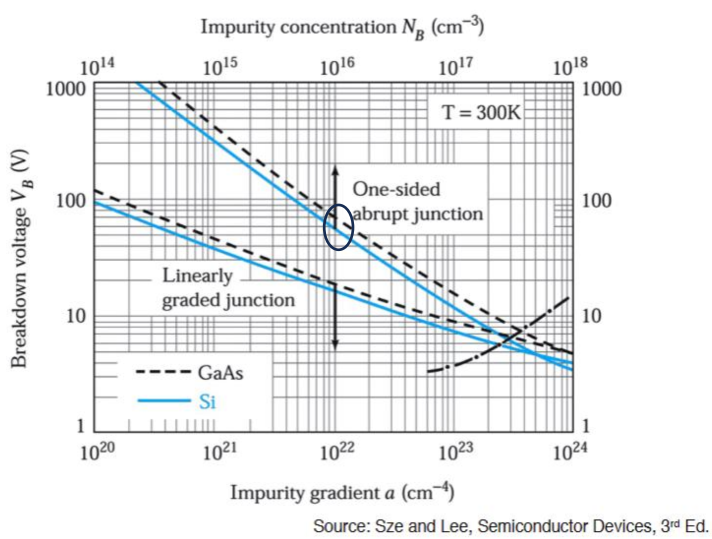


Figure 2.1.2

As circled above we can see that the -75V value we obtained is correct and thus we can use it to calculate the maximum electric field in the junction. We use the following equation and the values obtained above from the graph and V_{bi}.

$$\mathcal{E}_{crit} = \frac{qN_D}{\varepsilon}\sqrt{\frac{2\varepsilon_S(V_{bi}+V_B)}{q}\frac{1}{N_D}}$$

Thus, we get the maximum electric field before breakdown as 427876 V/cm.

3.Forward Bias

As we have already learned regular diodes have a threshold voltage. In simpler terms, any voltage above this value will produce a current through the diode. The threshold voltage of regular diodes is known as 0.7V. Below is the IV graph obtained when a voltage between 0 - 1V passes through it.

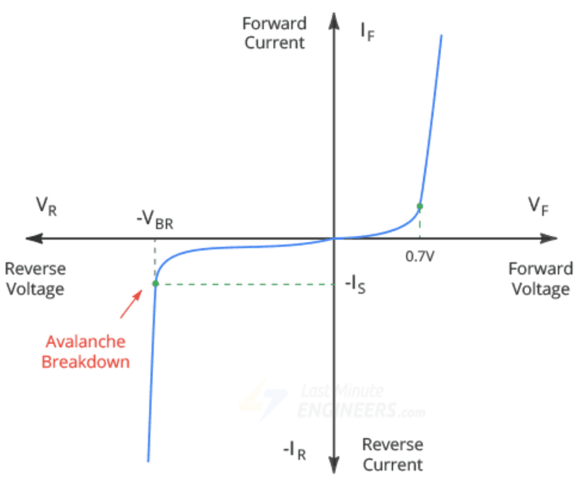


Figure 3.1 [1]

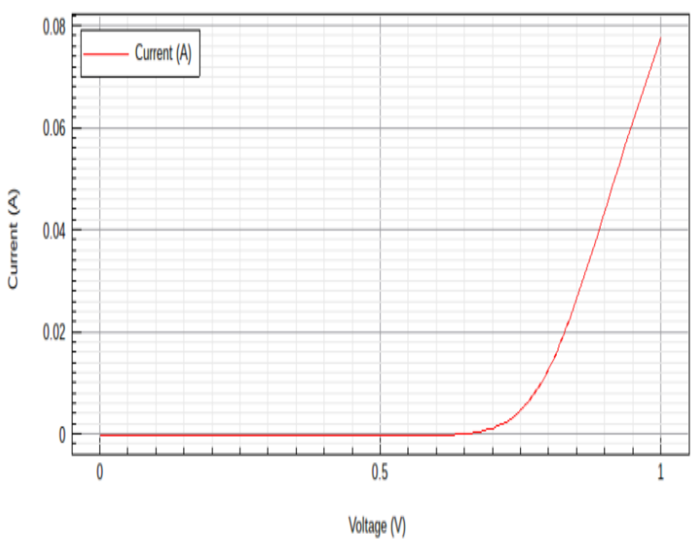


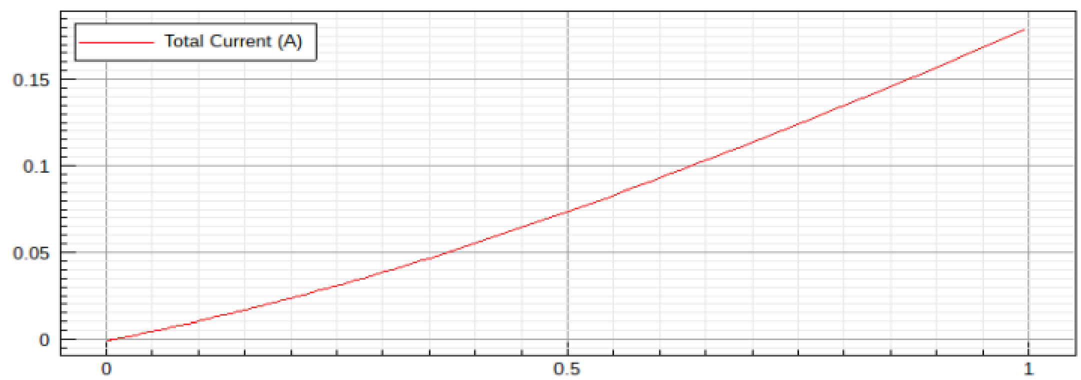
Figure 3.2

Image 3.1 depicts the IV characteristics of a Diode, and we can see the same reciprocated in Image 3.2 where we can see that current is recorded starting at approximately V=0.7V. This is mainly due to the potential barrier at the P and N junction (depletion region). This barrier is formed due to the energy difference between the electrons and holes and is responsible for an energy drop of about 0.7V. Once this barrier is passed then drift current can occur hence the above IV characteristics.

4.High Temperature Simulation

4.1)Voltage from 0-1V Forward Bias

At the temperature set to T=600K, we can observe the below IV graph from 0-1V.



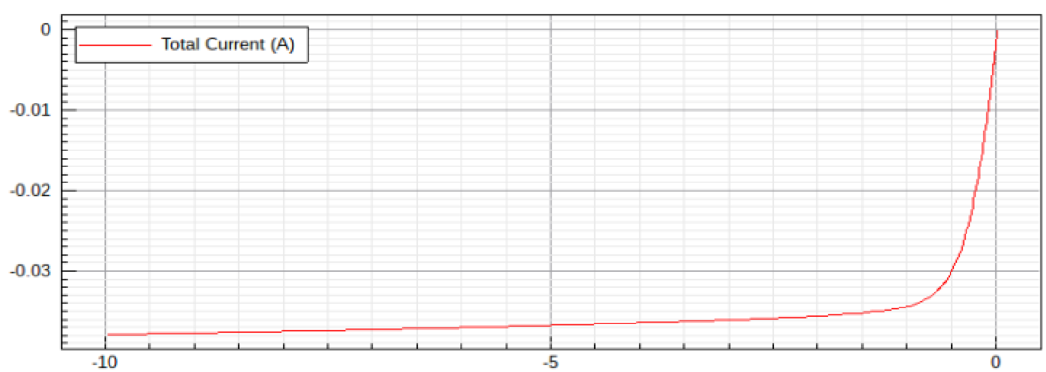
Voltage (V)

It can be said that at 600K the higher temperatures contribute to higher carrier mobility thus the current will exponentially increase with respect to the following diode equation.

$$I = I_0\left(e^{\frac{eV}{kT}} - 1\right)$$

4.2)Voltage from -10V-0V Reverse Bias

At the temperature set to T=600K, we can observe the below IV graph from -10V-0V.



Voltage (V)

Similar to the forward bias the increase in temperature will contribute to higher carrier mobility. Due to this it can be seen that the reverse current slightly increases as voltage decreases from 0 to -10V.

5.Gaussian Doping

Below is the graph depicting the built-in potential of the Gaussian Doped junction.

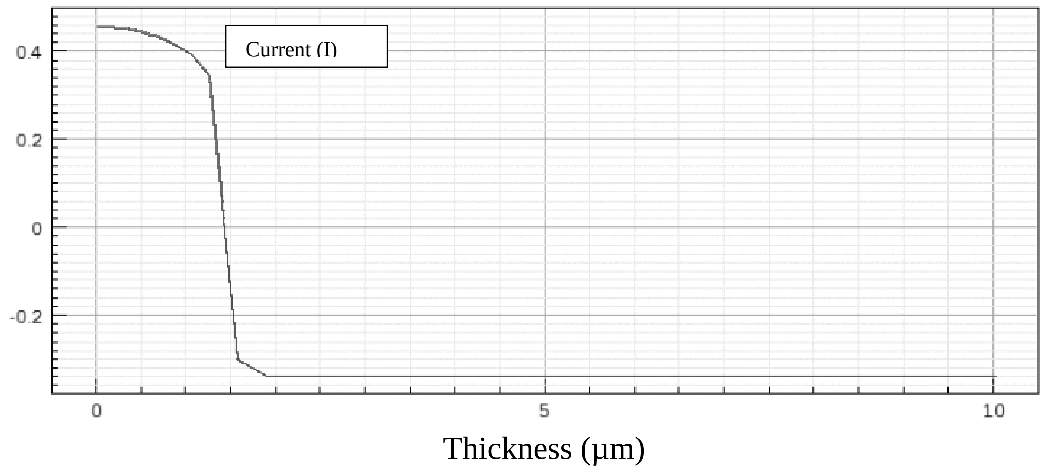


Figure 5.1

By using the same technique as part 1 we can estimate the built-in potential and the depletion width.

When observed closely the potential is 0.46 – (-0.33) = 0.79V.

The depletion width is 1.57 – 1.26 = 0.31μm.

Overall Comparison

	Part 1 Estimation	Part 5 Estimation	Theoretical Calculation
Built in Potential (V)	0.79	0.79	0.95
Depletion Width (μm)	0.35	0.31	0.393

Figure 5.2

Built-in potential comparison

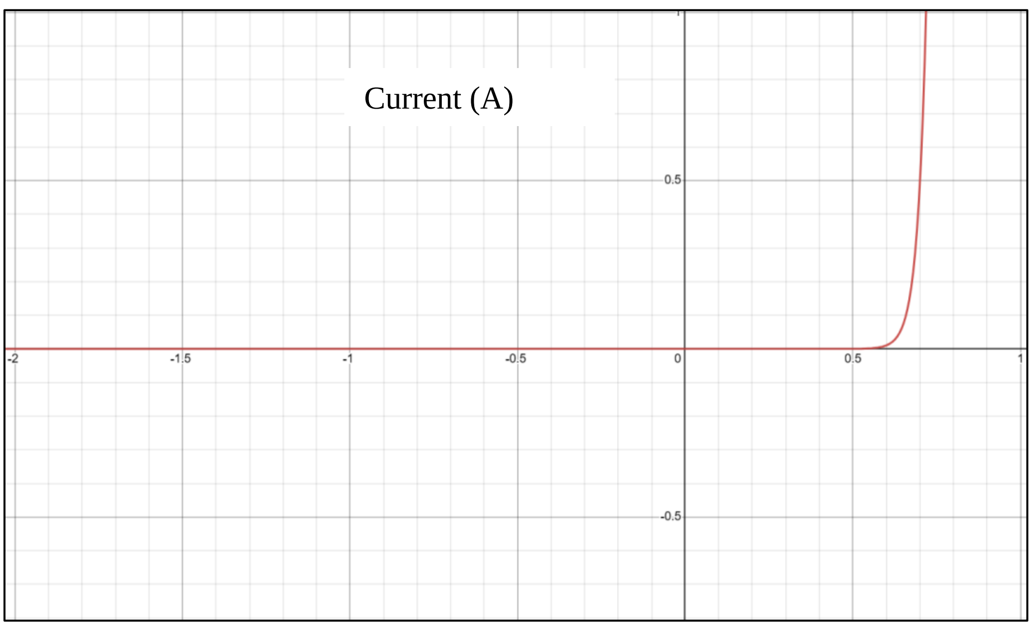
The above estimated built-in potential is the same as that estimated in part 1 and hold the same difference in value when compared to the calculated built in potential in Part 1 of 0.95V.

Depletion Width comparison

The above estimated depletion width of the Gaussian diode is slightly lower in value when compared to the value estimated in Part 1 and is noticeable different with respect to the theoretical depletion width calculated in Part 1 which is 0.393µm.

5.2 IV Characteristics

The IV characteristics remain the same as the previous graph with the threshold voltage at 0.7V. The only difference that is noticeable is in the axes as the below graph extends to -2V.



Voltage (V)

Figure 5.2.1: IV graph

Conclusion

The above report has been compiled with respect to the project and portray my though process and results obtained throughout the simulations. The document was compiled in order to assist the understanding of the P-N junction and how Sentaurus simulations can be interpreted.

References

[1] *B-cdn.net*, 2023. https://lastminuteengineers.b-cdn.net/wp-content/uploads/basic/Diode-IV-Characteristics.png (accessed Nov. 19, 2023).