ECE335 Introduction to Electronic Devices

# Project 2

## Design a Deep Submicron NMOS

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# Introduction

This report provides a concise exploration of the fundamental principles, technical characteristics, and design considerations associated with transistors, with a specific focus on deep micron NMOS (Negative Metal-Oxide-Semiconductor) transistors. Transistors are pivotal components in electronic devices, serving as the building blocks for integrated circuits. The evolution of transistor technology, particularly the advent of deep micron NMOS transistors, plays a crucial role in advancing the performance and miniaturization of semiconductor devices.

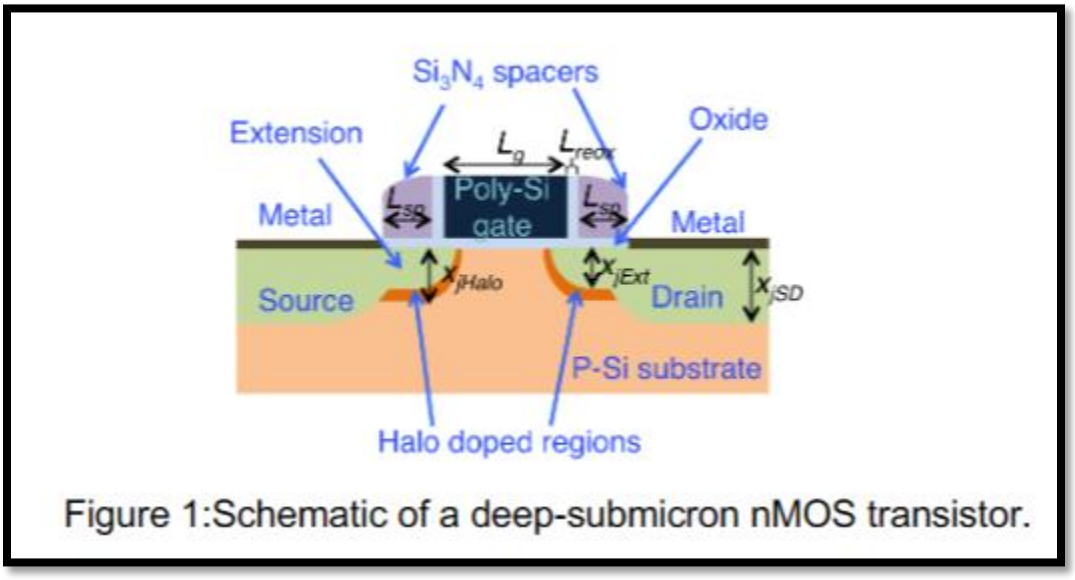

Figure 1:Schematic of a deep-submicron nMOS transistor.

# Section A: Background Research

1.)

| Feature | Feature Explanation | Purpose of Feature | Affect on Transistor Operation |
|---|---|---|---|
| Extension Doping | Extension doping refers to the intentional doping of semiconductor material in the extension region of a transistor. | - Mitigate Short-Channel Effects.<br>- Control Threshold Voltage. | Extension doping in a transistor affects its operation by modulating the electric field in the |

| | | | |
|---|---|---|---|
| | | - Optimize Transistor Performance.<br>- Reduce Reverse Short-Channel Effects. | channel region, influencing key parameters such as the threshold voltage. This modulation helps mitigate short-channel effects, optimize transistor performance, and reduce the impact of process variations. |
| Halo Doping | Halo doping is a semiconductor fabrication technique involving the intentional introduction of dopants into specific regions of a transistor structure, typically in the vicinity of the source and drain regions. | - Mitigate Short-Channel Effects.<br>- Suppress Drain-Induced Barrier Lowering (DIBL).<br>- Improve Junction Leakage Control.<br>- Enhance Transistor Performance.<br>- Prevent Lateral Encroachment. | Halo doping in a transistor influences its operation by adjusting the doping concentration around the source and drain regions. This modification helps control the threshold voltage, mitigates short-channel effects, and suppresses phenomena like drain-induced barrier lowering (DIBL). |
| Spacer | A spacer is a thin layer of material deposited on the sidewalls of the gate structure of a MOSFET. | - Dimensional Control.<br>- Dopant Profile Control. | Spacers in a transistor affect its operation by providing precise dimensional control, especially in defining |

| | | | |
|---|---|---|---|
| | | - Isolation Between Features. | the width of critical features like the gate. They contribute to mitigating short-channel effects, influencing the effective channel length, and optimizing the dopant profile during source and drain formation. |

Table 1: Research on extension doping, halo doping and spacers.[1][2]

2.)

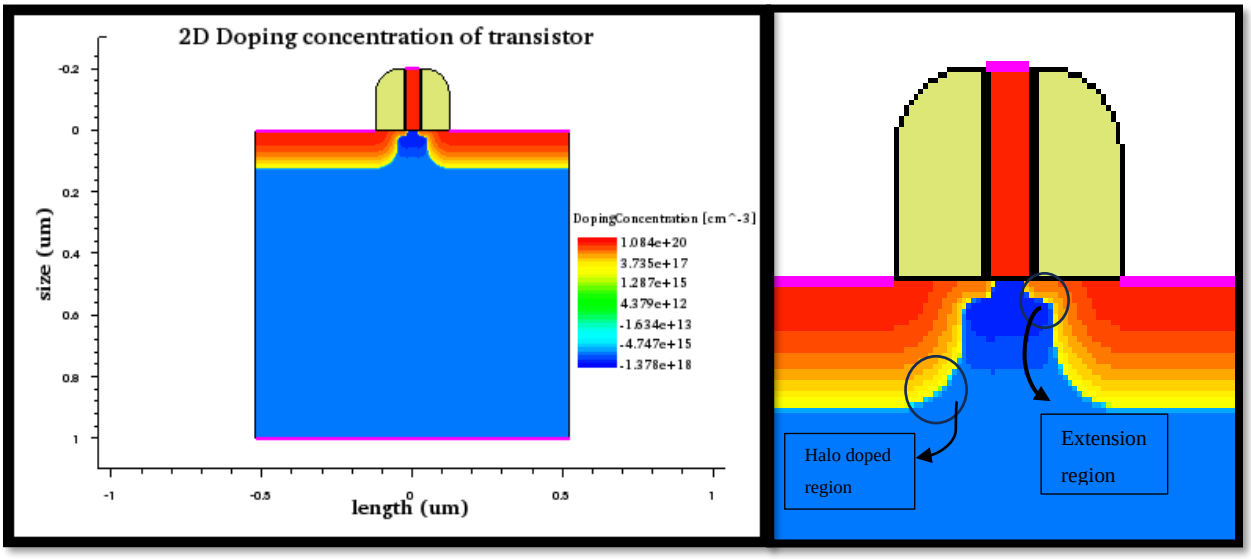


Figure 2: Images depicting 2D doping concentrations of a 0.045nm length NMOS transistor and the halo and extension regions of the transistor.

The halo doped region and extension region in Figure 2 has been identified and labelled with respect to Figure 1 which depicts a deep micron NMOS transistor.

3.)

| | |
|---|---|
| LP | Low Power |
| G | General Purpose |
| HS | High Speed |
| IO | Input/Output |
| HVT | High Voltage Transistor |
| LVT | Low Voltage Transistor |

Table 2: Acronyms and what they stand for.

4.)

| Current State | Advantages |
|---|---|
| Higher Ion | The stronger current flow during the ON state of the transistor leads to improved performance of transistor as well as providing better switching speeds. |
| Lower Ioff | The lower current flow during the OFF state of the transistor leads to reduced power consumption as well as providing enhanced standby performance. |

Table 3: Changes to current states and their advantages.

The above statements reflect in the Table 1 of the TSMC paper as we can see that for LP transistors you can see very low Ioff levels thus indicating improved power efficiency whilst for HS transistors, it can be seen to have higher Ion values thus leading to better performance.

# Section B: Design

1.) The NMOS transistor portrayed below has been carefully designed in order to follow the set restrictions of Ioff ≤ 35 nA/μm and Ion ≥ 700 uA/μm. The transistor parameters such as the substrate doping concentration, halo and extension doping , gate oxide thickness and source-drain depth have been calculated carefully with clear explanations as you progress through this report.

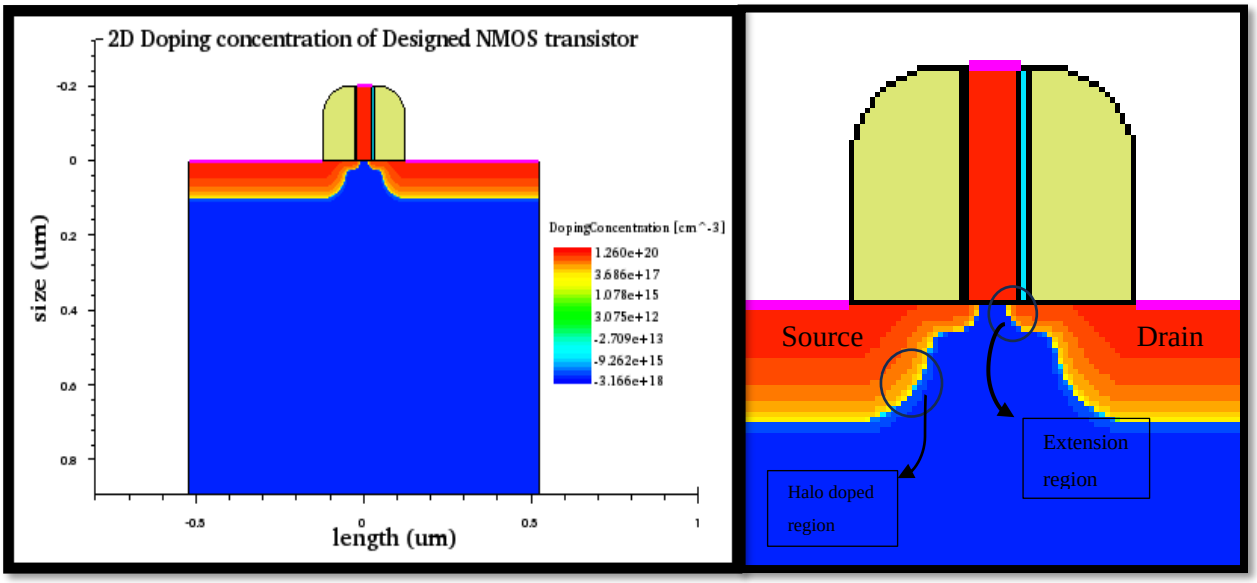


Figure 3: Images depicting the 2D doping concentration of the designed transistor as well as a magnified version of it showcasing the source, drain, halo, and extension doped regions.

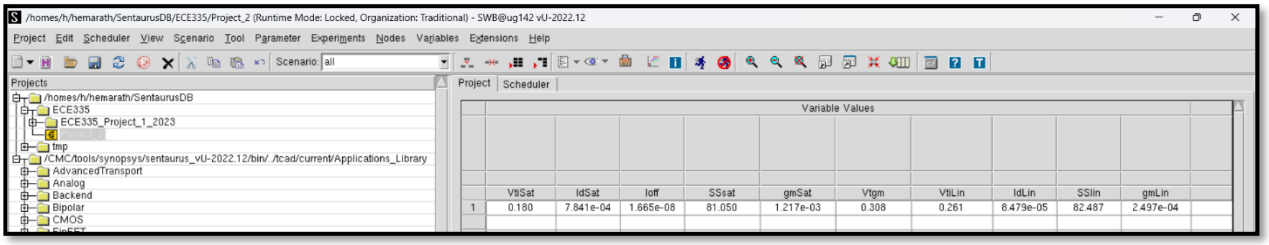


Figure 4: Snapshot of Sentaurus workbench showing device specifications for the designed transistor.

| VtiSat | IdSat | Ioff | SSsat | gmSat | Vtgm | VtiLin | IdLin | SSlin | gmLin |
|---|---|---|---|---|---|---|---|---|---|
| 0.180 | 7.841e-4 | 1.665e-8 | 81.05 | 1.217e-3 | 0.308 | 0.261 | 8.479e-5 | 82.49 | 2.497e-4 |

Table 4: Table containing above snapshot values for clarity.

Therefore, as presented above it is visible that the Ioff value of $1.665 \times 10^{-8}$ and the Ion value of $7.841 \times 10^{-4}$ falls within the requirements for the design. In order to achieve the above results, the following parameters were used.

| Parameter Modified | Value |
|---|---|
| Substrate Doping | $1.6 \times 10^{18}$ |
| Halo Doping | $2.4 \times 10^{18}$ |
| Extension Doping | $3.0 \times 10^{19}$ |
| Gate Oxide Thickness | 1nm |
| Source-Drain Junction Depth | 0.1 µm |

Table 5: Table with the modified parameters.

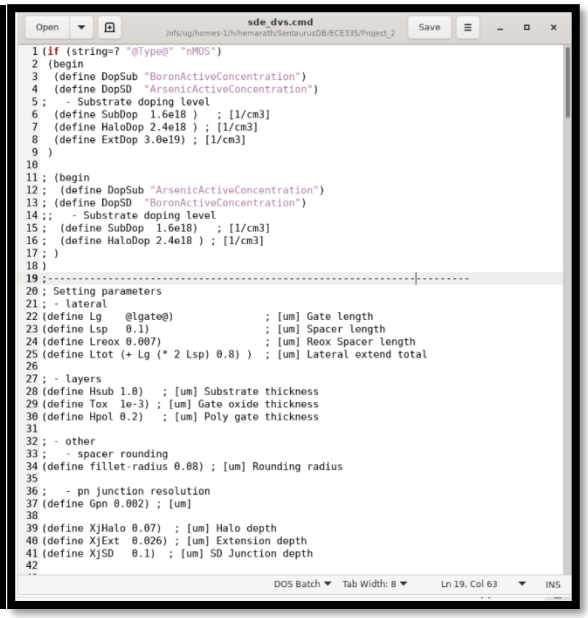


Figure 4: Modification for the sde_dvs file.

2.) There were a couple of methods which I tried to implement in order to come up with the above parameters that provide a feasible design.

Method 1: Make use of the equations to come up with parameter values that provide the necessary result. The following equation was taken to account initially, but the methodology was discarded as there were way too many unknowns to come up with an accurate solution.

$$I_{on} = \frac{1}{2}\mu C_{ox}\frac{w}{L}\left(v_{gs} - v_{th}\right)^2$$

Method 2: Observe changes to Ion and Ioff with respect to changes in each parameter and come up with possible values from the noted changes. For each parameter the first change was done via an educated guess in order to note down how the currents behaved. The procedure is explored below:

Change in Substrate Doping

Initially I experimented with substrate doping concentrations of around $1.4x10^{17} – 1.6x10^{17}$ and noted that Ion slightly increases and Ioff slightly decreases as the concentration increased. Then I decided to see the effects of increasing the value close to that of halo doping concentration. The above increase paid dividends as Ion value increased significantly whilst the Ioff value decreased. It was also noted that as the substrate concentration increases past the halo doping concentration there were errors that occurred thus pointing me towards the halo doping concentration for the next modification. As I was confident that the halo doping concentration needed modification, the substrate concentration value was left at $1.6x10^{18}$.

Change in Halo Doping

Taking the above results and trend into account, my initial guess was to observe the results as the halo doping concentration doubled to $3.0x10^{18}$. It was seen that both Ion and Ioff reduced by large amounts. The above test concluded that as halo doping concentration increased, both the state current decreased and Ion was negatively affected. Thus, I decided to experiment with a similar range of around $2.4x10^{18} – 2.6x10^{18}$ as I did with substrate doping. Keeping within the bounds of the above range, it was evident that having the halo doping concentration at $2.4x10^{18}$ provided us with the best results although Ion was still out of the acceptable range.

Change in Extension Doping

After the above changes, the remaining goal is to increase the Ion value such that it is within the acceptable range. We try to tackle this by increasing the extension doping concentration. As above I started by doubling the extension doping value. The above change provided positive feedback as it was evident that the Ion value increased. Thus, I continued increasing the extension doping value, until the Ion value was within the acceptable range. This occurred at a concentration of $3.0x10^{19}$ but the Ioff value was now out of the acceptable range.

Obtaining feasible Ioff Value

After completing the above steps, it was evident that Ioff had to be reduced to meet the requirements. As the handout has a range provided for the oxide thickness, I decided to start of with the lower bound of the given range 1nm. Fortunately, simulating with the above value provided the result of a lowered Ioff value. After that I decided to experiment the effects of

reducing the source-drain depth hoping for a reflection of the above result. As I lowered the source-drain depth Ioff value decreased but as the value approached 0.1 µm I noticed that the Ion value was close to its accepted boundary value. At this stage both my Ion and Ioff values were within range. Therefore, I decided to conclude further experimenting and make use of the above values.

3.) The following graphs portray the $I_d$ vs $V_{gs}$ for the designed transistor in linear and saturation regimes.

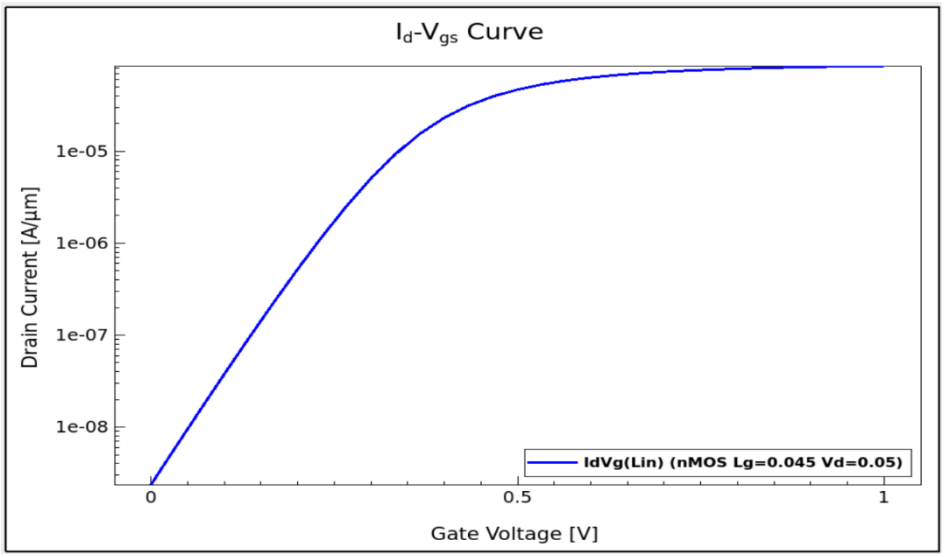


Figure 5: $I_d$ vs $V_{gs}$ graph for Vds = 50 mV (low drain voltage, linear regime)

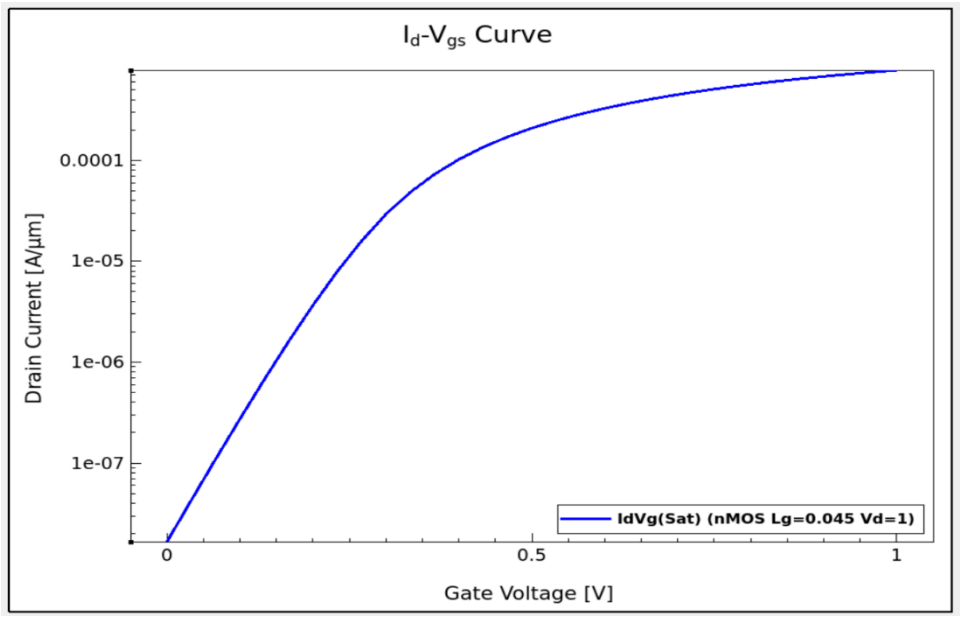


Figure 6: $I_d$ vs $V_{gs}$ graph for Vds = Vdd (saturation regime)

4.) For our current design it can be seen that the SSlin is 82.487mV/dec and SSsat is 81.050mV/dec. Thus, it is evident that both the subthreshold swings are lower than 100mV/dec, thereby meeting the transistor specification in the TSMC paper. Furthermore, when comparing our Vtlin and Vtsat values with that found in Figure 4 of the TSMC paper it is evident that both the values we obtain are higher in value. This may occur due to further optimization of the design by TSMC as well as differences in doping material used for the doping processes.

5.) Drain Induced Barrier Lowering (DIBL): When the drain voltage rises in metal-oxide-semiconductor field-effect transistors (MOSFETs), a phenomenon known as Drain Induced Barrier Lowering, or DIBL, takes place. It describes how the influence of the drain voltage lowers the energy barrier between a MOSFET's source and drain regions.[3]

Effect on Transistor: DIBL causes the transistor's effective channel length to decrease as the drain voltage rises. The threshold voltage (Vt) drops as a result of this reduction in effective channel length, which may cause a decline in transistor performance. Reduced on/off current ratios, higher subthreshold leakage current, and a less distinct transition between the on and off states are all possible effects of lower threshold voltages.[3]

The DIBL of the design can be calculated with the following equation:

$$DIBL = -\frac{V_{Th}^{DD} - V_{Th}^{Low}}{V_{DD} - V_{D}^{low}}$$

Design parameter values:

$V_{Th}^{DD}$ = 0.261V

$V_{Th}^{Low}$=0.180V

$V_{DD}$=1V

$V_{D}^{low}$=0.05V

$$DIBL = \frac{0.261 - 0.180}{1.00 - 0.05} mV\ /\ V$$

Therefore, for our design we get a DIBL value of **85.263mV/V**.

6.)

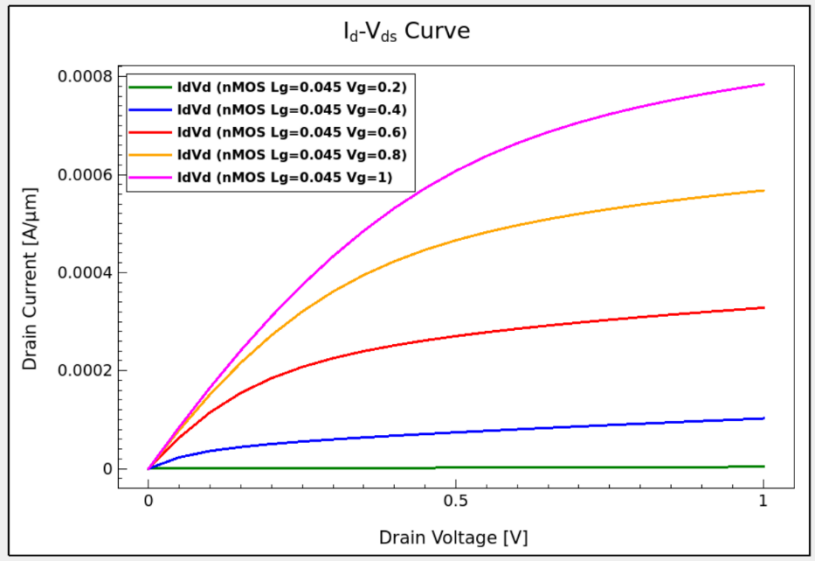


Figure 7: Ids vs. Vds for Vgs = 0.2, 0.4, 0.6, 0.8, and 1.0V for 0 ≤ Vds ≤ Vdd

In the above graph for the curve where Vg=0.2V there is almost no drain current for drain voltage changes indicating the transistor is always going to be in cutoff mode. For all the other curves the transistor operates in two modes, saturation and linear. The linear region can be identified from the linear slope of the curve whereas the saturation region can be identified where the current tends to get flattened out. It can also be seen that the current line is not horizontal at the end of the curve thus the transistor does not follow the ideal square law dependence of an ideal MOSFET. This can happen due to short channel effects and existence of velocity saturation in the designed transistor.

## Conclusion

The above document acts as a report to show the characteristics of a deep submicron NMOS and the design steps taken to design a transistor in Sentaurus for given requirements. It also portrays the characteristics of a NMOS transistor and its behaviour to parameter changes.

References

[1] Raised source/drain MOSFET with dual sidewall spacers | IEEE journals ..., https://ieeexplore.ieee.org/document/75721/ (accessed Dec. 6, 2023).

[2] Wikipedia Contributors, “Doping (semiconductor),” Wikipedia, Sep. 27, 2019. https://en.wikipedia.org/wiki/Doping_(semiconductor)

[3] “Drain-induced barrier lowering,” Wikipedia, Mar. 13, 2023. https://en.wikipedia.org/wiki/Drain-induced_barrier_lowering (accessed Dec. 06, 2023).