Danmarks Tekniske Universitet DTU

Gb Ethernet Switch Specification

34349: FPGA design for Communication Systems
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Group

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Contents

1 Ethernet protocol and frame format

The Ethernet frame is received in octets and it is formatted like shown in Figure 1:

Preamble	SFD	Destination MAC	Source MAC	Length/ Type	Data (Payload)	FCS
7 bytes	1 byte	6 bytes	6 bytes	2 bytes	42-1497 bytes	4 bytes

Figure 1: Ethernet 802.3 Raw Frame Format

The Destination MAC Address (6 bytes) and Source MAC Address (6 bytes) identify the recipient and sender, respectively. The Payload/Data (42–1497 bytes) carries the actual data, and the Frame Check Sequence (FCS) (4 bytes) provides a CRC (Cyclic Redundancy Check) value. In Table 1 are the descriptions of each field:

Field	**Size**	**Description**
Preamble	7 bytes	Pattern of alternating 1s and 0s (10101010...) that allows devices to synchronize
SFD (Start Frame Delimiter)	1 byte	10101011 - indicates the start of the frame
Destination MAC Address	6 bytes	Physical address of the destination device
Source MAC Address	6 bytes	Physical address of the source device
Length/Type	2 bytes	Indicates either the length of the data or the protocol type
Data (Payload)	42-1497 bytes	The actual data being transmitted
FCS (Frame Check Sequence)	4 bytes	Cyclic Redundancy Check for error detection

Table 1: Ethernet Frame Field Descriptions

2 Diagram

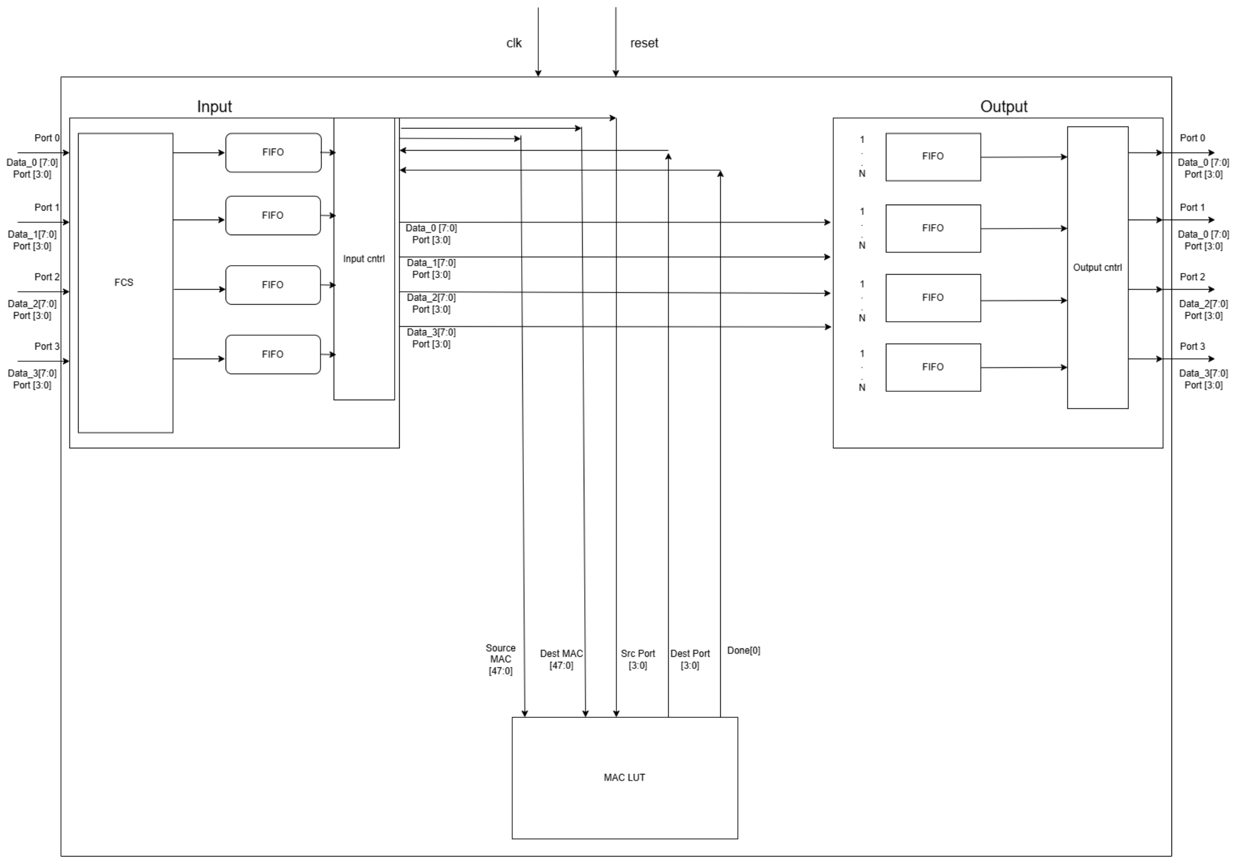

Figure 2: Overview of the Gigabit Ethernet Switch

3 Input

For the input module, there are 4 input ports, each receiving 8 bits of data. The data are then passed to the FCS checker.

3.1 FCS

The parallel FCS checker receives octets of data from the ethernet frame and verifies its validity. The octets are passed simultaneously to the input synchronous FIFOS. If the frame is not valid, then the corresponding FIFO is flushed.

3.2 FIFOs

For each input port, there is one synchronous FIFO of size 4096 bytes (at least twice the size of the ethernet frame). The data from the FIFOs are fed intro the input control module.

3.3 Input Control

The input control module is responsible for distinguishing between the different fields of the frame, communicating with the MAC LUT module and deciding which input fifo will transmit it's data to the output module. The input control will transmit octets of data to the output module as well as information about the output port given by MAC LUT.

4 MAC table + learning

The MAC module contains a dual port RAM of size 8192 x Address size (48 bits) + Port (4 bits). Inside MAC module there exists a submodule responsible for hashing. The hashing algorithm used is the Jenkins Hash due to its simplicity, performance and collision avoidance [1]. The MAC module performs two operations :

- Learning Phase: During the MAC learning phase the source address is given as input and hashed with the Jenkins algorithm. The result is used as an index to the table where the port that the packet was received as well as the address are stored.
- Forwarding Phase : In the forwarding phase the destination address is hashed to produce the index to the look up table. If an entry is found, the packet is transmitted to all possible ports. Otherwise, it is transmitted to the port corresponding to the entry.

The 4-bit port signal is determined as follows:

- 0000 : Transmit to port 0
- 0001 : Transmit to port 1
- 0010 : Transmit to port 2
- 0011 : Transmit to port 3
- 1111 : Broadcast to all ports

5 Switch fabric + output queues

To minimize Head-Of-Line(HOL) blocking, we will use a cross-point queuing switch.

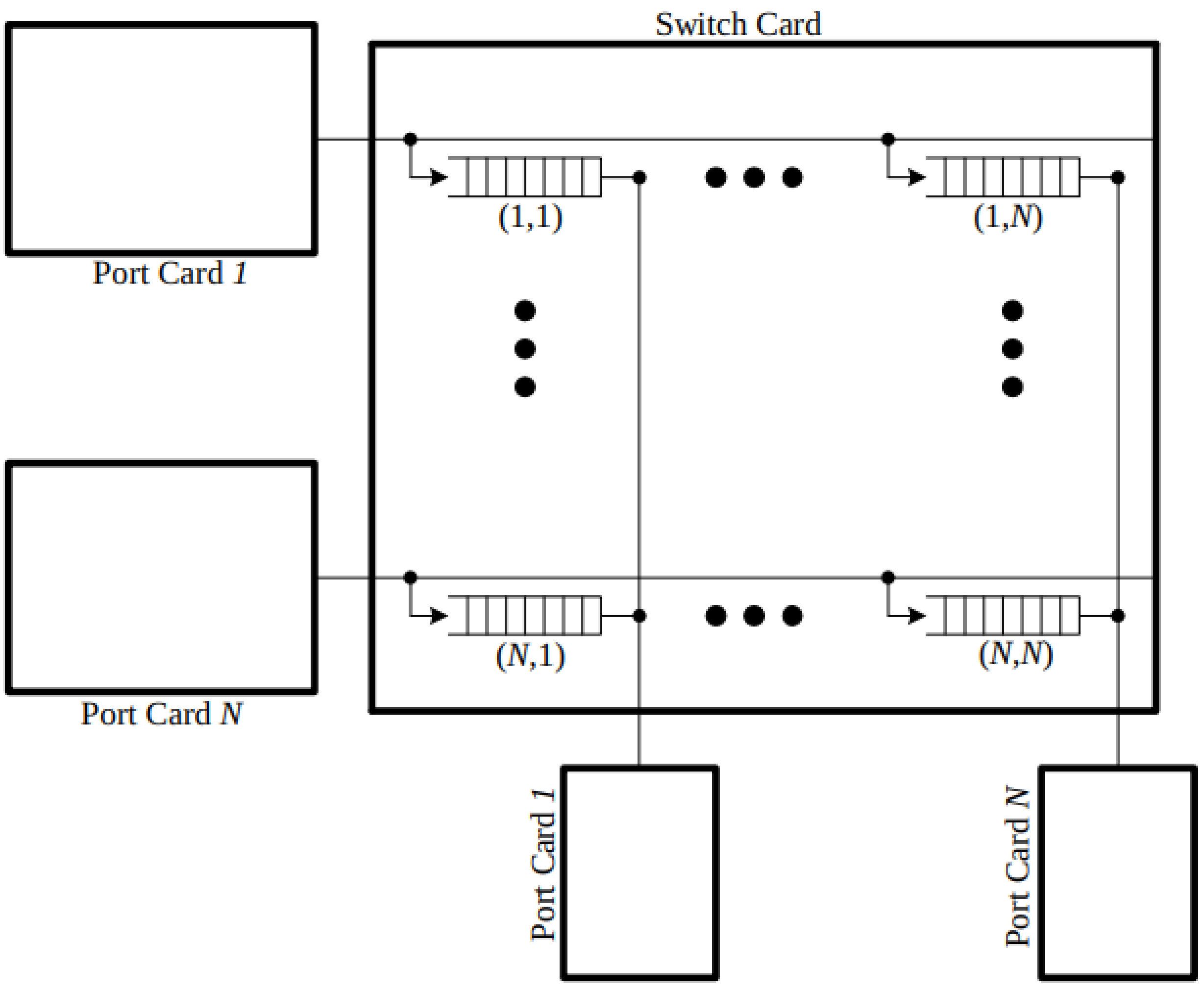

Figure 3: Cross-point Queuing

Packets will arrive on the corresponding input line of the cross-point from the input control. As shown in Figure 3 the queuing occurs at the cross-points themselves. For this design we will use 4096 byte FIFO's at the input ports to ensure availability.

References

[1] F. Yamaguchi and H. Nishi, “Hardware-based hash functions for network applications,” pp. 1–6, 12 2013.