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December 2014

FSA642
Low-Power, Three-Port, High-Speed MIPI Switch

Features

- Low On Capacitance: 7.0 pF Typical
- Low On Resistance: 7.0 Ω Typical
- Wide -3db Bandwidth: 1 GHz Typical
- 24-Lead UMLP (2.5 x 3.4 mm) Package
- 8 kV ESD Rating; >16 kV Power/GND ESD Rating

Applications

- Dual Camera Applications for Cell Phones
- Dual LCD Applications for Cell Phones, Digital Camera Displays, and Viewfinders

Description

The FSA642 is a bi-directional, low-power, high-speed analog switch. The pin out is designed to ease differential signal layout and is configured as a triple-pole, double-throw switch (TPDT). The FSA642 is optimized for switching between two MIPI devices, such as cameras or LCD displays and on-board Multimedia Application Processors (MAP).

The FSA642 is compatible with the requirements of Mobile Industry Processor Interface (MIPI). The low-capacitance design allows the FSA642 to switch signals that exceed 500 MHz in frequency. Superior channel-to-channel crosstalk immunity minimizes interference and allows the transmission of high-speed differential signals and single-ended signals, as described by the MIPI specification.

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FSA642UMX	JG	-40 to +85°C	24-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 2.5 x 3.4 mm

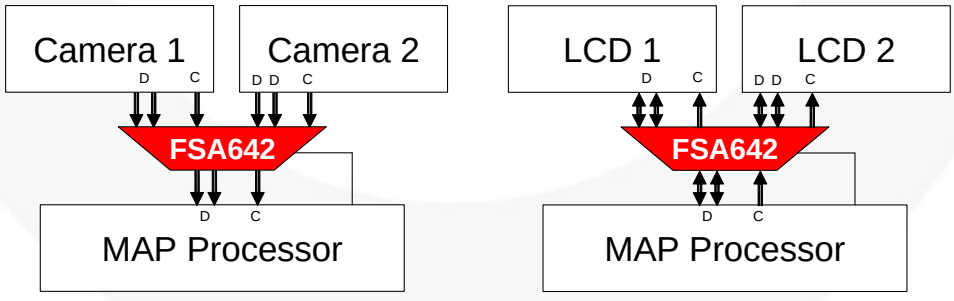


Figure 1. Application Block Diagram

Pin Configuration

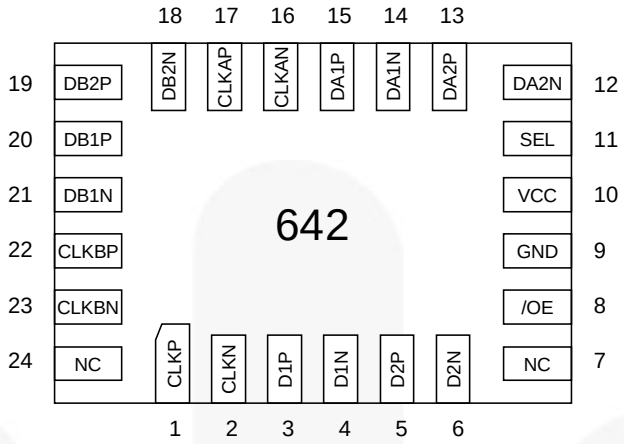


Figure 2. Pin Configuration (Top Through View)

Pin Definitions

Pin #	Name	Description
1, 2	CLKP, CLKN	Clock Path (Common)
3, 4	D1P, D1N	Data Path 1 (Common)
5, 6	D2P, D2N	Data Path 2 (Common)
7, 24	NC	No Connect (Float)
8	/OE	Output Enable (Active Low)
9	GND	Ground
10	VCC	Power
11	SEL	Select (0=A, 1=B)
12, 13	DA2N, DA2P	Data Path (A2)
14, 15	DA1N, DA1P	Data Path (A1)
16, 17	CLKAN, CLKAP	Clock Path (A)
18, 19	DB2N, DB2P	Data Path (2B)
20, 21	DB1P, DB1N	Data Path (1B)
22, 23	CLKBP, CLKBN,	Clock Path (B)

Functional Diagram

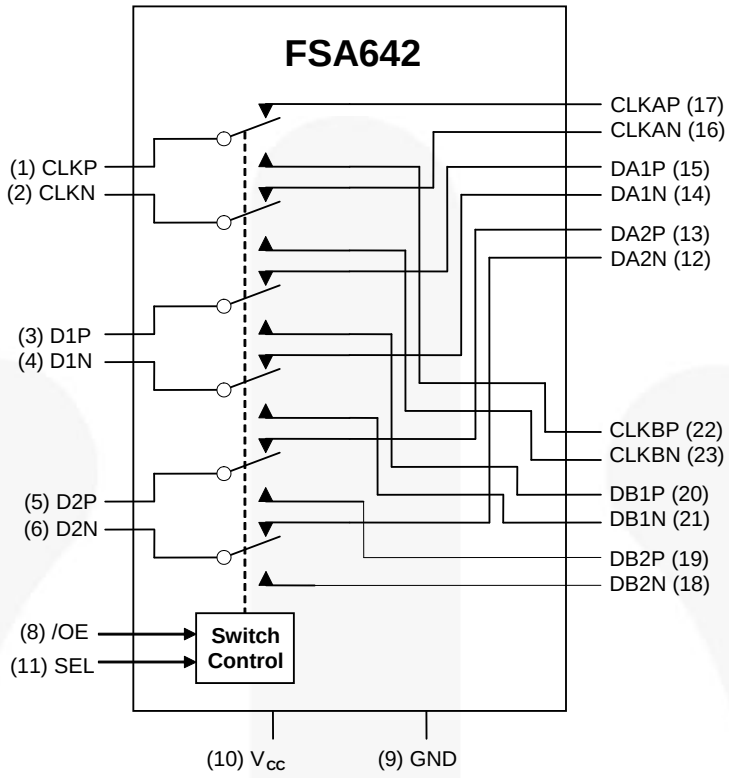


Figure 3. Functional Diagram

Truth Table

SEL	/OE	Function
Don't Care	HIGH	Disconnect
LOW	LOW	D1, D2, CLK=DA1, DA2, CLKA
HIGH	LOW	D1, D2, CLK=DB1, DB2, CLKB

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.50	+5.25	V
V_{CNTRL}	DC Input Voltage (SEL, /OE)[1]		-0.5	V_{CC}	V
V_{SW}	DC Switch I/O Voltage[1]		-0.5	V_{CC} + 0.3	V
I_{IK}	DC Input Diode Current		-50		mA
I_{OUT}	DC Output Current			50	mA
T_{STG}	Storage Temperature		-65	+150	°C
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins		6.5	kV
		I/O to GND		8.0	
		Power to GND		16.0	
	Charged Device Model, JEDEC: JESD22-C101			2.5	

Note:

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.65	4.30	V
V_{CNTRL}	Control Input Voltage (SEL, /OE)[2]	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	-0.5	V_{CC}-1	V
T_A	Operating Temperature	-40	+85	°C

Note:

2. The control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics

All typical values are T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=-40 to +85ºC			Units
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	I_{IN}=-18 mA	2.775			-1.2	V
I_{IN}	Control Input Leakage	V_{SW}=0 to 4.3 V	4.3	-1		1	µA
V_{IH}	Input Voltage High	V_{IN}=0 to V_{CC}	2.650 to 2.775	1.3			V
			4.3	1.7			
V_{IL}	Input Voltage Low	V_{IN}=0 to V_{CC}	2.650 to 2.775			0.5	V
I_{OZ}	Off-State Leakage	A,B=0+0.3 V to V_{CC}-0.3	4.3	-2		2	µA
I_{CC}	Quiescent Supply Current	V_{CNTRL}=0 or V_{CC}, I_{OUT}=0	4.3			1.0	µA
I_{CCT}	Increase in I_{CC} Current Per Control Voltage and V_{CC}	V_{CNTRL}=1.8 V	2.775			1.5	µA

DC Electrical Characteristics, Low-Speed Mode

All typical values are T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=-40 to +85ºC			Units
				Min.	Typ.	Max.	
R_{ON}	LS Switch On Resistance[3]	V_{SW}=1.2 V, I_{ON}=-10 mA, Figure 4	2.65		10	14	Ω
ΔR_{ON}	LS Delta R_{ON}[4]	V_{SW}=1.2 V, I_{ON}=-10 mA (Intra-pair)	2.65		0.65		Ω

Notes:

3. Measured by the voltage drop between A/B and CLK/Dn pins at the indicated current through the switch.
4. Guaranteed by characterization.

DC Electrical Characteristics, High-Speed Mode

All typical values are T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=-40 to +85ºC			Units
				Min.	Typ.	Max.	
R_{ON}	HS Switch On Resistance[5]	V_{SW}=0.4 V, I_{ON}=-10 mA, Figure 4	2.65		7.0	9.5	Ω
ΔR_{ON}	HS Delta R_{ON}[6]	V_{SW}=0.4 V, I_{ON}=-10 mA (Intra-pair)	2.65		0.65		Ω

Notes:

5. Measured by the voltage drop between A, B, and Dn pins at the indicated current through the switch.
6. Guaranteed by characterization.

AC Electrical Characteristics

All values are at R_L=50Ω and R_S=50Ω and all typical values are V_{CC}=2.775V at T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=-40ºC to +85ºC			Units
				Min.	Typ.	Max.	
O_{IRR}	Off Isolation(7)	f=100 MHz, R_T=50 Ω Figure 14	2.775		-35		dB
Xtalk	Non-Adjacent Channel Crosstalk(7)	f=100 MHz, R_T=50 Ω Figure 15	2.775		-55		dB
BW	-3 db Bandwidth(7)	C_L=0 pF, R_T=50 Ω Figure 13	2.775		1.0		GHz
t_{ON}	Turn-On Time SEL, /OE to Output	C_L=5 pF, V_{SW}=1.2 V Figure 6, Figure 7	2.650 to 2.775		20	37	ns
t_{OFF}	Turn-Off Time SEL, /OE to Output	C_L=5 pF, V_{SW}=1.2 V Figure 6, Figure 7	2.650 to 2.775		15	27	ns
t_{PD}	Propagation Delay(7)	C_L=5 pF Figure 6, Figure 8	2.775		0.25		ns
t_{BBM}	Break-Before-Make Time	C_L=5 pF, V_{SW1}=V_{SW2}=1.2 V Figure 12	2.650 to 2.775	3	5	8	ns

Note:
7. Guaranteed by characterization.

AC Electrical Characteristics, High-Speed

All typical values are V_{CC}=2.775V at T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	T_A=-40ºC to +85ºC			Units
			Min.	Typ.	Max.	
$t_{SK(Part\_Part)}$	Channel-to-Channel Skew Across Multiple Parts(8,9)	V_{SW}=0.2 $Vdiff_{PP}$, C_L=5 pF		40	80	ps
$t_{SK(Chl\_Chl)}$	Channel-to-Channel Skew Within a Single Part(8)	V_{SW}=0.2 $Vdiff_{PP}$, C_L=5 pF, Figure 9		15	30	ps
$t_{SK(Pulse)}$	Skew of Opposite Transitions in the Same Differential Channel(8)	V_{SW}=0.2 $Vdiff_{PP}$, C_L=5 pF		10	20	ps

Notes:
8. Guaranteed by characterization.
9. Assumes the same V_{CC} and temperature for all devices.

Capacitance

Symbol	Parameter	Conditions	T_A=-40ºC to +85ºC			Units
			Min.	Typ.	Max.	
C_{IN}	Control Pin Input Capacitance(10)	V_{CC}=0 V		1.5		pF
C_{ON}	Dn/CLK- On Capacitance(10)	V_{CC}=2.775 V, /OE=0 V, f=1 MHz, at 25°C, Figure 11	6.0	7.0	9.0	
C_{OFF}	Dn/CLK Off Capacitance(10)	V_{CC}=2.775 V, /OE=2.775 V, f=1 MHz, Figure 10		2.5		

Note:
10. Guaranteed by characterization.

Test Diagrams

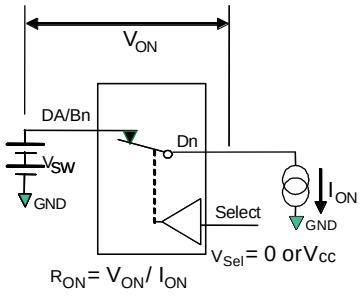
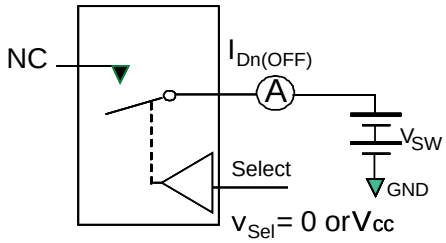
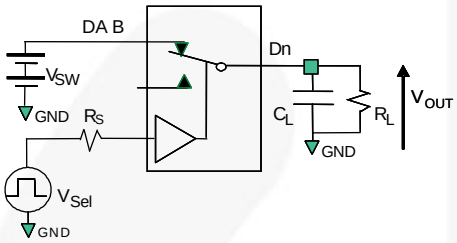


Figure 4. On Resistance



**Each switch port is tested separately

Figure 5. Off Leakage



RL, RS, an CL ar fu ctions of th ap lication environment (se AC Tables for spe ific v lues)
CL inclu es test fixture an stra capacitance

Figure 6. AC Test Circuit Load

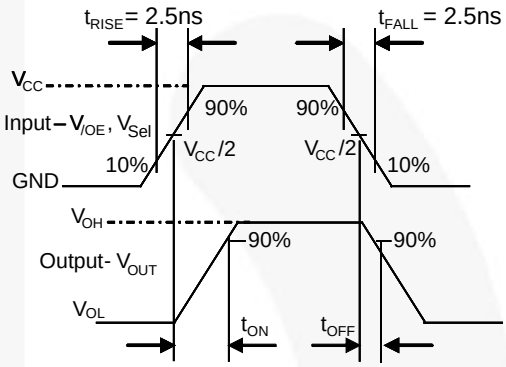


Figure 7. Turn-On / Turn-Off Waveforms

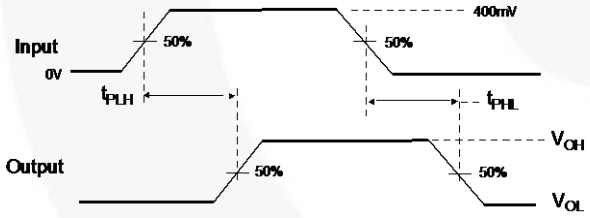


Figure 8. Propagation Delay ($t_R t_F$ – 500 ps)

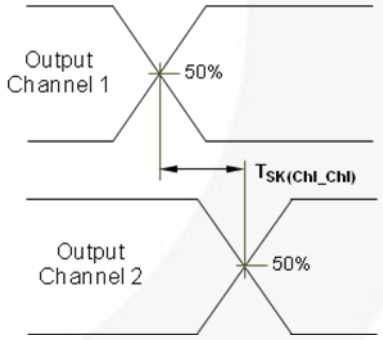


Figure 9. Channel-to-Channel Skew

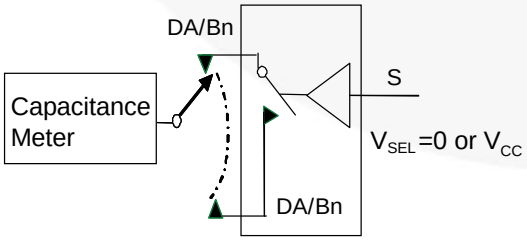


Figure 10. Channel Off Capacitance

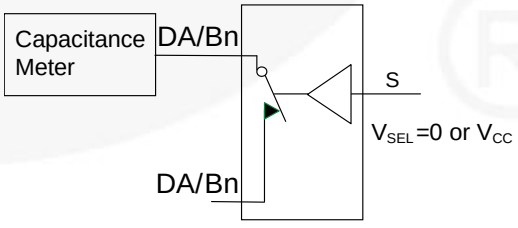
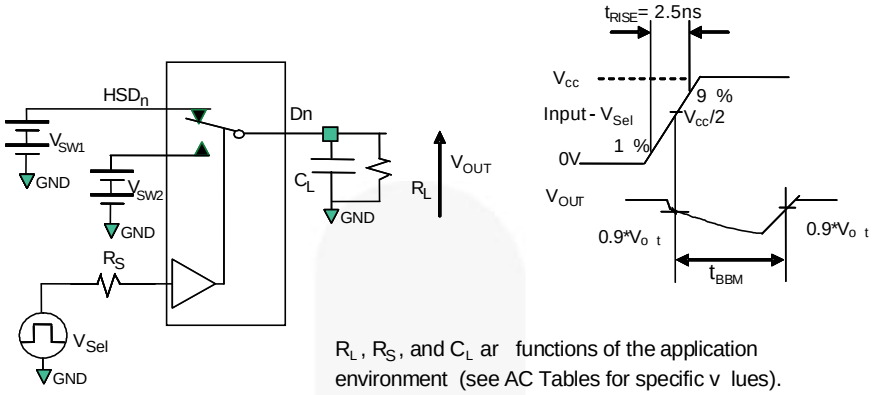


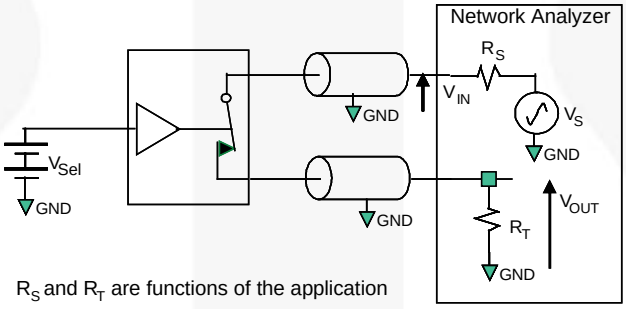
Figure 11. Channel On Capacitance

Test Diagrams (Continued)



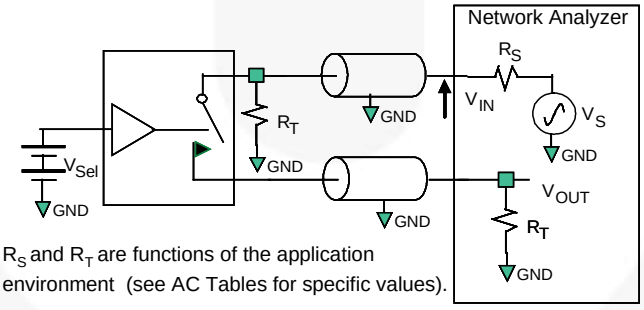
R_L, R_S, and C_L ar functions of the application environment (see AC Tables for specific v lues). C_L includes test fixture and stra capacitance.

Figure 12. Break-Before-Make Interval Timing



R_S and R_T are functions of the application environment (see AC Tables for specific values).

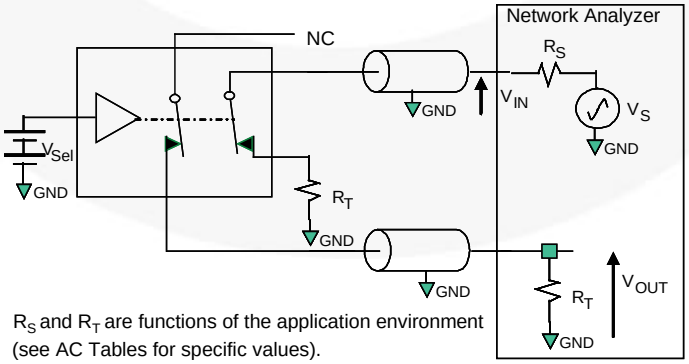
Figure 13. Bandwidth



R_S and R_T are functions of the application environment (see AC Tables for specific values).

Off isolation = 20 Log (V_{OUT} / V_{IN})

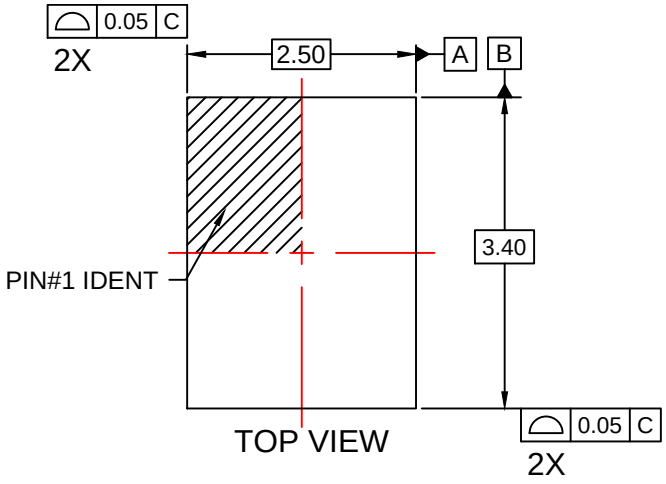
Figure 14. Channel Off Isolation



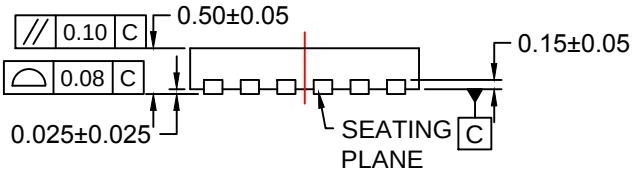
R_S and R_T are functions of the application environment (see AC Tables for specific values).

Crosstalk = 20 Log (V_{OUT} / V_{IN})

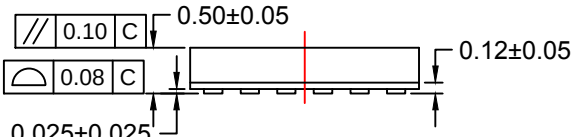
Figure 15. Non-Adjacent Channel-to-Channel Crosstalk



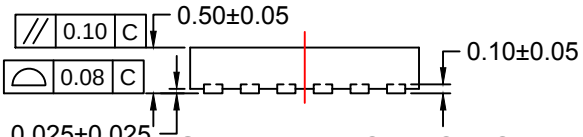
TOP VIEW



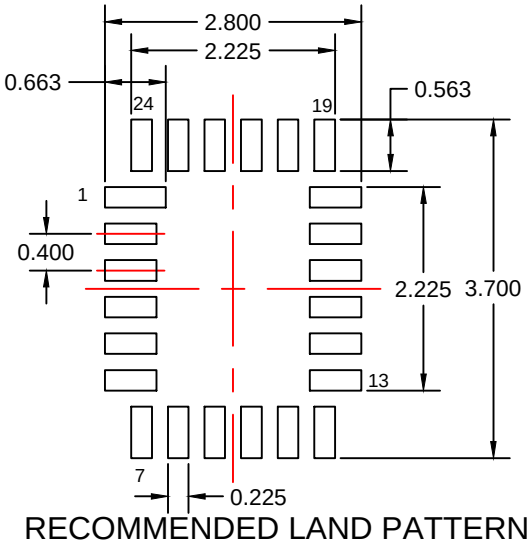
SIDE VIEW -OPTION A



SIDE VIEW -OPTION B



SIDE VIEW -OPTION C



RECOMMENDED LAND PATTERN

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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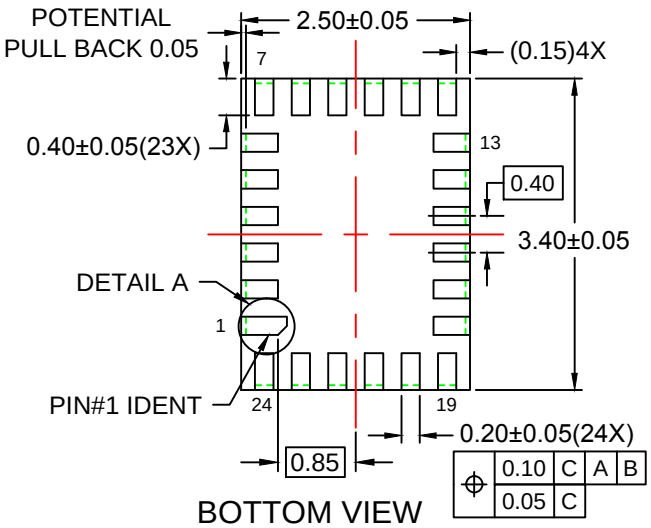
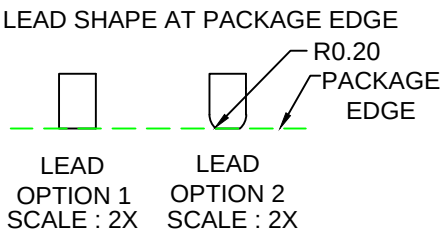
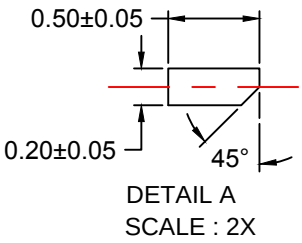


BOTTOM VIEW





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