STICK DIAGRAMS AND FLOORPLANNING

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Home directories

- Normally, things work pretty much ”out of the box” in Unix, but your home directory is dependent on files that set the environment.
- To get other scripts to work throughout the semester, you need to perform this command only **once**.

1. Log into your account either on VNC or SSH
2. `/classes/ecen4303F23/copy_csh.sh`
3. If you are in a VNC session, kill your terminal, and start a new one; otherwise, in ssh, just logout and log back in.

- Any problems, please let me know.
- Again, this should be done only once.

ECE machines

- ECE machines (7 – about 4-7 users/machine):
  - `shire.ecen.okstate.edu`
  - `moria.ecen.okstate.edu`
  - `angmar.ecen.okstate.edu`
  - `bree.ece.okstate.edu`
  - `combe.ecen.okstate.edu`
  - `dale.ecen.okstate.edu`
  - `rivendell.ecen.okstate.edu`

Use your best manners on the system!!!

- Once you get your account, practice, practice!
- Do NOT wait – you might get overwhelmed, if you don't start now.
- Any issues with your passwords, visit with me – avoid Emailing me as I have way too many Emails.

Files

- Throughout the semester, I will store files you may need for assignments and the project in a directory.
- This directory is `/classes/ecen4303F23`
- Remember, that you can set the tools up by typing `eda-tools,` but only have you have run the `copy_csh.sh` command.
- Every time you start a new terminal and want to use any tools, you must run the `eda-tools` command.
- A new terminal kills all your old environmental variables and runs `.cshrc` again (fyi).

Static CMOS Inverter

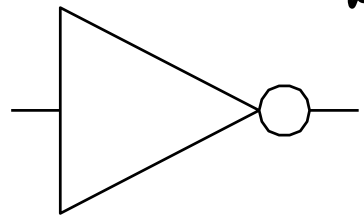
A	Y
0	1
1	0

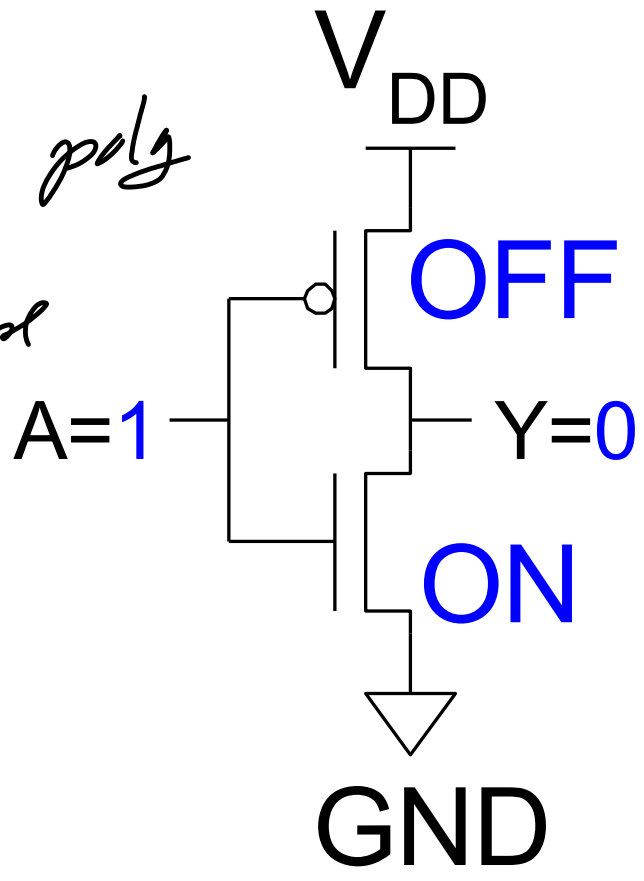
sky 130A

: paint poly

white dots are errors! DRC

select and hit y





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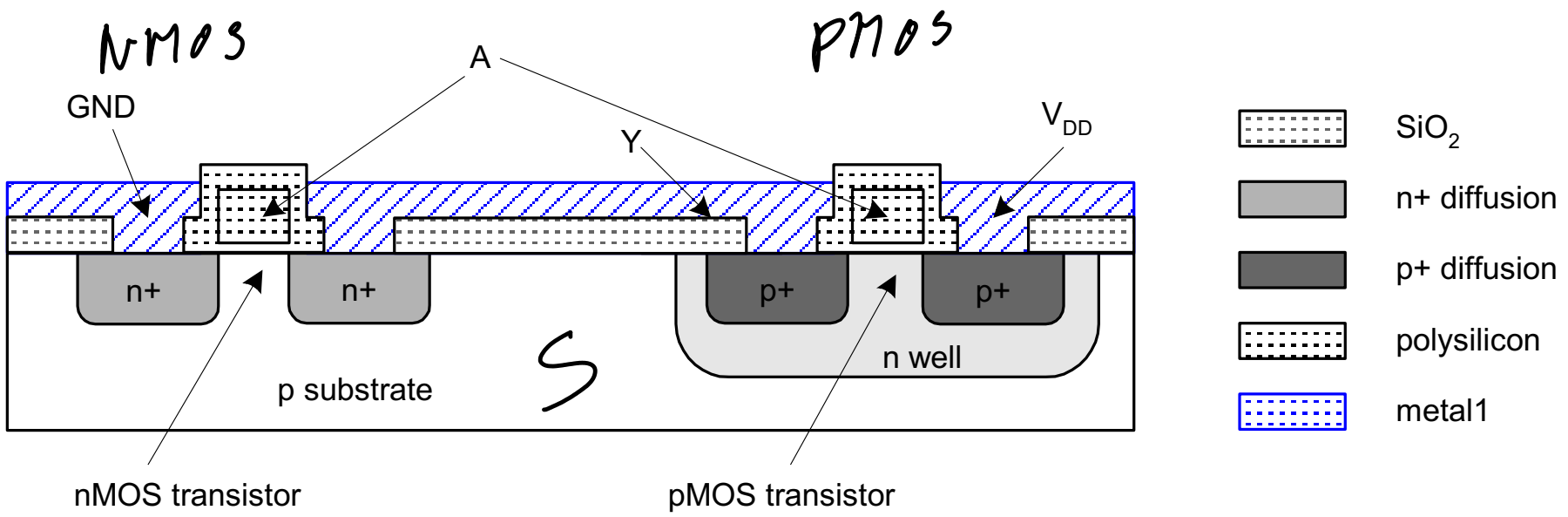
stinoj.gi

CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process like the printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process
  - To get this to be fabricated you need some way of putting layers into a Computer-Aided Design (CAD) tool.
  - This tool is called a layout editor (magic is our layout editor).
  - Layout editors are 2D realizations of 3D structures.

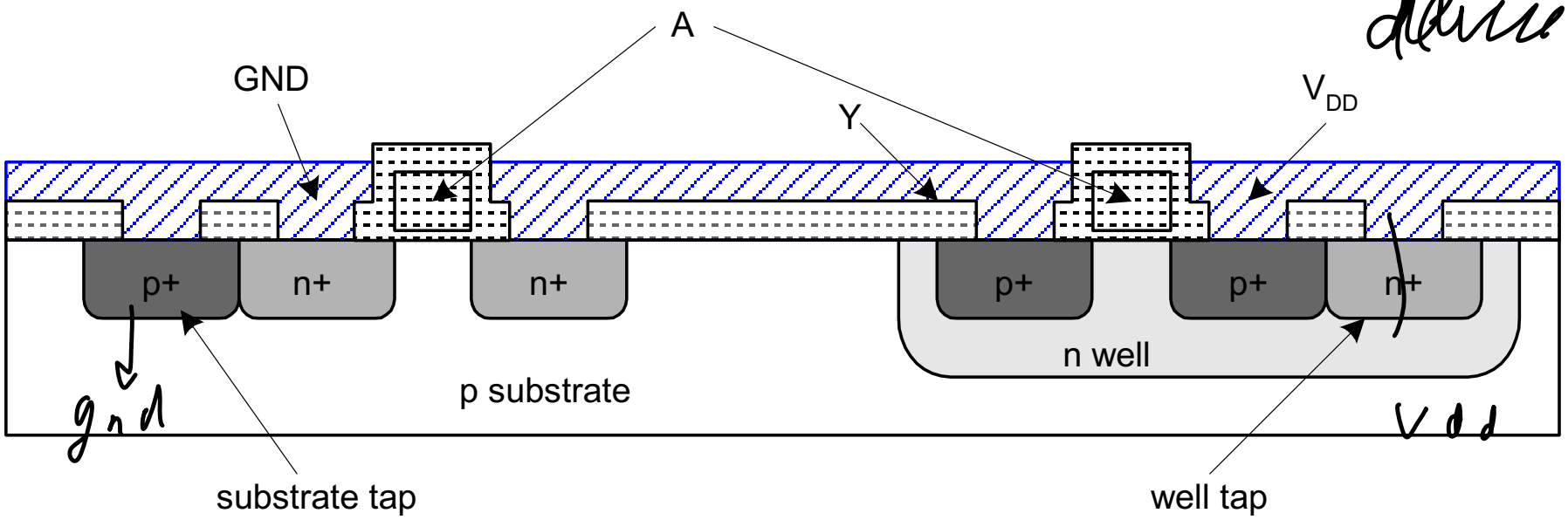
Inverter Cross-section

- Typically use p-type substrate for nMOS transistor
  - Requires n-well for body of pMOS transistors
  - Several alternatives: SOI, twin-tub, etc.



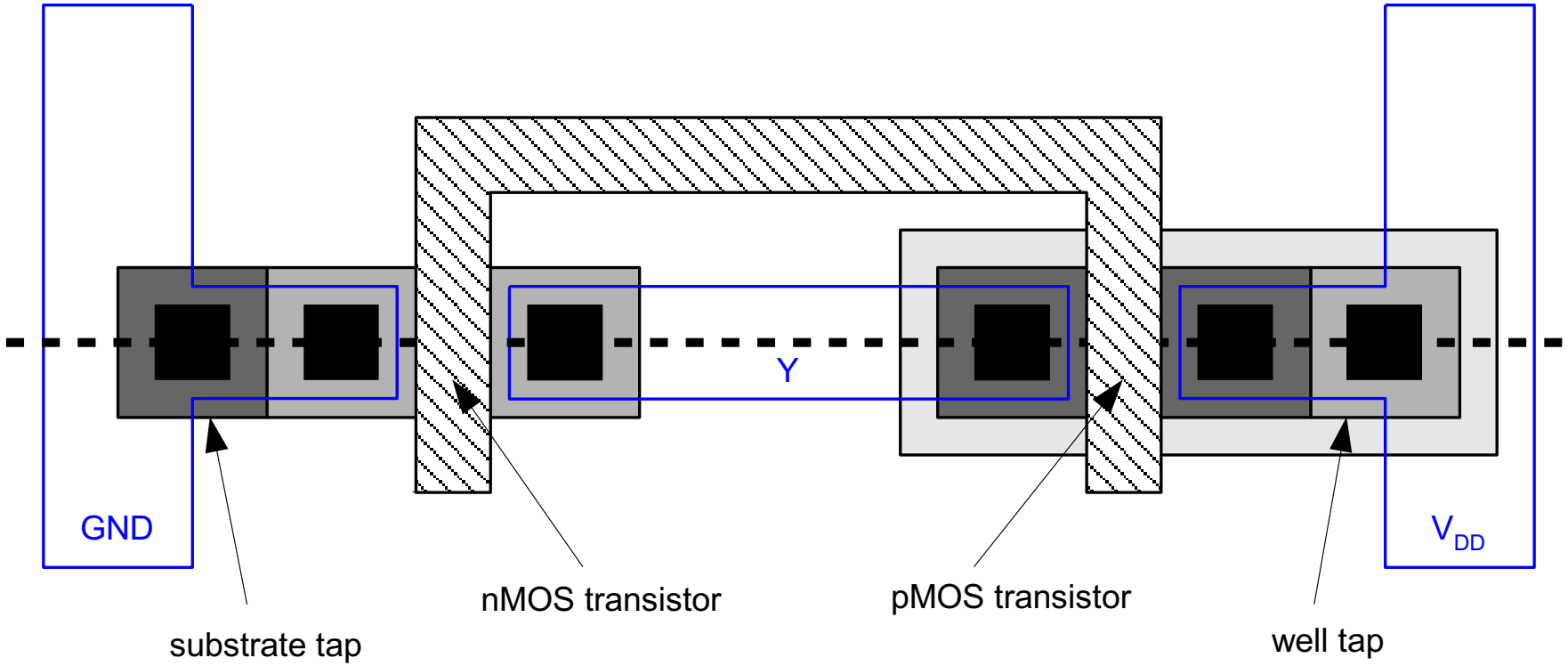
Well and Substrate Taps

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



Inverter Mask Set

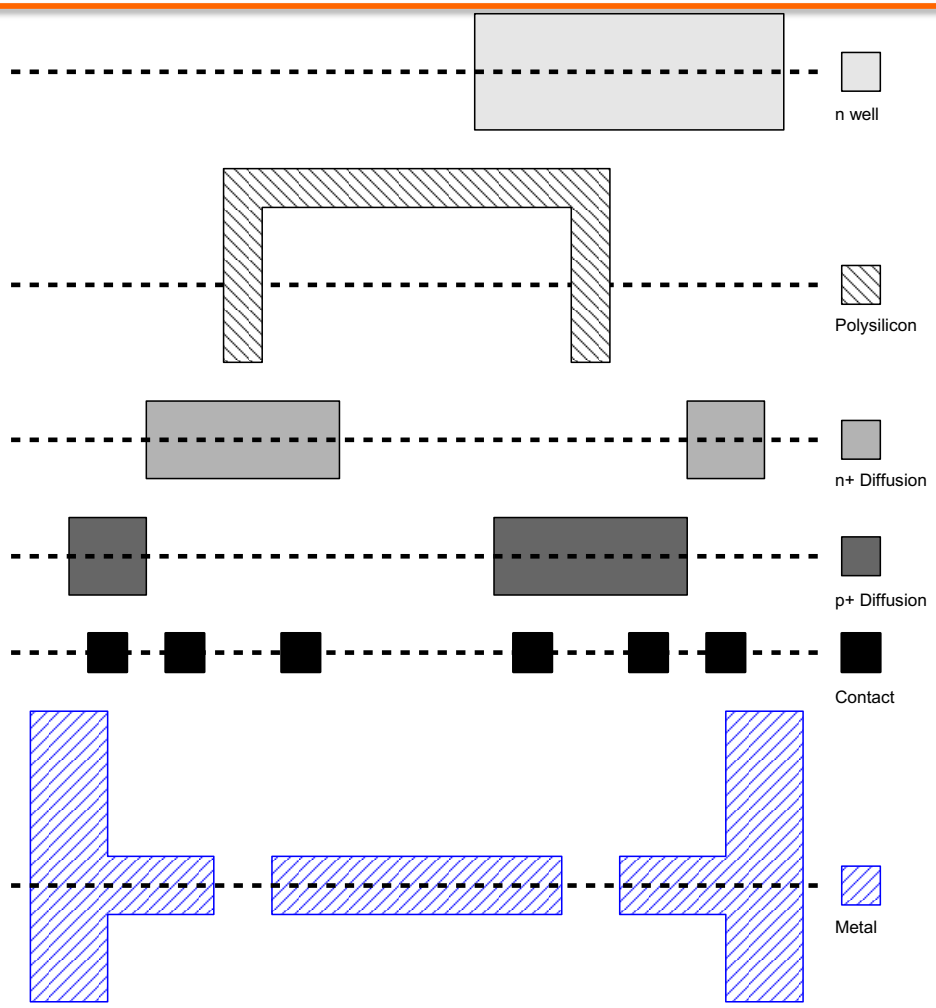
- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal

nwell
poly
ndiff
pdiff
ndc / pdc
m_1, m_2, m_3



FEOL → Transistors
front end of the line

BEOL → back end of the line
↳ metals

Artwork

- “Let’s crack open the crayons!!”

[Crayola]

Stick Diagrams

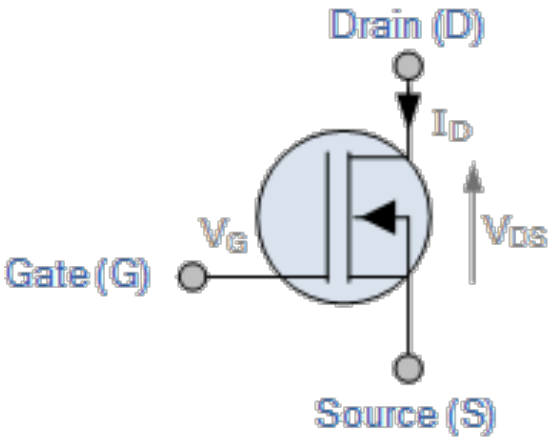
- Stick diagrams are used to avoid the endless time sink that layout can be (however, its loads of fun!)
- Let's try the inverter
  - Blue = metal1
  - Green = $n_{diffusion}$
  - Brown = $p_{diffusion}$
  - Red = poly
  - Dot = contact (black)
  - Purple = Metal2

Gate Layout

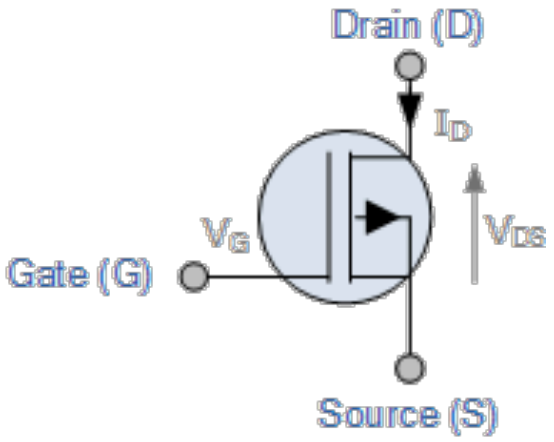
- Layout can be very time consuming : its an art!!!!!!
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - V_{DD} and GND should abut (standard height)
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts
    - What?

Revisiting Good'ol Kirchoff!

- Remember Kirchoff's Voltage Law
  - All loops around a loop are 0!
- Even though we don't understand the basic operation of MOSFETs yet, let's look at the symbol we will use!
- This is just a property of making sure that voltage always gets measured according to a certain level.
  - Make sure the Voltage has no fluctuation.



N-channel



P-channel

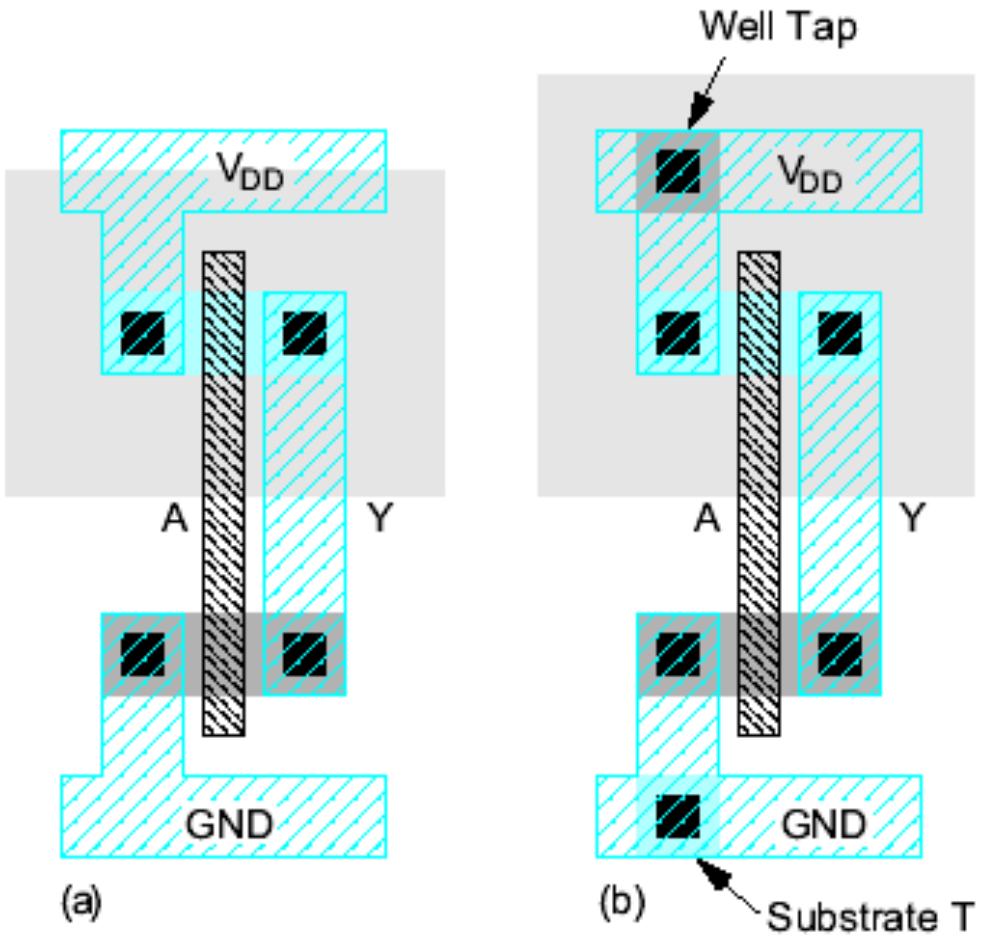
MOSFET : 4 terminals!!!

- MOS devices have 4 terminals!
  - We will learn the operation well, I assure you.
  - But, for our design assume the following even though we have been drawing the two as 3 terminals
- Let's try it!!!

Inverter Gate

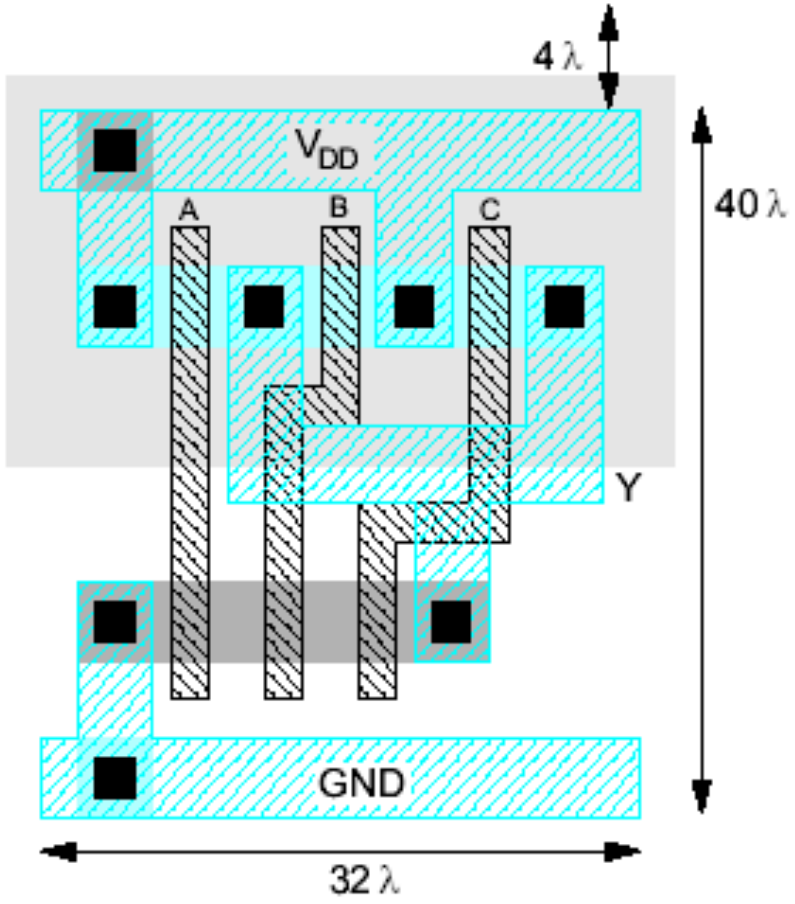
2 input nand : NAND2

Example: Inverter



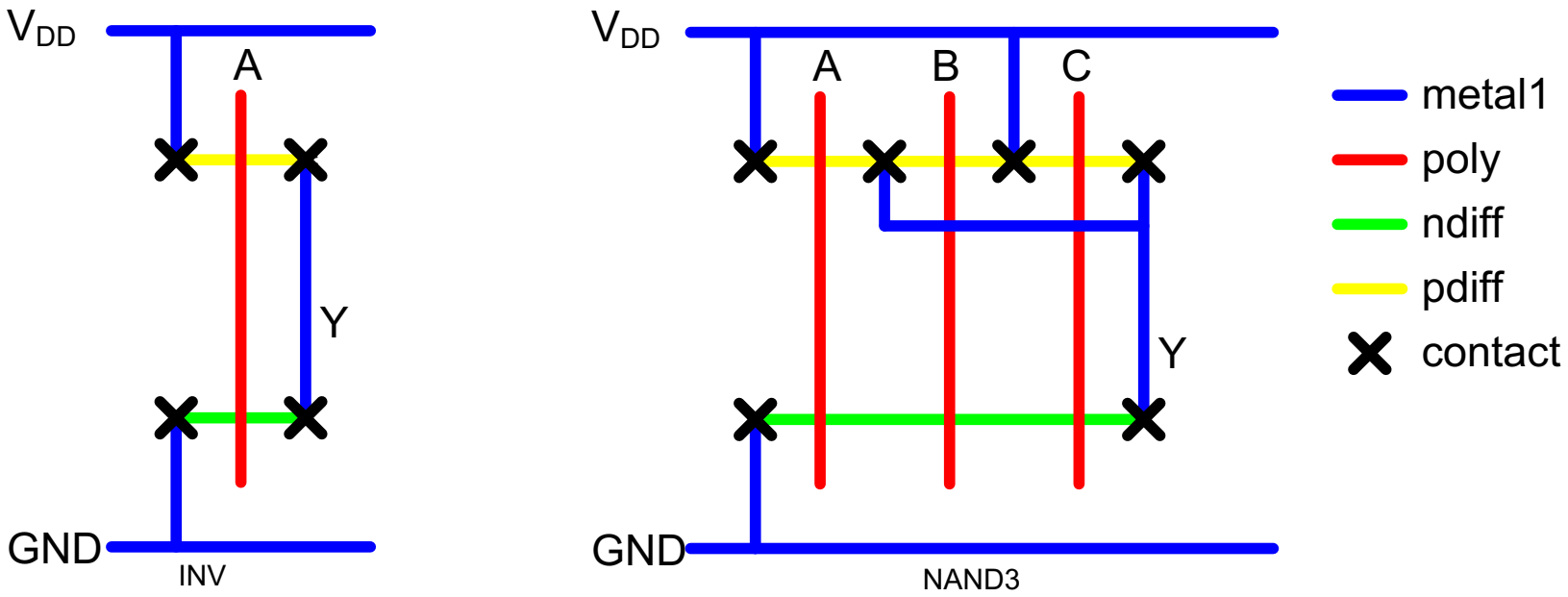
Example: NAND3

- Horizontal N-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 V_{DD} rail at top
- Metal1 GND rail at bottom
- 32 λ by 40 λ



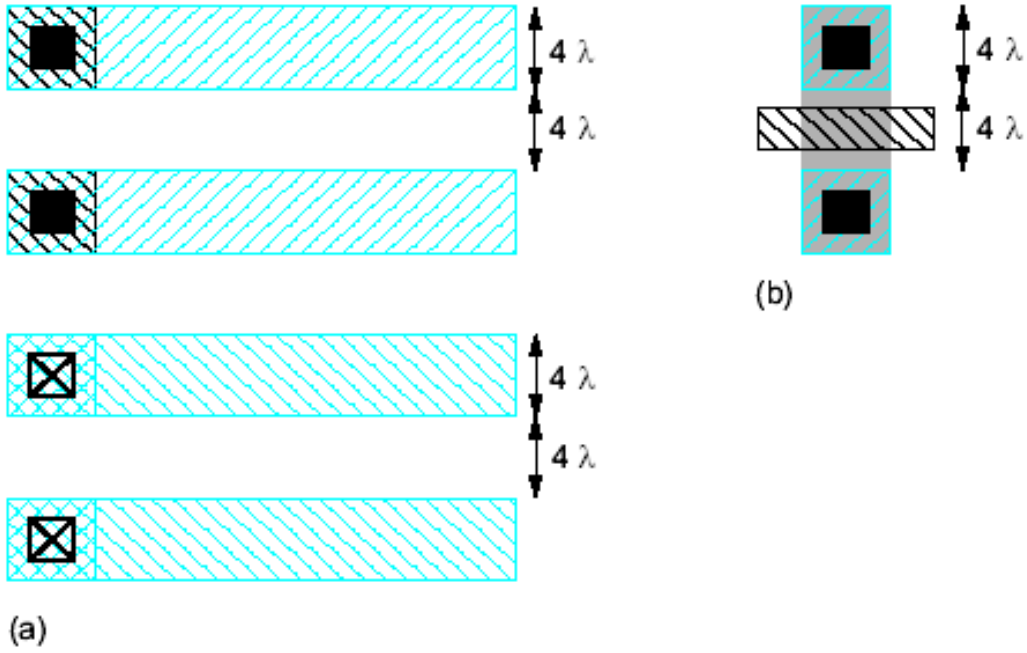
Stick Diagrams

- *Stick diagrams* help plan layout quickly
  - Need not be to scale
  - Draw with color pencils or crayons or dry-erase markers



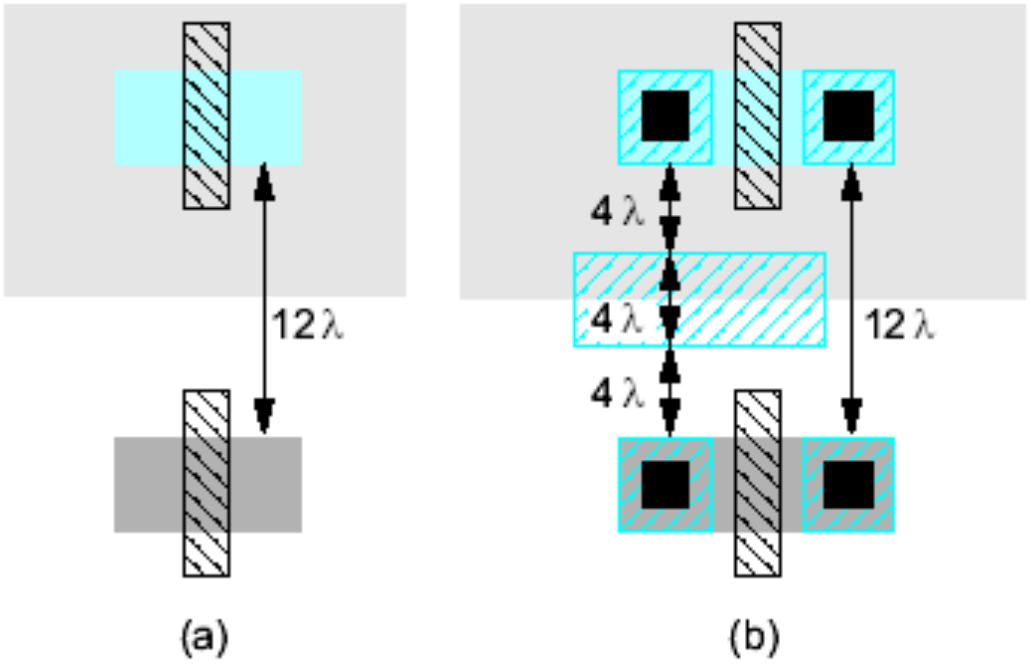
Wiring Tracks

- A *wiring track* is the space required for a wire
  - 4 λ width, 4 λ spacing from neighbor = 8 λ pitch
- Transistors also consume one wiring track



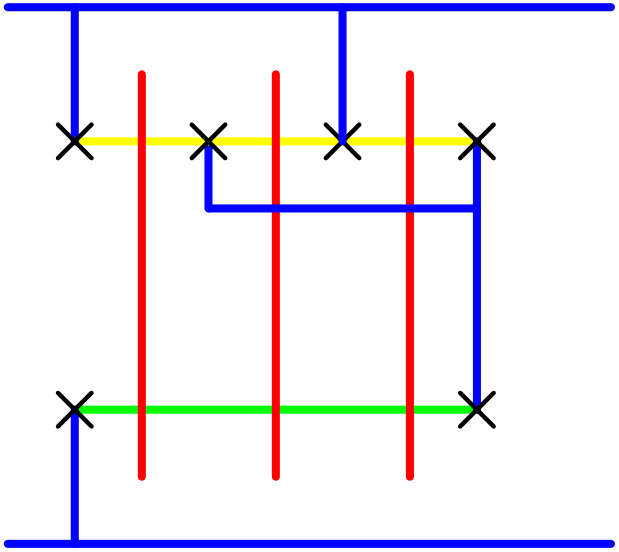
Well spacing

- Wells must surround transistors by 6 λ
  - Implies 12 λ between opposite transistor flavors
  - Leaves room for one wire track



Area Estimation : Rule of 8

- Estimate area by counting wiring tracks
  - Multiply by 8 to express in λ



More complicated Example : NOR3

Substrate Contact Census

- So, how many substrate contacts should I use?
- In this class, we will adopt the methodology that 1 substrate contact per transistor.
- Some companies may change this depending on test results.
- Companies will usually hire talented visual engineers that are called layout engineers.
  - These individuals are like gold for a company in that they can make the difference between success and failure.
  - They are highly coveted positions.

Summary

- Who said you cannot make a living out of coloring stuff?
- Layout is a great technique to learn even if you are not doing it daily but stick diagrams are essential to be successful.
  - Learning stick diagrams helps you understand the importance of floorplanning, as well.
- Layout is done by experience, and we will do several layouts for assignments.