



PN JUNCTIONS

James E. Stine, Jr.

Edward Joullian Endowed Chair in Engineering

Oklahoma State University

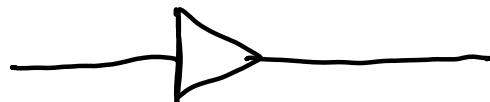
Electrical and Computer Engineering Department

Stillwater, OK 74078 USA

james.stine@okstate.edu

Administrivia

- Remember, to enhance your lectures with readings or skimming of chapter.
 - I gave chapter readings on the tentative schedule (Today: Chapter 1.5)
 - Understand the science behind why something happens.
 - Ask questions on slack, in person or with Zoom.



$$V > 0.7 \quad i = \infty$$

$$V < 0.7 \quad i = 0$$

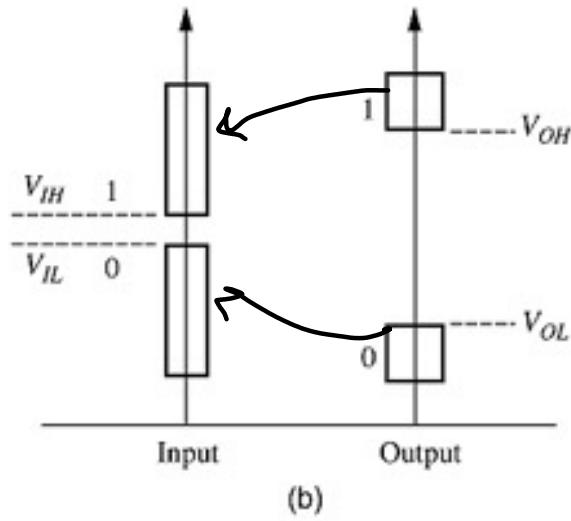
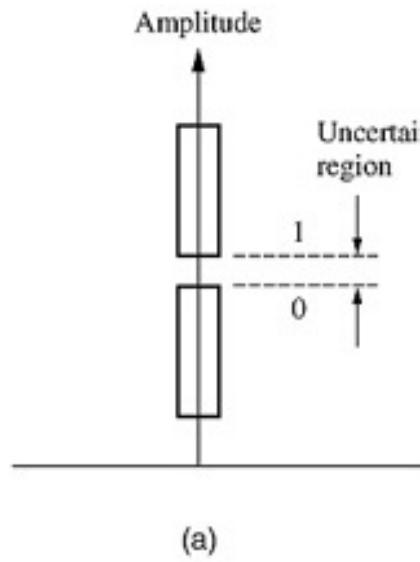
Digital Gates

- Digital Gates involve two basic structures:
 - Pull-Down Network or PDN
 - “The Driver”
 - Pull-Up Network or PUN
 - “The Load”
- The key is to find gates that work complementary to each other (i.e., when one is down, one can compensate or pick up the slack).
 - It is essential element of digital gates!
 - **ALL DIGITAL GATES ARE ANALOG IN NATURE!!!**
 - This is why I emphasize the understanding what's going on underneath despite my experience in the digital implementation of Systems.
 - <http://www.opencores.org> == BAD UNDERSTANDING!

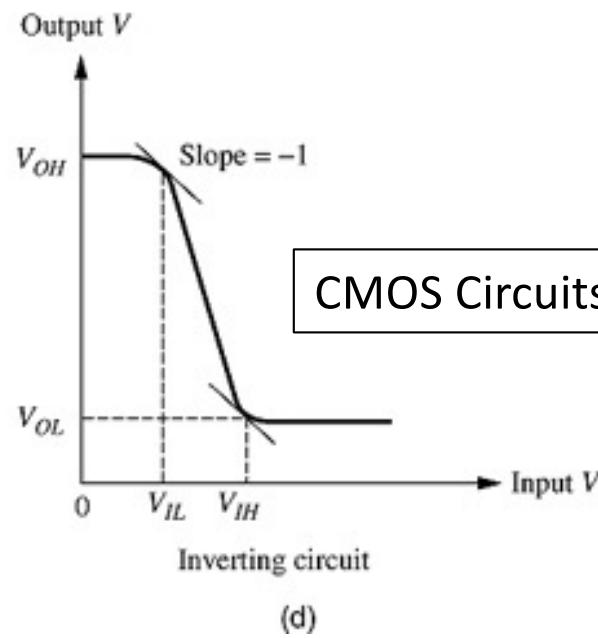
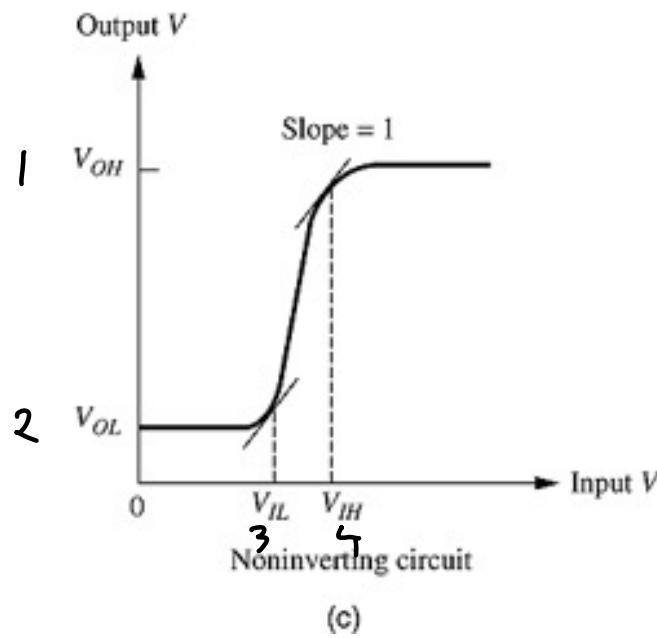
*diodes help keep voltage
close to 0*

Transmissibility!

this is about the noise margin

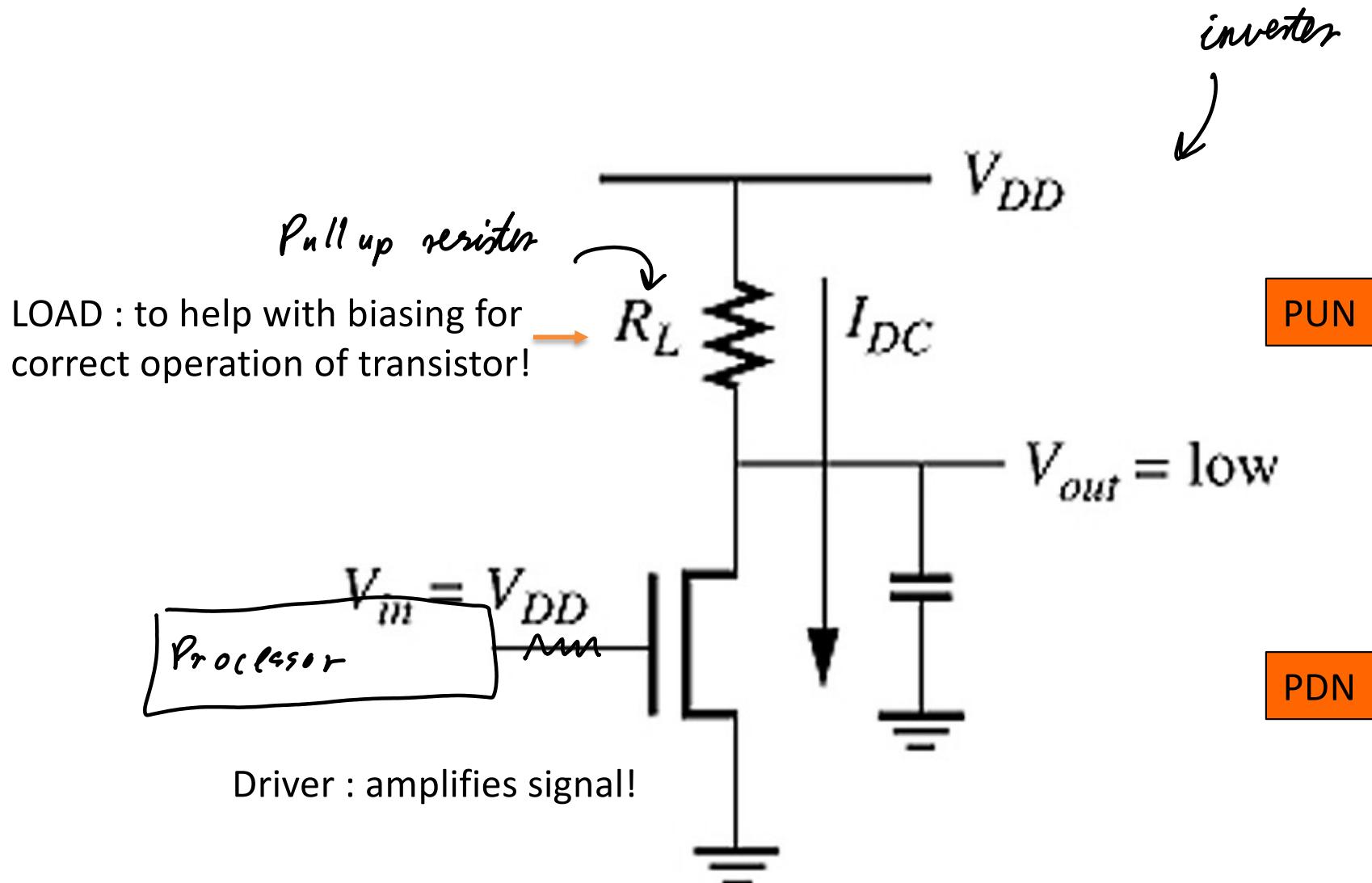


How well can we keep
a logic 1 or a logic 0!



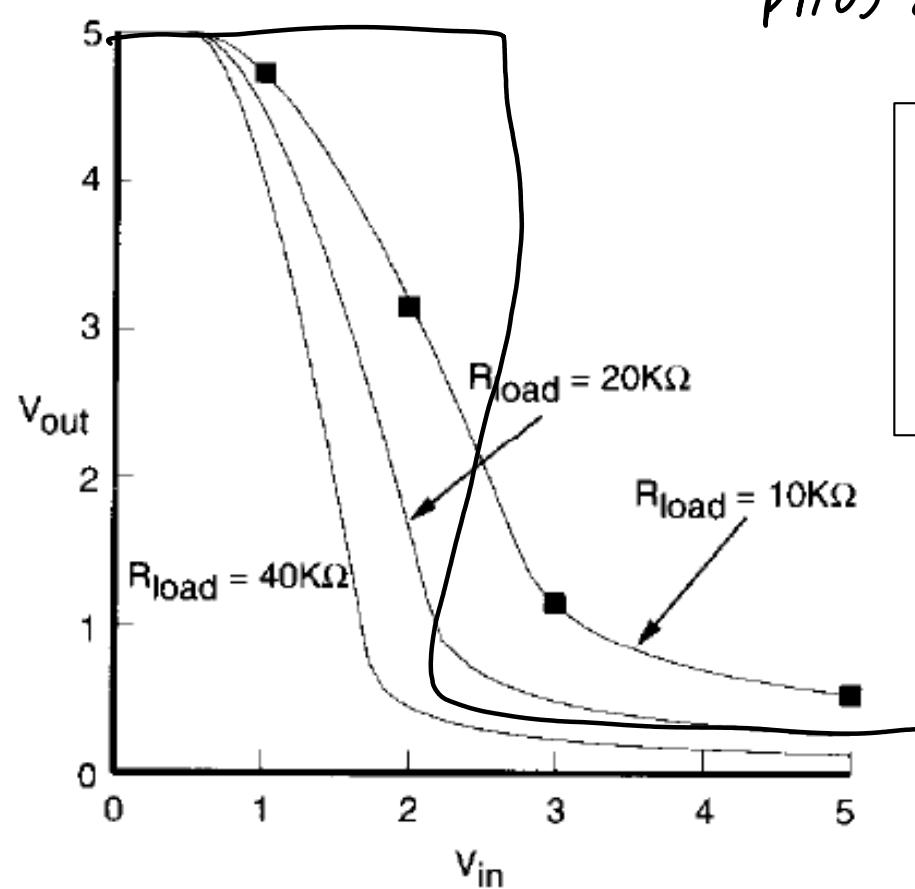
[Hodges/Jackson/Saleh]

One Solution



[Hodges/Jackson/Saleh]

VTC of Resistive Load NMOS gate

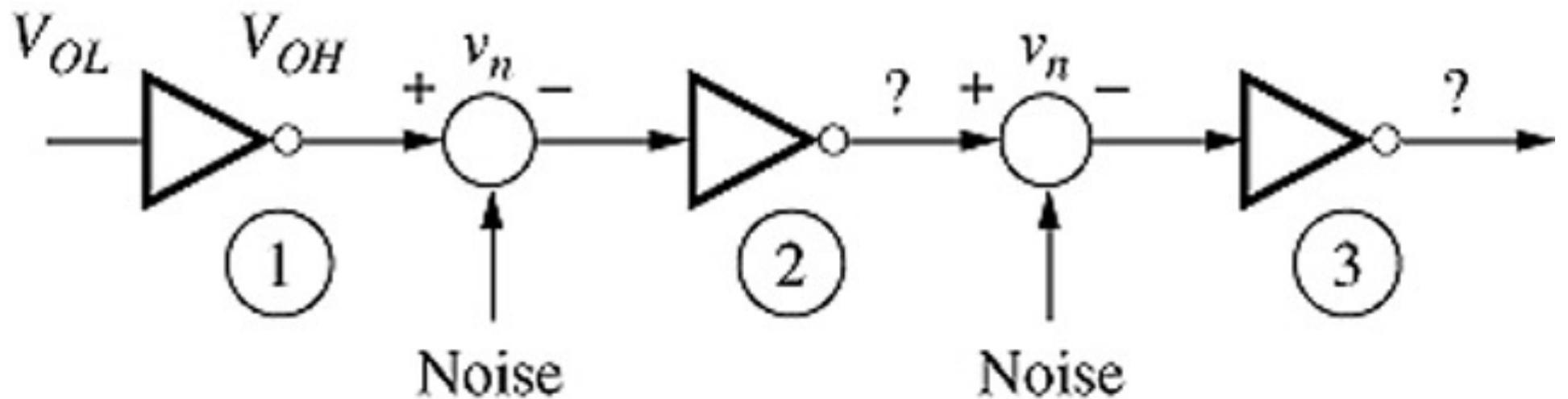


NMOS can alter its resistance

Also, hard to make a
40 $k\Omega$ resistor within
CMOS even with a
serpentine or meander
structure!

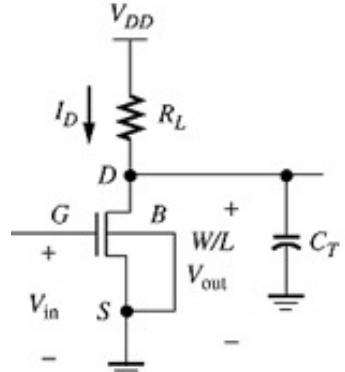
[K. Roy, Purdue]

Noise Margin

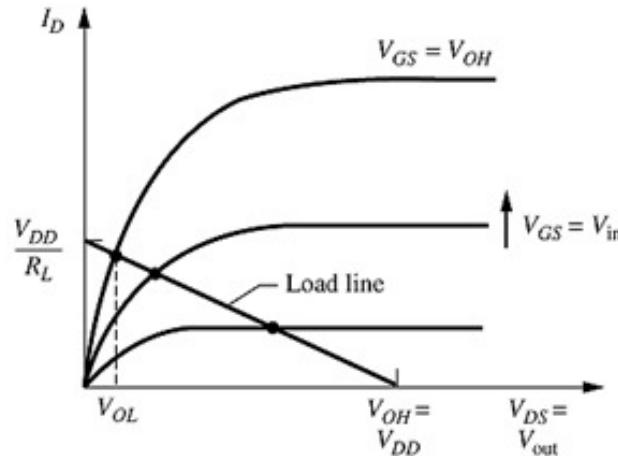


- When designing digital circuitry, we have to make sure all signals are resistive from extraneous input voltages (i.e., noise).
- This means that we should make sure it drives the transistor well in its certainty regions (i.e., VDD/VSS).
- We hope that we can avoid uncertainty regions.
- If possible, turn off all extraneous current when its not at VDD/VSS for energy reduction.

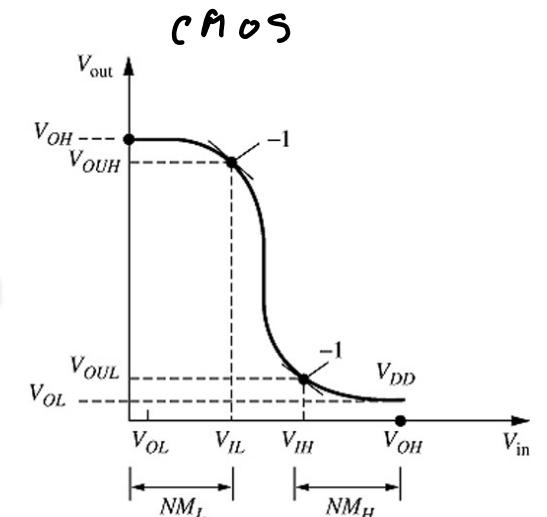
Resistive Load



(a) Inverter

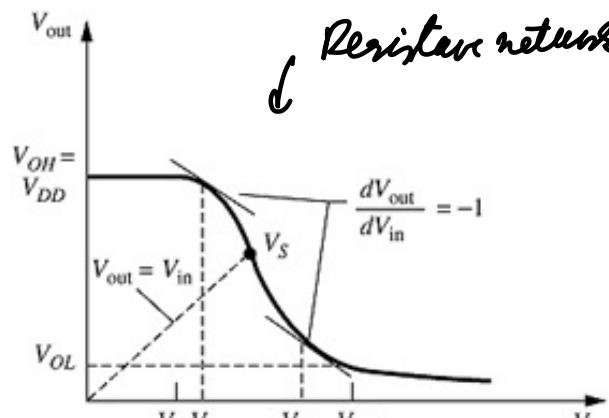


(b) Drain characteristics and load line



VTC

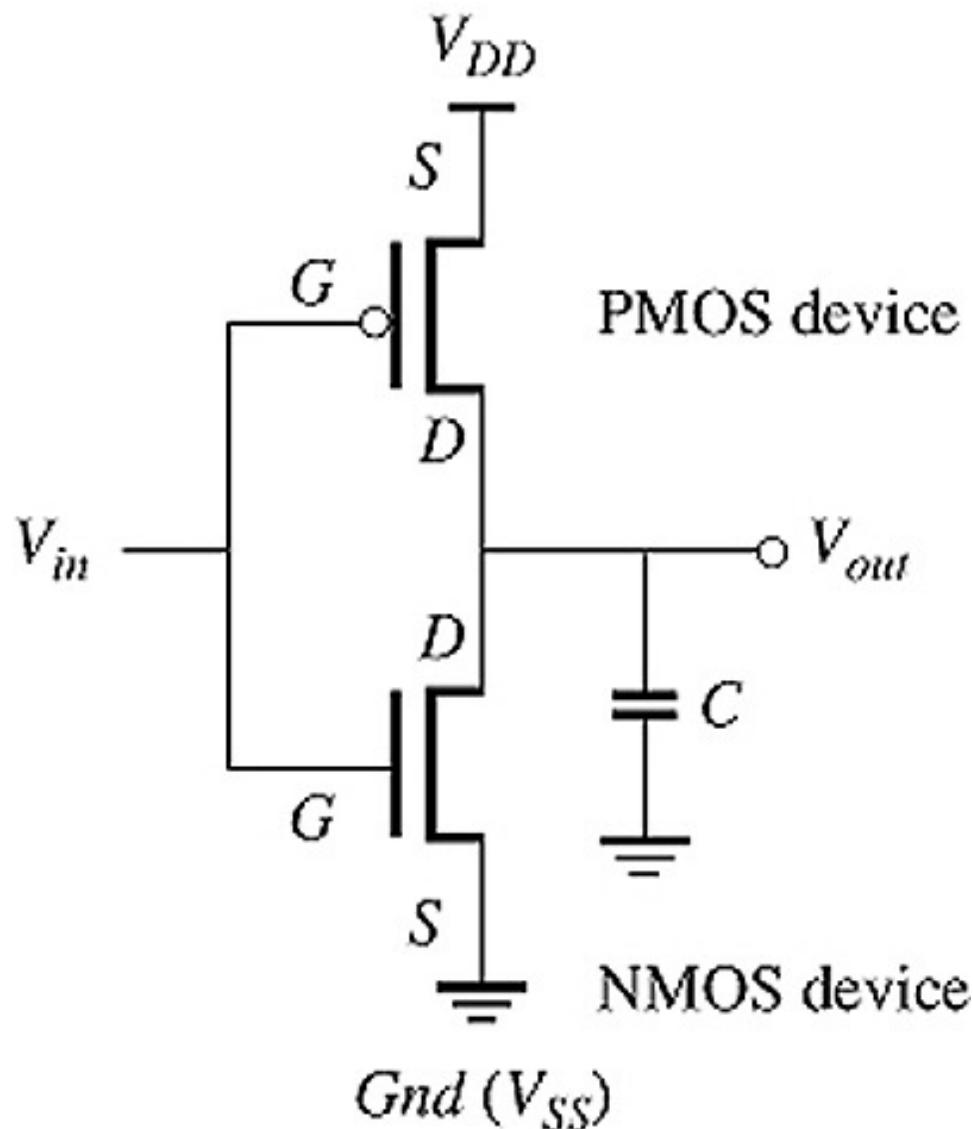
$V_{OH}, V_{OL}, V_{IH}, V_{IL}$



(c) Voltage transfer characteristic

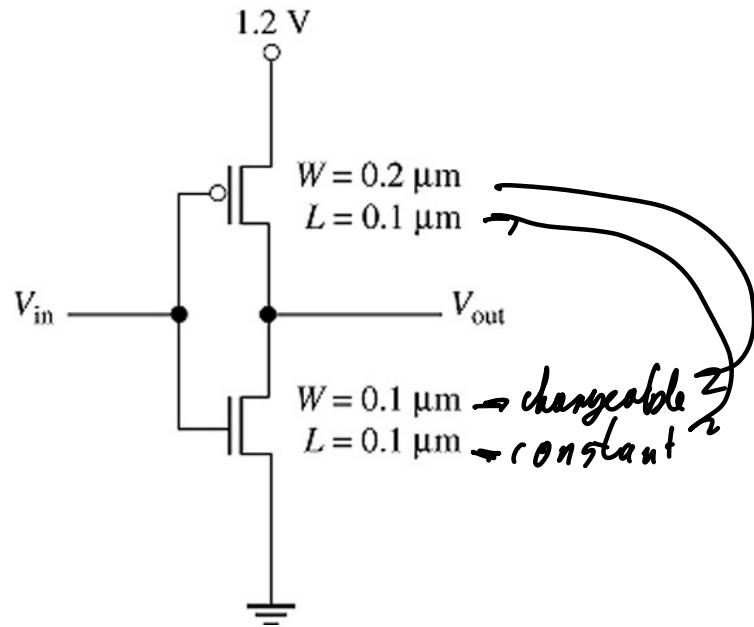
VTCs are characterized for all Voltages between VSS and VDD for digital operation!

Best Solution Today!

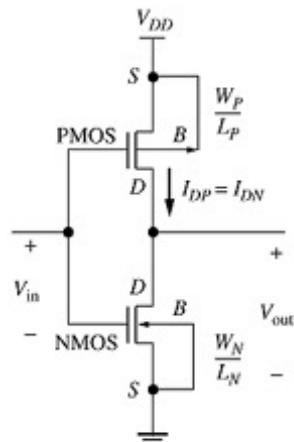


[Hodges/Jackson/Saleh]

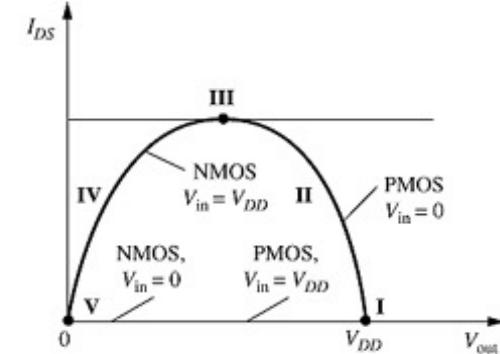
CMOS VTC



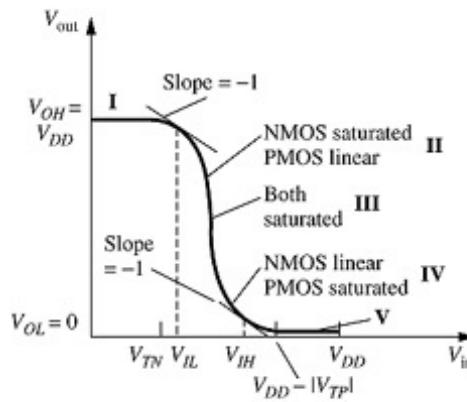
Care must be taken to choose engineering design choices for W/L to make sure each transistor complements each other!



(a) Inverter

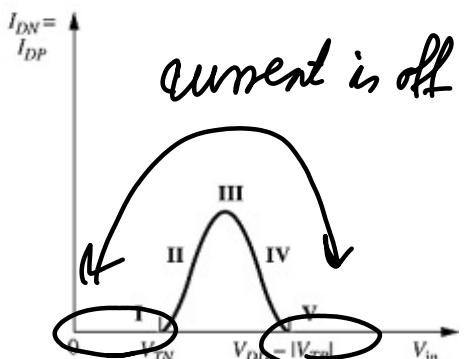


(b) Load line

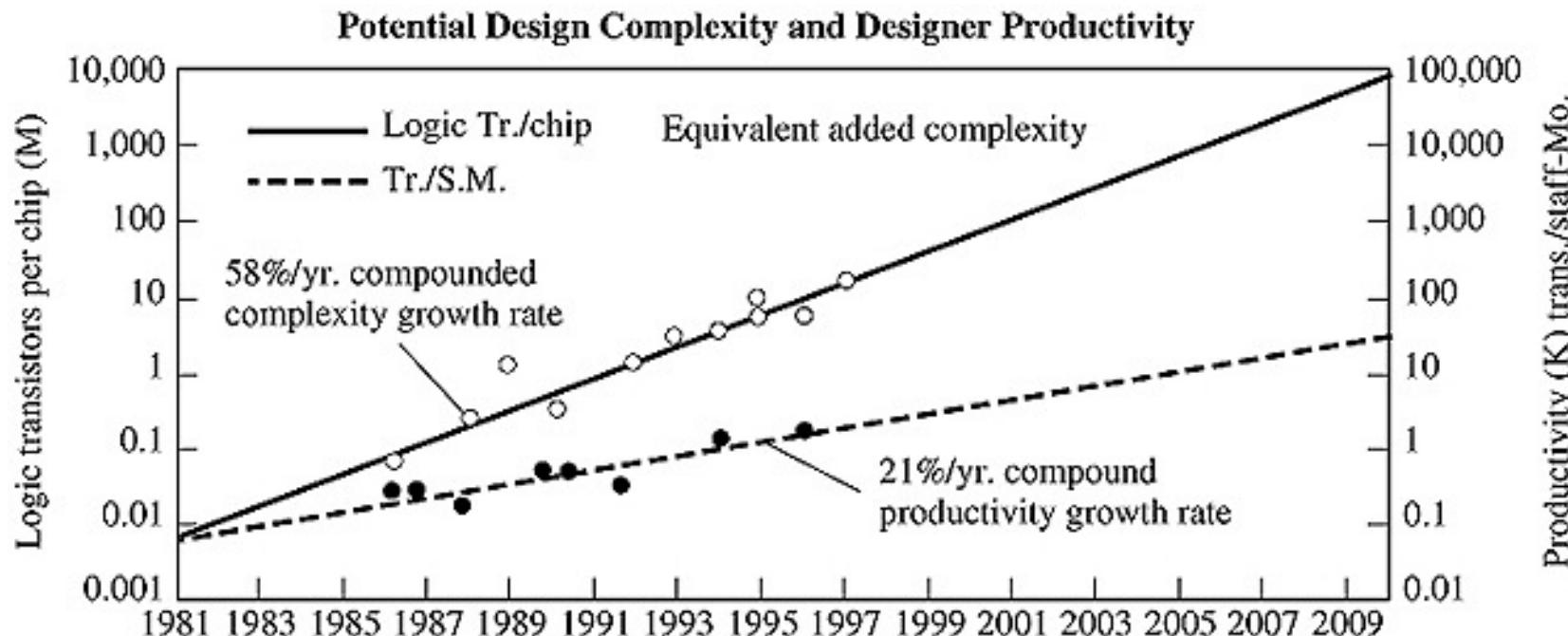


(c) Voltage transfer characteristic and current

[Hodges/Jackson/Saleh]



Remember it's a bu\$iness!



Design cost for a 50M transistor chip (2003)

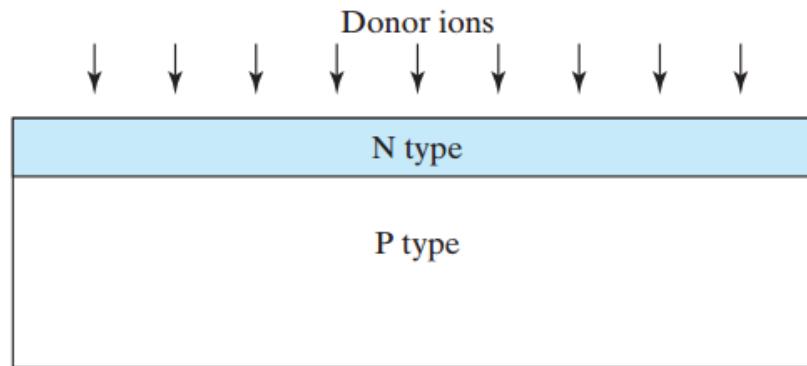
- Gates required (4 tx per gate) 12.5M
- Gates/day (verified) ~1K (including memory)
- Total eng. days 12,500
- Total eng. years 35
- Cost/eng. year \$200K
- Total people cost \$7M

[Hodges/Jackson/Saleh]

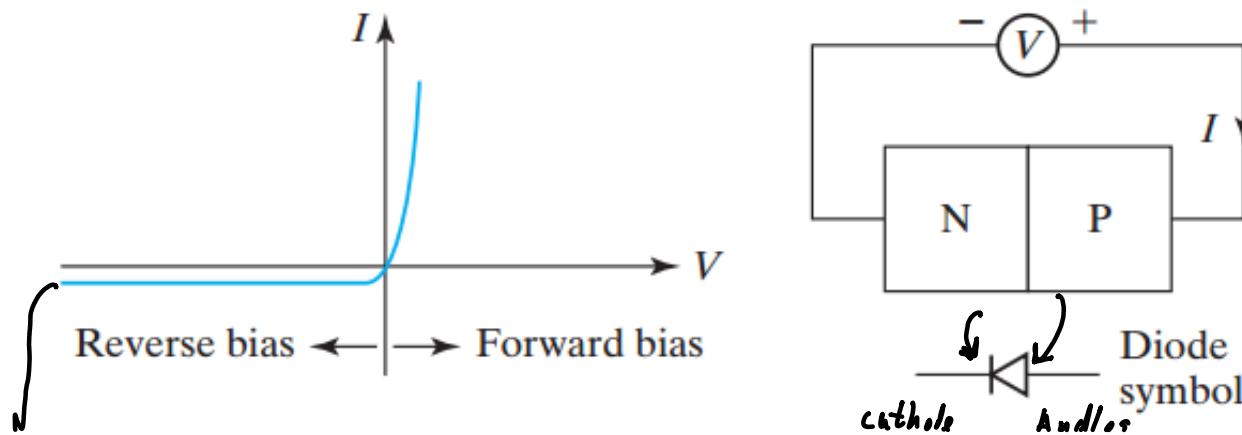
Actual cost may be \$10–15M to get actual prototypes after fabrication.

pn Junctions

- A pn junction is typically fabricated by implanting or diffusing donor atoms into a p-type substrate to form an n-type layer:



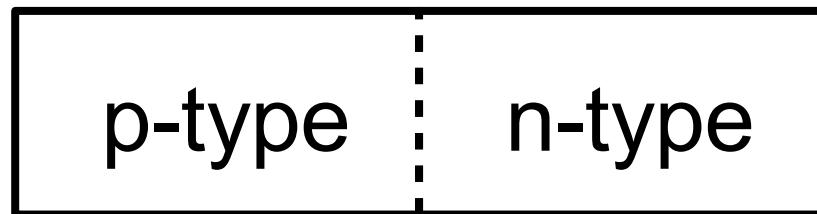
- A pn junction has a rectifying current-vs.-voltage characteristic:



[Pierret]

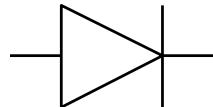
p-n Junctions

- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction (great for isolation from current in areas you do not want current to flow!!!)



anode
anode

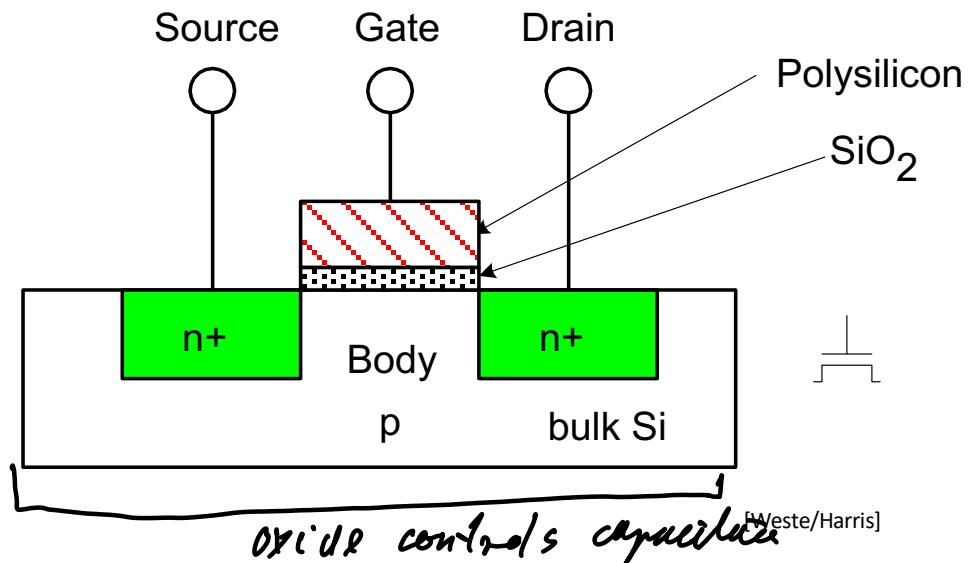
cathode



[Weste/Harris]

nMOS Transistor

- Four terminals: gate, source, drain, body or substrate.
- Gate – oxide – body stack looks like a capacitor
 - Gate and body are conductors
 - SiO_2 (oxide) is a very good insulator and super easy to grow.
 - Called metal – oxide – semiconductor (MOS) capacitor
 - Even though gate is no longer made of metal*
- There are two popular forms of nMOS transistors today: bulk CMOS and Silicon-on-Insulator (SOI) CMOS.

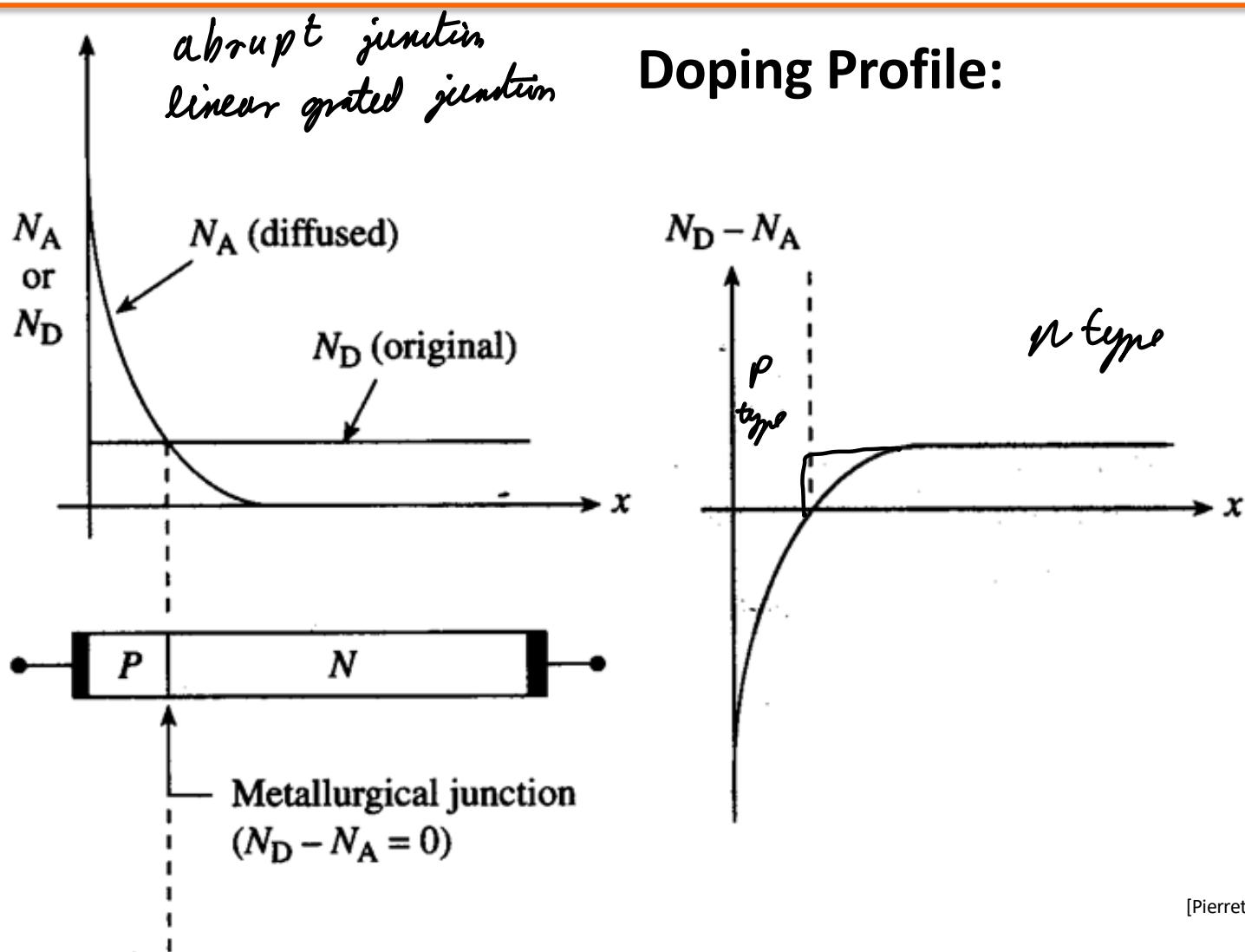


* Metal gates are returning today!

on silicon

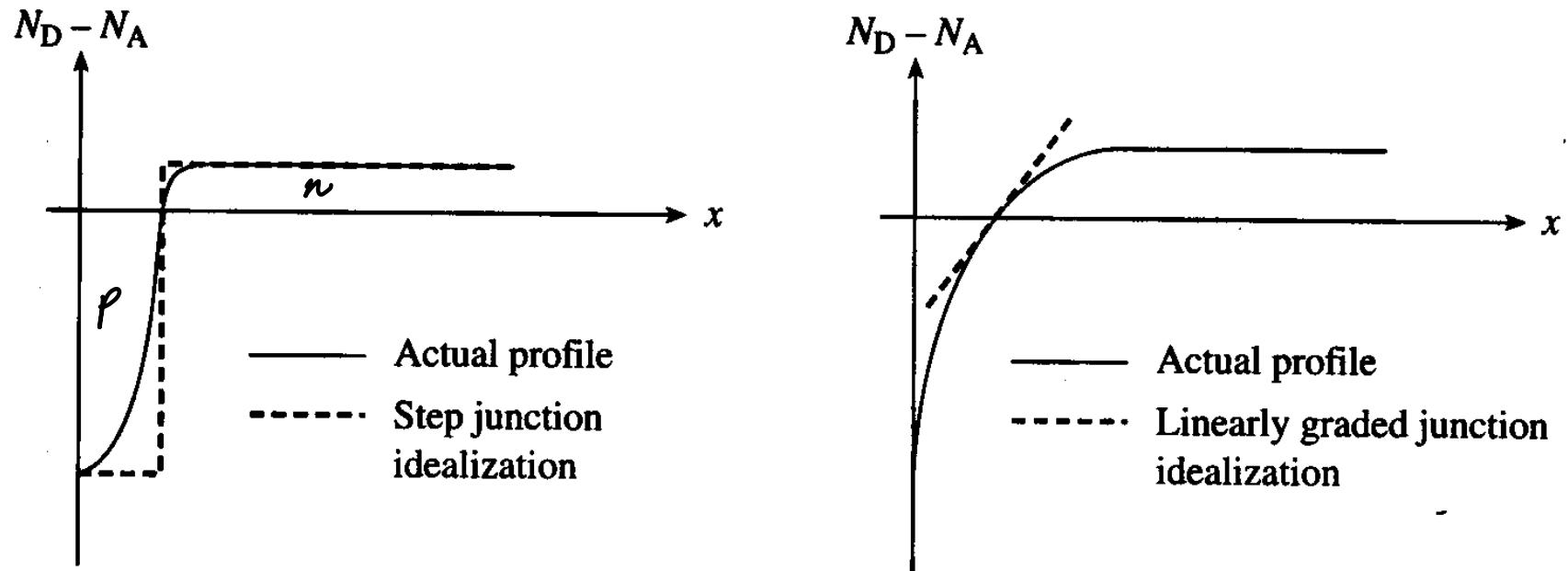
Today, researchers are still searching for a replacement for CMOS although CMOS will be around for another 20-30 years easily due to its great properties and its easy to build.

Terminology



[Pierret]

Idealized pn Junctions



[Pierret]

- In the analysis going forward, we will consider only the net dopant concentration on each side of the pn junction:

$N_A \equiv$ net acceptor doping on the p side: $(N_A - N_D)_{p\text{-side}}$

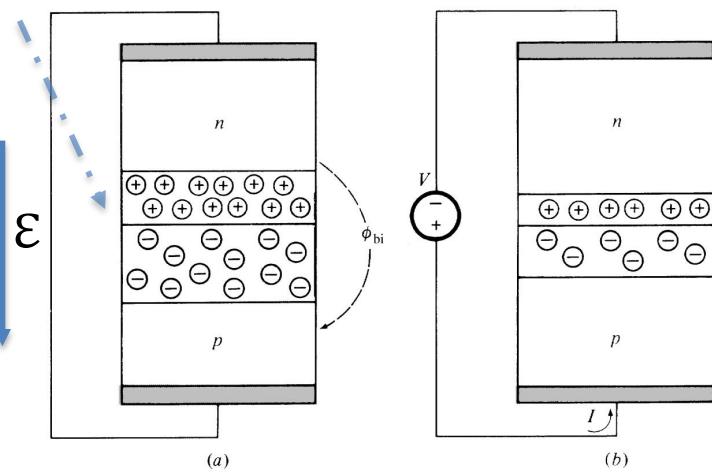
$N_D \equiv$ net donor doping on the n side: $(N_D - N_A)_{n\text{-side}}$

Three Defined Regions

Depletion region

ϕ_{bi} : "built-in potential"

0 v all around



Depletion region is in the middle of the device and represents area where holes and electrons are positively charged donor and negatively charged acceptor atoms and is always assumed to be sharply defined!!

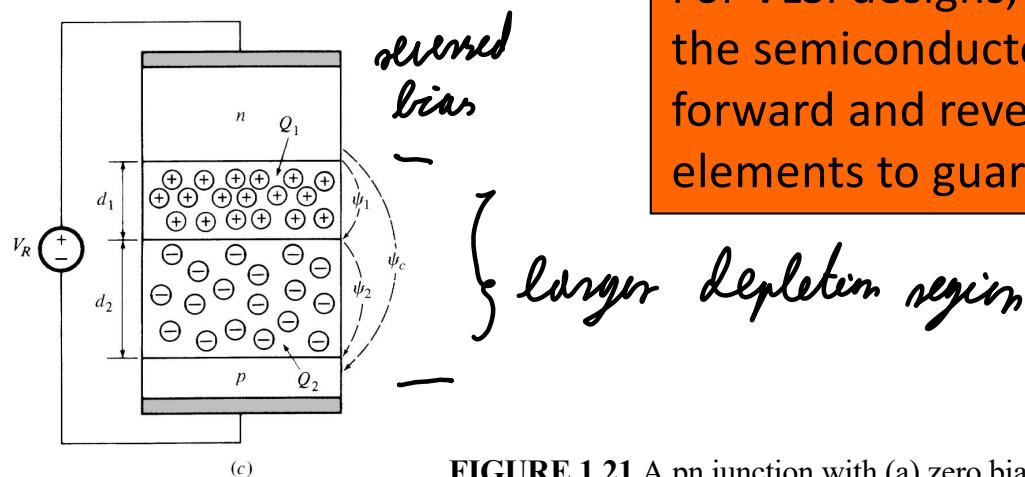


FIGURE 1.21 A pn junction with (a) zero bias, (b) forward bias, (c) reverse bias.

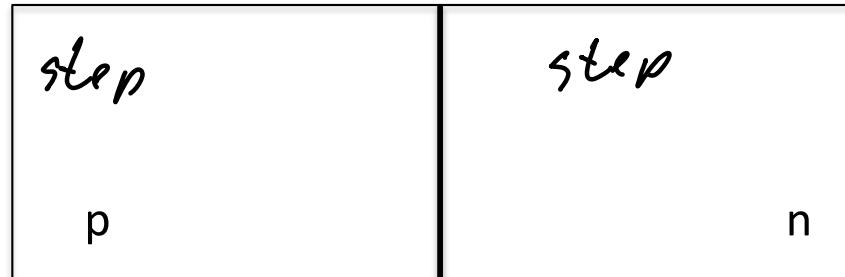
- all the orbits are filled
- depletion region
- Equilibrium
 - Non-equilibrium, forward biased
 - Non-equilibrium, reverse biased

For VLSI designs, it is important that the semiconductor have both forward and reverse biased elements to guarantee isolation.

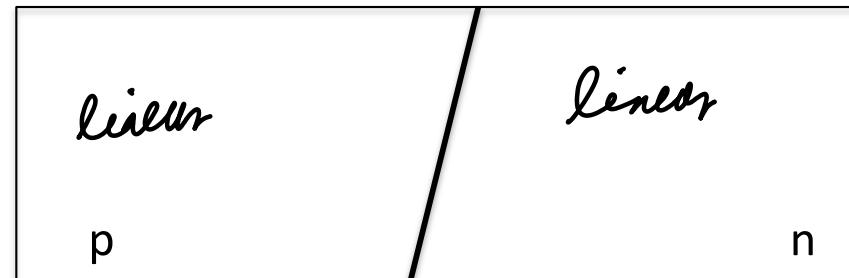
Important Pre-concept

- Remember that the ideas do not make sense unless we can fabricate these devices.
- They are much more complicated than they look.
 - But we can generalize things usually using two common simplistic approaches.

Most common –
simplifies analysis
(we will use this for
most of the lectures)



Step Junction



Linearly-
graded
junction

pn junction at equilibrium

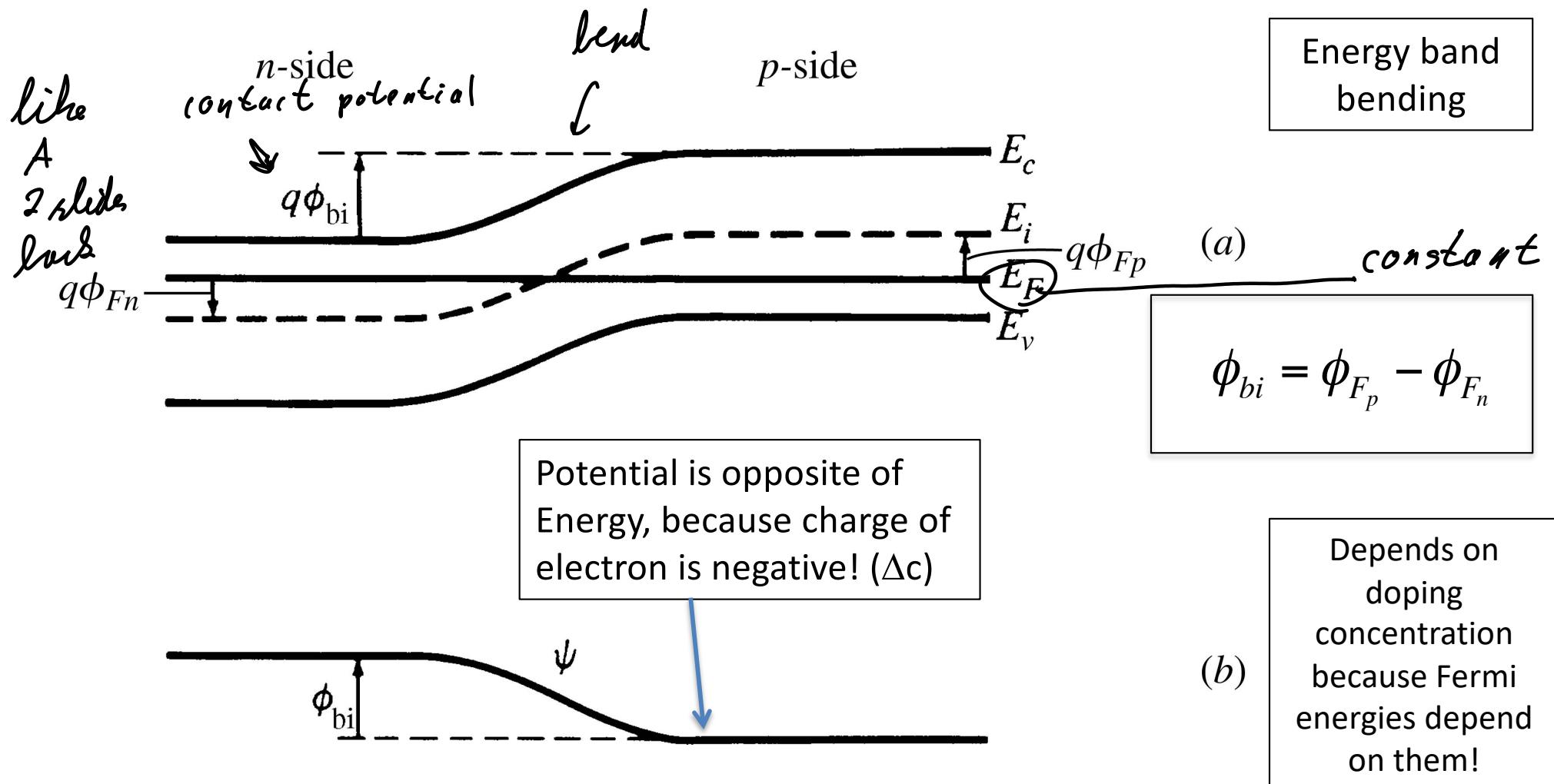
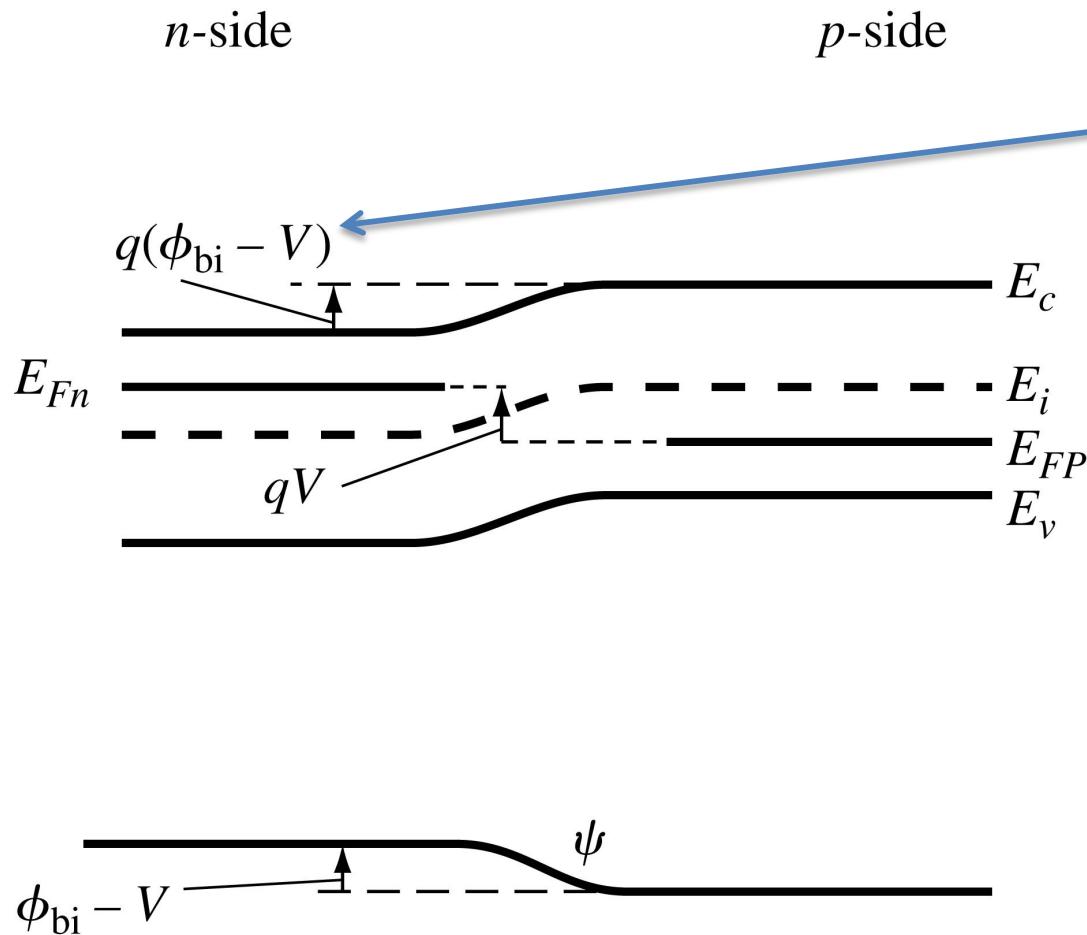


FIGURE 1.22 (a) Energy band diagram and (b) potential for a pn junction with zero bias.

Applying Forward Bias : non-equilibrium



Higher energy on n and p side, because way Voltage source is connected (i.e., + connected to p and – connected to n)

(a)

$$I \approx I_0 \cdot (e^{V/\phi_t} - 1)$$

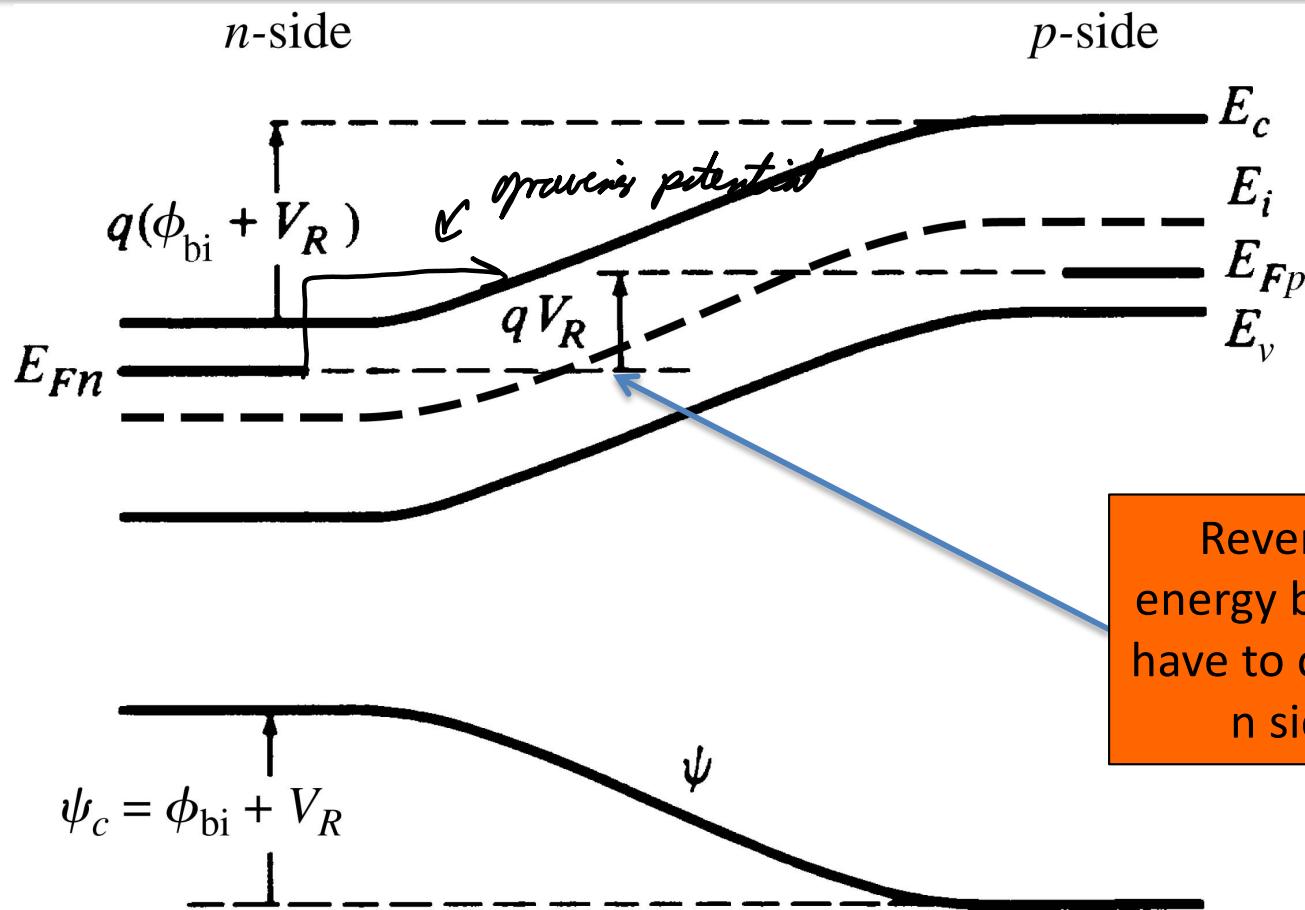
I_0 depend on junction geometry and physical parameters of the semiconductor material and is an increasing function of temperature

(b)

Actually bends less!

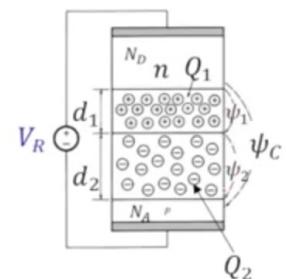
FIGURE 1.23 (a) Energy band diagram and (b) potential for a pn junction under forward bias V .

Non-equilibrium : Reverse Bias



Assume a step junction

(a)



Reverse bias raises the energy barrier that electrons have to climb to get from the n side to the p side.

(b)

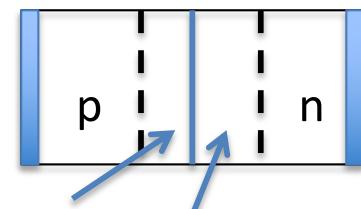


FIGURE 1.24 (a) Energy band diagram and (b) potential for a pn junction under reverse bias V_R .

Charge neutrality!

$$Q_1 + Q_2 = 0$$

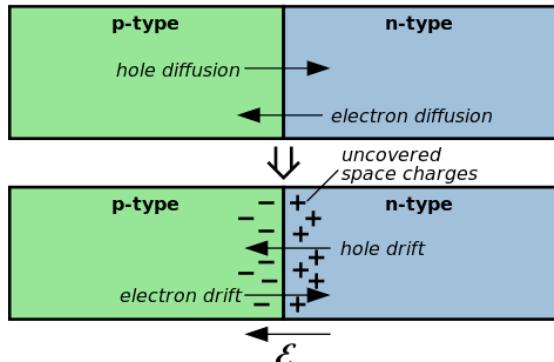
Charge Neutrality

- If the cross-sectional area of the junction is A , the part of the depletion region in the n side has a volume equal to $d_1 \cdot A$ and, therefore, a total number of ionized atoms equal to $d_1 \cdot A \cdot N_D$.

$$Q_1 = +q \cdot (d_1 \cdot A) \cdot N_D$$

- Similarly, the total charge on the p side of the depletion region due to ionized acceptor atoms is

$$Q_2 = -q \cdot (d_2 \cdot A) \cdot N_A$$



$$Q_1 = -Q_2$$

$$\frac{d_1}{d_2} = \frac{N_A}{N_D}$$

$$\epsilon_{peak} = \frac{q \cdot N_D \cdot d_1}{\epsilon_S} = \frac{q \cdot N_A \cdot d_2}{\epsilon_S}$$

[Wikipedia]

pn region : closer up!

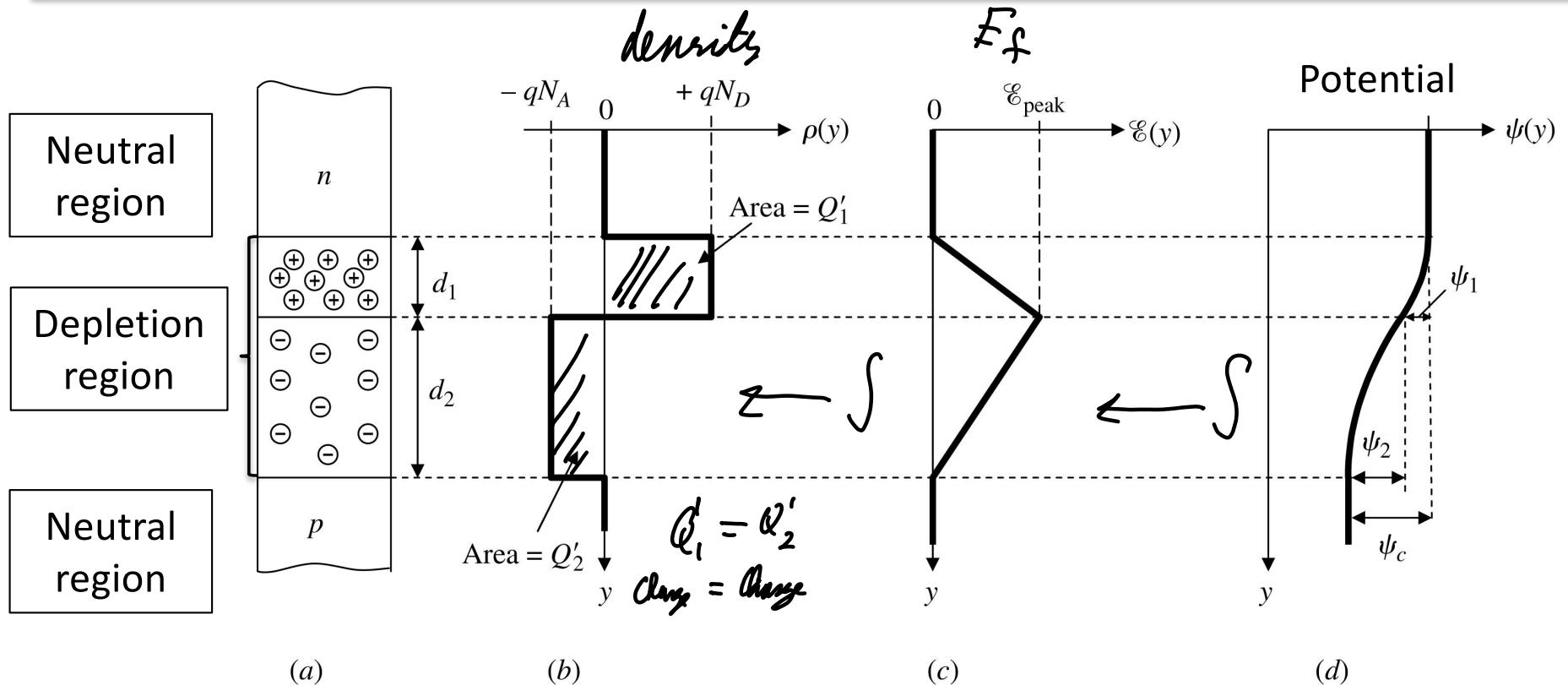
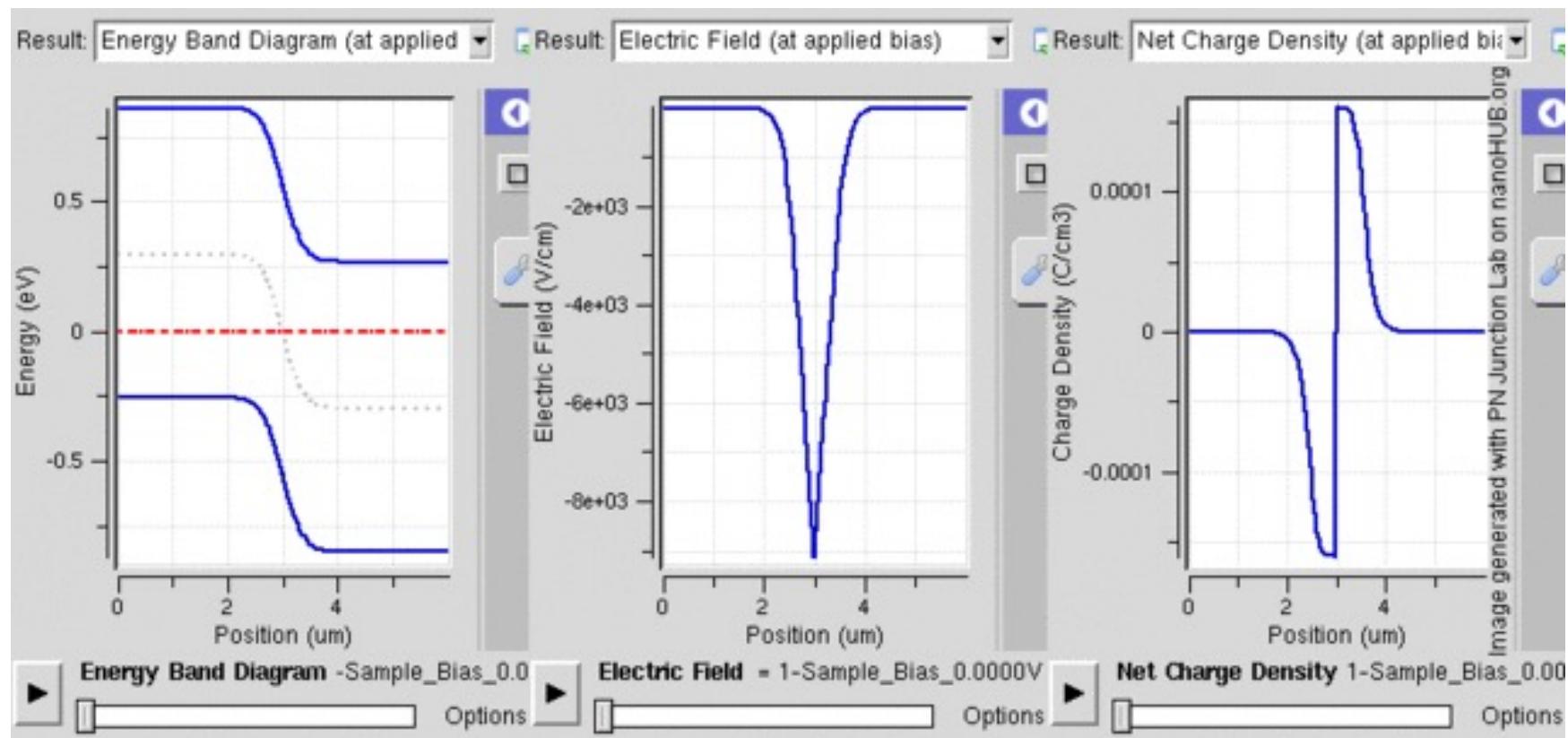


FIGURE 1.25 (a) A reverse-biased pn junction; (b) charge density; (c) electric field; (d) potential.

Nice Graphic



[Wikipedia]

Two Sided (abrupt) pn Junction

- Similar derivations for depletion region distances which can be analogous to the distance between dielectric in a capacitor can be made (see p38).

$$\psi_1 = \frac{\varepsilon_{peak} \cdot d_1}{2} = \frac{q \cdot N_D \cdot d_1^2}{2 \cdot \varepsilon_S}$$

$$\psi_2 = \frac{\varepsilon_{peak} \cdot d_2}{2} = \frac{q \cdot N_A \cdot d_2^2}{2 \cdot \varepsilon_S}$$

$$\psi_1 + \psi_2 = \psi_c$$

Charge neutrality

$$d_1 = \frac{N_A}{N_D} \cdot d_2$$

$$(N_A \cdot d_2)^2 \cdot \frac{N_A + N_D}{N_A \cdot N_D} = \frac{2 \cdot \varepsilon_S}{q} \cdot \psi_c$$

$$d_1 + d_2 = \sqrt{\frac{2 \cdot \varepsilon_S}{q} \cdot \frac{N_A + N_D}{N_A \cdot N_D} \cdot \psi_c}$$

↙ per area

$$Q'_2 = \frac{Q_2}{A} = -q \cdot d_2 \cdot N_A = -\sqrt{2 \cdot q \cdot \varepsilon_S} \cdot \sqrt{\frac{N_A \cdot N_D}{N_A + N_D} \cdot \psi_c}$$

Either side is not degenerate!!

One Sided pn Junction

$n \geq 10^{19} \text{ cm}^{-3}$

- Many times, we want to heavily dope one side of the junction, so this becomes a n⁺p junction (here we assume step (abrupt) junction)

$$N_D \gg N_A$$

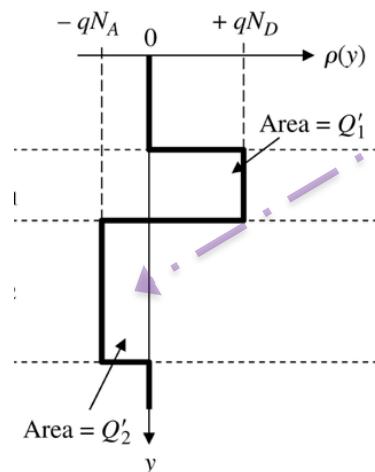
Practically all of the depletion region extends into the p side

$$d_1 \ll d_2$$

$$\psi_1 \ll \psi_2$$

$$d_2 \approx \sqrt{\frac{2 \cdot \varepsilon_S}{q \cdot N_A}} \cdot \sqrt{\psi_c}$$

$$\psi_2 \approx \psi_c = \phi_{bi} + V_R$$



$$Q'_2 = \frac{Q_2}{A} = -\sqrt{2 \cdot q \cdot \varepsilon_S \cdot N_A} \cdot \sqrt{\psi_c}$$

Outside the depletion region, the current is carried mostly by majority carriers

MOS Transistor

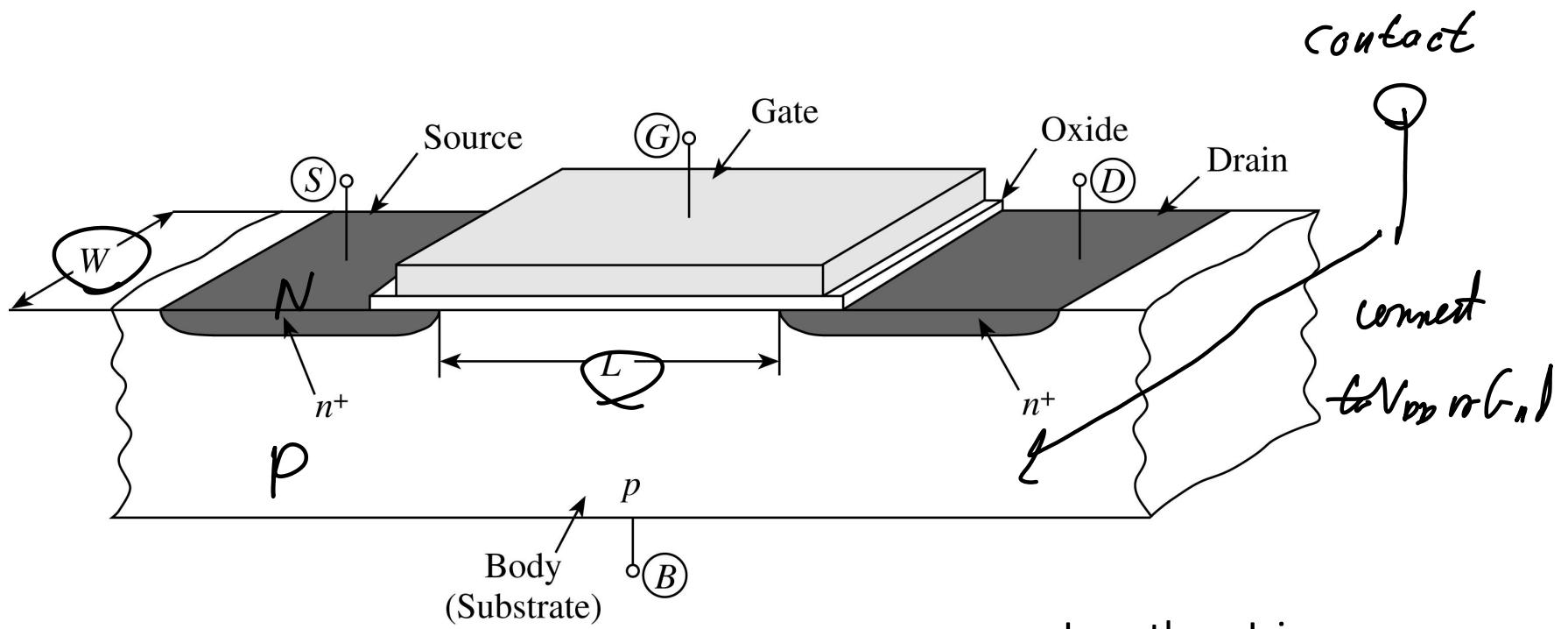
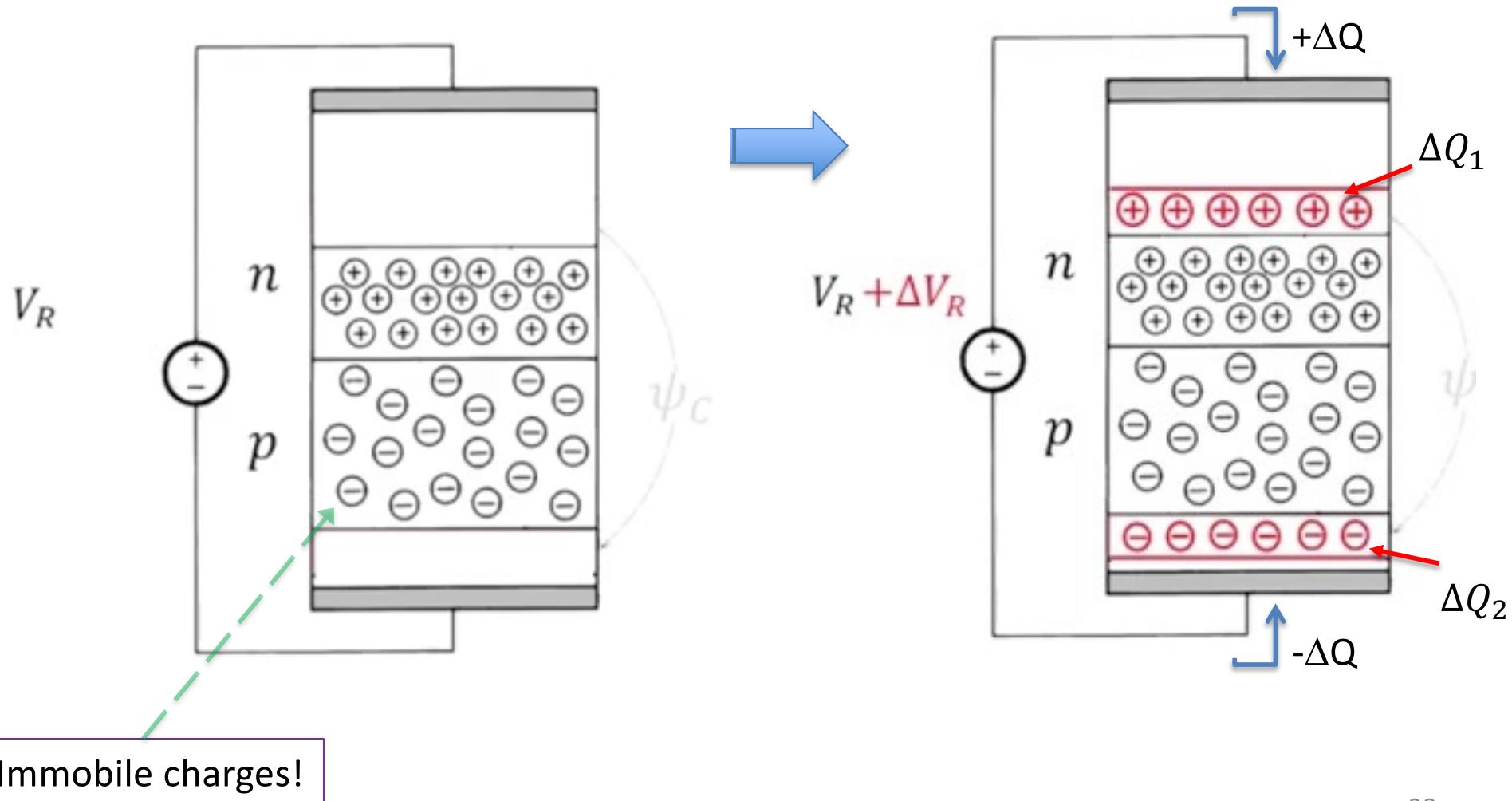


FIGURE 1.30 Simplified structure of an n-channel MOS transistor.

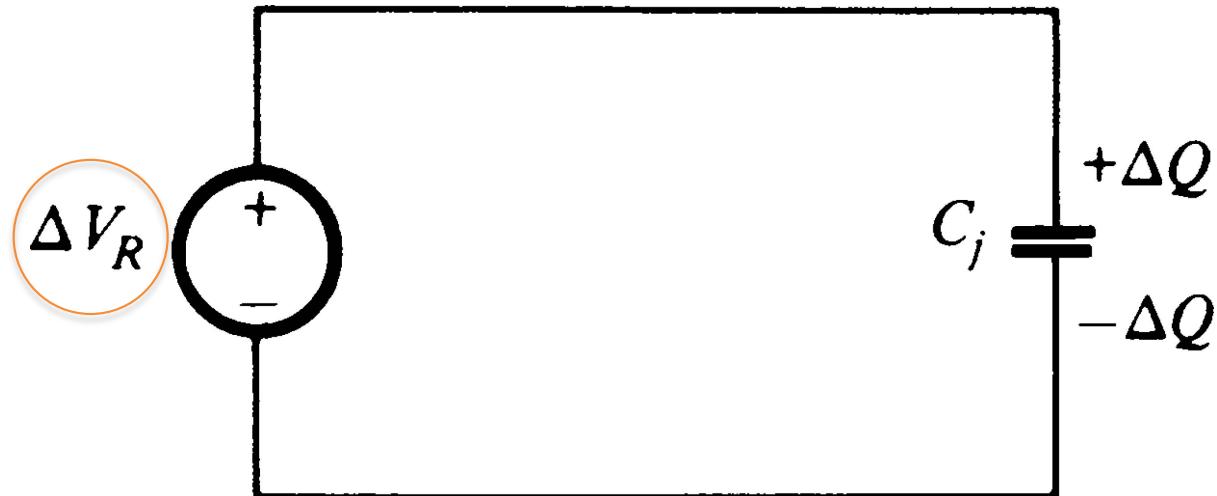
Length or L is sometimes called the minimum feature size!

Reverse Voltage (small-signal capacitance)



Analogy : Capacitance

vibrator \rightarrow varying capacitor



Assumed as a
linear
capacitor!



FIGURE 1.27 Small-signal equivalent circuit of a reverse-biased pn junction driven by a voltage source.

$$C_j = \frac{\Delta Q}{\Delta V_R} \text{ fF} \quad \Delta V_R \rightarrow 0 \quad \Delta Q \rightarrow 0$$
$$\Delta Q = -\Delta Q_2$$

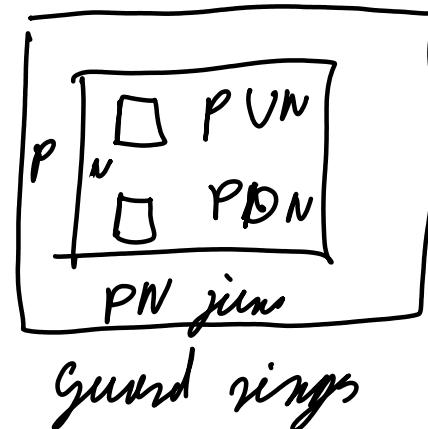
Always follows
Physics/Chemistry

Capacitance

- Capacitance is the ultimate destructor (not CS meaning ☺) of the NMOS/PMOS circuitry.
 - But, for the benefit of the perfect load, we can overcome this limitation.
 - Engineering is always about outweighing the positives from the negatives.

$$C_j = \frac{\Delta Q}{\Delta V_R} \quad C'_j = \frac{\Delta Q'}{\Delta V_R}$$

*keeps the
 E_S isolated!*



Called the junction capacitance and defines the effective charge per Voltage in a given region!

Junction (depletion) Capacitance

- Junction capacitance per area is a function of charge and reverse Voltage as more charge is incrementally grown in the depletion region.

$$C'_j = \frac{\Delta Q'}{\Delta V_R} \rightarrow -\frac{dQ'_2}{dV_R} = \frac{\sqrt{2 \cdot q \cdot \varepsilon_S \cdot N_A}}{2 \cdot \sqrt{V_R + \phi_{bi}}}$$

One-sided
Step junction

Important SPICE
parameter (C_{J0})

$$C'_j = \frac{C'_{j0}}{\left[\left(\frac{V_R}{\phi_{bi}} \right) + 1 \right]^{\alpha_j}}$$

generalized

- Linear graded junction $\alpha_j = \frac{1}{3}$
- Non linearly graded junction or step junction is between $\frac{1}{2}$ and $\frac{1}{3}$

Junction Capacitance

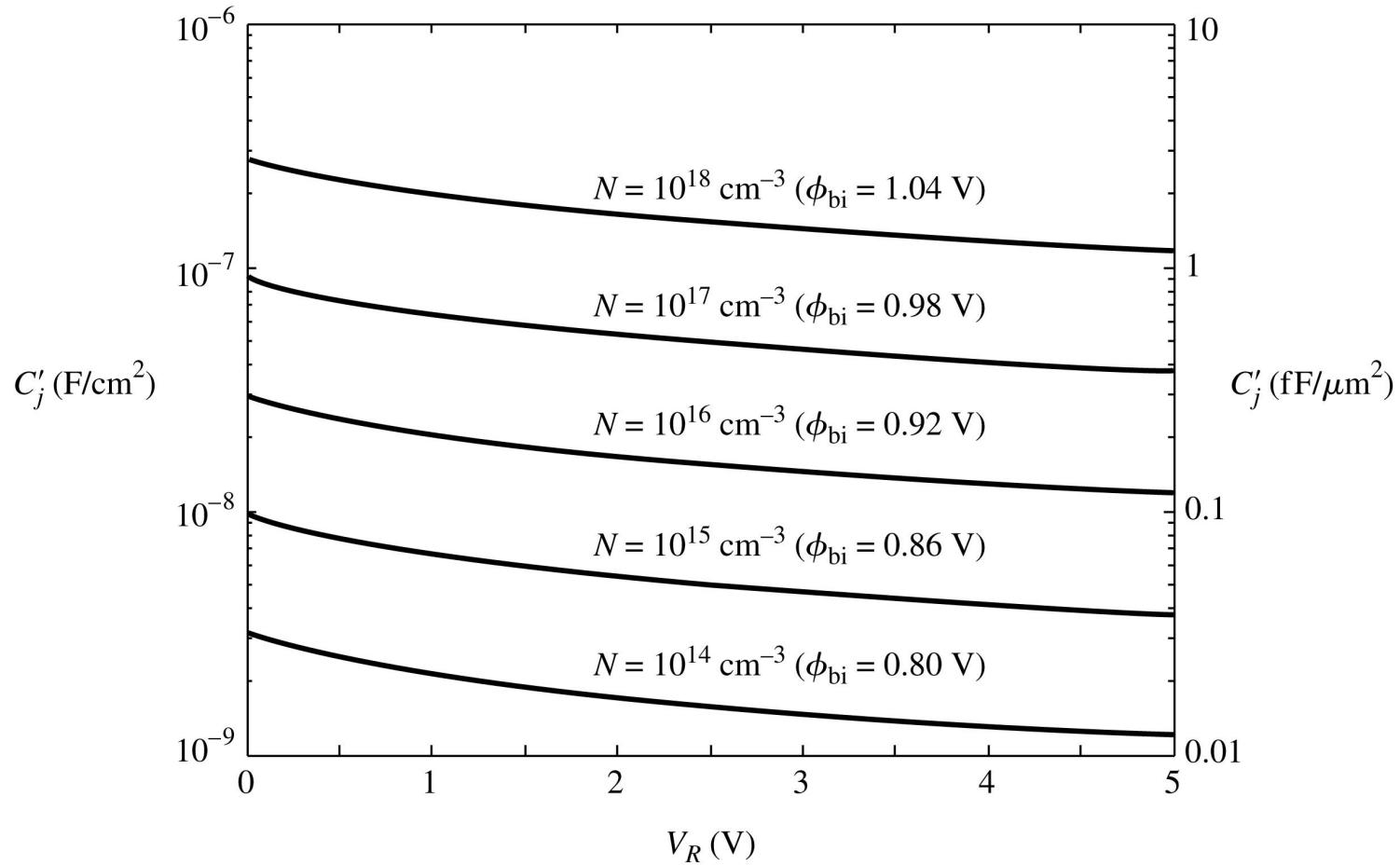
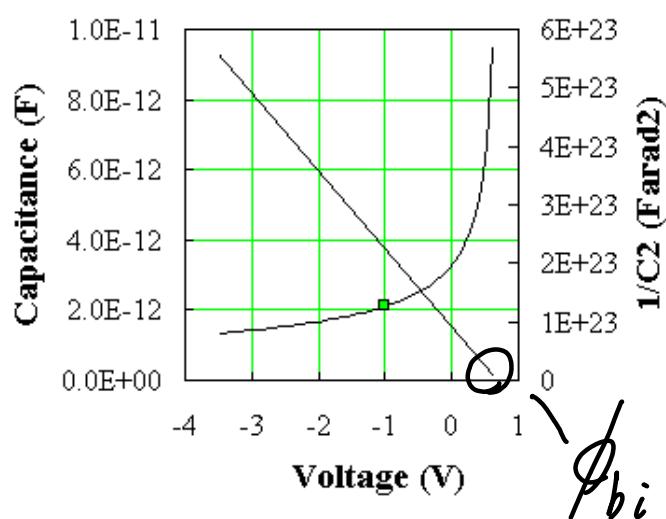


FIGURE 1.28 One-sided step-junction small-signal capacitance per unit area vs. reverse-bias voltage, with doping concentration of the lightly doped side as a parameter. The heavily doped side is assumed degenerate; corresponding approximate values of built-in voltage are indicated. T = 300 K.

Capacitance of pn junction

- 2 types of capacitance associated with a pn junction:
 - C_{dep} : depletion (junction) capacitance
 - C_D : diffusion capacitance (due to variation of stored minority charge in the quasi-neutral regions)
- Both capacitances are non-linear (oh-oh)
 - <https://wiki.analog.com/university/courses/electronics/electronics-lab-pn-junction-cap#:~:text=The%20PN%20junction%20capacitance%20is,capacitance%20is%20equal%20to%20zero.>



$$\frac{1}{C_j^2} = \frac{2}{q \cdot \epsilon_S} \cdot \frac{N_A + N_D}{N_A \cdot N_D} \cdot (\phi_{bi} + V_R)$$

Interesting Fact: The built-in voltage is obtained at the intersection of the $1/C^2$ curve and the horizontal axis, while the doping density is obtained from the slope of the curve.

I-V Relationship

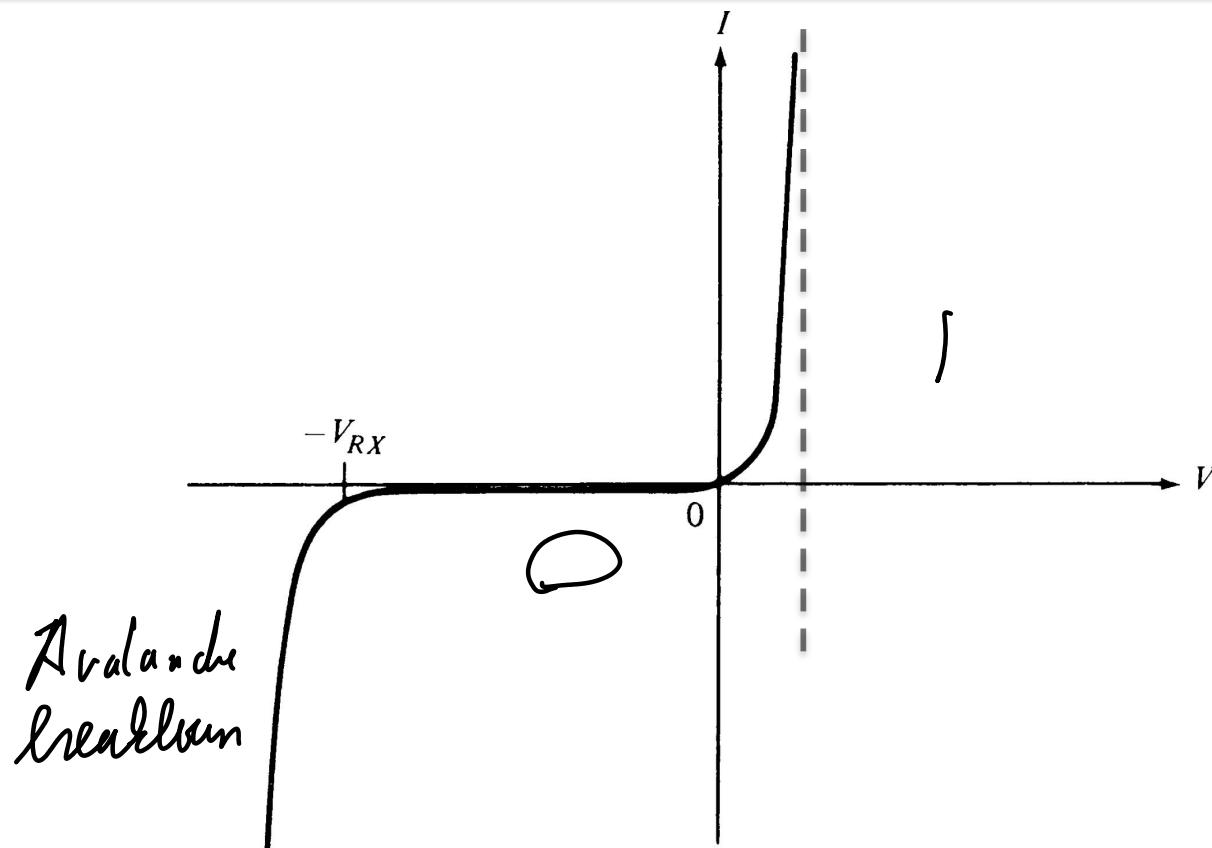
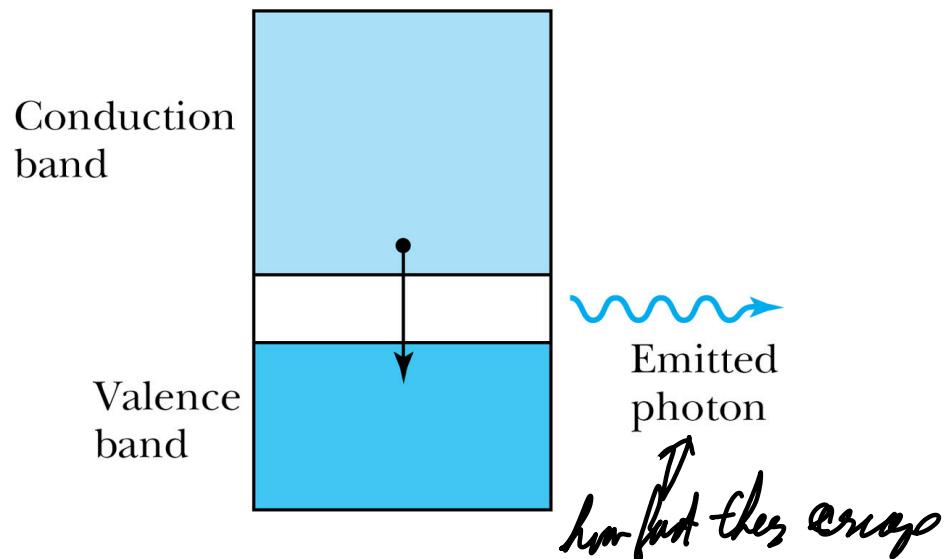


FIGURE 1.26 Current vs. voltage for a pn junction.

Light-Emitting Diodes (LEDs)

- Another important kind of diode is the **light-emitting diode (LED)**. Whenever an electron makes a transition from the conduction band to the valence band (effectively recombining the electron and hole) there is a release of energy in the form of a photon (Figure 11.17). In some materials the energy levels are spaced so that the photon is in the visible part of the spectrum. In that case, the continuous flow of current through the LED results in a continuous stream of nearly monochromatic light.

Figure 11.17: Schematic of an LED. A photon is released as an electron falls from the conduction band to the valence band. The band gap may be large enough that the photon will be in the visible portion of the spectrum.



Photovoltaic Cells

- An exciting application closely related to the LED is the **solar cell**, also known as the **photovoltaic cell**. Simply put, a solar cell takes incoming light energy and turns it into electrical energy. A good way to think of the solar cell is to consider the LED in reverse (Figure 11.18). A *pn*-junction diode can absorb a photon of solar radiation by having an electron make a transition from the valence band to the conduction band. In doing so, both a conducting electron and a hole have been created. If a circuit is connected to the *pn* junction, the holes and electrons will move so as to create an electric current, with positive current flowing from the *p* side to the *n* side. Even though the efficiency of most solar cells is low, their widespread use could potentially generate significant amounts of electricity. Remember that the “solar constant” (the energy per unit area of solar radiation reaching the Earth) is over 1400 W/m², and more than half of this makes it through the atmosphere to the Earth’s surface. There has been tremendous progress in recent years toward making solar cells more efficient.

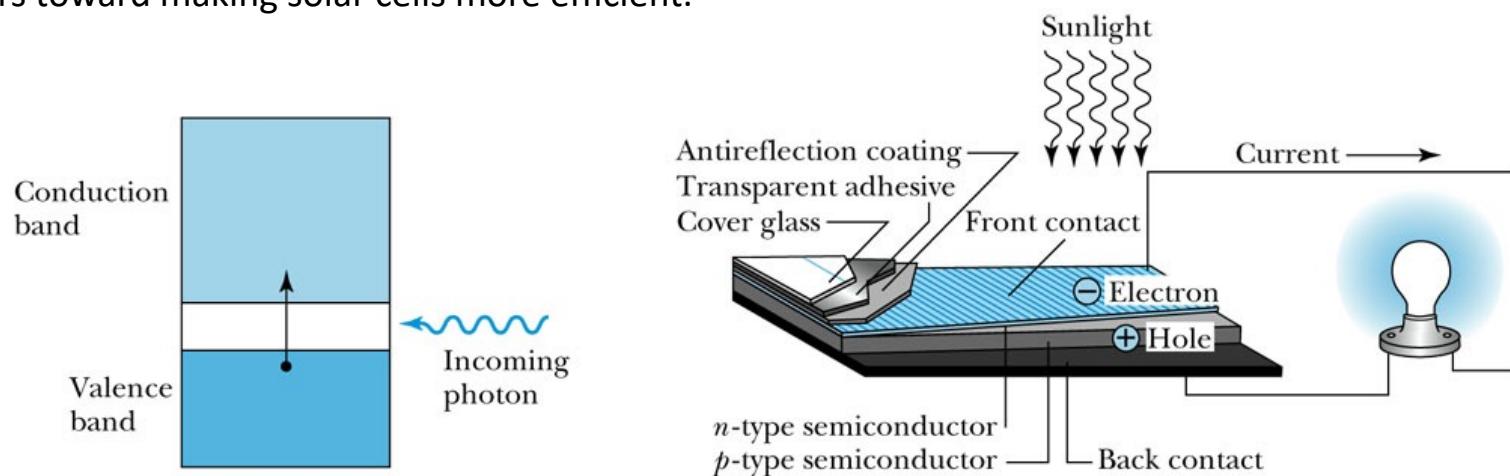
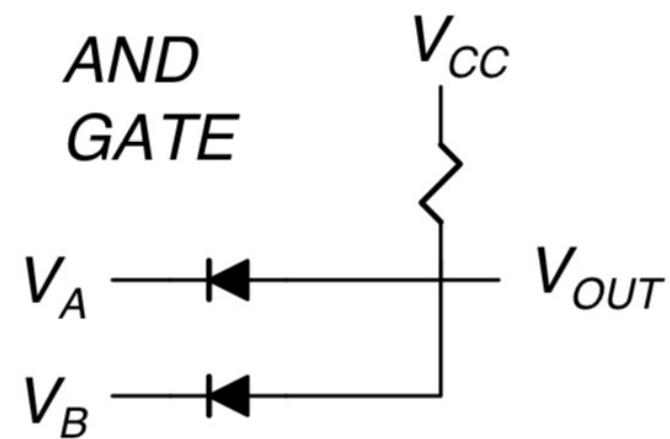
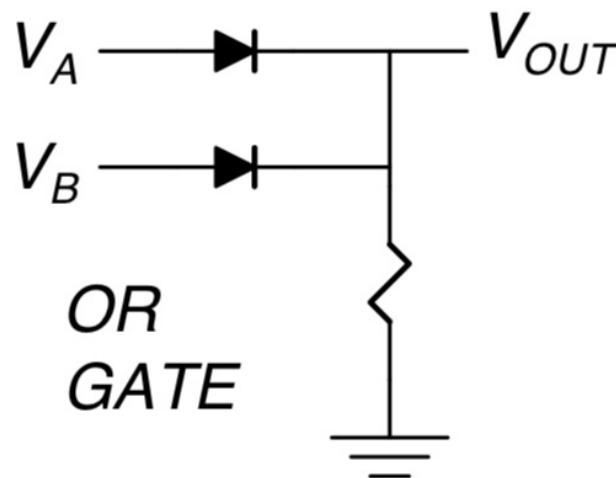


Figure 11.18: (a) Schematic of a photovoltaic cell. Note the similarity to Figure 11.17. (b) A schematic showing more of the working parts of a real photovoltaic cell. *From H. M. Hubbard, Science 244, 297-303 (21 April 1989).*

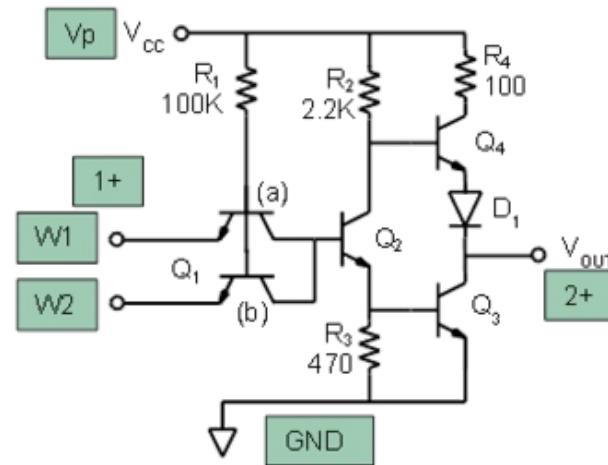
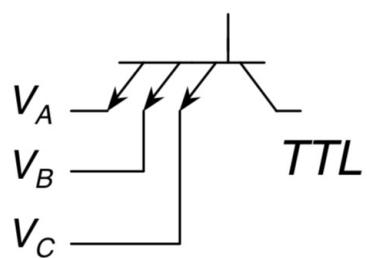
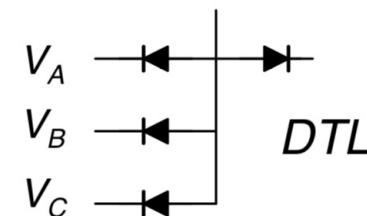
DTL

- Early computers when transitioning to semiconductors, could use diodes.
- These are called Diode Transistor Logic.
- Unfortunately, DTL suffers from voltage degradation from one stage to the next.
- It also only permits OR and AND functions ☹.



TTL

- DTL was really replaced with TTL or transistor-transistor logic which a majority of gates were made of during the 1970s and 1980s.
- In TTL, a single multi-emitter BJT replaces the input diodes , resulting in a more area-efficient design.
- TTL gates were also reasonably fast, easy to build, and could be used with multiple gates and connections.



TTL NAND gate

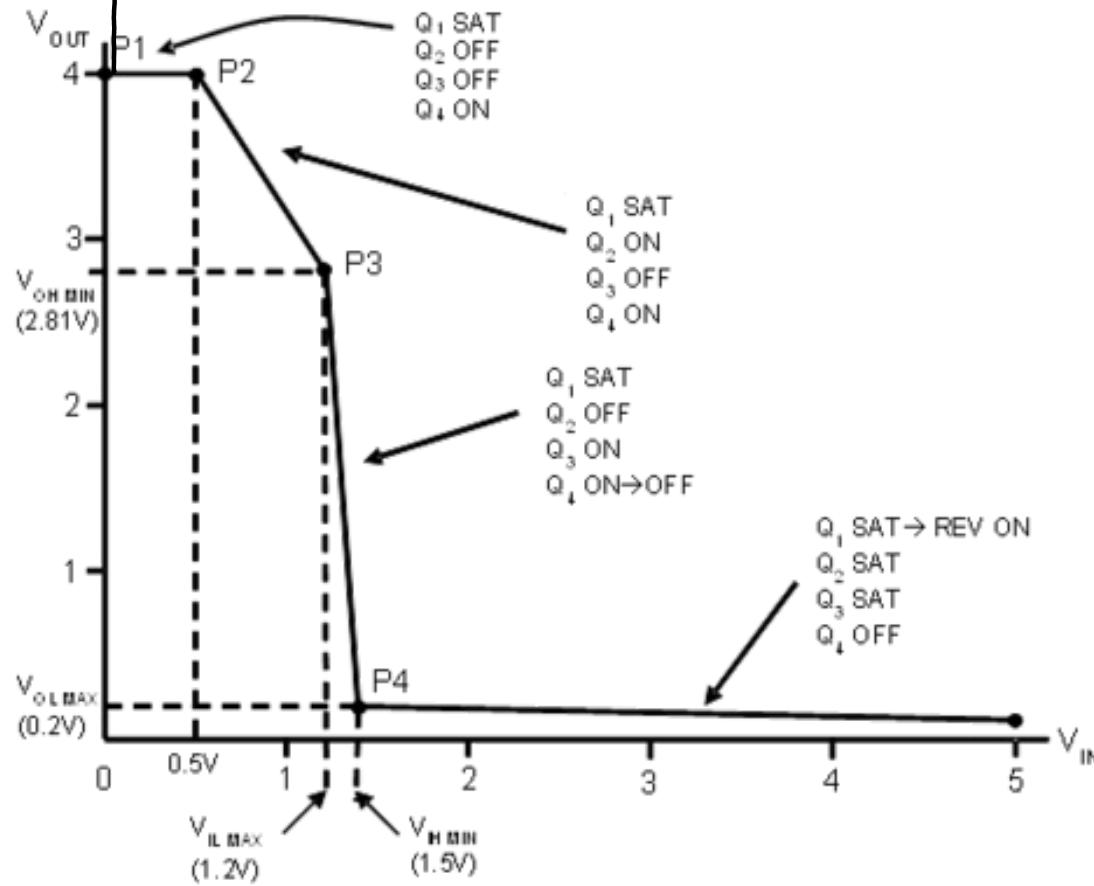
TTL inverter VTC

V_{DD}

• Cool Link: <https://wiki.analog.com/university/courses/electronics/electronics-lab-27>



AHEAD OF WHAT'S POSSIBLE™



[Smithsonian]

Steve Wozniak TTL board for Apple I

What is the takeaway?

- Can easily make a switch out a pn junction!!!
- We can also use the pn junction to isolate areas for non-current flow.
- Unfortunately, as the charge grows, it eventually sits in a non-ideal situation with a Reverse Voltage and some amount of charge.
 - This ultimately results in a capacitance per unit area.
 - Ultimately slows down a circuit due to the charge needed to get the full potential.
- We will explore more concepts in coming lectures including current versus voltage bias.
- CMOS is still “it” and we will find that its robustness and ease in making logic makes it, by far, the choice of digital logic designers today.