



SWITCHES AND WHY ARE THEY IMPORTANT FOR DIGITAL

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Friendly Reminder

- HW0 due tonight – don't miss free points!
- Any questions, feel free to contact me.
- Do not forget HW1 is due a week from today!!!.

Combining Energy Band Diagrams

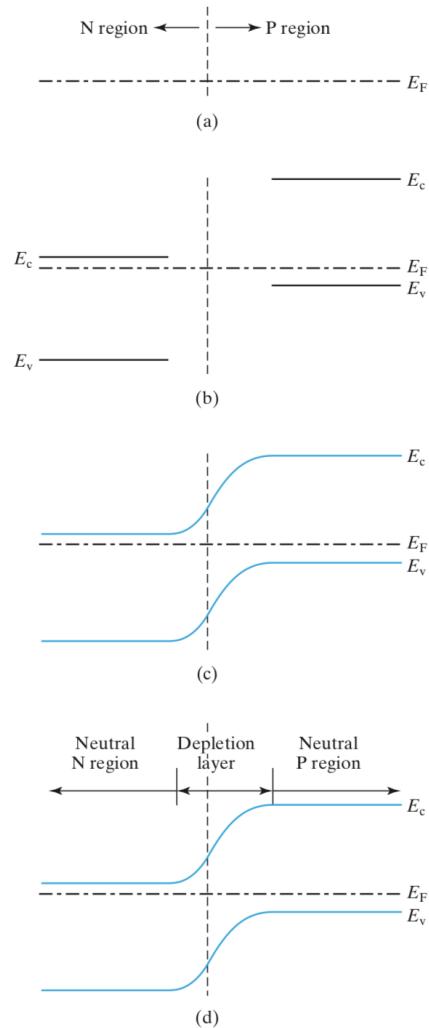


FIGURE 4-3 (a) and (b) Intermediate steps of constructing the energy band diagram of a PN junction. (c) and (d) The complete band diagram.

[Chenming Hu]

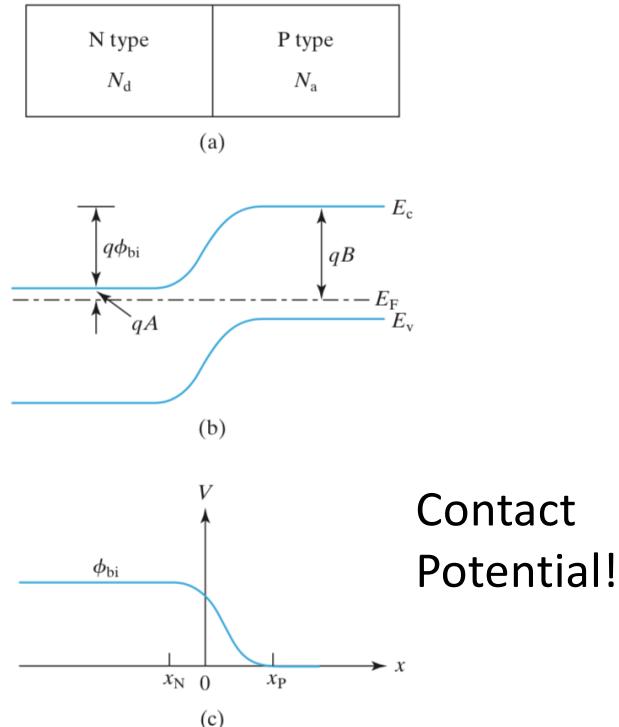
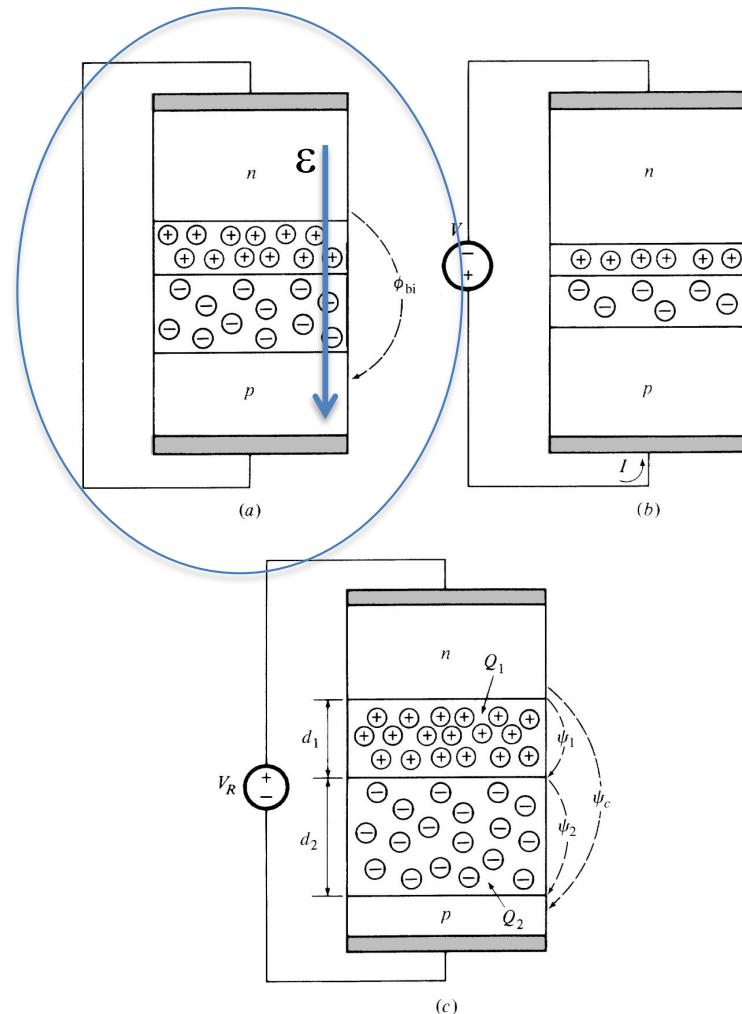


FIGURE 4-4 (a) A PN junction. The built-in potential in the energy band diagram (b) shows up as an upside down mirror image in the potential plot (c).

$$\phi_{bi} = \frac{k \cdot T}{q} \cdot \ln \frac{N_D \cdot N_A}{n_i^2}$$

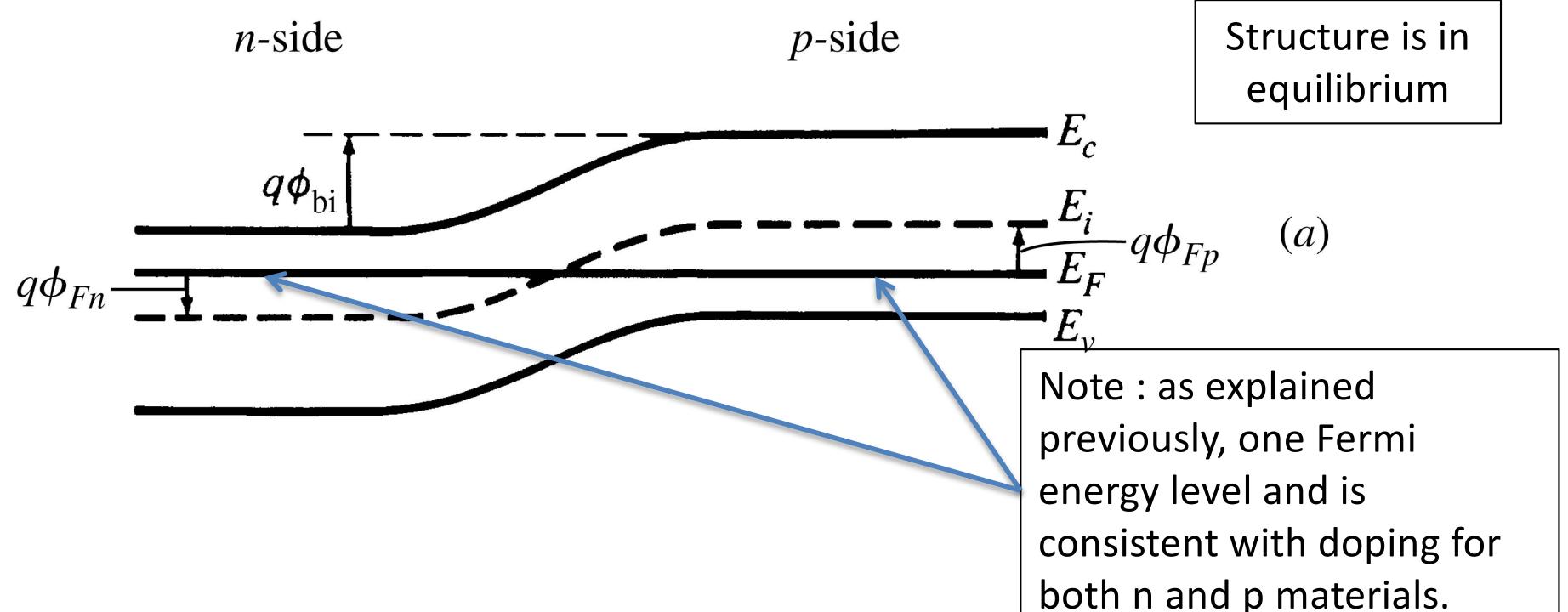
(more later on this...)

pn junction : combine (zero bias)



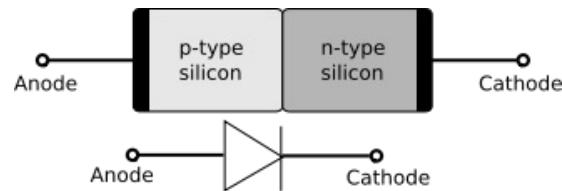
- Assume that connection between two devices is actually a step junction and that each side is uniformly doped.
- ϕ_{bi} : built-in potential
 - Why?

n and p energy bands @equilibrium (zero bias)



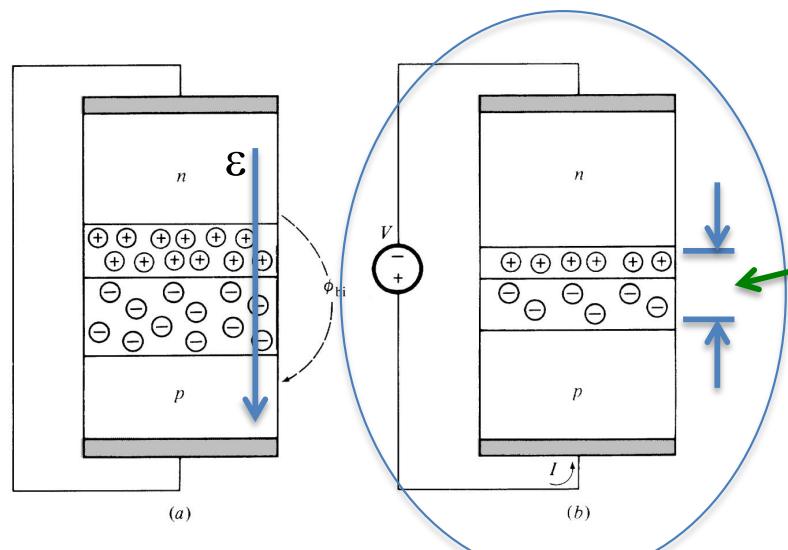
$$\phi_{bi} = \phi_{Fp} - \phi_{Fn}$$

FIGURE 1.22 (a) Energy band diagram and (b) potential for a pn junction with zero bias.



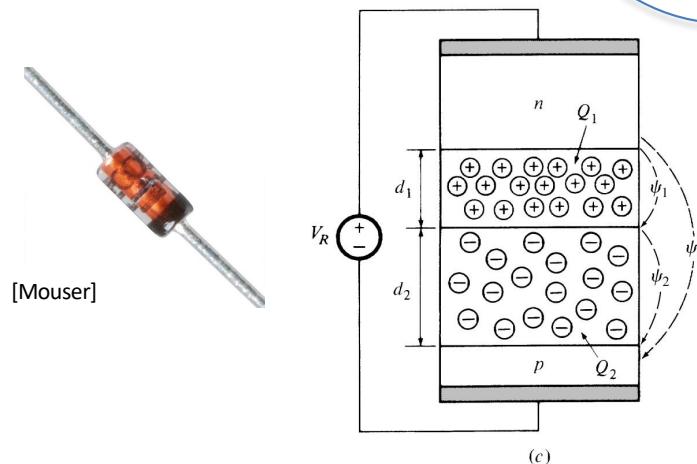
<https://www.youtube.com/watch?v=JBtEckh3L9Q>

pn junction : now add bias!

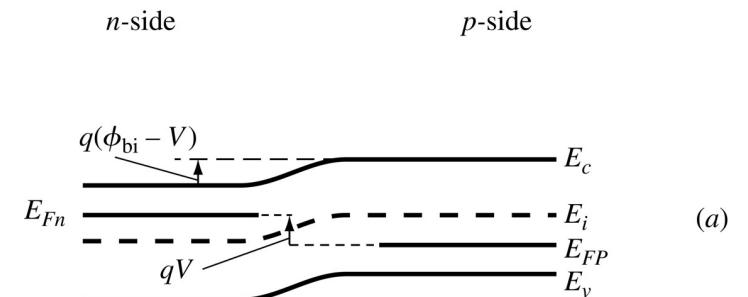


Depletion Region : combined area where two meet and have electrons and holes interact!

Structure is in non-equilibrium

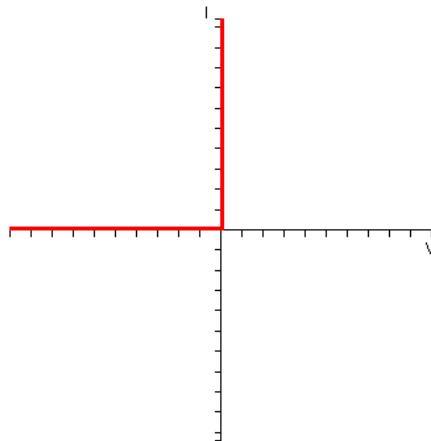


Forward biased (positive to p-type, negative to n-type)
Reverse biased (negative to p-type, positive to n-type)



Simplify Voltage for Current

- How can we actually get Voltage to apply a switch?
 - This is an interesting concept and the idea is to take the current out of the view.
 - Simplify the Voltage as an actual two state system:
 - VDD (power supply)
 - VSS (ground)
- Original designers did not have this luckily.
 - They had to deal with two states, but at different levels.



[wiki]

DID YOU
KNOW



Some systems will use VDD! or VDD bang to indicate it is a global supply!

Voltage Transfer Characteristic

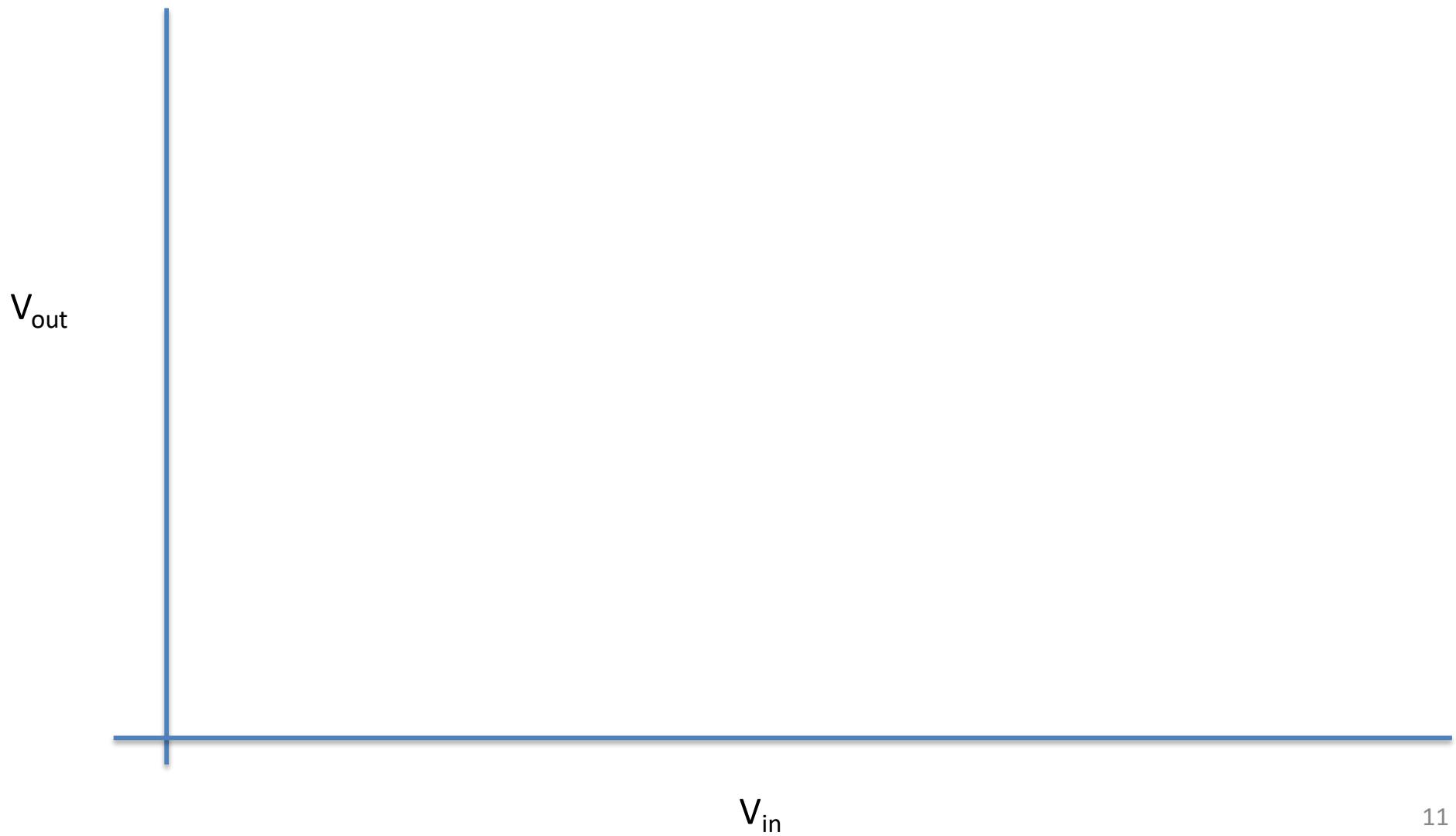
Digital Levels

- Instead of worrying about specific Voltage levels, it would be easier to have certain levels. If a Voltage level falls somewhere in this level it is either a Logic 0 or Logic 1.
 - Allows us to compute the output only for inputs in the allowable range.
 - Very simple.
 - Model transistor as being conducting or non-conducting: Aha!!! a switch!
 - However, always make sure Voltage is somewhere in one of the two allowable ranges.
 - Otherwise, the Voltage level is not valid.
 - Would also be nice to be able to make levels restore if they fall somewhere in the middle of the allowable range.
 - This makes the abstraction on the digital value of 0 or 1.

Digital Abstraction

- Divide Voltage levels into discrete levels.
 - Logic 0 = True.
 - Logic 1 = False.
 - Logic X = somewhere between True and False.
 - Undefined = could be devastating to a device, therefore, must be avoided.
- These are modeled by popular Hardware Descriptive Languages as VHDL and Verilog.
- Each logic gate restores the logic level.
 - Noise is not cumulative.
 - Output Voltage range is narrower than input range.
 - Noise margin determines transmissibility of gate.

VTC Revisited and Defined



4 Values

- V_{OH}
 - Usually, designated by design (the only one)
- V_{OL}
- V_{IL}
- V_{IH}

$m = \text{derivative} = \Delta Y / \Delta X$ (usually always there within circuit simulation)

Noise Margins

- Define values to give details on what can be connected to other circuits!

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

recommended operating conditions (see Note 3)

		SN5404			SN7404			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			16			16	mA
T _A	Operating free-air temperature	-55	125		0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

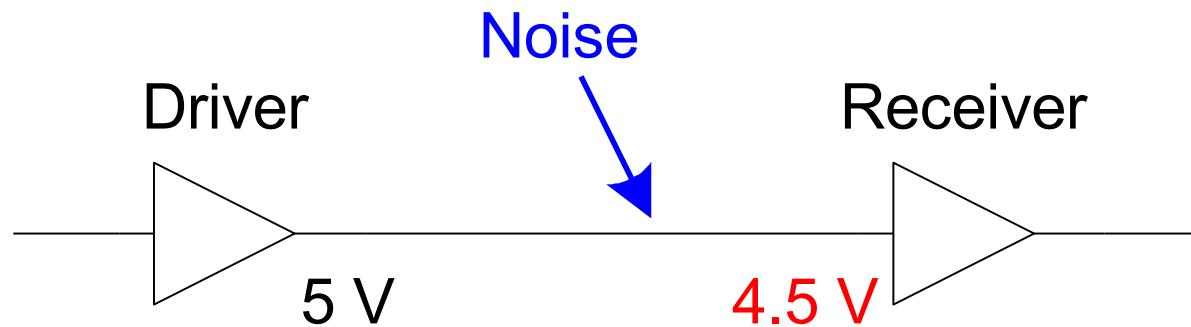
[TI databook SN7404]

Logic Levels

- Discrete voltages represent 1 and 0
- For example:
 - 0 = *ground* (GND) or VSS or 0 volts
 - 1 = V_{DD} or 5 volts
- What about 4.99 volts? Is that a 0 or a 1?
 - What about 3.2 volts?
- *Range* of voltages for 1 and 0
 - Different ranges for inputs and outputs to allow for *noise*

What is Noise?

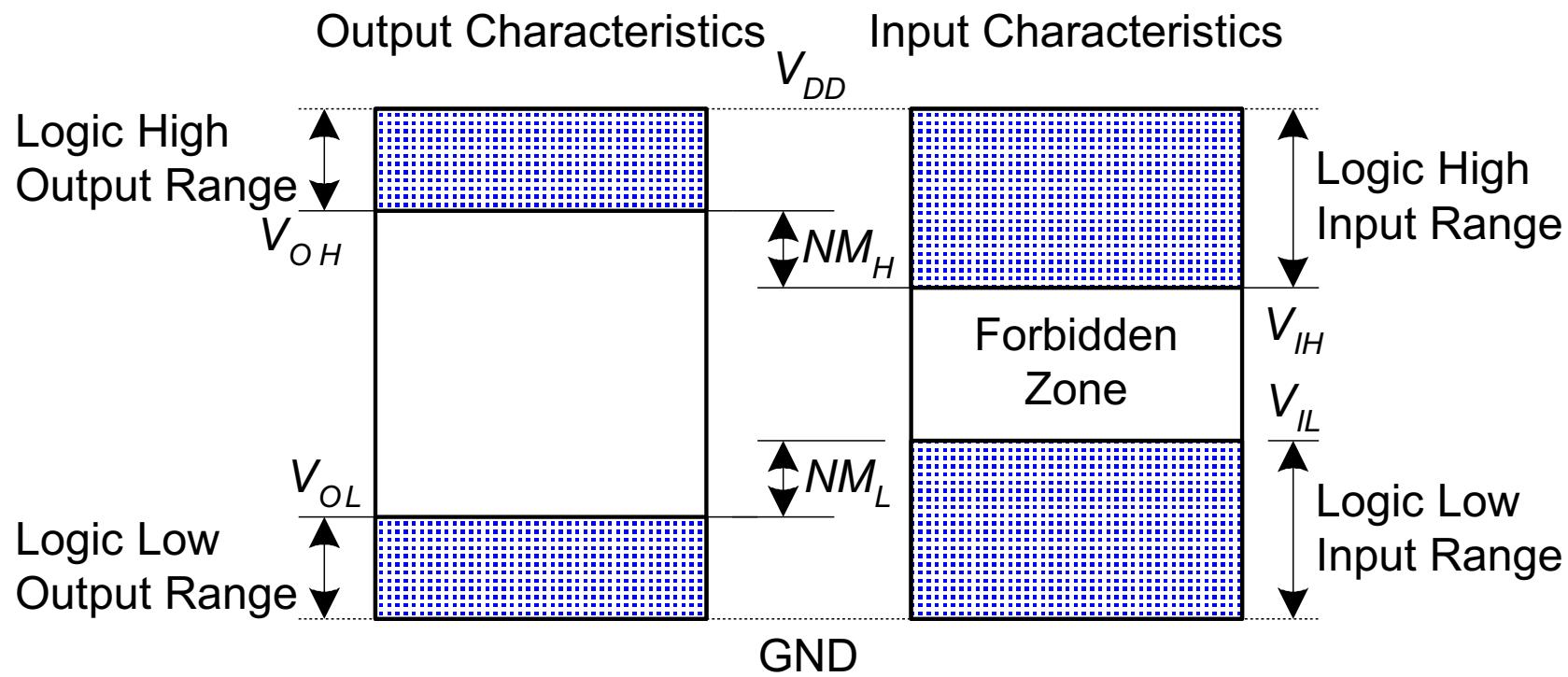
- **Anything that degrades the signal**
 - e.g., resistance, power supply noise, coupling to neighboring wires, etc.
- **Example:** a gate (driver) outputs 5 V but, because of resistance in a long wire, receiver gets 4.5 V



The Static Discipline

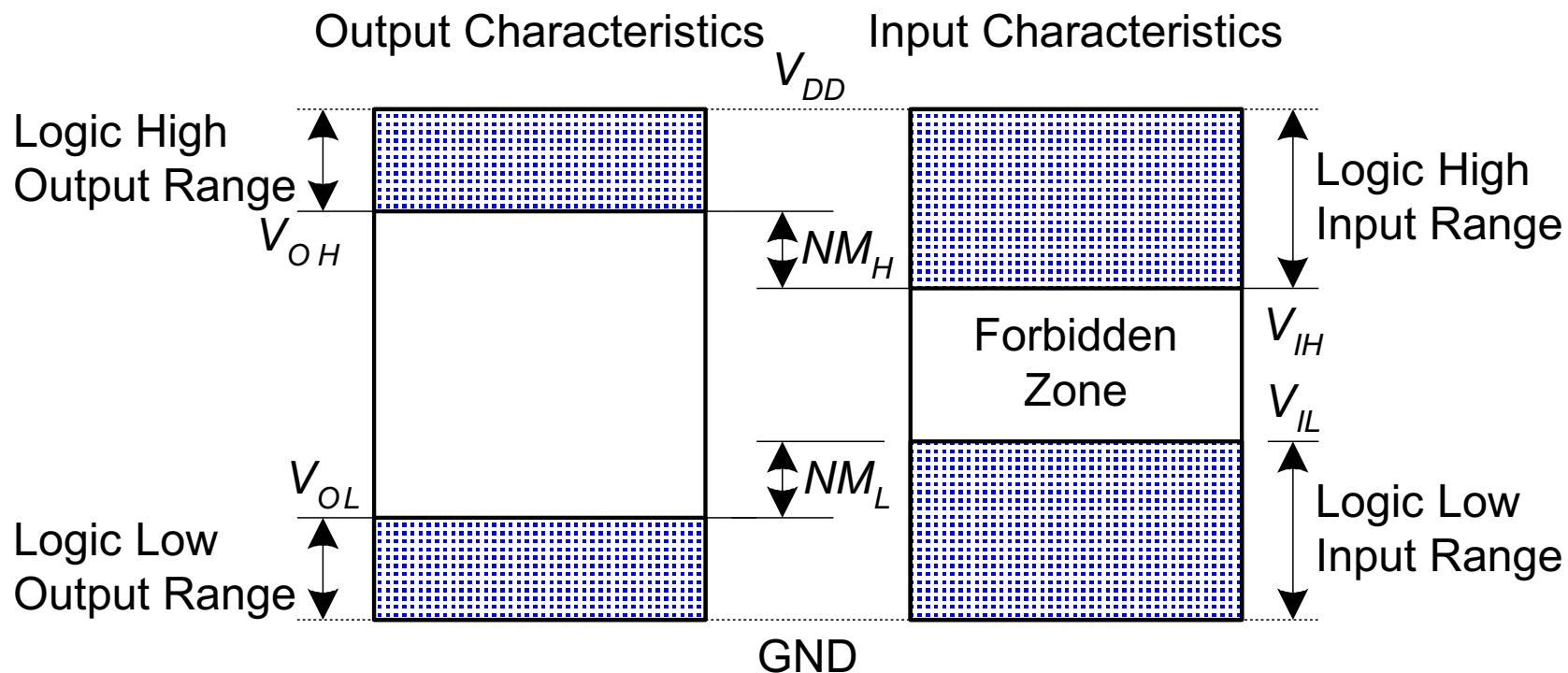
- With logically valid inputs, every circuit element must produce logically valid outputs.
- Use limited ranges of voltages to represent discrete values.
- Gates are limited by how much current and voltage they can produce.
 - Current ultimately leads to specific voltages that define its Noise Margin.

Logic Levels



[Harris]

Noise Margins



[Harris]

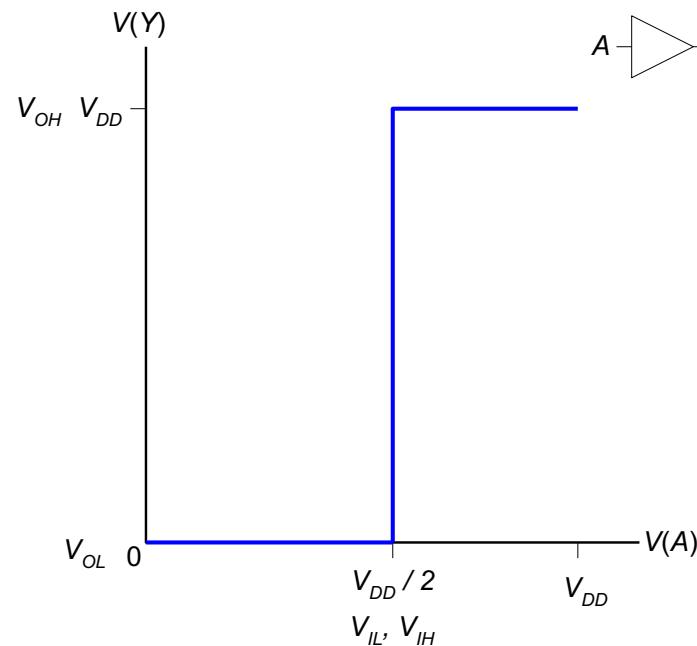
$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

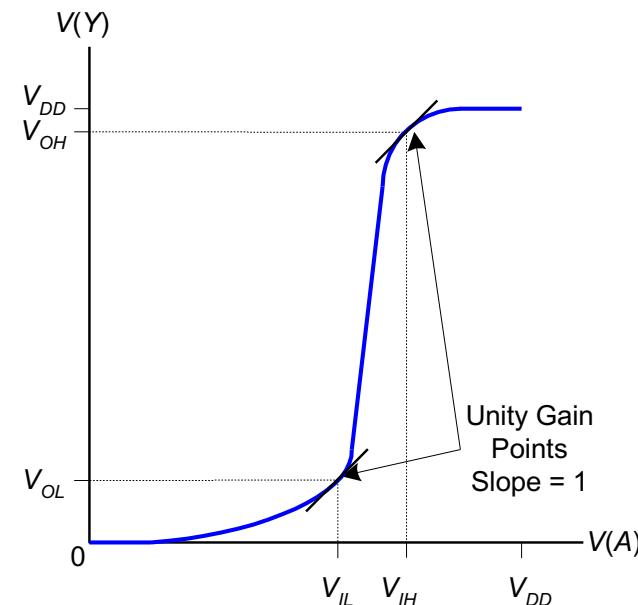


DC Transfer Characteristics

Ideal Buffer:



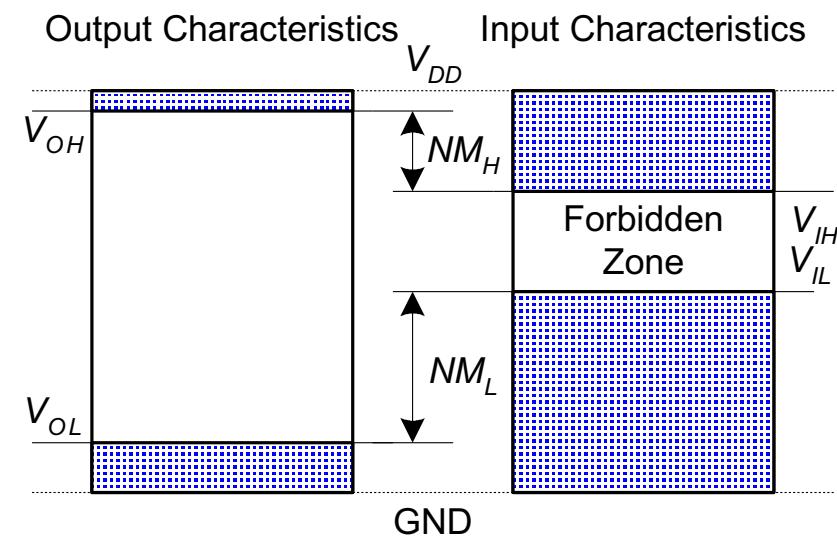
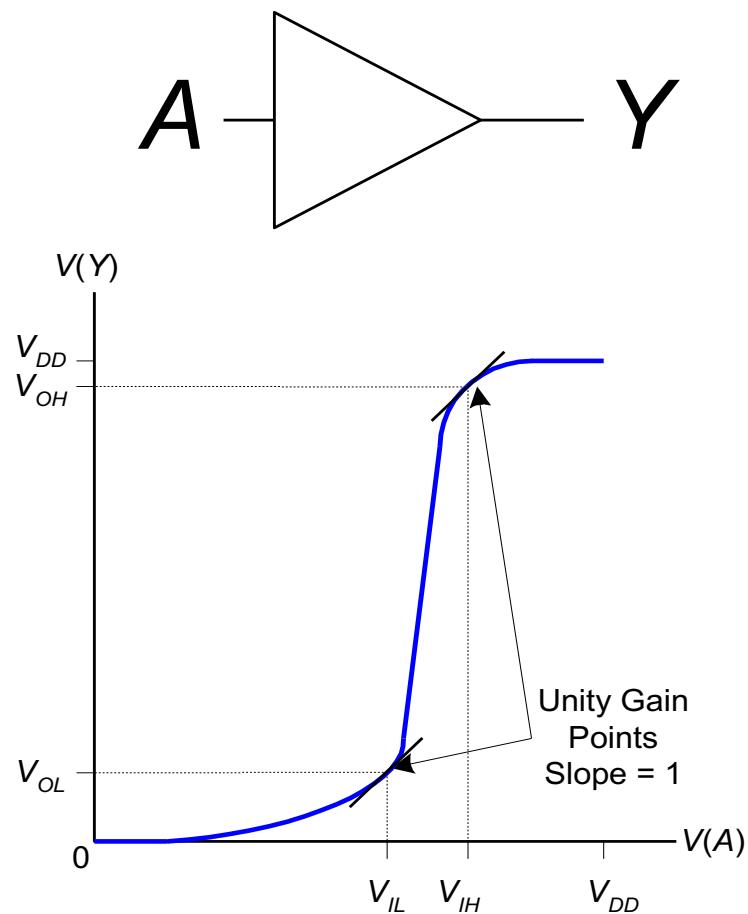
Real Buffer:



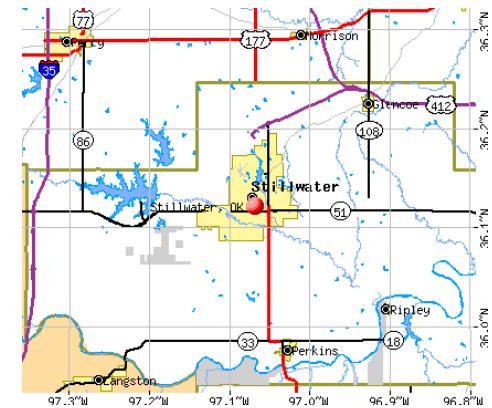
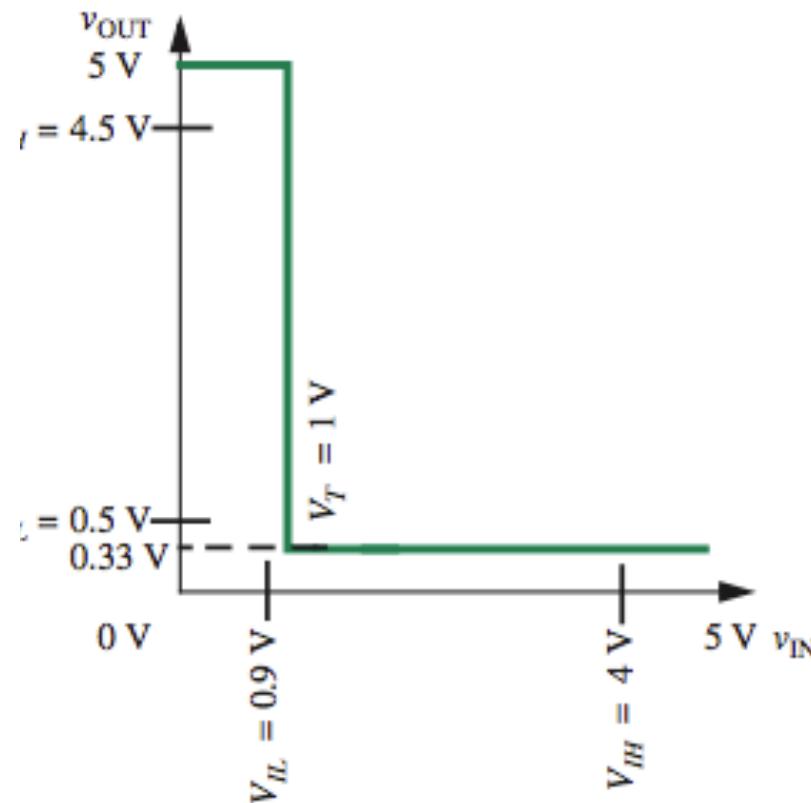
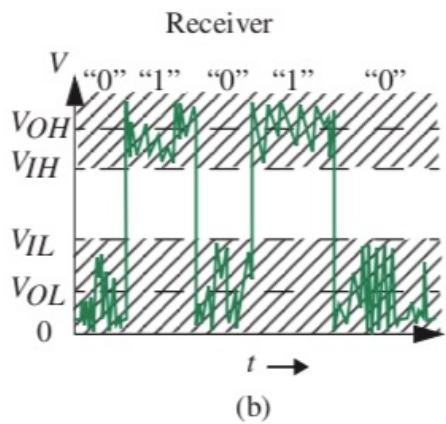
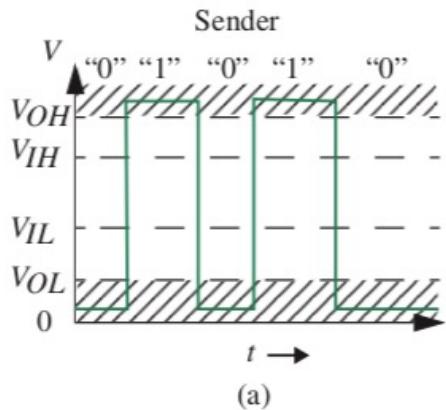
$$NM_H = NM_L = V_{DD}/2$$

$$NM_H, NM_L < V_{DD}/2$$

DC Transfer Characteristics



Non-traditional VTC



Mapping

Note: V_{IL} is below V_T

VDD Scaling

- In 1970's and 1980's, $V_{DD} = 5\text{ V}$
- V_{DD} has dropped
 - Avoid frying tiny transistors
 - Save power
- 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, 1.0 V, ...
- Be careful connecting chips with different supply Voltages



Logic Family Examples

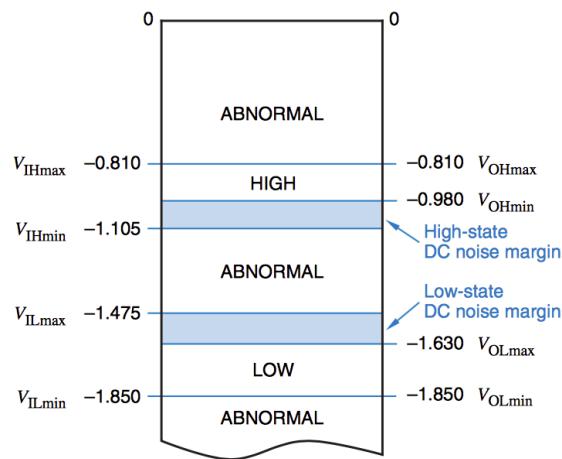
Logic Family	V_{DD}	V_{IL}	V_{IH}	V_{OL}	V_{OH}
TTL	5 (4.75 - 5.25)	0.8	2.0	0.4	2.4
CMOS	5 (4.5 - 6)	1.35	3.15	0.33	3.84
LVTTL	3.3 (3 - 3.6)	0.8	2.0	0.4	2.4
LVCMOS	3.3 (3 - 3.6)	0.9	1.8	0.36	2.7

[Harris]

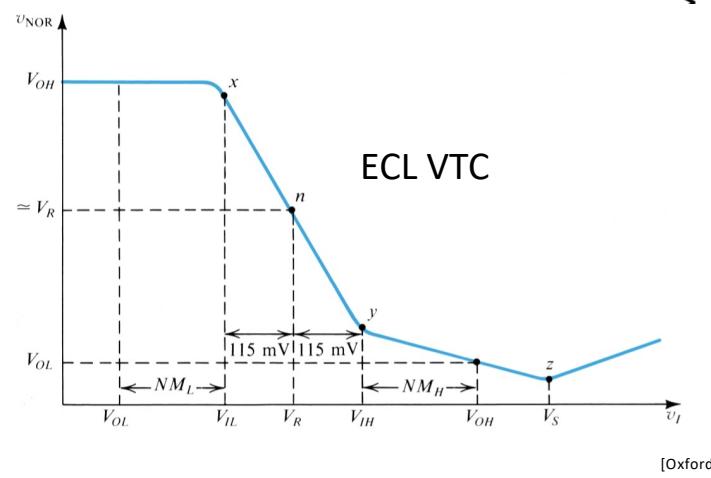
Emitter Coupled Logic



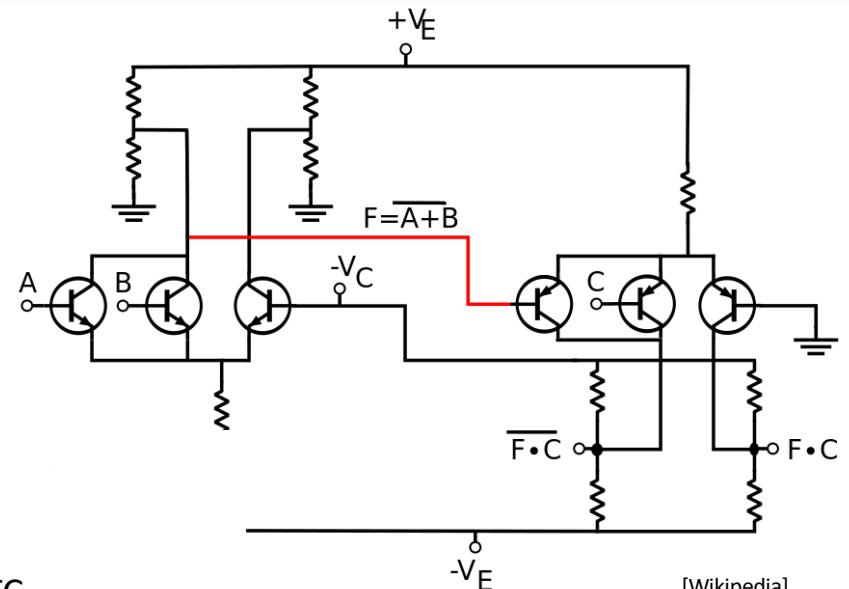
[Cray]



[Wakerly]



Early fast computers utilized current-steering or ECL or Emitter-Coupled Logic as it was extremely fast, but power hungry and hard to power up/control.



[Wikipedia]

What kind of VTC do we really want?



CMOS : pair of NMOS/PMOS



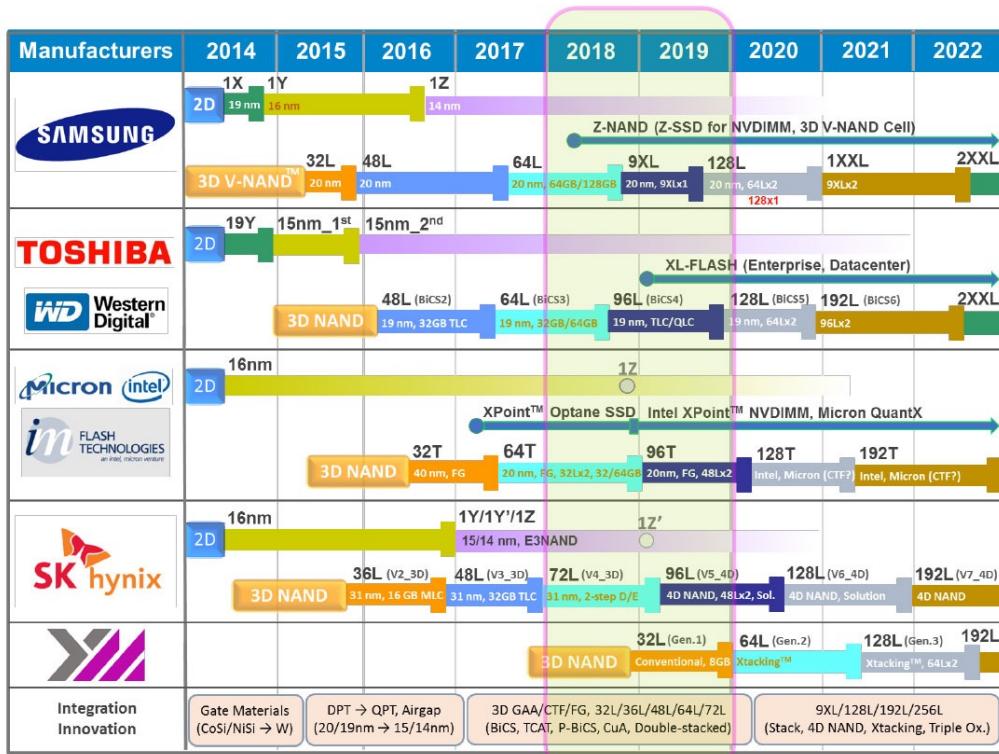
Now: After 45 Years from the 1st single MOSFETs



4 TB USB drive

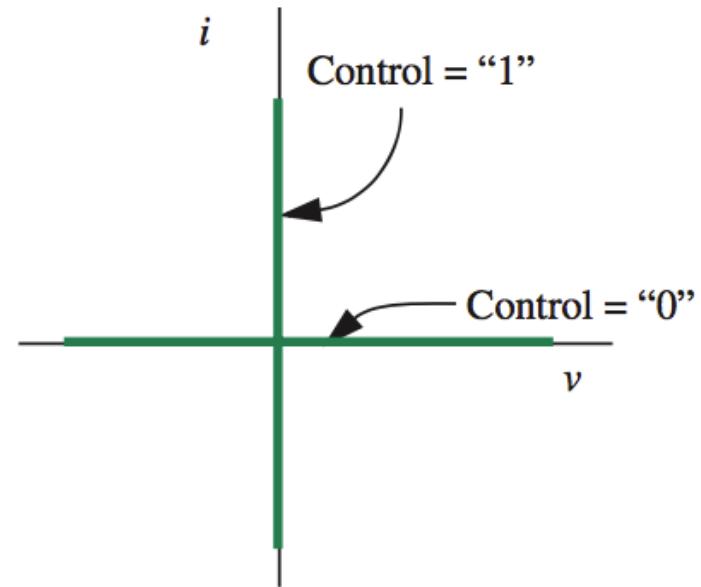
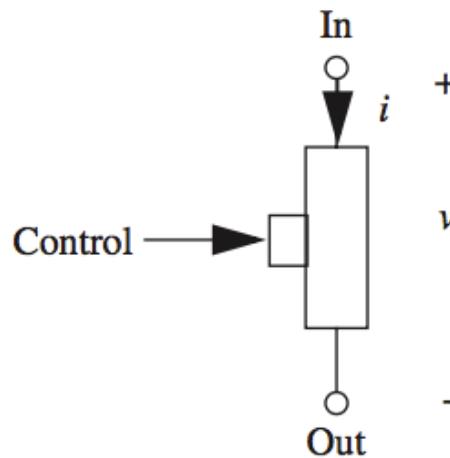


Flash Roadmap



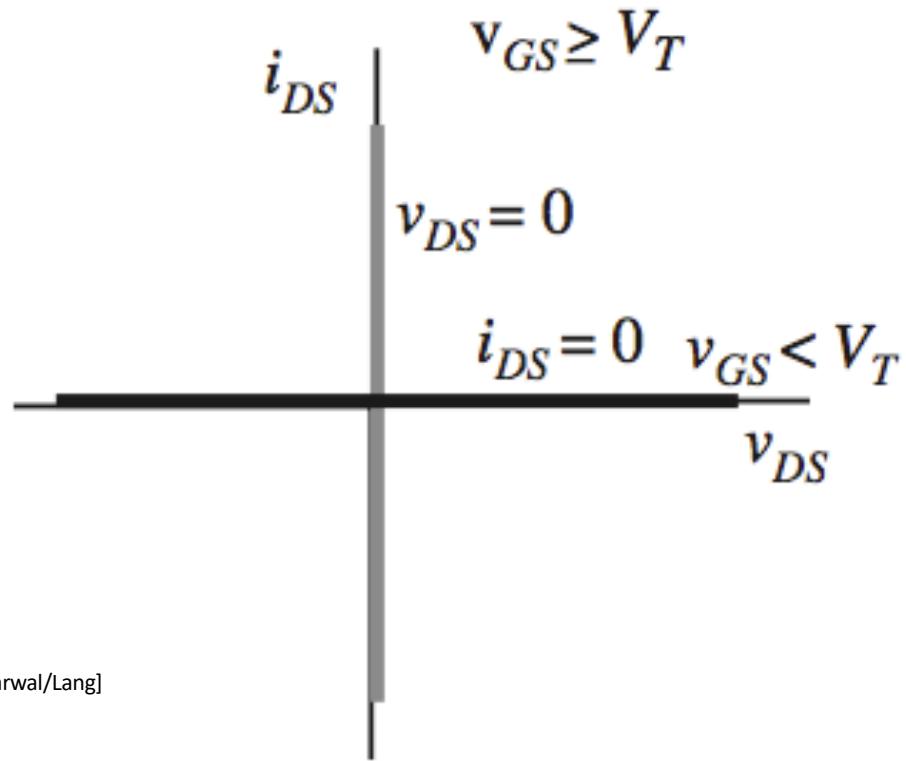
Building a switch

- The $v i$ characteristics of a switch can also be expressed in algebraic form as:
 - Control = 0, $i = 0$
 - Control = 1, $v = 0$

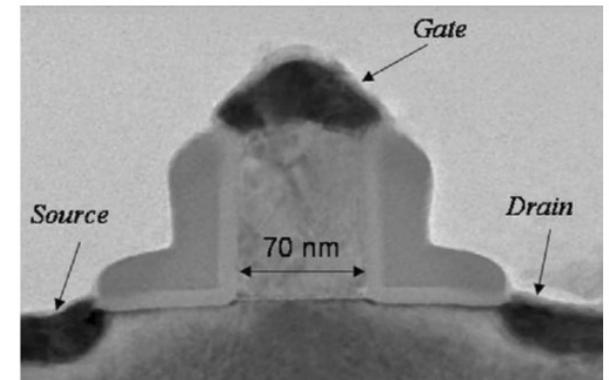


[Agarwal/Lang]

nMOS switch



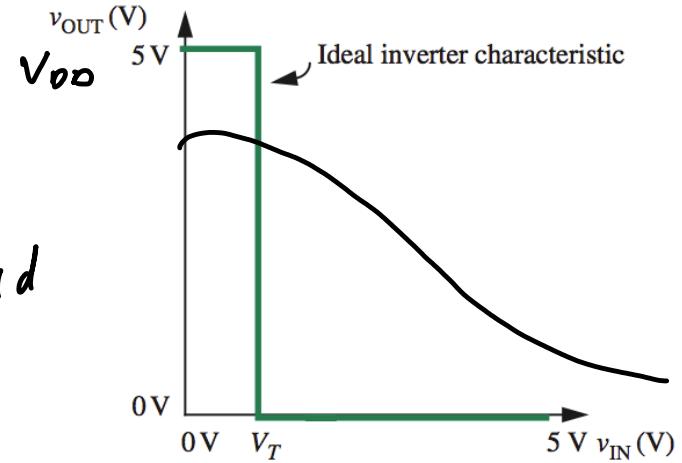
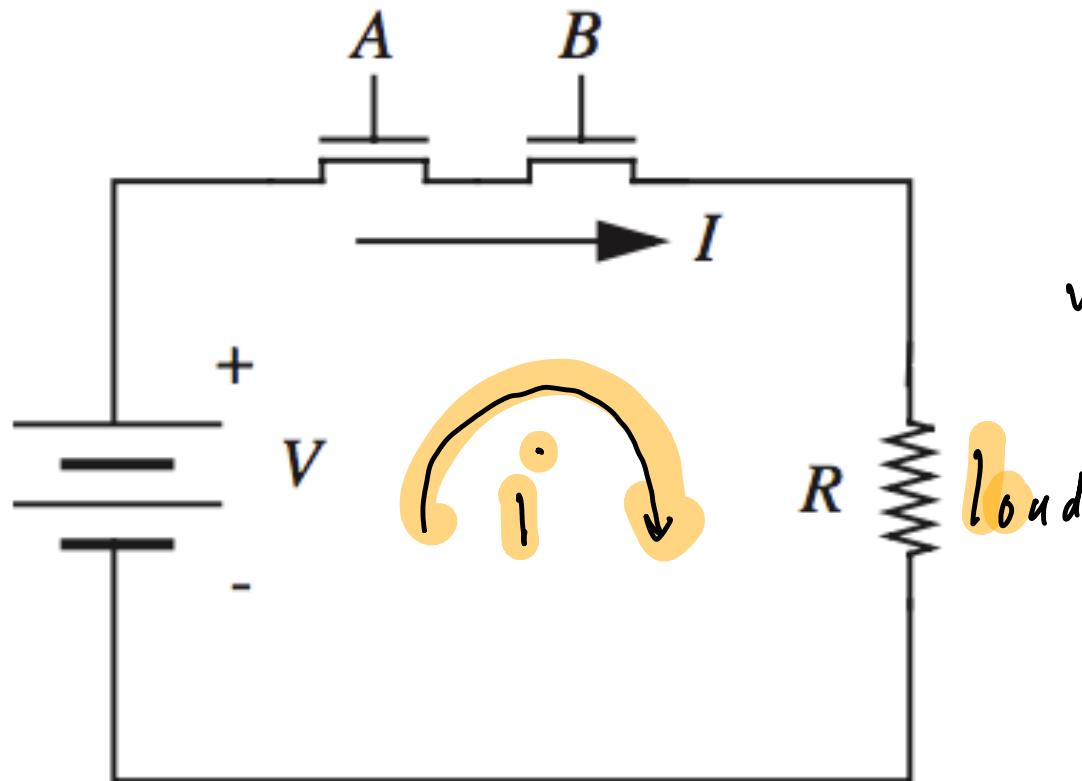
[Agarwal/Lang]



[Intel]

Cross-sectional TEM
(transmission electron
microscope) picture of Intel's
130nm logic transistor

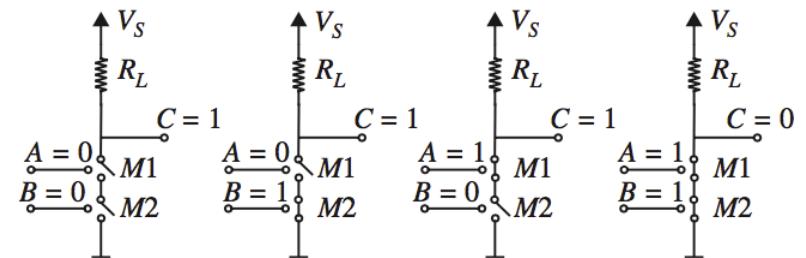
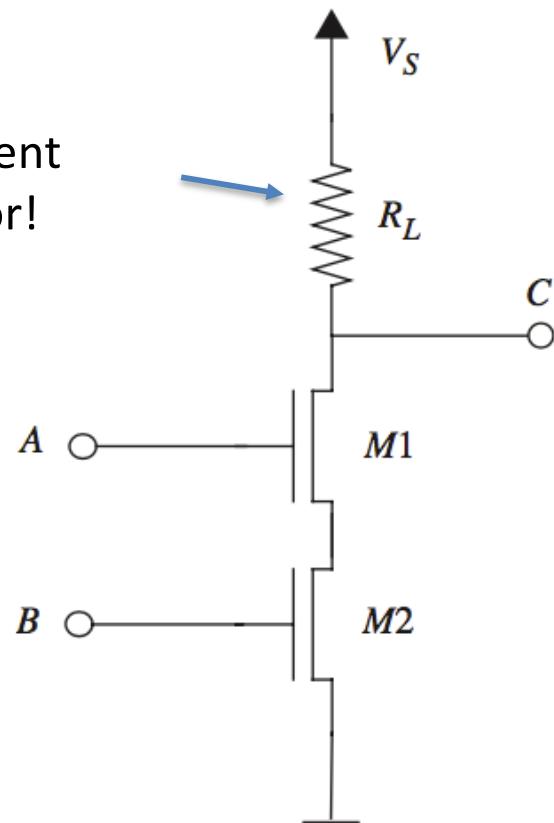
What's the easiest switch?



[Agarwal/Lang]

Adapt

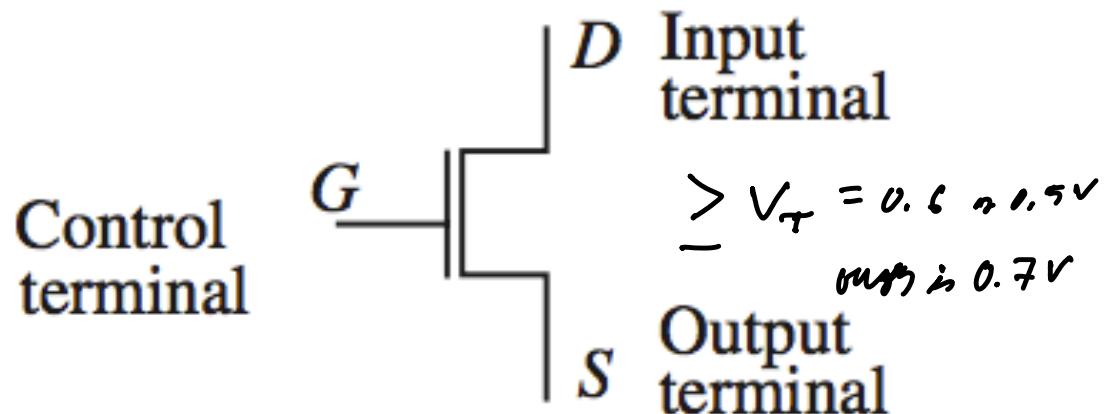
loading of current through resistor!



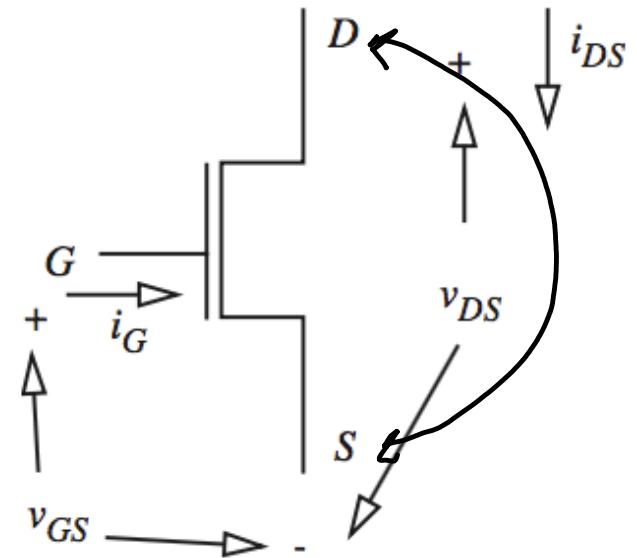
How would we make an OR gate?

[Agarwal/Lang]

nMOS

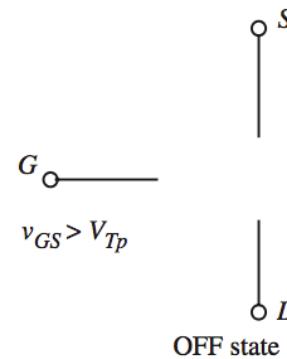
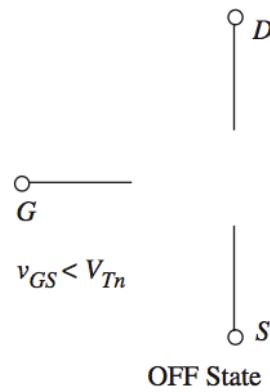
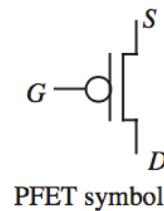
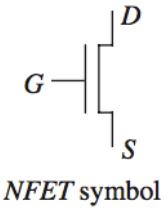


[Agarwal/Lang]

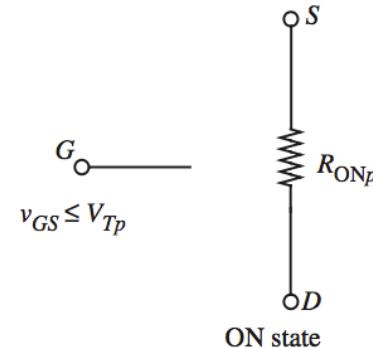
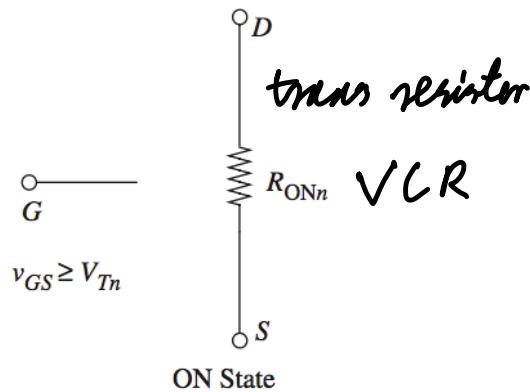


- Two ports are used to control the current and voltage.
- We utilize a switch model or S model to handle turning it on or off!
- The device is in the ON state when v_{GS} crosses a threshold voltage V_T , otherwise it is off.
- Our typical value for V_T for n-channel MOSFETs is 0.7 volts, but it can be varied by the manufacturing process.

nMOS/pMOS Pair



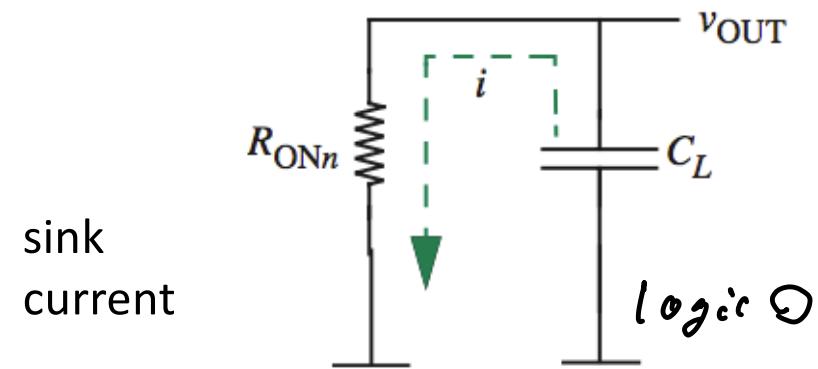
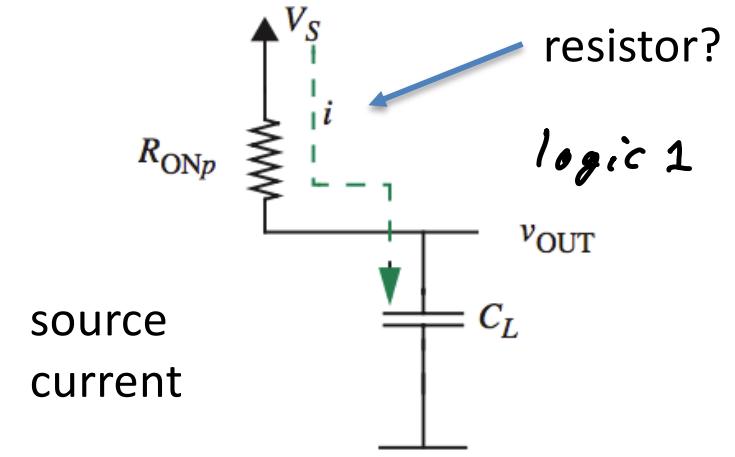
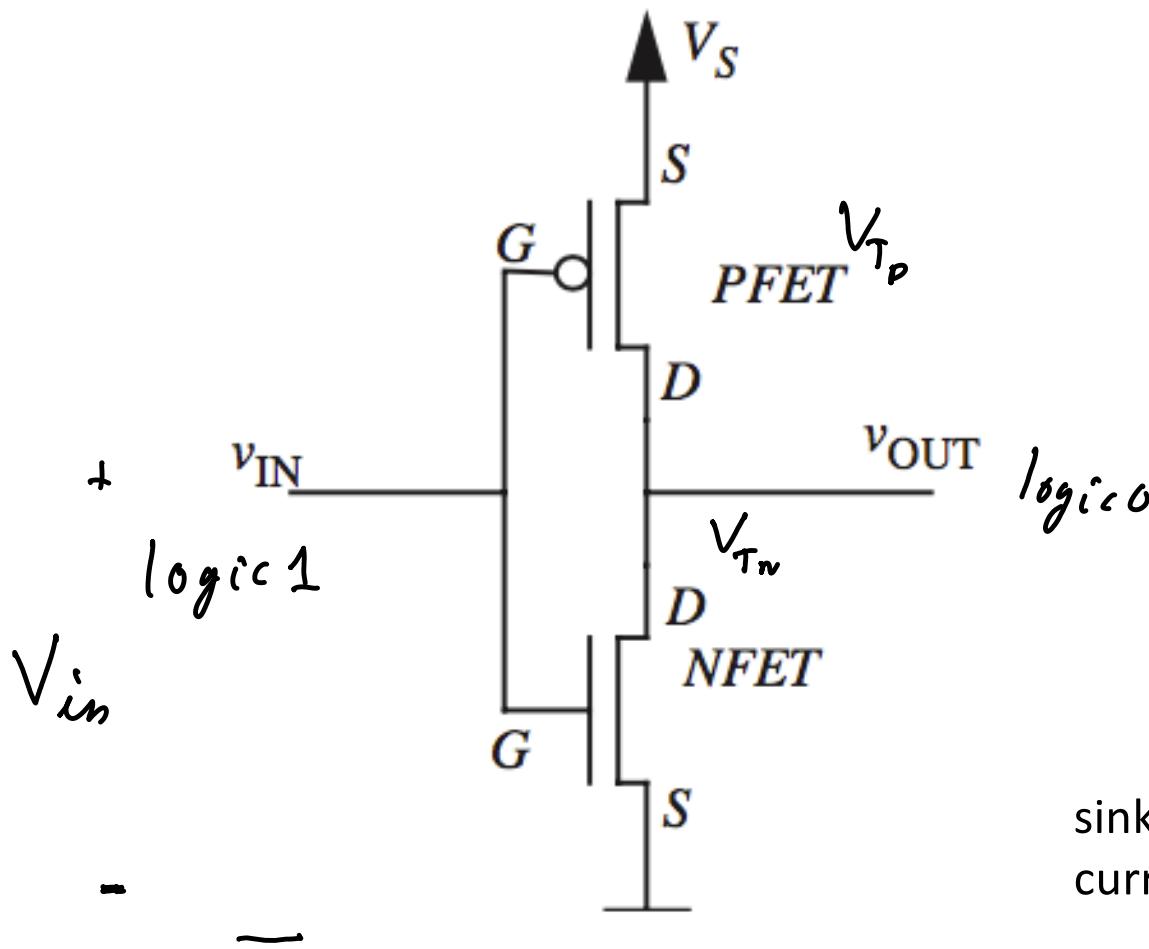
Use two elements to turn **on** portion **off** while it turns the other one on



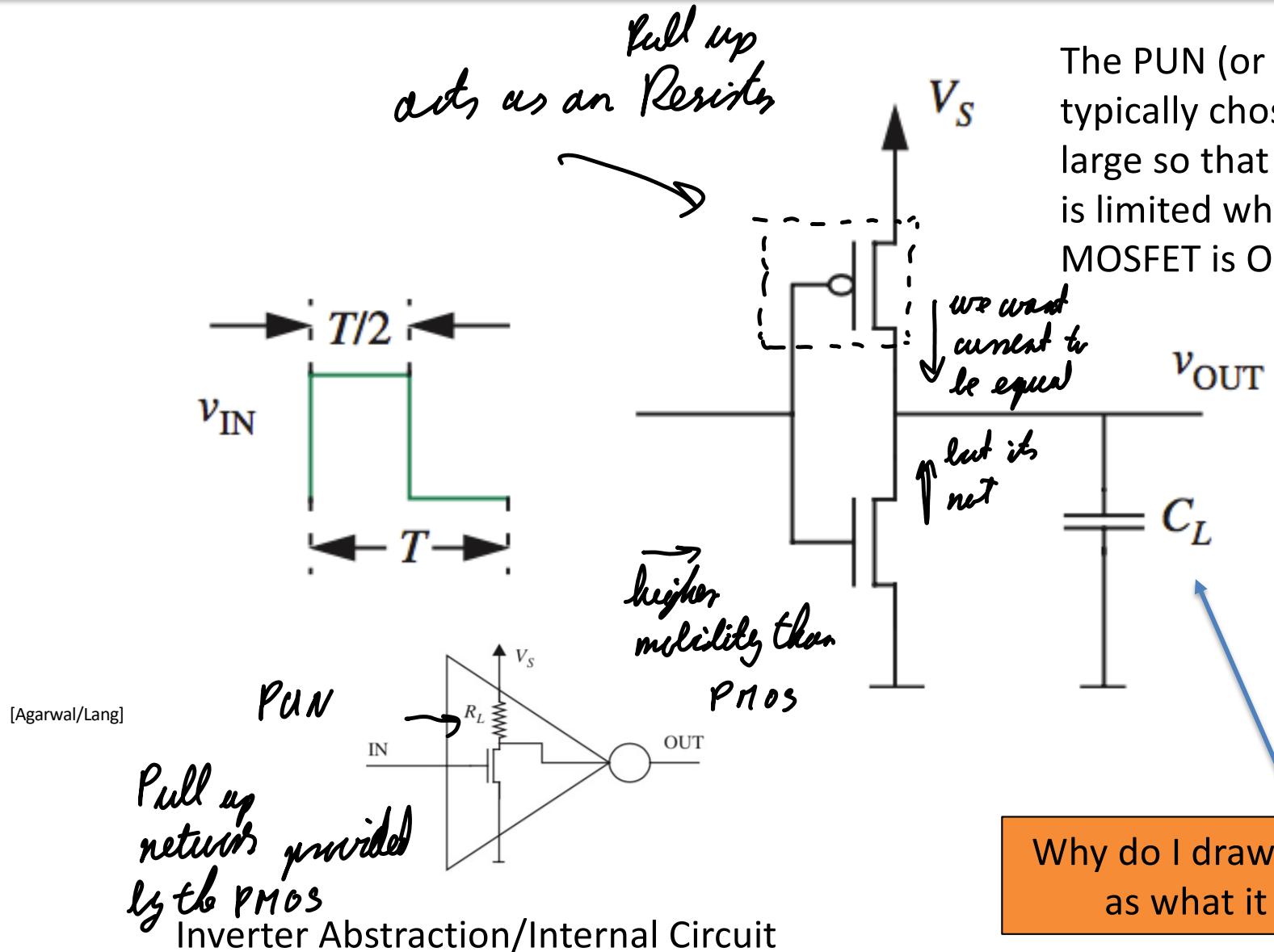
[Agarwal/Lang]

static

CMOS Inverter



CMOS Inverter



The PUN (or R_L) is typically chosen to be large so that the current is limited when the MOSFET is ON.

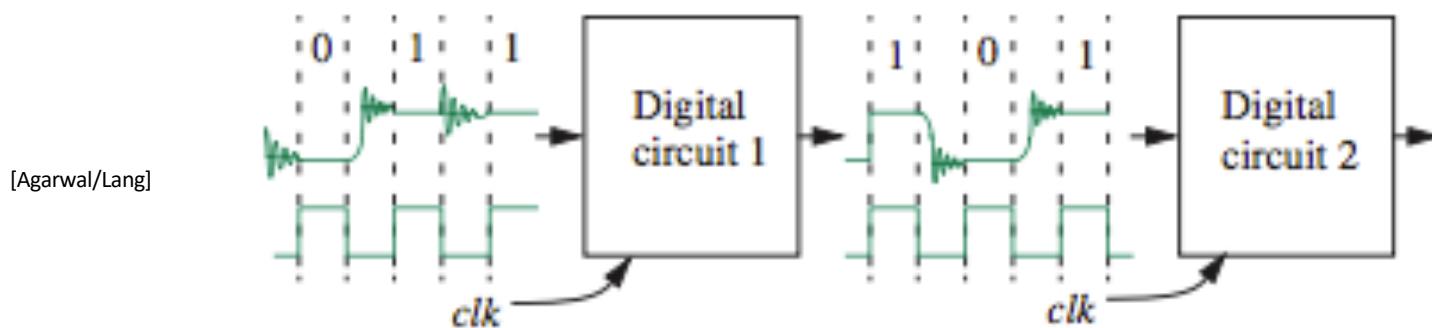
Why do I draw a capacitor as what it drives? 34

Nature of Output

- Although CMOS is great, it has a drawback in that it takes the output and inverts the input causing inversion.
- Also, these gates tend to output values based on its VDD and VSS/GND values, therefore, they are typically called **static** CMOS gates.
 - Output that is not constant given a non-changing input is called dynamic gates.
- These static complementary pairs always create inverting output.
 - All CMOS static gates are inverting!
 - NAND (not AND)
 - NOR (not NOR)
- How do I build a buffer? AND gate? OR gate?

Switching

- Because these digital gates are constantly switching and although they are static, they want them to exist for a specific amount of time.
- Therefore, designers use a clock to clock or latch values into a register to hold them for a definitive amount of time.
- Clocks are still used today to help hold values, so they can be used.
- Researchers and Professional users are experimenting with ways to hold these values by use of signals called semaphores (asynchronously).
 - This is still not common, because most software tools work with clocks

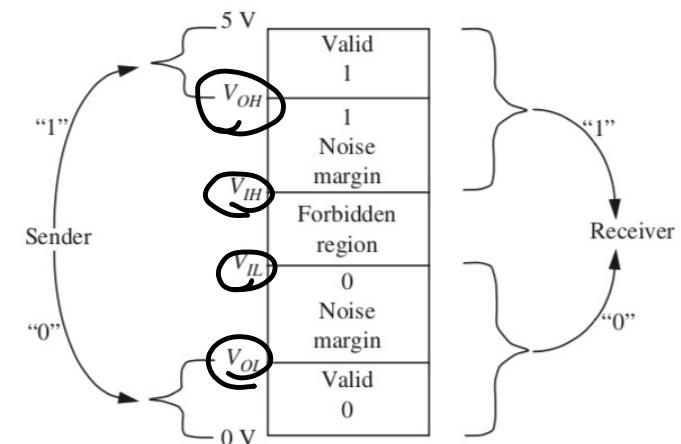
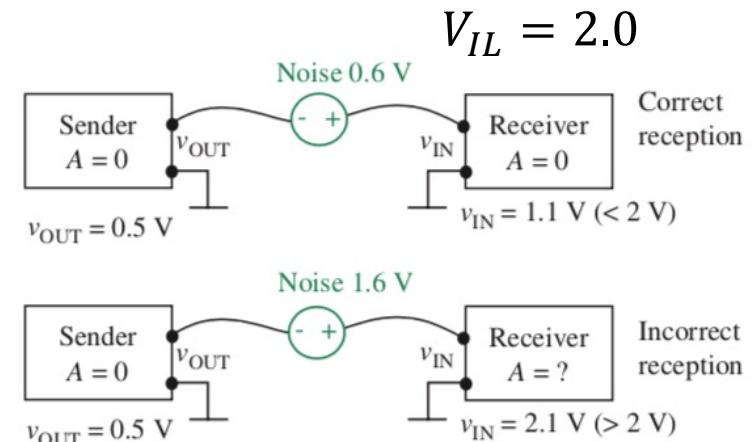


clocks are very important

Noise and Noise Margin

- To send a logical 0, the sender must produce an *output* voltage value that is less than V_{OL} . Correspondingly, the receiver must interpret *input* voltages below V_{IL} as a logical 0.
- Similarly, to send a logical 1, the sender must produce an *output* voltage value that is greater than V_{OH} . Further, the receiver must interpret voltages above V_{IH} as a logical 1.
- Noise Margin:** The absolute value of the difference between the prescribed output voltage for a given logical value and the corresponding forbidden region voltage threshold for the receiver is called the *noise margin* for that logical value.

Interesting Note: Many books just assume voltages are between VSS/VDD when in fact many are designed to handle voltage above and below this value!



[Agarwal/Lang]

**SN5404, SN54LS04, SN54S04,
SN7404, SN74LS04, SN74S04
HEX INVERTERS**

SDLS029C – DECEMBER 1983 – REVISED JANUARY 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I : '04, 'S04	5.5 V
'LS04	7 V
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN5404			SN7404			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-0.4			-0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	-55	125	0			70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

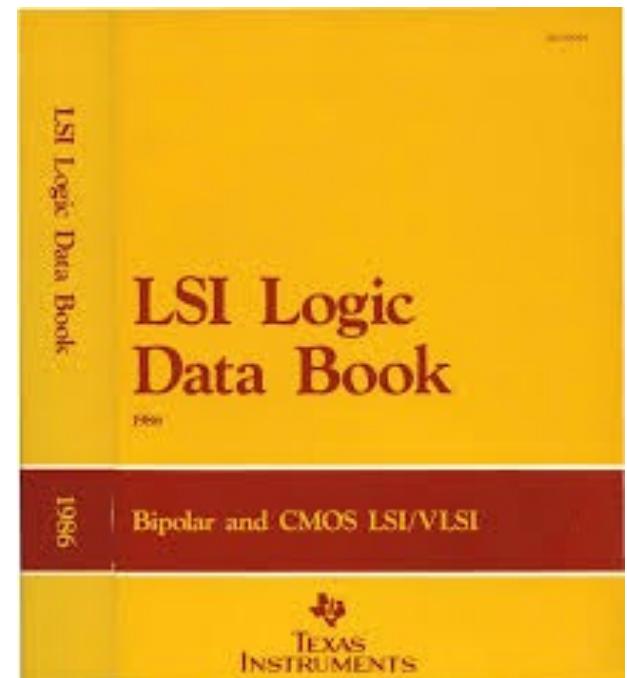
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	SN5404			SN7404			UNIT
		MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40	μA
I_{IL}	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS}¶$	$V_{CC} = \text{MAX}$	-20	-55	-18	-55		-55	mA
I_{CCH}	$V_{CC} = \text{MAX}$, $V_I = 0 \text{ V}$		6	12		6	12	mA
I_{CCL}	$V_{CC} = \text{MAX}$, $V_I = 4.5 \text{ V}$		18	33		18	33	mA

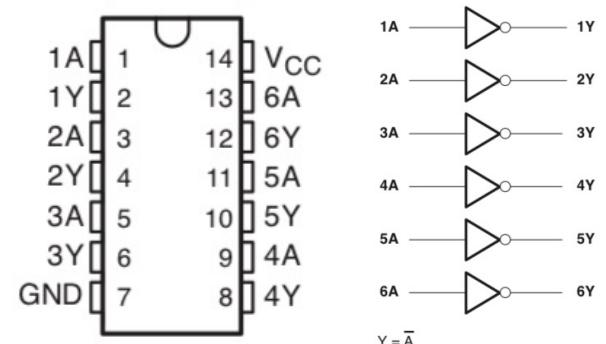
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

¶ Not more than one output should be shorted at a time.

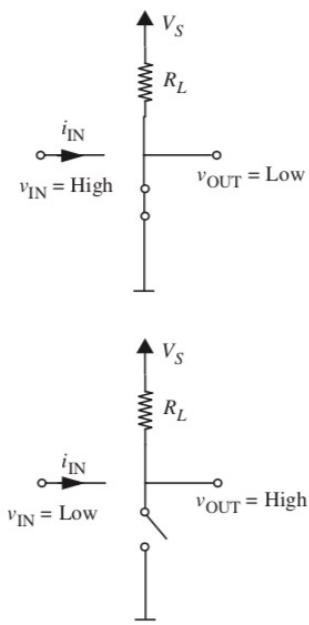


(TOP VIEW)



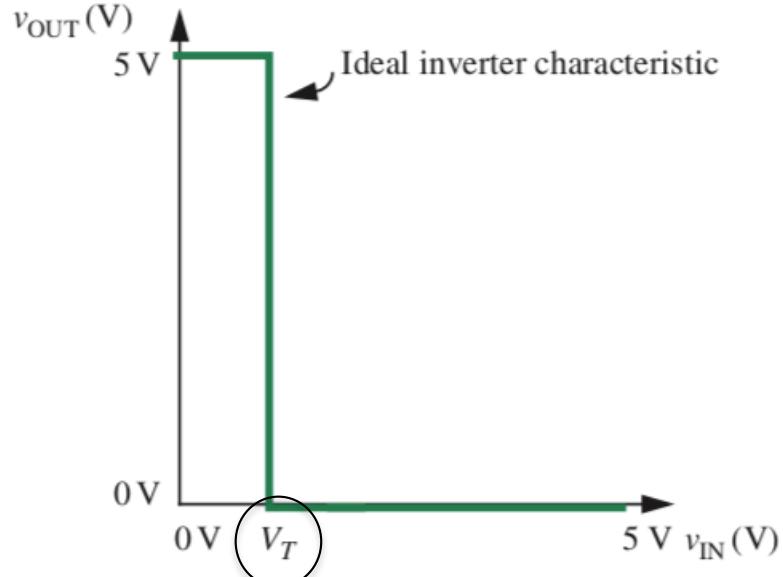
S(witch) model

- We can approximate the operation of the gate by assuming either ON or OFF.
 - nMOS devices are typically called OFF devices because they are typically OFF at 0 V
 - pMOS devices are typically called ON devices because they are typically at ON at 0 V



Truth Table

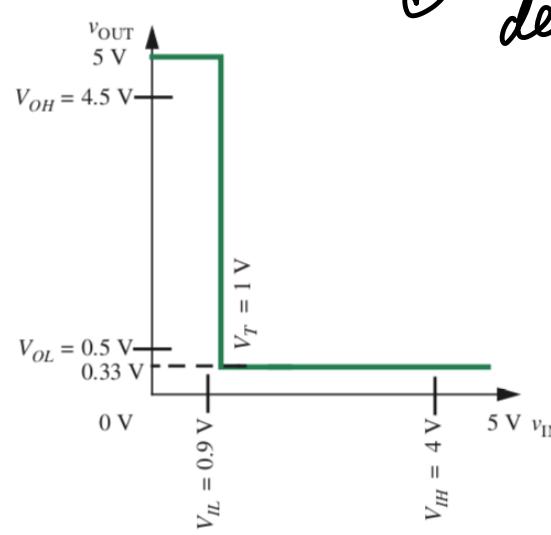
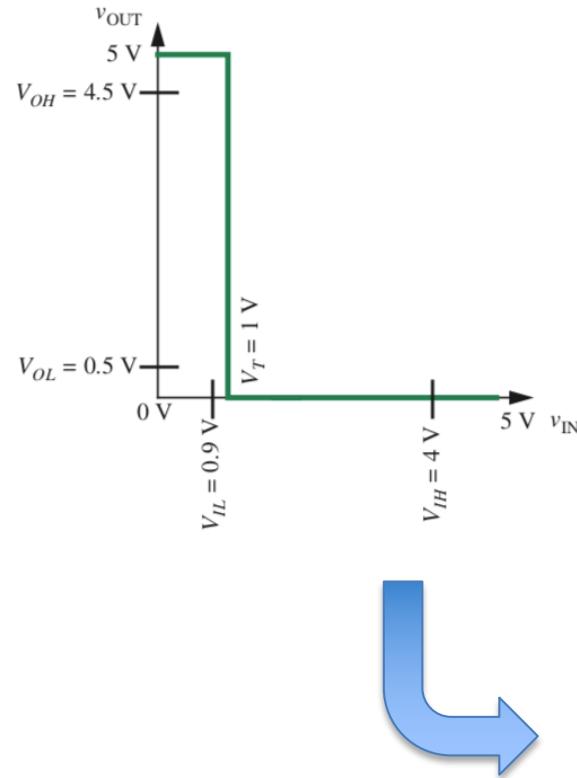
In	Out
0	1
1	0



[Agarwal/Lang]

Mapping ≠ Reality

- Our existence is that we think mapping, but in reality the circuit has side effects that have to be accounted for due to reality.

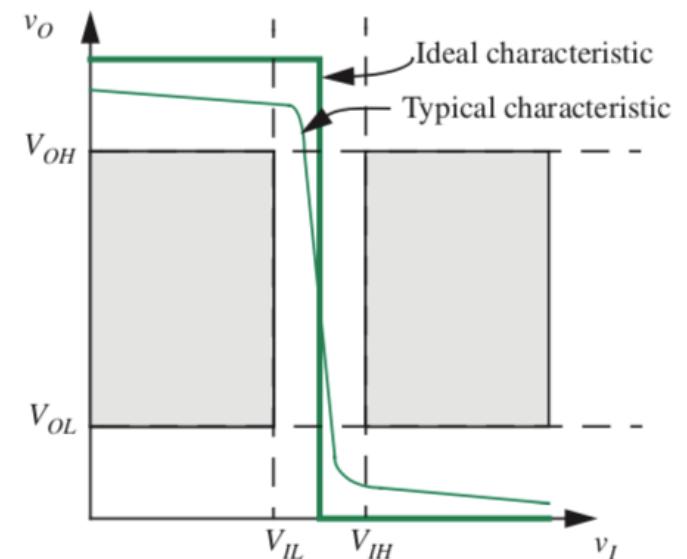
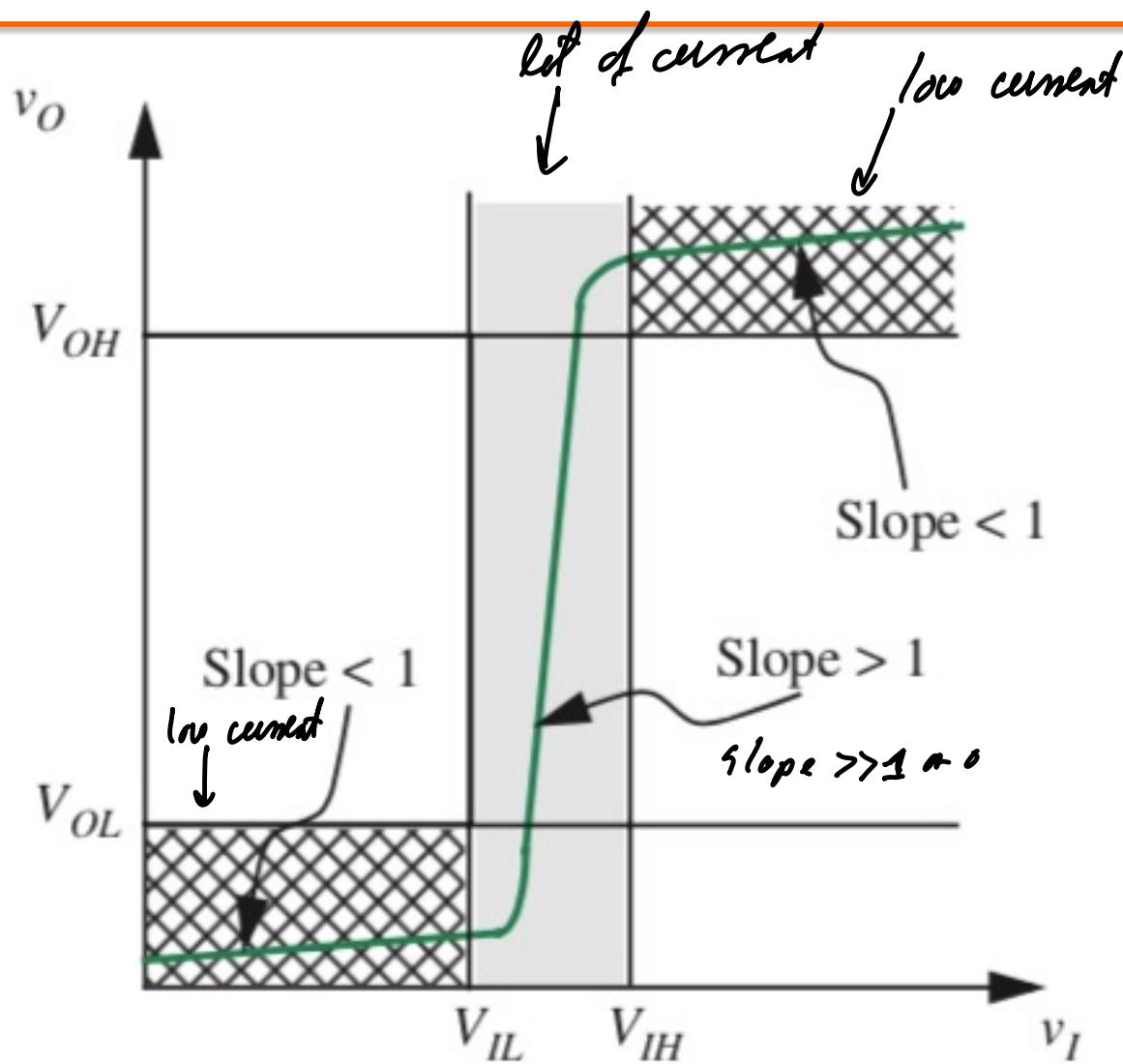


Let's not forget a MOSFET is an amplifier first and foremost!

Real kind of devices



Noise Margin $\rightarrow m=1$



$$\text{Power} = V_S \cdot I = \frac{V_S^2}{R_{pun} + R_{pdn}}$$

Summary

- We have learned the basis of what a digital circuit is.
- The Voltage Transfer Characteristic or VTC is essential to determine, based on every input and output, what the digital abstraction is.
- The Noise Margin (NM) defines how well this VTC works and large NMs are beneficial for digital circuitry.
 - Loading or putting output loads on a digital circuit affects the transistor by putting excessive capacitance on its output.
 - This extra capacitance (due to Silicon Dioxide) ultimately leads to slower circuitry.
 - Designers will spend lots of time to understand the best possible loading that is needed for their circuit to optimize their application.