# AS-3 Timing Circuits

Revision sheet

## 1 Capacitors

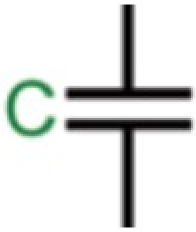


Figure 1: Circuit symbol for a capacitor

Capacitors store charge. The equation
$Q = CV$
can be used to calculate how much charge is stored in the capacitor. The unit of capacitance (C) is the Farad (F). Usually a capacitor will be in the region of micro/ nano/ pico farads.

### 1.1 Series And Parallel

The total capacitance of capacitors in series can be calculated using the following formula:
$\frac{1}{C_{total}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + ...$
The total capacitance of capacitors in parallel can be calculated using the following formula:
$C_{total} = C_1 + C_2 + C_3 + ...$

### 1.2 Time Constant

When a resistor and capacitor are connected in series, they form a RC network. The equation $T = R \times C$ links them together, where T is the time constant and is measured in seconds.

### 1.3 Charging A Capacitor

The circuit below can be used to charge a capacitor.

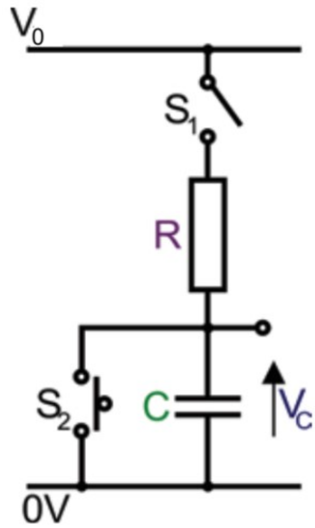


Figure 2: Circuit for charging a capacitor

We'll assume that the capacitor is initially fully discharged, therefore $V_C = 0$. When we close the switch, capacitor starts charging and current 'flows'. As the capacitor charges, the rate of charging slows down. A larger resistor will cause slower charging, therefore with 0 resistance, the capacitor would charge 'instantly'. In the diagram above, the purpose of $S_2$ is to discharge the capacitor so that the experiment can be repeated.

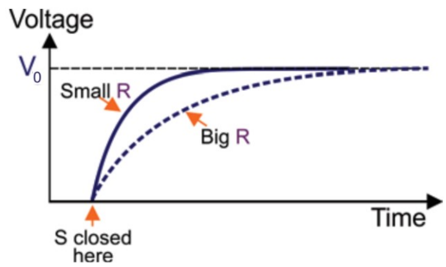


Figure 3: Graph showing voltage change over time when charging a capacitor

The equation to find the voltage over the capacitor ($V_C$) at a given time ($t$) is given below.
$V_C = V_0\left(1 - e^{-\frac{t}{RC}}\right)$
The time taken to get a certain voltage over the

capacitor equation (for charging) can be seen below.
$t = -RC \ln \left(1 - \frac{V_C}{V_0}\right)$

#### 1.3.1 General Rules

$V_C = 0.5V_0$ after $0.69RC$ ($V_C$ = half the supply voltage)
$V_C \approx V_0$ (fully charged) after $5RC$.

### 1.4 Discharging Capacitors

The circuit below can be used to discharge a capacitor.

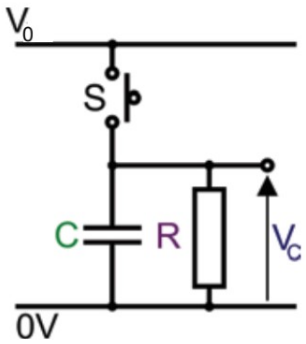


Figure 4: Circuit for discharging a capacitor

Pressing switch $S$ instantly charges the capacitor. Discharging begins when S is released. C discharges through R.

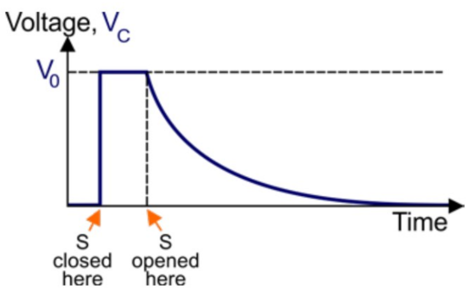


Figure 5: Graph showing voltage change over time when discharging a capacitor

The equation to find the voltage over the capacitor ($V_C$) at a given time ($t$) is given below.
$V_C = V_0 e^{-\frac{t}{RC}}$
The time taken to get a certain voltage over the capacitor equation (for discharging) can be seen below.
$t = -RC \ln \left(\frac{V_C}{V_0}\right)$

#### 1.4.1 General Rules

$V_C = 0.5V_0$ after $0.69RC$
$V_C \approx 0V$ after $5RC$ (fully discharged)

## 2 Monostable Circuits

A monostable is a circuit which produces a single timing pulse. It has only one stable state; which it stays in until triggered, then it moves to the unstable state for a set period of time then returns to the stable state.

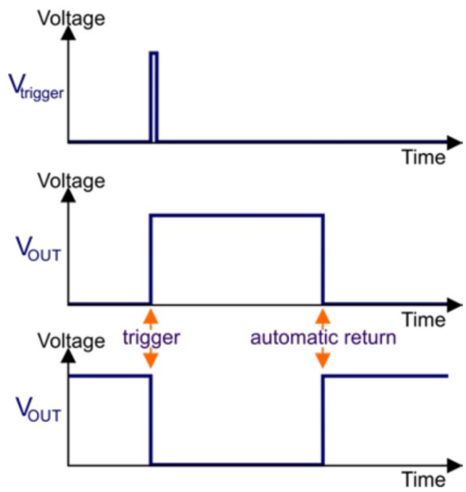


Figure 6: Monostable circuit behaviour

### 2.1 NOT Gate Monostable

NOT gates have something called a switching threshold - this is the point at which they will invert their input. This can be used to design a NOT gate monostable.

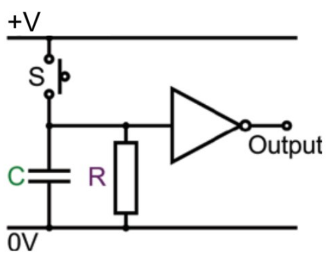


Figure 7: Circuit for a NOT gate monostable

The output of the monostable can be shown on a graph.

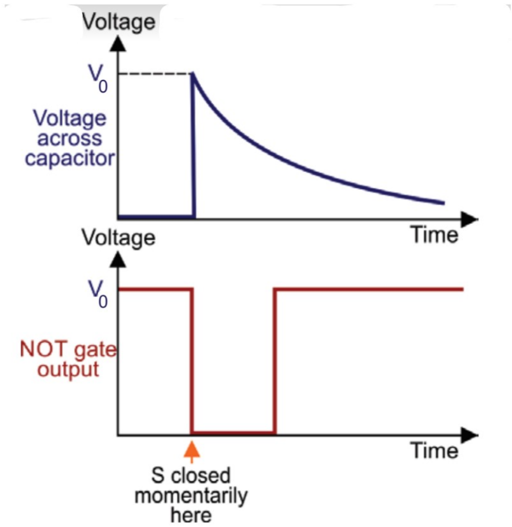


Figure 8: Graph showing the NOT gate monostable

### 2.1.1 Delayed Response Monostable

The resistor can be moved and another switch added which gives a circuit that produces a delay before triggering the monostable.

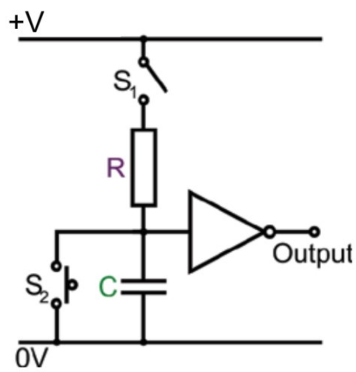


Figure 9: Circuit for a delayed NOT monostable

This gives us the following graphed output.

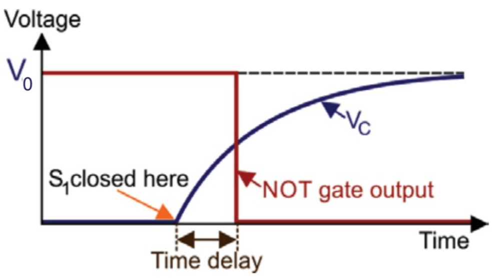


Figure 10: Graph showing the delayed NOT gate monostable

## 2.2 555 Timer Monostable

The 555 Timer IC can be used to build a monostable as seen below.

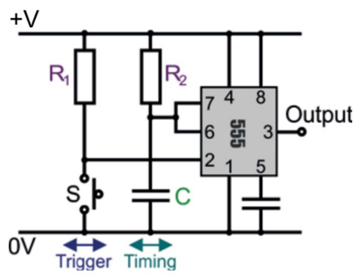


Figure 11: Circuit for a 555 timer monostable

$T = 1.1RC$ where resistor used is $R_2$.
Once the button is pressed, the monostable triggers and behaves as expected. You cannot retrigger the 555 monostable mid pulse by pressing the button down again. The output will stay high all the time the button is pressed, even if T is over.

## 2.3 Uses Of Monostables

Monostables can be used to de-bounce a switch.

# 3 Astable Circuits

These have no stable states. They oscillate between on and off. The time on ($T_H$) is called a Mark and the time off ($T_L$) is called a space. The time period can be calculated as follows:
$T = T_L + T_H$. The time on and time off do not have to be equal. The following graph shows this.

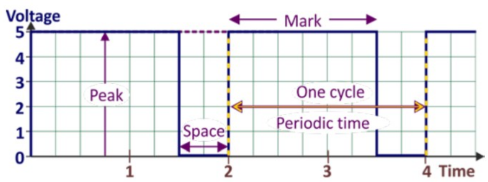


Figure 12: Graph showing the behaviour of an astable

The output is a square wave. The frequency can be calculated using the equation seen below.
$f = \dfrac{1}{t} = \dfrac{1}{T_H + T_L}$

## 3.1 Schmitt Inverter Astable

A Schmitt Inverter can be used to build an astable. It has upper and lower switching thresholds which makes it really useful for this. It's upper threshold is $\frac{2}{3}V_S$ and its lower threshold is

$\frac{1}{3}V_S$. The Schmitt Inverter Astable has the following circuit diagram.

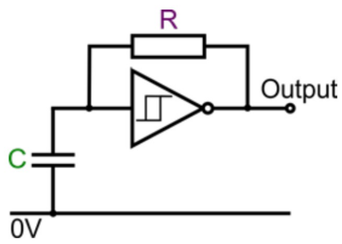


Figure 13: Circuit for a Schmitt inverter astable

This produces the following output graph.

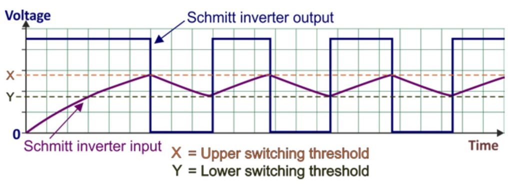


Figure 14: Graph showing the inputs, output and switching thresholds of a Schmitt inverter astable

The Mark:Space ratio will always be 1:1 and the equation for frequency is as follows.

$f = \dfrac{1}{RC}$

## 3.2 555 Timer Astable

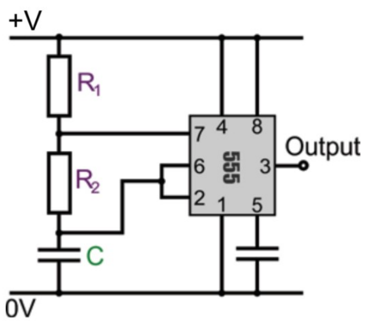


Figure 15: Circuit for a 555 timer astable

The capacitor charges through $R_1$ and $R_2$, providing the time on

$T_H = 0.7(R_1 + R_2)C$

The capacitor discharges through $R_2$, providing the time off

$T_L = 0.7R_2C$

The frequency can be calculated with the following equation

$f = \dfrac{1.44}{(R_1 + 2R_2)C}$

The Mark-Space ratio can be calculated using one of the following equations, to one.

$\dfrac{T_H}{T_L} = \dfrac{R_1 + R_2}{R_2} = \dfrac{T_{on}}{T_{off}} : 1$

It is impossible to have a Mark-Space ratio of 1:1, however if $R_2 >> R_1$, $\dfrac{T_H}{T_L}$ can be closer to 1.