Radio Frequency Circuits & Antenna

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Homework: 9

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1 The following small signal model describes a CMOS amplifier:

i. Find f_t and f_{max} of the transistor at the given operating point, assuming that C_{gs}=15[fF], C_{gd}=5[fF], R_g=5W, the overdrive voltage $(V_{GS} - V_{TH})$ is 0.2V, the current I_D at the operating point is given by: $I_D = k(V_{GS} - V_{TH})^2$ with k=0.05$[mA/V^2]$, the voltage supply is $V_{DD} = 0.9V$ and the IV curve of the transistor is given by the following figure:

The transistor is saturated: $V_{ds} > V_{od}$:

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})}, \quad g_m = \frac{2I_d}{V_{od}} = \frac{2(0.54 \cdot 10^{-3})}{0.2} = 5.4[m\Omega^{-1}] \tag{1}$$

$$f_t = \frac{5.4[m\Omega^{-1}]}{2\pi(20[fF])} = 43[GHz] \tag{2}$$

$$f_{max} = \frac{f_t}{\sqrt{2\pi f_t C_{gd} R_g + R_g/r_o}} \tag{3}$$

Solving for r_o, using linear equation relations:

$$\frac{x - 0.8}{0.8 - 1} = \frac{y - 0.52}{0.52 - 0.55} \tag{4}$$

$$y = \frac{3}{20}(x - 0.8) + 0.52 \tag{5}$$

$$0 = \frac{3}{20}(x - 0.8) + 0.52 \tag{6}$$

$$-0.52 \cdot 20/3 = x - 0.8 \tag{7}$$

$$-0.52 \cdot 20/3 + 0.8 = x \tag{8}$$

$$\therefore V_a = -2.667[V] \tag{9}$$

$$r_o = \frac{|V_a|}{I_d} = \frac{2.66}{0.52} = 5.13[k\Omega] \tag{10}$$

$$\therefore f_{max} = \frac{43 \cdot 10^9}{\sqrt{2\pi \cdot 43 \cdot 10^9 \cdot 5 \cdot 10^{-15} \cdot 5 + 5/5130}} = 489.1[GHz] \tag{11}$$

ii. Repeat Section i above, assuming now that C_{gd} can be neglected. What is the error (in percentages) between the exact calculation and the approximated one?

$$f_t = 57.3 \rightarrow \delta = 33.25\% \tag{12}$$

$$f_{max} = 342.57 \rightarrow \delta = 42.77\% \tag{13}$$

iii. Repeat Section i above, assuming now that the width of the transistor (W) has twice the size than it had in Section i. In your calculations specify what parameters are affected by this change, and why.

I_D will double as it has a direct proportional relation to it, but f_t will remain the same as: $C_{gs} = 2/3C_{ox} \cdot W/L$, and $C_{gd} = 1/3C_{ox} \cdot W/L$. We can then induce that f_t will be the same value, and f_{max}, will decay by a factor close to $1/\sqrt{2}$.

iv. Repeat Section i above, assuming now that the number of fingers of the transistor (N) has twice the size than it had in Section i. In your calculations specify what parameters are affected by this change, and why.

Similar to the previous question we get the same relations as before but now for a factor of N, which implies that f_t won't change, and f_{max}, reduces by $1/\sqrt{N}$.

2 For the small signal model of the transistor that is given in Question 1 Section i above, design an octagonal inductor that will match the output of the transistor to 50Ω at 10GHz, assuming that the inductor is implemented by a top metal layer made of copper (conductivity of $\sigma = 5.96 \cdot 10^7[S/m]$) with a cross section of 2mm x 2mm, surrounded by Silicon Dioxide with $\varepsilon_r = 4.1$. The inductor should include 2 windings (turns) with a spacing of 1mm between them. Follow the steps below:

i. Find the required inductance for the matching.

$$Z_{in} = \Big((R_l + jX_l)||\frac{1}{j\omega C_l} + j\omega L\Big)||\frac{1}{j\omega C_s} \tag{14}$$

Then for matching we get:

$$L = 5.39[nH], \quad C = 32[fF] \tag{15}$$

ii. What is the approximated area of the inductor?

Approximated area $= d_{out}^2$, then we can elaborated as follows:

$$L = \frac{K_1\mu \cdot n^2 d_{avg}}{1 + K_2\rho} \tag{16}$$

$$d_{avg} = \frac{d_{out} + d_{in}}{2}, \quad \rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \tag{17}$$

$$d_{in} = d_{out} - 0.01[\mu m] \tag{18}$$

We can then see that the solution for $d_{out} = 0.517[\mu m] \quad \therefore \quad A \approxeq 0.267[\mu m^2]$

iii. What is the Q factor of the inductor?

Let us assume a to be the outwards side of the octagon and b to the inner side of the octagon, then:

$$d_{out} = a(1+\sqrt{2}), \quad d_{in} = b(1+\sqrt{b}) \tag{19}$$
$$a = 214.15[\mu m], \quad b = 210[\mu m] \tag{20}$$

$$l = 8(a+b) = 3393.22[\mu m] \tag{21}$$
$$\delta = \sqrt{\frac{2}{\sigma\mu\omega}} = 0.65[\mu m] \tag{22}$$
$$A_{skin} = 4 - 0.49 = 3.51[@mm^2] \tag{23}$$
$$R = \frac{l}{\rho A_{skin}} = 16.21[\Omega] \tag{24}$$
$$Q = \frac{2\pi f L}{R} = 19 \tag{25}$$

iv. Estimate is the SRF of the inductor, assuming that only the parasitic capacitance between the windings affects the SRF.

Assuming cylindrical form for the capacitor:

$$C = \frac{2\pi\varepsilon_r\varepsilon_0 L}{\ln[d_{out}/d_{in}]} = [26fF] \tag{26}$$
$$SRF = \frac{1}{2\pi\sqrt{LC}} = 14[GHz] \tag{27}$$

3 What will be the insertion loss of a mixer based on a switch if the LO signal will be a rectangular waveform with a duty cycle of 33%? (meaning, the pulse width is T and the total time period is 3T).

We know that the F.T. of a rectangular pulse with 1/3 duty cylce is given by:

$$\mathcal{F}(\omega) = \sum_{n=\infty}^{\infty} \frac{4}{n} \sin\left(\frac{n\pi}{3}\right) \delta\left(\omega - \frac{2\pi n}{3T}\right) \tag{28}$$

Then using coeff with value 1 we get the insertion loss as follows:

$$IL = 20\log\left(4\sin\left(\frac{\pi}{3}\right)\right) = 10.79[dB] \tag{29}$$

4 An RF switch is implemented by the resistor that is presented in figure 1 (biased with an overdrive voltage of 0.2V).

i. Find the R_{on} of a switch.

Through graphical analysis we know that and knowing that R_{on} is given by 1/slope relation:

$$R_{on} = 700[\Omega] \tag{30}$$

ii. What can be done in order to lower this resistance to 10Ω or below?

As R_{on} has a a inverse relation to V_{od} we could increase it's value until such condition is satisfied. Something else, which is bounded by chip design technology and architecture would be to increase W, but we normally would avoid it for consuming space and deteriorating other parameters.

iii. What will be the insertion loss of the switch if Ron will be 10Ω?

If we ignore the parasitic capacitance:

$$\underline{\underline{R}} = \begin{bmatrix} 1 & 10 \\ 0 & 1 \end{bmatrix} \tag{31}$$

$$S_{21} = \frac{2}{A + B/Z_0 + C \cdot Z_0 + D} = \frac{10}{11} \tag{32}$$