Mixed Analog-Digital VLSI Final Project Report

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1 Introduction

For the MADVLSI (Mixed Analog-Digital VLSI) Spring 2021 Final Project, we set out to build a temperature sensor packed with switched capacitors and a $\Sigma\Delta$ Modulator. Not knowing what we got ourselves into, we spent countless hours trying to address various technical and PDK challenges when trying to implement everything including large arrays of switched capacitor based circuits. Realizing the challenges for first-timers like us, we scaled our project back to a temperature sensor built with a switched capacitor bandgap reference and a dual slope Analog to Digital Converter. Here in this report, we present our schematic design and layouts for this dual slope ADC-based temperature sensor.

2 Circuit Design

2.1 Self-Biased Two-stage Cascode Op-Amp

We started the project using the folded-casecode op-amp design we developed in Mini-project 3. However, the design suffers from a ceiling on the allowable common mode voltage as we analyzed in the mini project three reports. Once the common mode voltage exceed 1.0 V, the bias transistor in the PMOS differential pair of the aforementioned design would come out of saturation and can no longer act as current source. This is a problem widely faced by many members of the class. To address this issue, Prof. Minch has developed the self-biased two-stage cascode op-amp shown in Figure 2. The op-amp is consisted of several segments. The leftmost part of the capacitor is both a NMOS and a PMOS differential pairs. It allows the op-amp to accept nearly rail-to-rail input. To the right of it was the op-amp output of the familiar folded-cascode form, with the current mirrors built with the low-voltage Wilson current mirror instead of diode connected current mirrors. At the output stage is the addition of an wide yet minimal length inverter with a Miller capacitor between the gate and common source of the inverter. In the leftmost segment, we have one NMOS differential pair and one PMOS differential pair. To the right of the differential pairs, the output segment and the common source of the transistors to quench instability during feedback.

This op-amp design is used in the integrator and temperature independent bandgap reference.

2.2 Integrator

We used a common configuration for our integrating circuit. This can be seen in the following image,

The circuit was used in the dual-slope ADC with a V_{ref} value in the middle of the supply (0.9 V). The amplifier used was the Self-Biased Two-stage Cascode Op-Amp shown in the section above.

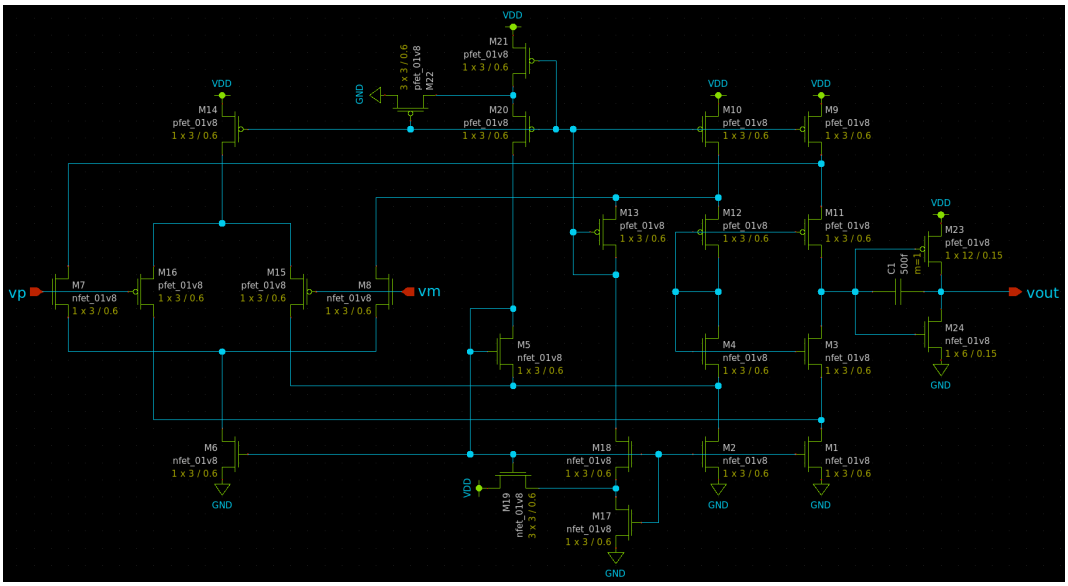

Figure 1: Self-biased Two-stage Cascode Schematic Design

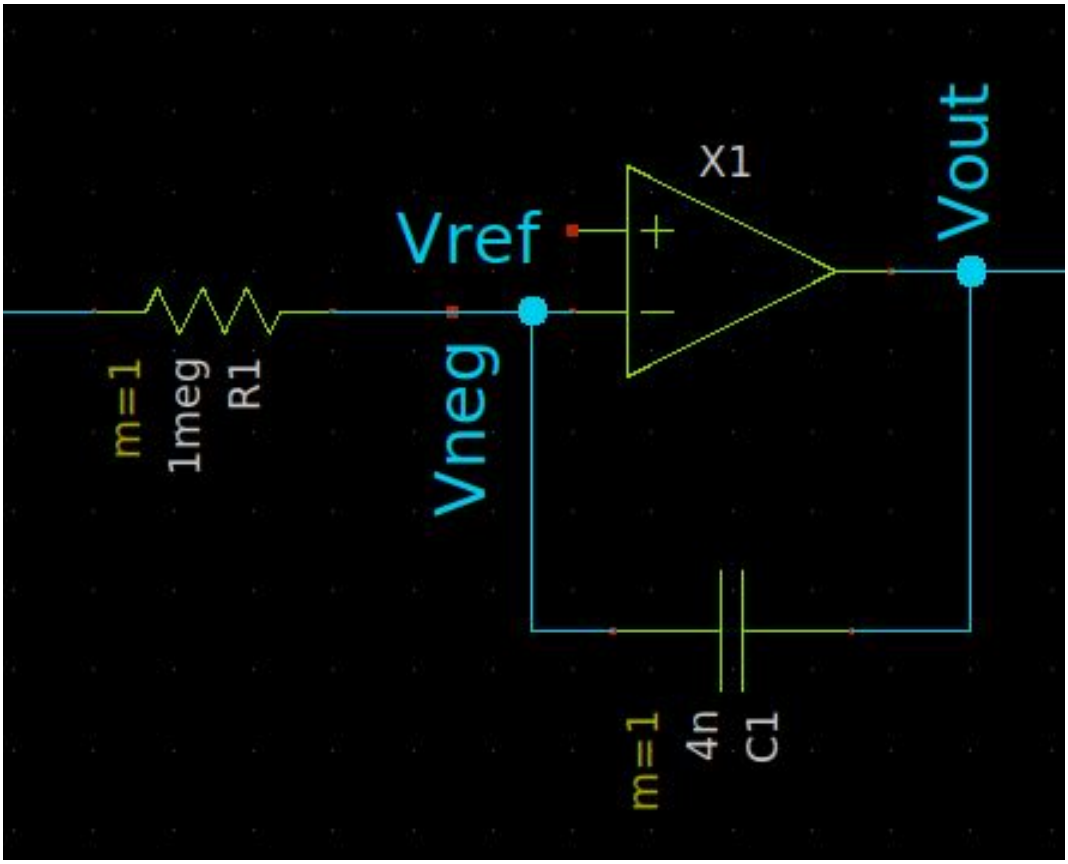

Figure 2: Integrator schematic

The full swing amplifier allowed us to more effectively create an integrator compared to the folded-cascode differential amplifier developed in MP3 due to its increased gain and wider input voltage

range. When using a reference voltage to create a virtual ground, the increased swing proved to be extremely useful.

2.3 Temperature Independent Bandgap Voltage

The bandgap reference generation consists of several stages. First, we need to bias the a few PMOS transistor to provide adequate current into the PNP transistors. Then, we need to sample the base-emitter voltage of the PNP transistors to arrive at proportional-to-absolute-temperature (PTAT) and complementary-to-absolute-temperature (CTAT) voltages. The PTAT voltage is ΔV_{be}, the difference in voltage between the two branches of PNP transistors. The CTAT Adding a properly scaled PTAT voltage to the CTAT voltage allows us to arrive at a temperature independent voltage. The CMOS transistor size is Width 3 and Length 0.6. The variable *mult* for setting transistor multiplicity is set to 8. We implemented the circuit in switched capacitors. The resulting voltages means that roughly eight times amplification on ΔV_{be} will help us get a reasonably temperature independent voltage as evidenced in Figure 5. The voltage range spanned less than 10 mV from -10$\circ C$ to 100 $\circ C$.

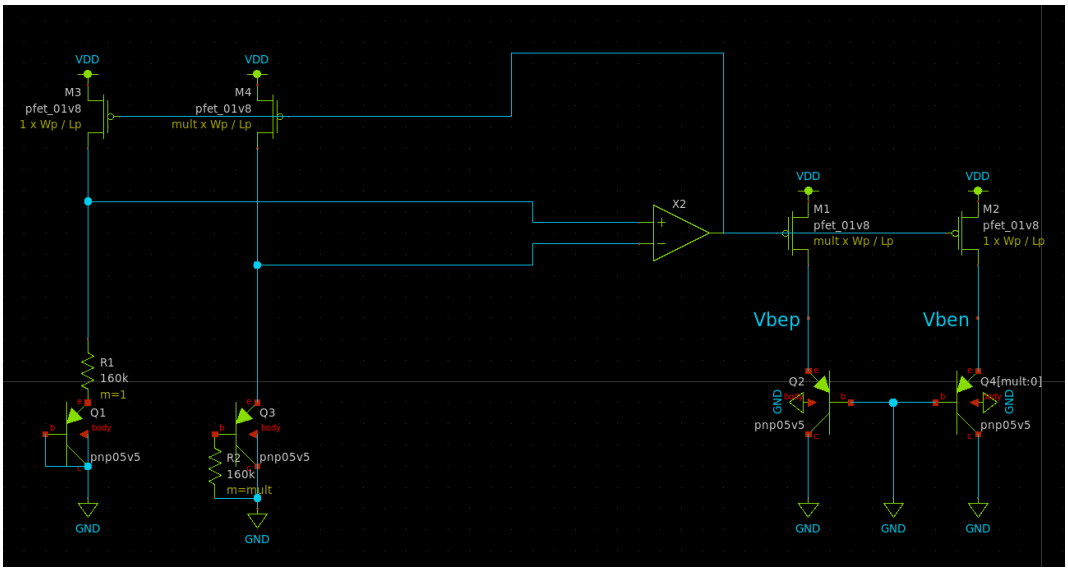

Figure 3: Bandgap circuit with PNP transistors. An op-amp along the the PNP circuit on the left is used to generate the proper biasing for the PMOS to act as independent current sources across temperature ranges

Building another difference amplifier for ΔV_{be}, referenced to the temperature independent voltage, gives us a voltage that is PTAT. This PTAT voltage is supplied to the input of the dual slope analog-to-digital converter (ADC) to do a digitized output. As you may see in Figure 6.

We may need a higher amplification than what is currently shown in the report to fully utilize the range of our ADC, but the circuit as is shows the robust linear increase in voltage with respect to temperature. Through some careful calibration and processing, we are confident that one can deduce temperature from the circuit.

Because the integrator would need a continuous time input, we make an identical copies of all of the aforementioned switched capacitor circuits with inverted switch clocks. Through the ping-pong arrangement, we were able to provide a continuous available voltage only with some downward spikes at clock edges.

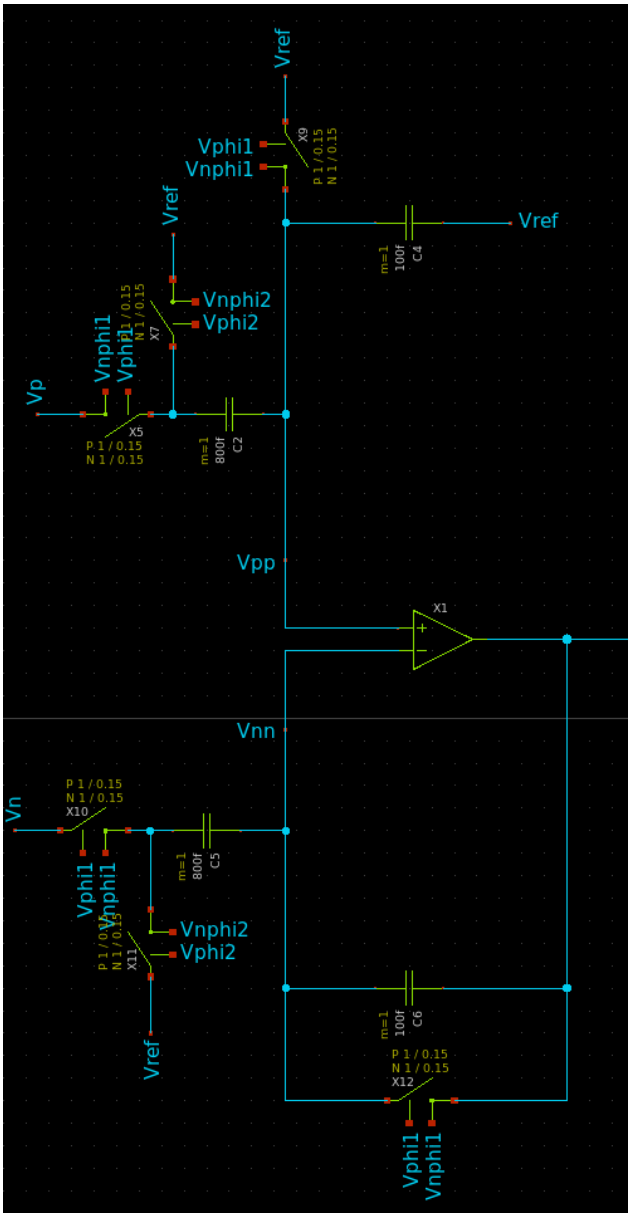

Figure 4: Switched capacitor difference amplifiers for deriving temperature independent voltages.

2.4 ADC

To implement a dual-slope ADC, we used the integrator described above, a comparator for a flag signal, and a counter for timing. Since the integrator requires both an up-going and down-going slope, we used a reference voltage of 0.9 V to create a virtual ground. The schematic for the entire ADC can be seen below,

Through a series of different input voltages, we find this converter works as we would expect. An example simulation or result from the converter is shown below,

From this, we can see that the binary output is 01110000 for an analog input of 1.3 V. To compute the converted voltage from the ADC, we find $\frac{01110000}{100000000} = \frac{112}{256} = 0.4375$. We multiply this ratio by 0.9 V and then reference it to $V_{ref} = 0.9V$, yields an output converted voltage of 1.29375

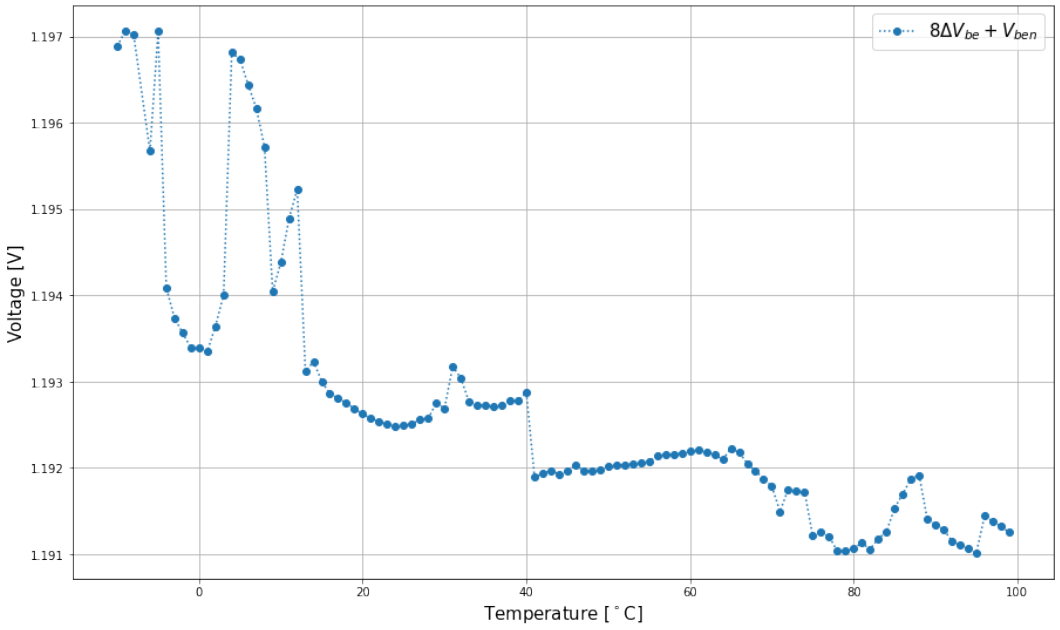

Figure 5: Temperature Independent Voltage output

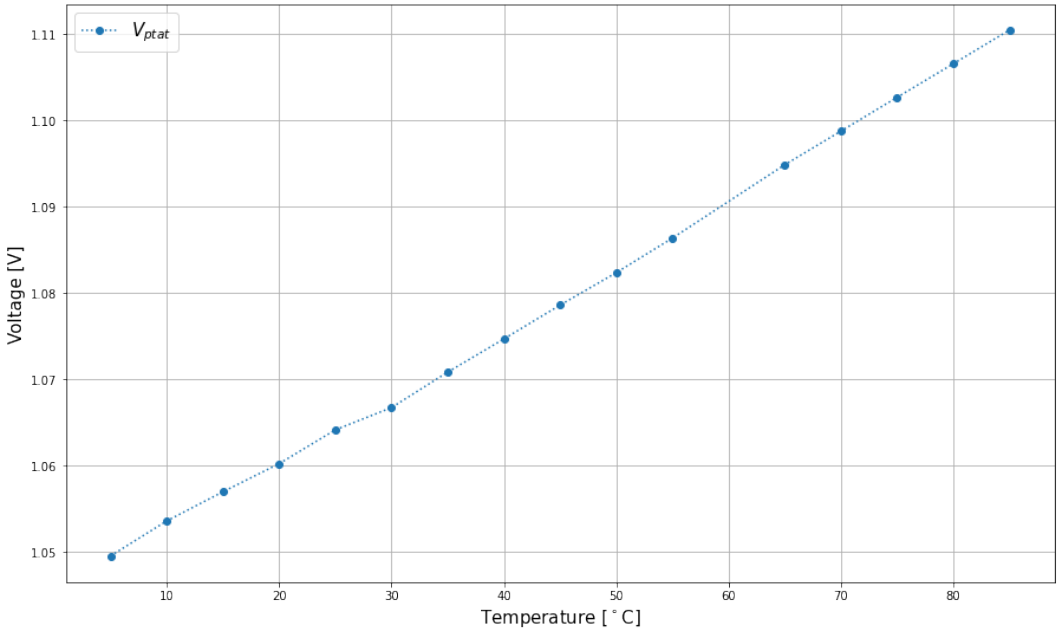

Figure 6: Output voltage with respect to the temperature

V. Which is quite close to the input voltage.

During tests, another way we considered the converted voltage was as the ratio of the slopes as the change in voltage was the same for both the up-going and down-going responses. In practicality, we will require off chip resistor and capacitors for this converter due to their large sizes.

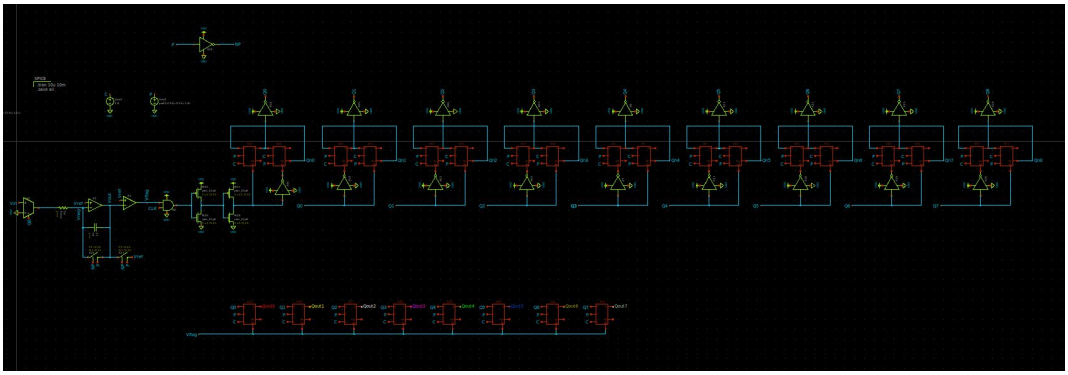

Figure 7: Dual-Slope Analog-Digital Converter Overall Schematic

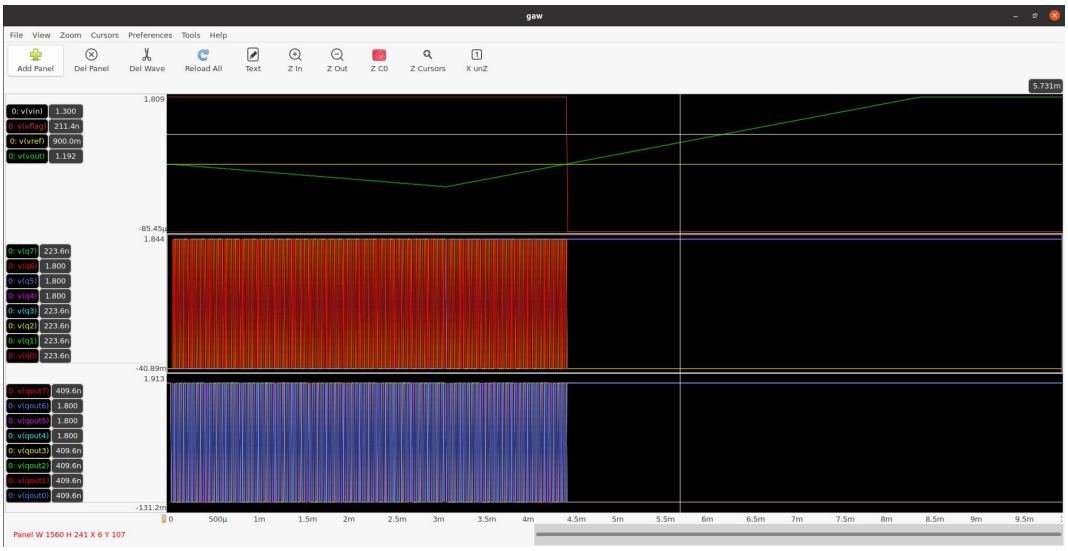

Figure 8: Dual-Slope Analog-Digital Converter Simulation

2.4.1 Comparator

The comparator we used was based on the Self-Biased Two-Stage Cascode Op-Amp. The only differences include the removal of the miller capacitor for improved speed and the output stage being buffered with progressively wider transistors for increased drive strength. The comparator used is shown below,

This comparator was used to enable the counter as well as toggle the output register.

2.4.2 Counter

We designed the counter as a nine-bit ripple-carry adder. Each bit of the adder consists of two d-flip-flop (DFF) with inverted clocks to allow for edge sensitivity. The DFF also have preset and clear functionality to allow us to reset the counter at the end of either slopes to restart counting. The 9th bit is not used for data, and is instead used to select the input PTAT voltage or the GND as the integrator input to perform either of the two slope integration.

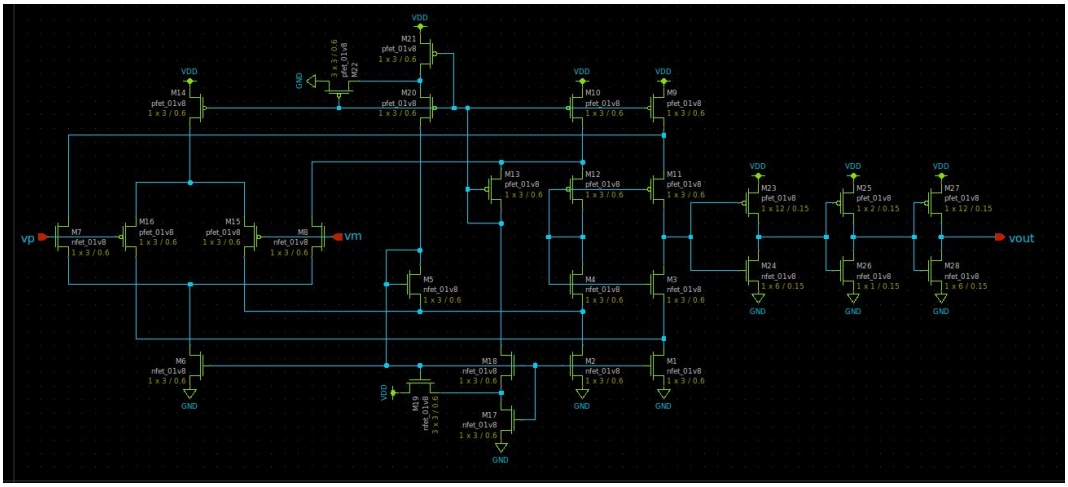

Figure 9: Comparator schematic

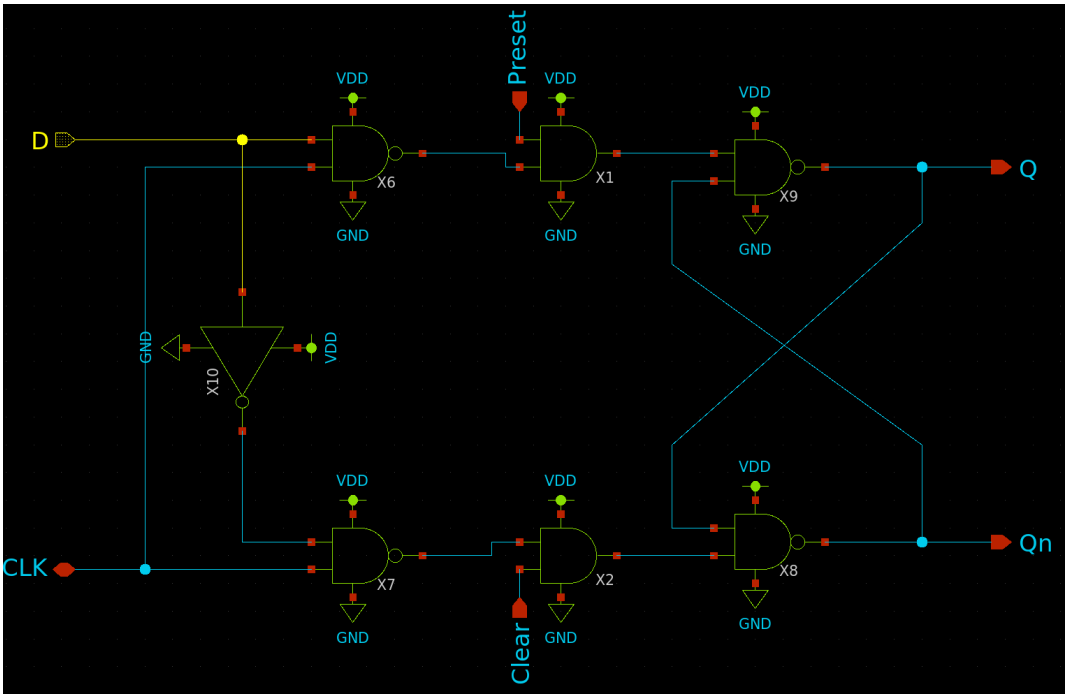

Figure 10: Underlying design of the DFF with preset and clear.

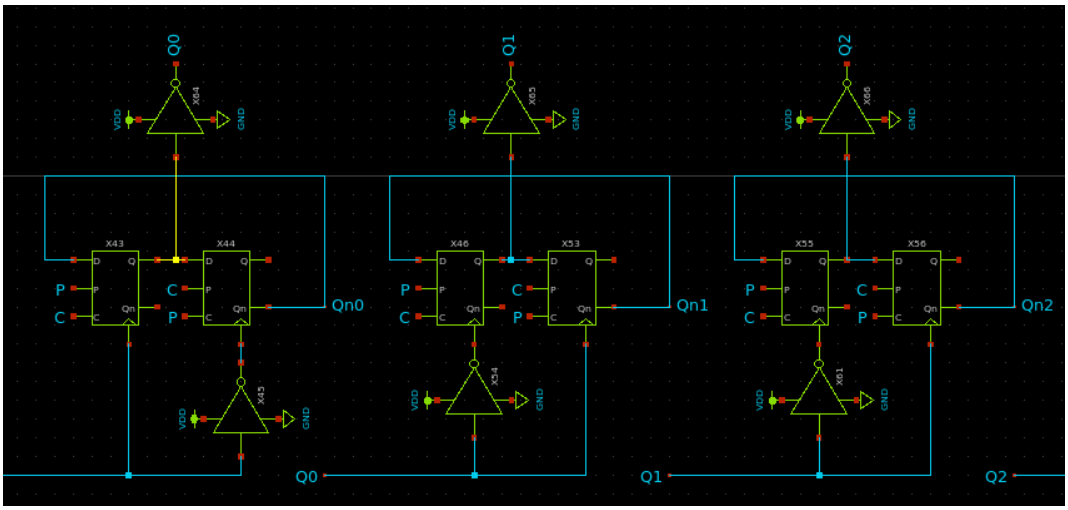

Figure 11: First three-bit of the ripple carry adder. The first bit is the only bit that have inverted clock on the right DFF. For the rest of the bits, the inverted clock is on the left DFF.

2.4.3 Output Register

The output register is made of 8 DFF's clocked by the same comparator output. Effectively, the output gets refreshed every time our integrator has integrated up to the reference voltage.

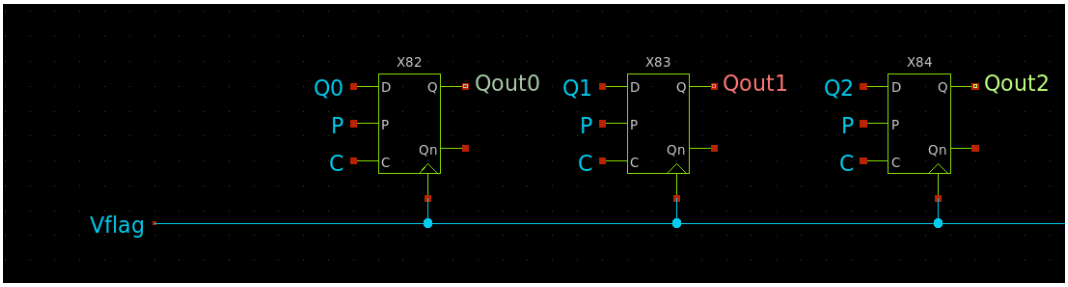

Figure 12: First three-bit of the 8-bit output register.

In the above image, V_{flag} represents the output of the comparator circuit, signaling the end of a dual-slope cycle for the ADC. The output is then held at the value of the counter when the comparator is tripped.

2.5 Overall Circuit Simulation

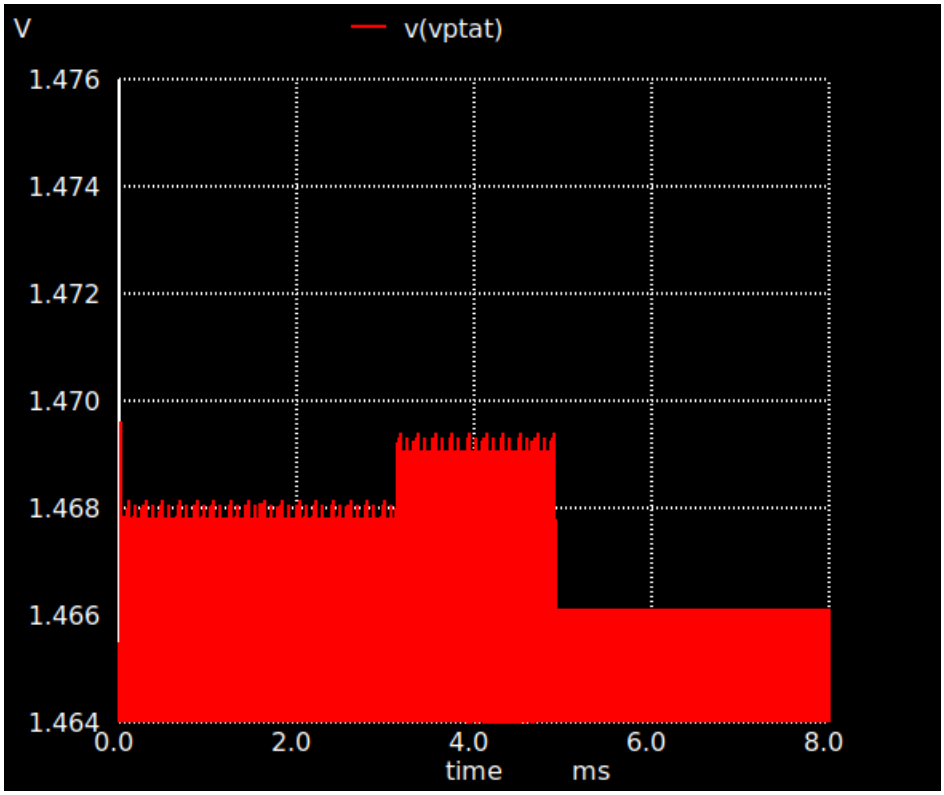

Figure 13: PTAT Voltage fed into the ADC.

We joined the circuit together in one single schematic files and ran simulations for the whole circuit together at 75 $^{\circ}C$. We observed that the corresponding PTAT voltage as the input to the

integrator is roughly 1.466-1.469 V in Figure 13. Directly at the output of the integrator is the downward and upward slopes. The downward slope is roughly $-131.813V/s$, and the upward slope is roughly $226.175V/s$. Coupled with our reference voltage of 0.9V at the integrator/comparator, the converted output voltage is

$$V_{out} = \frac{131.813}{226.175} \times 0.9V + 0.9V \approx 1.4245V \tag{1}$$

It is roughly 50 mV below than our actual input voltage. It could be an artifact of the voltage drop at capacitor switching, but we hope it may be adjusted through post conversion calibration if it results in significant deviation. Looking at the output register, we have $0'b10010101 = 0'd149$. Using this digital output to calculate the voltage as well:

$$V_{out} = \frac{149}{255} \times 0.9V + 0.9V \approx 1.426V \tag{2}$$

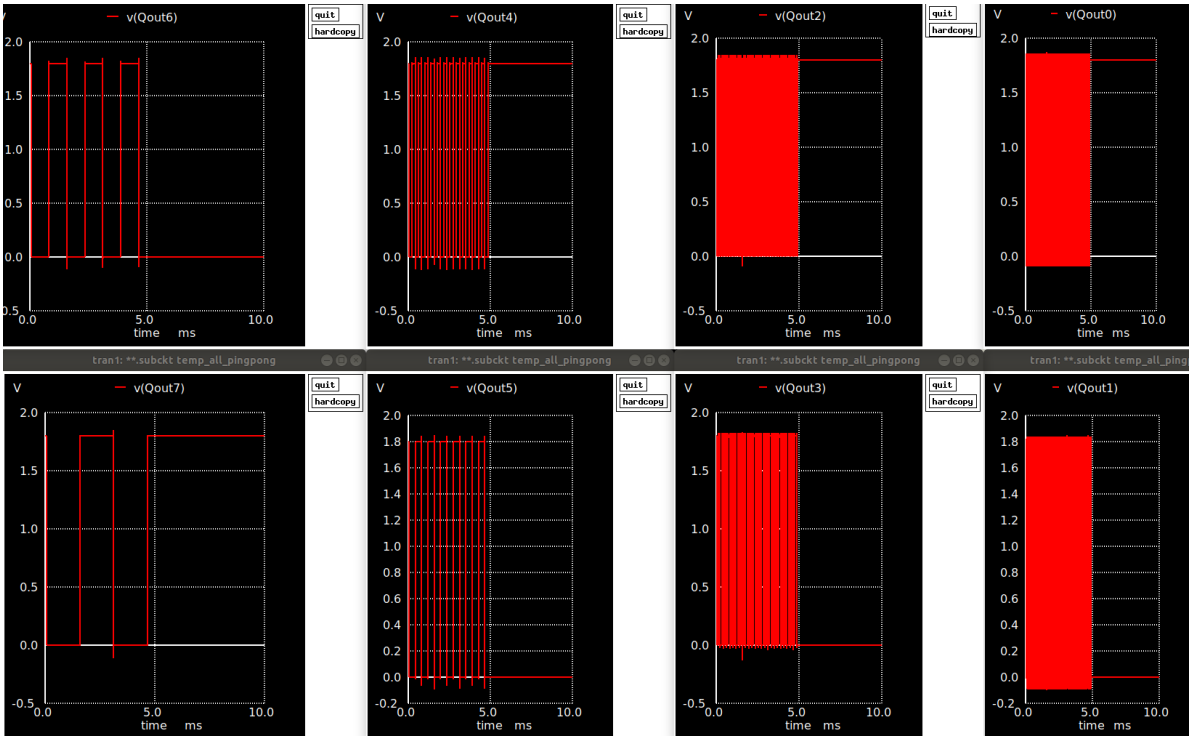

Figure 14: Digital output of the dual slope register. The digital output is 0'b10010101.

3 Layout

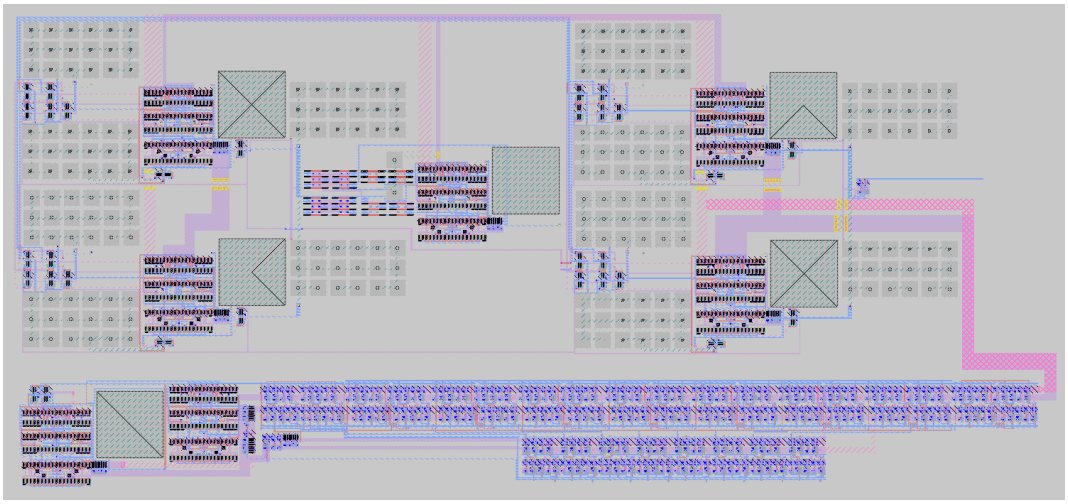

Figure 15: Layout for the temperature sensor circuit.

3.1 Self-Biased Two-Stage Cascode Op-Amp

For the self-bias two-stage cascode op-amp, we decided to layout the differential pair, current mirror, and cascode output in a vertical fashion. The top two rows of the circuit are the PMOS and NMOS differential pairs; the middle two rows are the cascode output stage; the bottom two rows are the low-voltage Wilson current mirrors. For the best analog matching practices, we padded each row and any gaps within rows with dummy transistors. We also applied common centroid once over the over self-biased op-amp stage. The output inverter stage and miller capacitor is added to the side. Because the purpose of the miller capacitors is to quench instabilities instead of performing some accurate analog computation, we laid out the $500fF$ cap in one piece.

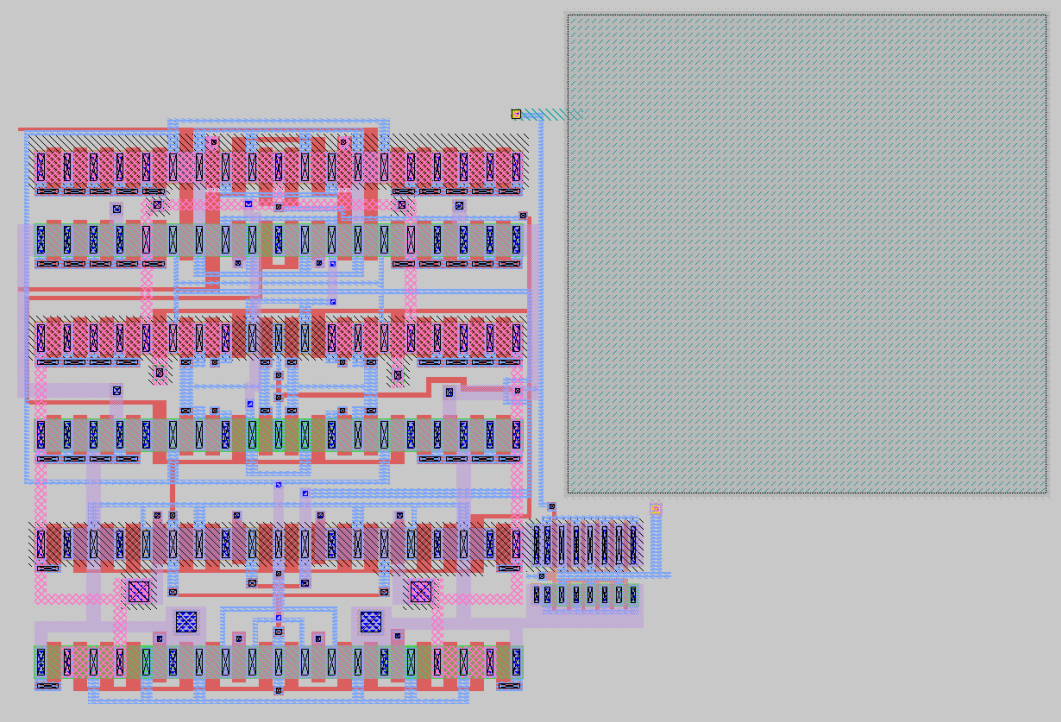

Figure 16: Layout for the self-biased 2 stage cascode amplifier.

3.2 Temperature Independent Bandgap Voltage

At the core of the temperature independent bandgap voltage circuit is the set of PNP transistors used for both biasing and bandgap voltage generation. Shown in the bottom left of Figure **??**, the PNP devices we actually use is surrounded by a set of dummy PNP devices for matching. For the resistors needed in the PMOS current source bias, they were one 160k resistor for one branch and eight 160k resistors in parallel for the other. For the best matching purposes, those effectively translate to eight 20k resistors in series for one and one 20k resistor for the other. The resistors were made with p- precision polysilicon and of dimension 0.35/3.5. Four op-amp were used here in total. One is for the purpose of driving PMOS current sources based on feedback. The other three are for the purpose of buffering the voltages at V_{be+} and V_{be-} such that subsequent stages can use these voltages to perform computations without degrading the source signals.

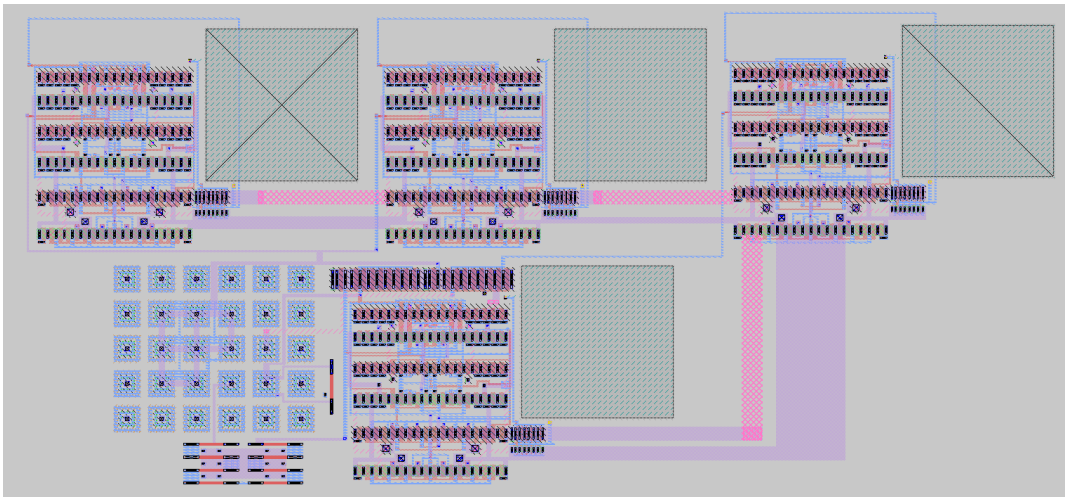

Figure 17: Layout for the Bandgap Circuit.

3.3 ADC

The ADC brings together the integrator, comparator, ripple-carry adder, and output register. This layout combines the connections between each of the subcells used within the dual-slope ADC. The analog component (integrator and comparator) are to the left within the cell, and the digital is to the right. The output register is at the bottom of the cell for easy connections to pins when this is put into a padframe.

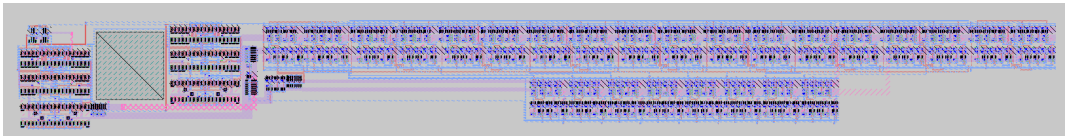

Figure 18: Layout for the Analog to Digital Converter.

3.3.1 Comparator

The comparator layout follows much of the same design principles as the amplifier we used. The differences include the output stage on the right side of the cell. This includes three inverters of various sizes and the removal of the capacitor on the output.

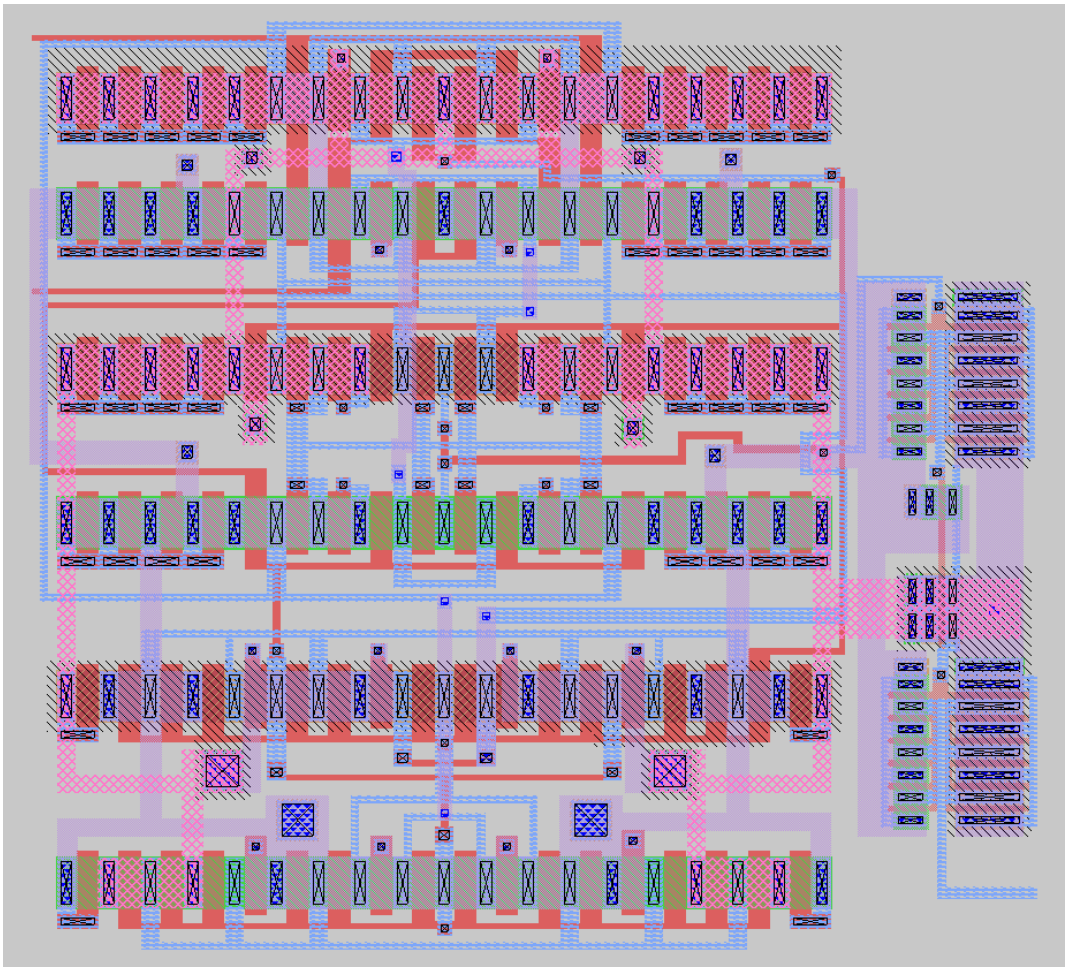

Figure 19: Layout for the Comparator Circuit.

3.3.2 Counter

The counter we used strung together several flip flops in the arrangement indicated by the schematic. The outputs line the bottom of the cell for easy connections with the output register shown in the following section.

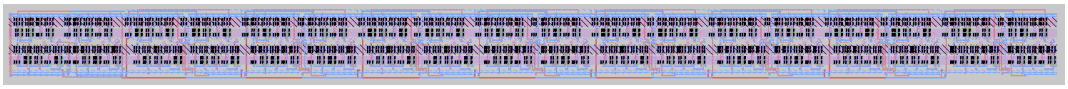

Figure 20: Layout for the Counter Circuit.

3.3.3 Output Register

The following image shows the layout for the output register. Much like the counter, the output bits can be accessed through the bottom contacts.

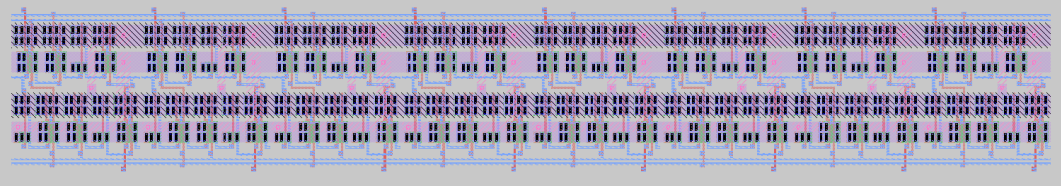

Figure 21: Layout for the Output Register Circuit.

3.3.4 Overall Temperature Sensor Layout

We combined all of the subcells of the circuit to form a fully integrated CMOS temperature sensor. The bandgap circuit is in the top left of the cell, the middle of the cell processes the bandgap voltages, and the bottom forms the dual-slope ADC and output register.

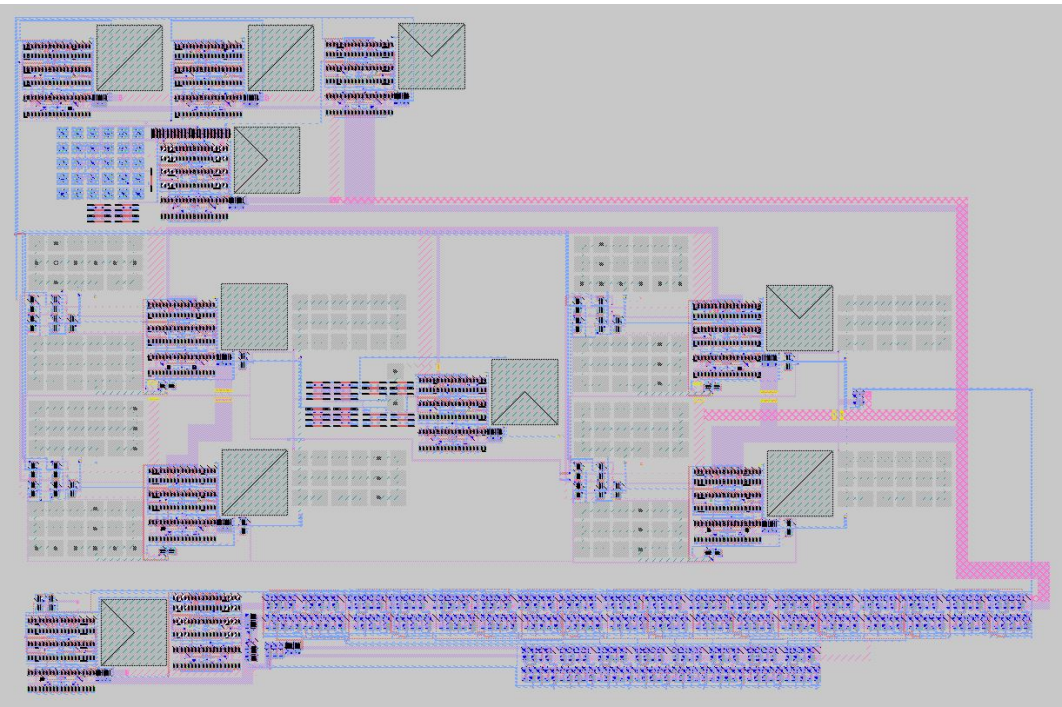

Figure 22: Entire Temperature Sensor Chip Layout

4 Layout versus Schematic

Our final output LVS output can be seen at the following link: https://github.com/ThomasJagielski/MADVLSI-Final_Project/blob/main/lvs/temperature_sensor/comp.out.

The LVS indicates a pin mismatch within the top level of the circuit. Interestingly, the subcircuits used appear to match to the schematic. Thus, we believe this error could be from the layout and schematic matching to different subcells in the overall schematic. All of the LVS files can be found in the following GitHub folder: *https://github.com/ThomasJagielski/MADVLSI-Finalproject/tree/main/lvs*.

5 References

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