

MADVLSI: Miniproject 1

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1 Design Files

GitHub link to design files: <https://github.com/ThomasJagielski/MADVLSI-MP1>.

- Layout = <https://github.com/ThomasJagielski/MADVLSI-MP1/tree/main/layout/revised>
- Schematic = <https://github.com/ThomasJagielski/MADVLSI-MP1/tree/main/schematic>
- LVS = <https://github.com/ThomasJagielski/MADVLSI-MP1/tree/main/LVS>

2 Schematic

2.1 Inverter

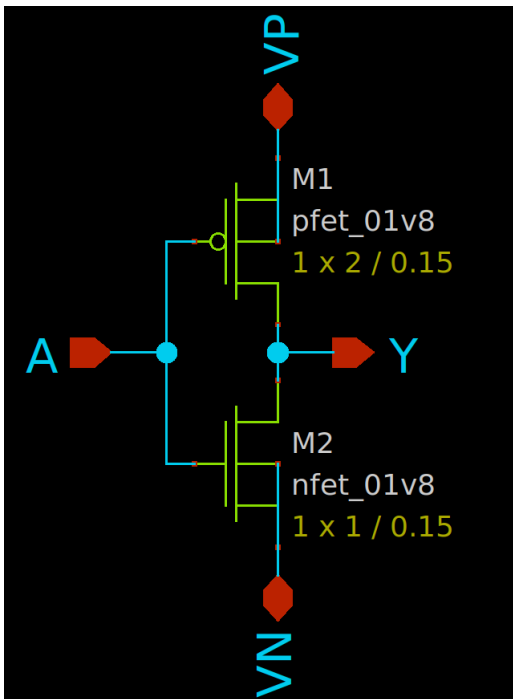


Figure 1: Conventional Inverter Schematic

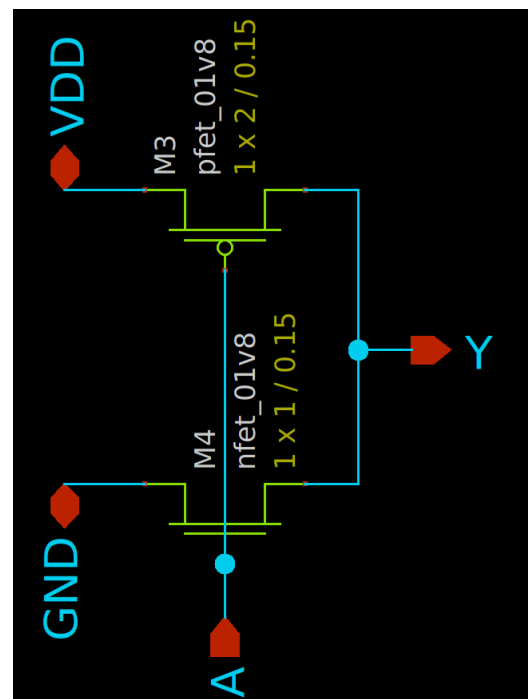


Figure 2: Inverter Layout Driven Schematic

2.2 NAND2

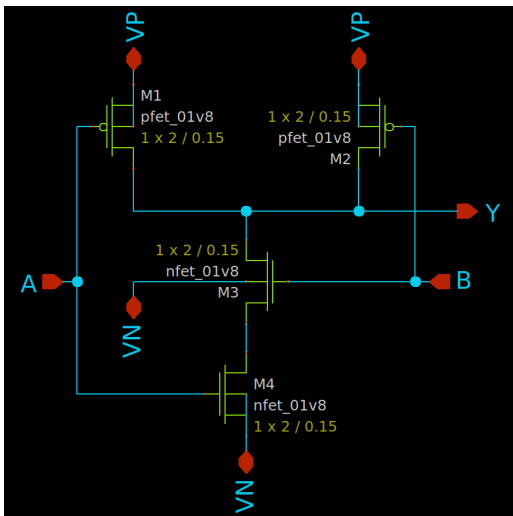


Figure 3: Conventional NAND2 Schematic

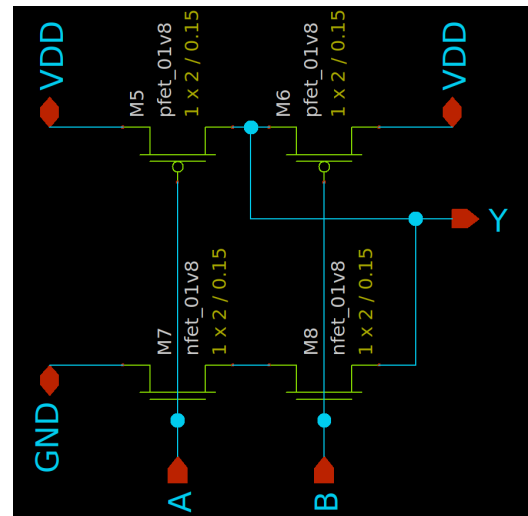


Figure 4: NAND2 Layout Driven Schematic

2.3 AND2

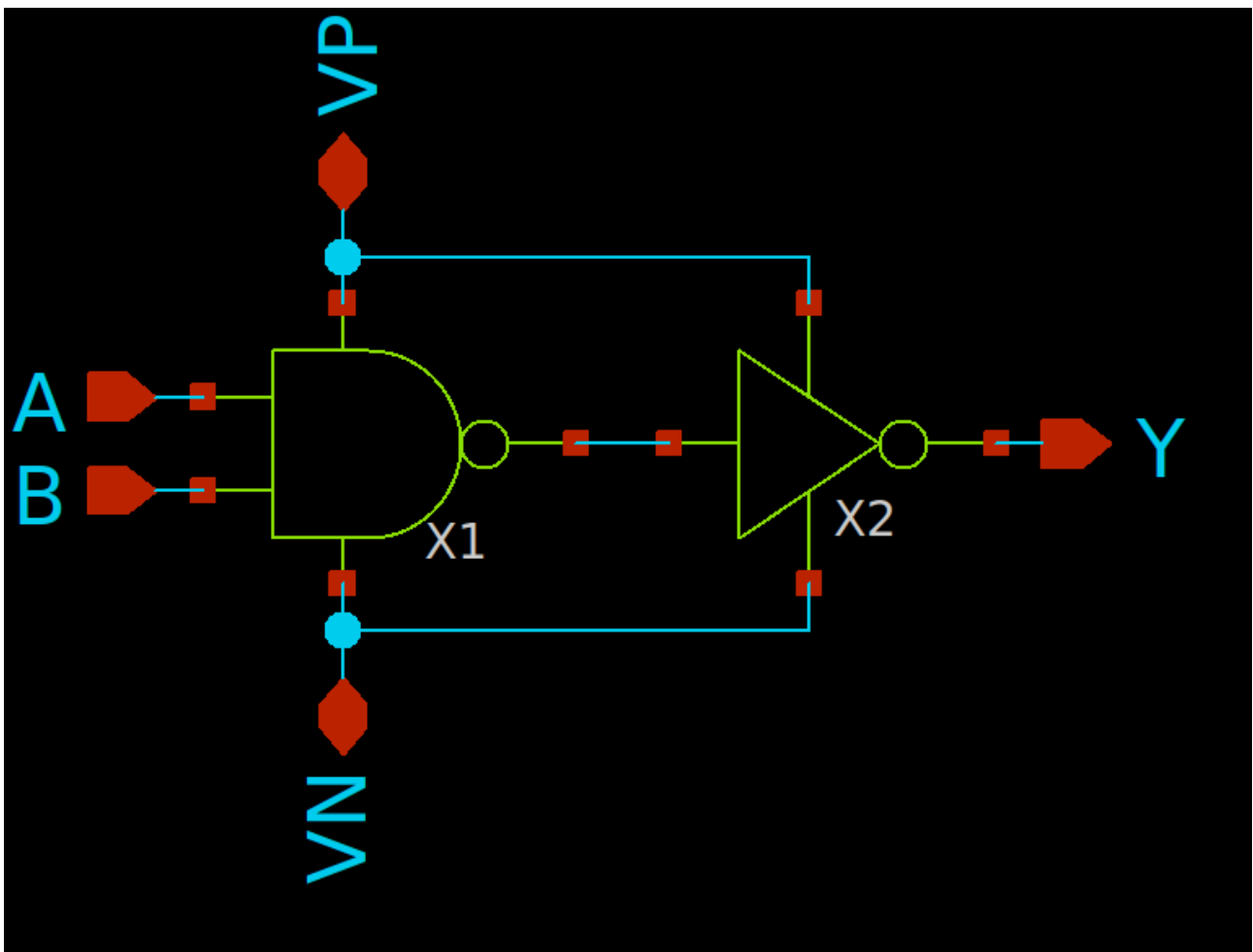


Figure 5: AND2 Schematic Using Inverter and NAND2 Subcircuits

3 Xschem Simulation

3.1 Schematic

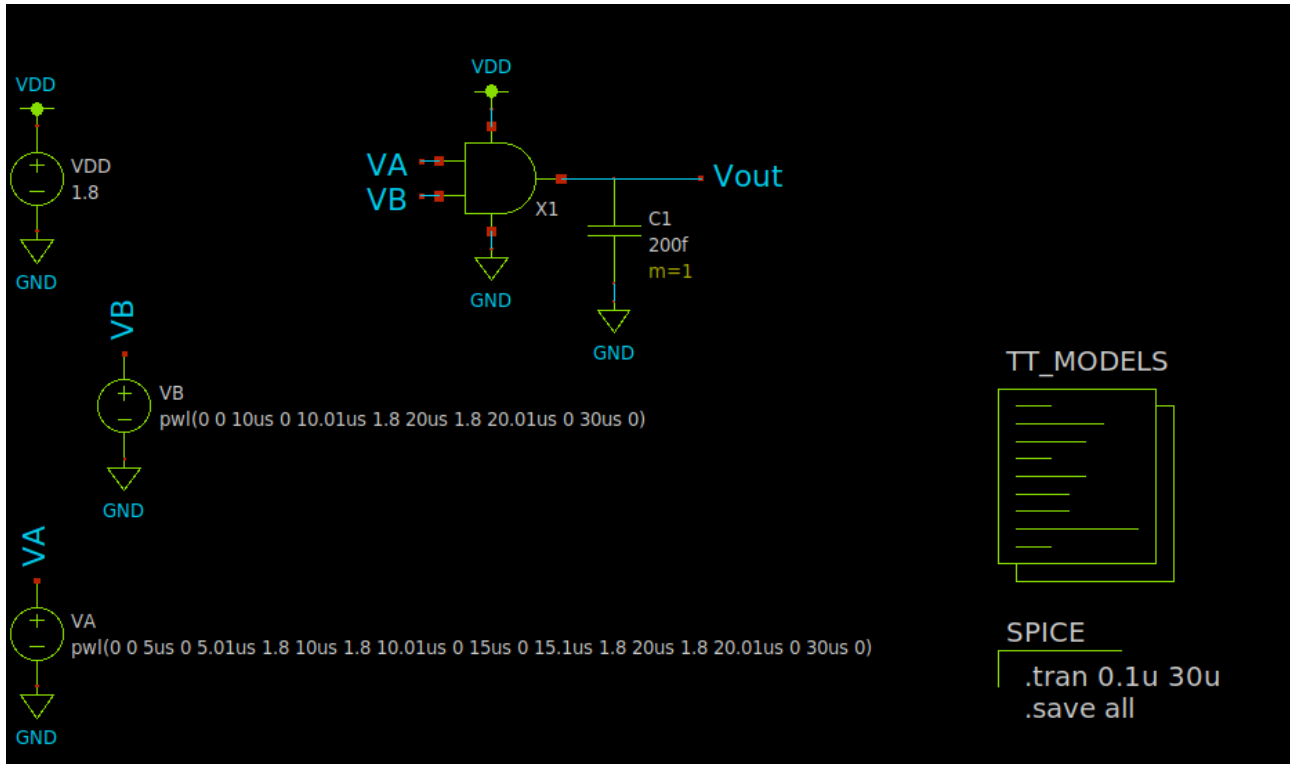


Figure 6: Simulation Schematic

3.2 Simulation Results

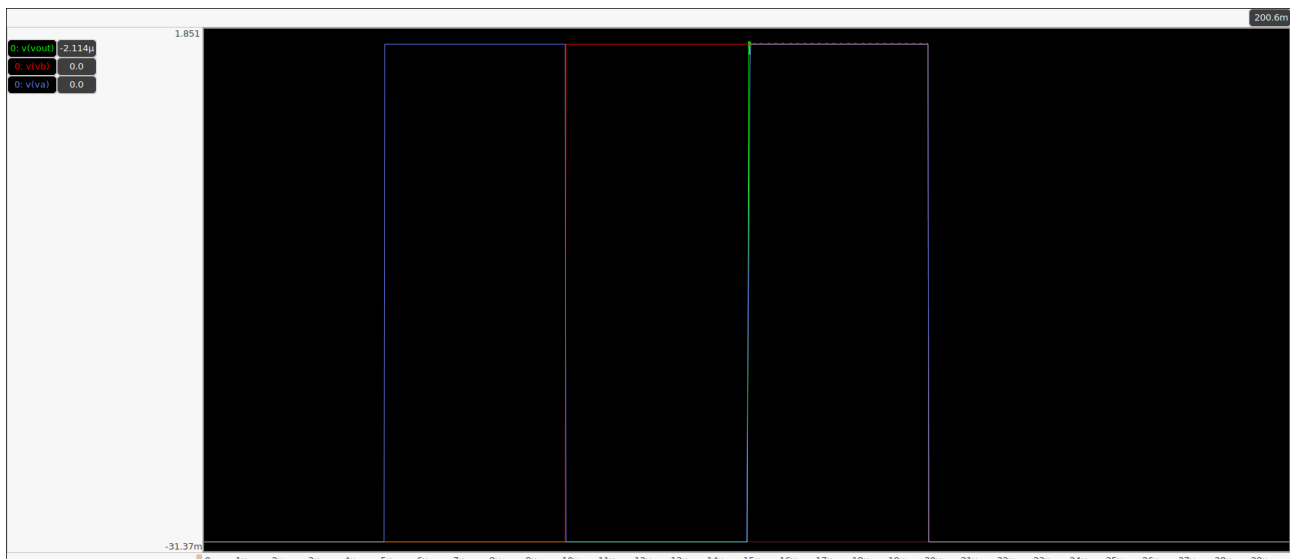


Figure 7: Simulation Waveform

This figure shows the output of the AND2 circuit sweeping through all possible inputs. From 0 to 5 μ s both A and B are low. From 5 μ s to 10 μ s A is high and B is low. From 10 μ s to 15 μ s A is low and B is high. From 15 μ s to 20 μ s both inputs are high and the output then goes high. After 20 μ s both inputs go low, which yields a low output signal.

4 Layout

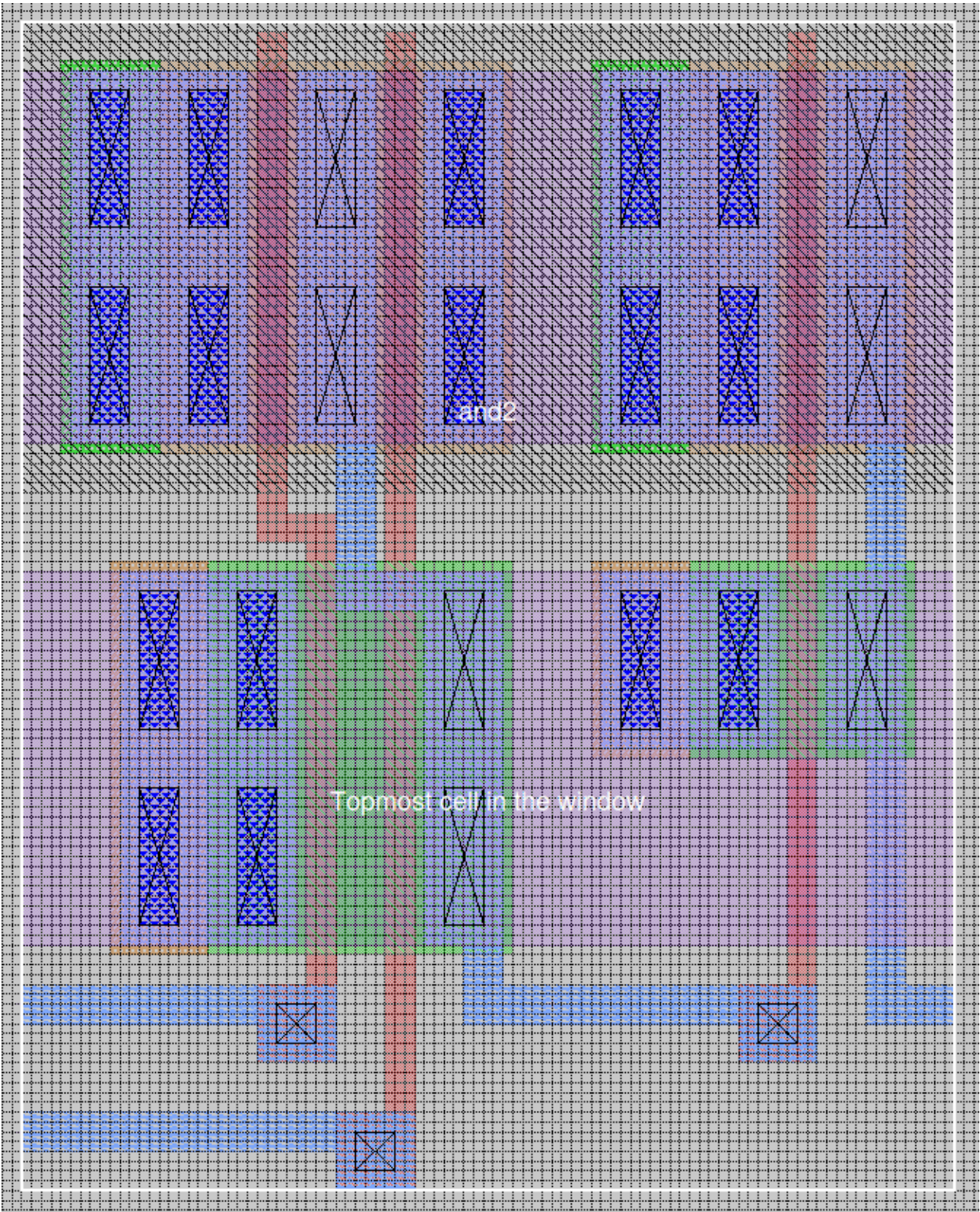


Figure 8: AND2 Layout Using Magic

5 Layout Verses Schematic

The following code block shows the .out file for the comparison between my layout extracted netlist and the schematic extracted netlist. For this comparison the files ./LVS/and2.spice and ./LVS/and2.schem.spice were used. Please note that and2.spice comes from the and2.mag file in the revised folder.

```
1 Equate elements:  no current cell.
2 Equate elements:  no current cell.
3
4 Subcircuit summary:
5 Circuit 1: inverter                                |Circuit 2: inverter
6 -----|-----
7 sky130_fd_pr__pfet_01v8 (1)                        |sky130_fd_pr__pfet_01v8 (1)
8 sky130_fd_pr__nfet_01v8 (1)                        |sky130_fd_pr__nfet_01v8 (1)
9 Number of devices: 2                               |Number of devices: 2
10 Number of nets: 4                                 |Number of nets: 4
11 -----|-----
12 Circuits match uniquely.
13 Netlists match uniquely.
14
15 Subcircuit pins:
16 Circuit 1: inverter                                |Circuit 2: inverter
17 -----|-----
18 Y                                                  |Y
19 A                                                  |A
20 VP                                                  |VP
21 VN                                                  |VN
22 -----|-----
23 Cell pin lists are equivalent.
24 Device classes inverter and inverter are equivalent.
25
26 Subcircuit summary:
27 Circuit 1: nand2                                    |Circuit 2: nand2
28 -----|-----
29 sky130_fd_pr__pfet_01v8 (2)                        |sky130_fd_pr__pfet_01v8 (2)
30 sky130_fd_pr__nfet_01v8 (2)                        |sky130_fd_pr__nfet_01v8 (2)
31 Number of devices: 4                               |Number of devices: 4
32 Number of nets: 6                                 |Number of nets: 6
33 -----|-----
34 Circuits match uniquely.
35 Netlists match uniquely.
36
37 Subcircuit pins:
38 Circuit 1: nand2                                    |Circuit 2: nand2
39 -----|-----
40 Y                                                  |Y
41 VN                                                  |VN
42 A                                                  |A
43 B                                                  |B
44 VP                                                  |VP
45 -----|-----
```

```

46 Cell pin lists are equivalent.
47 Device classes nand2 and nand2 are equivalent.
48
49 Subcircuit summary:
50 Circuit 1: and2.spice | Circuit 2: and2_xschem.spice
51 -----|-----
52 inverter (1) | inverter (1)
53 nand2 (1) | nand2 (1)
54 Number of devices: 2 | Number of devices: 2
55 Number of nets: 6 | Number of nets: 6
56 -----|-----
57 Circuits match uniquely.
58 Netlists match uniquely.
59 Cells have no pins; pin matching not needed.
60 Device classes and2.spice and and2_xschem.spice are equivalent.
61 Circuits match uniquely.

```