MADVLSI: Miniproject 1

Thomas Jagielski

February 2021

1 Design Files

GitHub link to design files: https://github.com/ThomasJagielski/MADVLSI-MP1.

- Layout = https://github.com/ThomasJagielski/MADVLSI-MP1/tree/main/layout/revised
- Schematic = https://github.com/ThomasJagielski/MADVLSI-MP1/tree/main/schematic
- LVS = https://github.com/ThomasJagielski/MADVLSI-MP1/tree/main/LVS

2 Schematic

2.1 Inverter

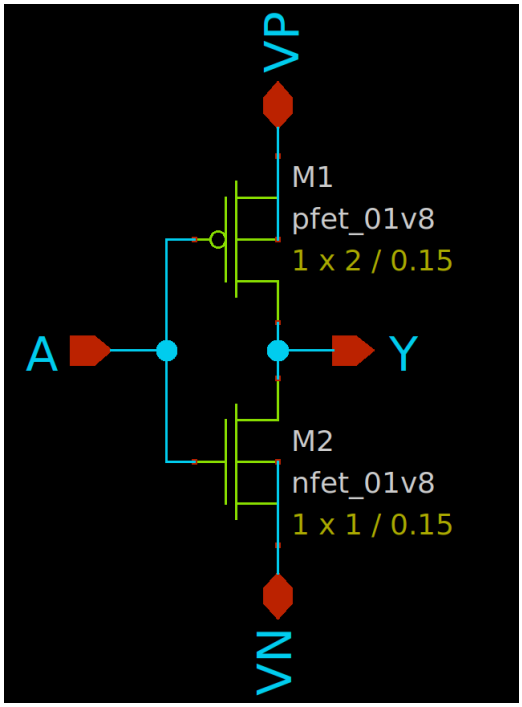

Figure 1: Conventional Inverter Schematic

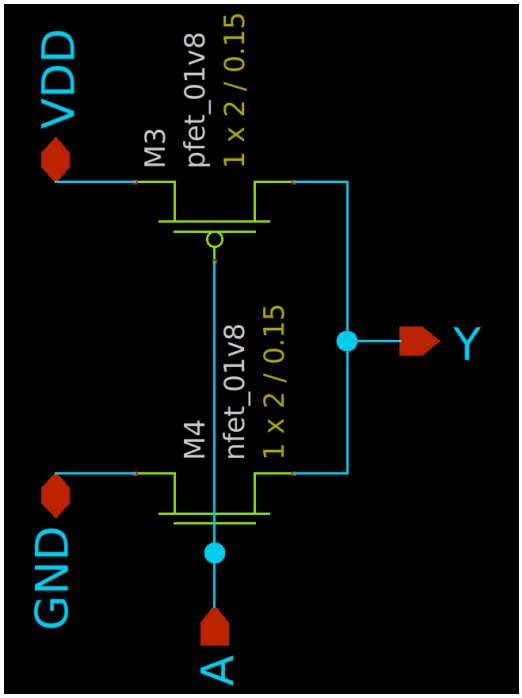

Figure 2: Inverter Layout Driven Schematic

2.2 NAND2

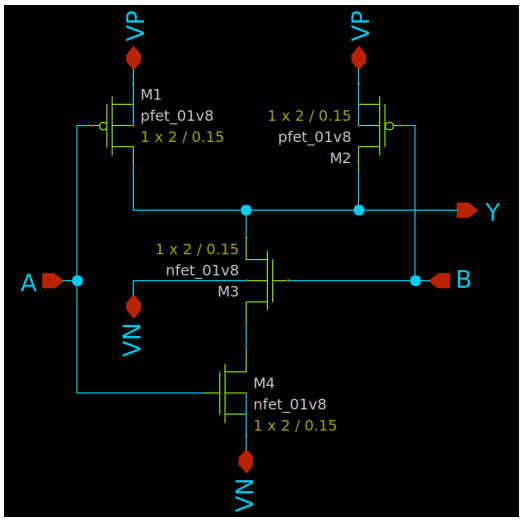

Figure 3: Conventional NAND2 Schematic

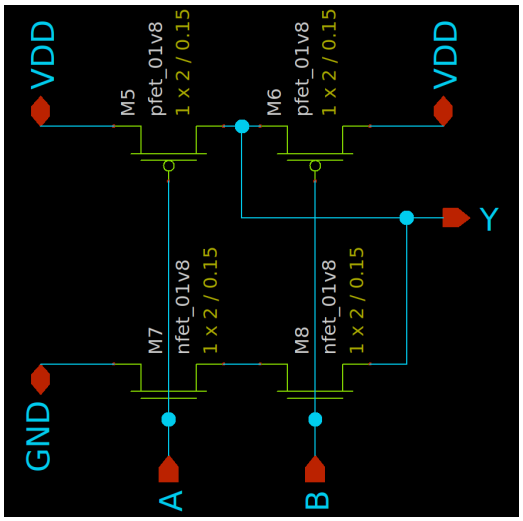

Figure 4: NAND2 Layout Driven Schematic

2.3 AND2

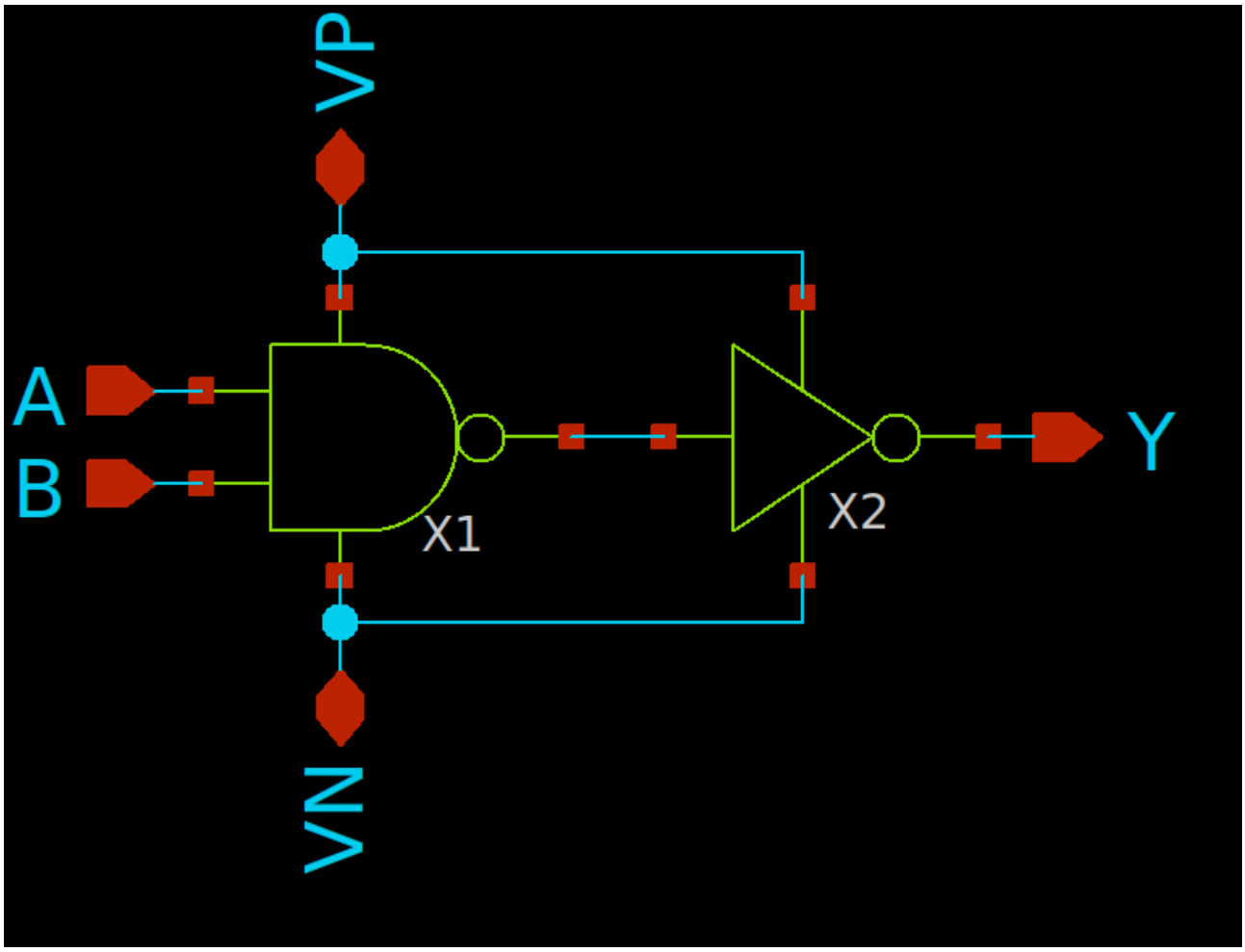

Figure 5: AND2 Schematic Using Inverter and NAND2 Subcircuits

3 Xschem Simulation

3.1 Schematic

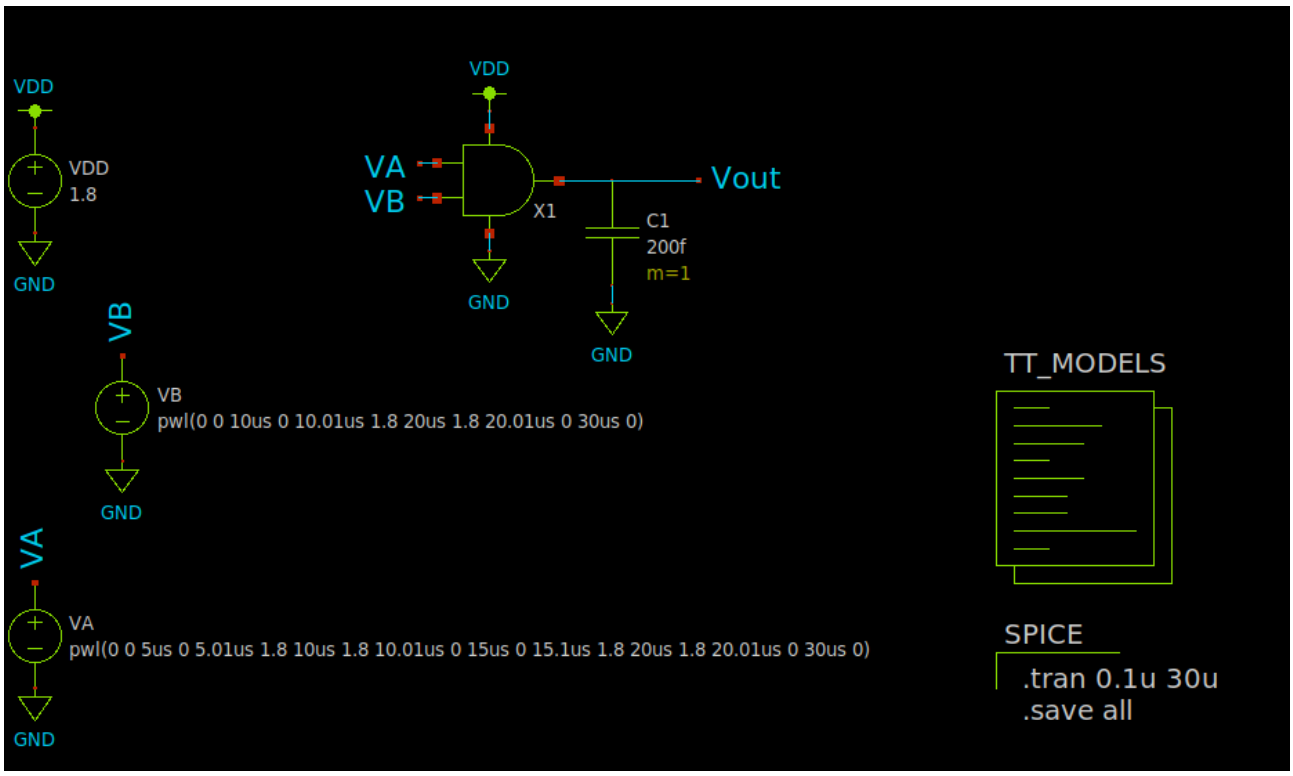

Figure 6: Simulation Schematic

3.2 Simulation Results

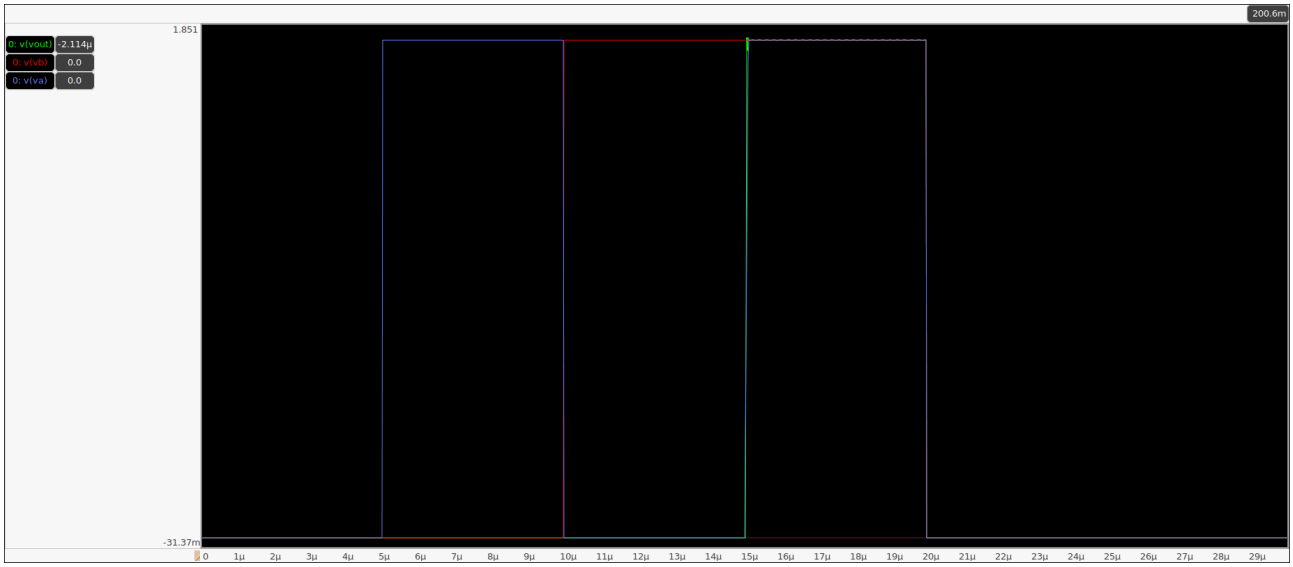

Figure 7: Simulation Waveform

This figure shows the output of the AND2 circuit sweeping through all possible inputs. From 0 to 5 μs both A and B are low. From 5 μs to 10 μs A is high and B is low. From 10 μs to 15 μs A is low and B is high. From 15 μs to 20 μs both inputs are high and the output then goes high. After 20 μs both inputs go low, which yields a low output signal.

4 Layout

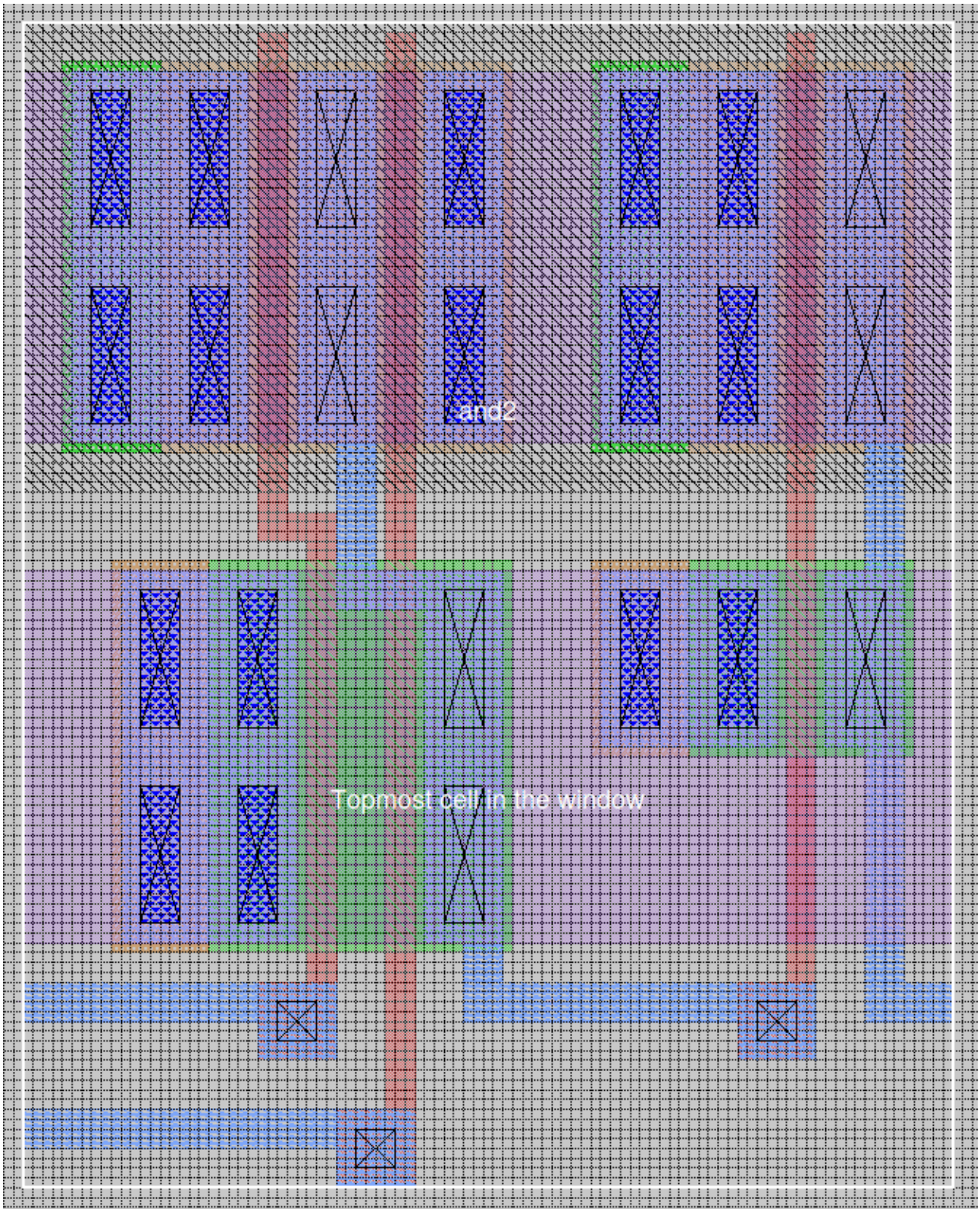

Figure 8: AND2 Layout Using Magic

5 Layout Verses Schematic

The following code block shows the .out file for the comparison between my layout extracted netlist and the schematic extracted netlist. For this comparison the files ./LVS/and2.spice and ./LVS/and2_schem.spice were used. Please note that and2.spice comes from the and2.mag file in the revised folder.

```
Equate elements:  no current cell.
Equate elements:  no current cell.

Subcircuit summary:
Circuit 1: inverter                        |Circuit 2: inverter
-------------------------------------------|-------------------------------------------

sky130_fd_pr__pfet_01v8 (1)                |sky130_fd_pr__pfet_01v8 (1)
sky130_fd_pr__nfet_01v8 (1)                |sky130_fd_pr__nfet_01v8 (1)
Number of devices: 2                       |Number of devices: 2
Number of nets: 4                          |Number of nets: 4
-------------------------------------------------------------------------------------------

Circuits match uniquely.
Netlists match uniquely.

Subcircuit pins:
Circuit 1: inverter                        |Circuit 2: inverter
-------------------------------------------|-------------------------------------------

Y                                          |Y
A                                          |A
VP                                         |VP
VN                                         |VN
-------------------------------------------------------------------------------------------

Cell pin lists are equivalent.
Device classes inverter and inverter are equivalent.

Subcircuit summary:
Circuit 1: nand2                           |Circuit 2: nand2
-------------------------------------------|-------------------------------------------

sky130_fd_pr__pfet_01v8 (2)                |sky130_fd_pr__pfet_01v8 (2)
sky130_fd_pr__nfet_01v8 (2)                |sky130_fd_pr__nfet_01v8 (2)
Number of devices: 4                       |Number of devices: 4
Number of nets: 6                          |Number of nets: 6
-------------------------------------------------------------------------------------------

Circuits match uniquely.
Netlists match uniquely.

Subcircuit pins:
Circuit 1: nand2                           |Circuit 2: nand2
-------------------------------------------|-------------------------------------------

Y                                          |Y
VN                                         |VN
A                                          |A
B                                          |B
VP                                         |VP
-------------------------------------------------------------------------------------------
```

```
Cell pin lists are equivalent.
Device classes nand2 and nand2 are equivalent.

Subcircuit summary:
Circuit 1: and2.spice                       |Circuit 2: and2_xschem.spice
--------------------------------------------|-------------------------------------------

inverter (1)                                |inverter (1)
nand2 (1)                                   |nand2 (1)
Number of devices: 2                        |Number of devices: 2
Number of nets: 6                           |Number of nets: 6
-----------------------------------------------------------------------------------------

Circuits match uniquely.
Netlists match uniquely.
Cells have no pins;  pin matching not needed.
Device classes and2.spice and and2_xschem.spice are equivalent.
Circuits match uniquely.
```