MADVLSI: Miniproject 2

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1 Design Files

GitHub link to design files: https://github.com/ThomasJagielski/MADVLSI-MP2. For the final design files please refer to all folders labeled with final_[subfolder].

- Layout = https://github.com/ThomasJagielski/MADVLSI-MP2/tree/main/layout/final_layout
- Schematic = https://github.com/ThomasJagielski/MADVLSI-MP2/tree/main/schematic/final_schematic
- LVS = https://github.com/ThomasJagielski/MADVLSI-MP2/tree/main/LVS/final_LVS

2 Schematic

For this miniproject two conditions were considered. The first used transistors all with strength 1, and the second used strength $\frac{1}{2}$ transistors in the pass transistor logic. As shown in the simulation results section later, the strength 1 transistor circuit does not propagate the signal through the shift register properly under worst case conditions. Thus, as discussed by Massimo Antonio Sivilotti in *Wiring Considerations in Analog VLSI Systems, with Application to Field-Programmable Networks*, the write-ability problem is present under slow transistor conditions. As a result, transistors with strength $\frac{1}{2}$ in the pass transistor logic network were used in the design for increased robustness, as demonstrated through corner analysis in the simulation section. This ratio between the pull down network and pass transistor logic ensures that the pull-down network transistors conductor more current than the pass transistors. Unless indicated otherwise, the circuit referenced throughout this report defaults to the schematic shown in Figure 1.

The following image shows a layout driven schematic for the CSRL positive-edge triggered D flip-flop with a ratio of 2 between the strength of the pull down transistors and the pass transistors. In order to create this ratio, the pass transistors were reduced to have a strength ratio of $\frac{1}{2}$ (M3 and M4). This was done in order to minimize layout area by sharing source/drain diffusions.

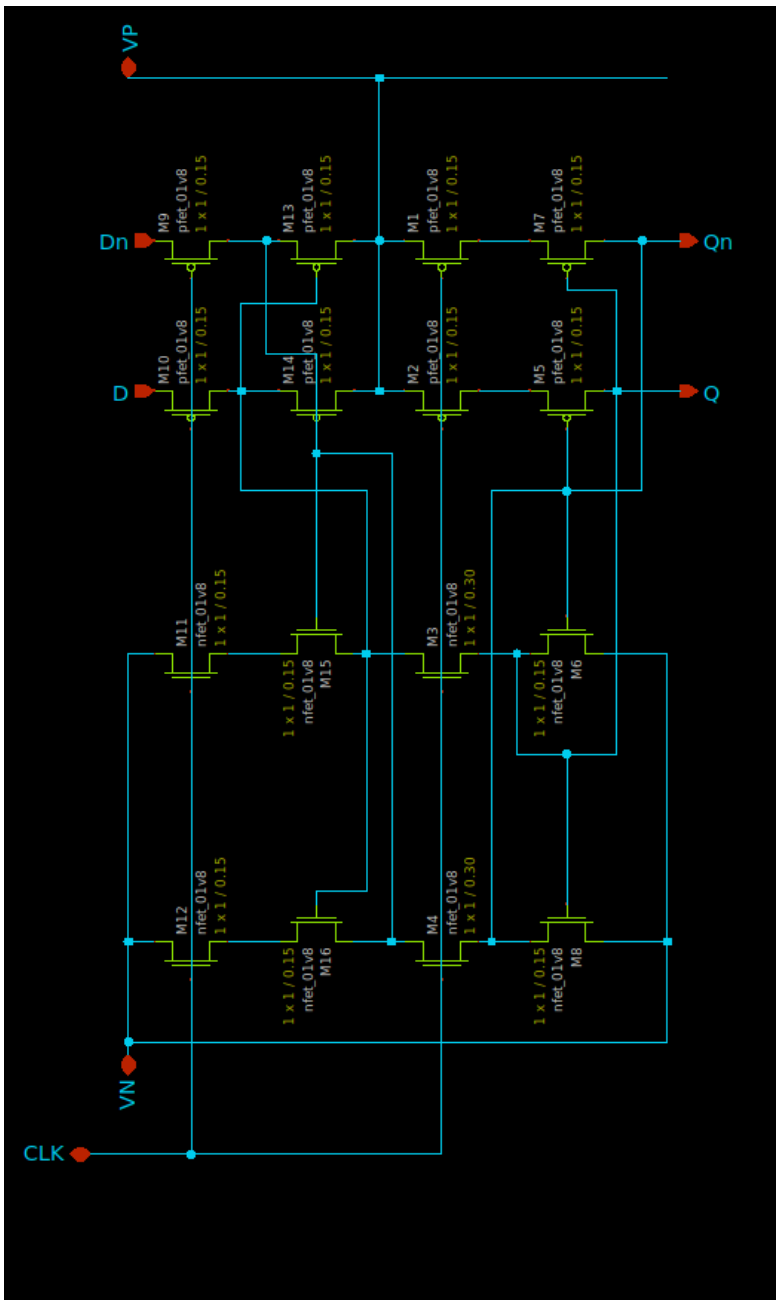

Figure 1: CSRL Positive Edge Triggered D Flip-Flop Layout Driven Schematic

3 Xschem Simulation

3.1 Schematic

The following image shows the test schematic and configuration used to simulate the circuit's function.

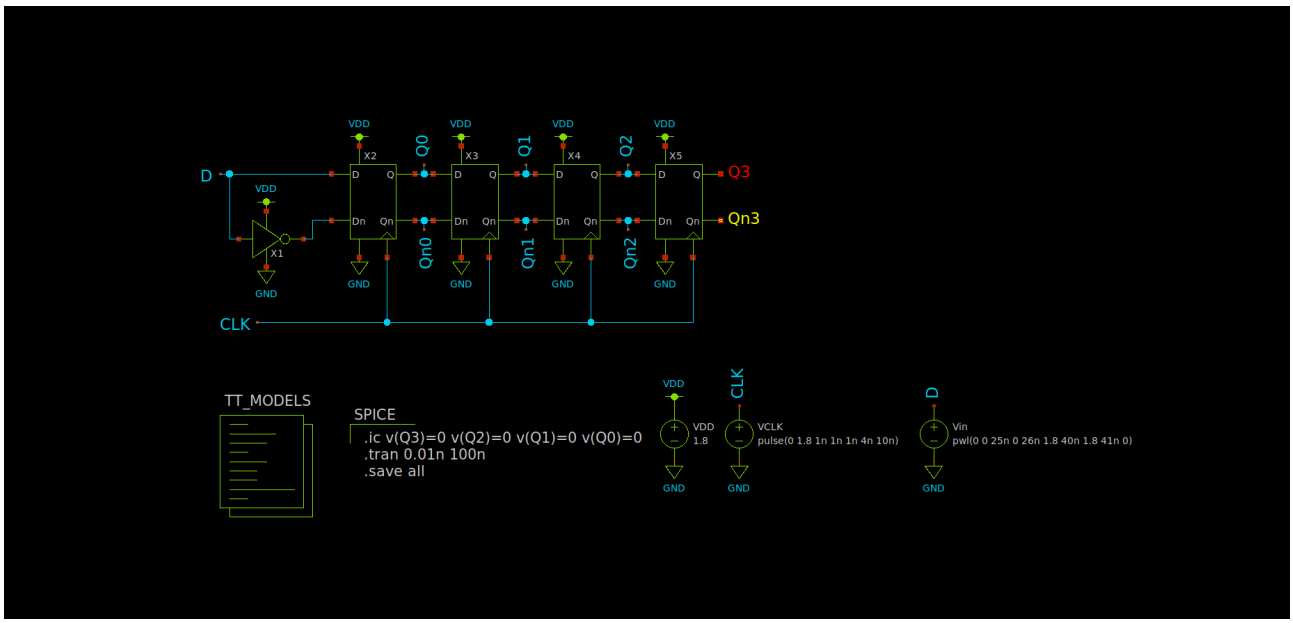

Figure 2: Simulation Schematic for Width 1 and Width 2 Cases

3.2 Simulation Results

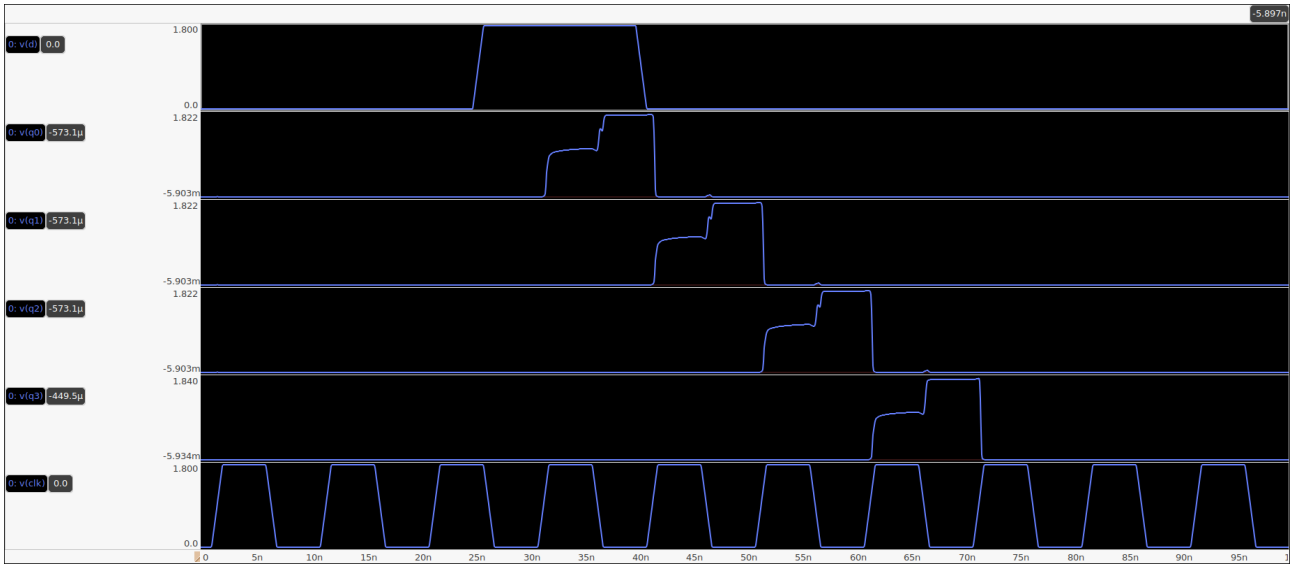

Figure 3: TT Model Simulation for Circuit Shown in Figure 1

We find that through corner analysis that the circuit functions as expected and similarly to what is shown in the figure above under all edge case considerations. Figures showing each of the corner case results can be seen at the following link https://github.com/ThomasJagielski/MADVLSI-MP2/tree/main/images/final_schematic_simulations.

3.2.1 Simulation with All Strength 1 Transistors

We will find that under the TT model, a circuit configuration with all transistors being strength 1 works as we expect. The output waveform for this model is shown below.

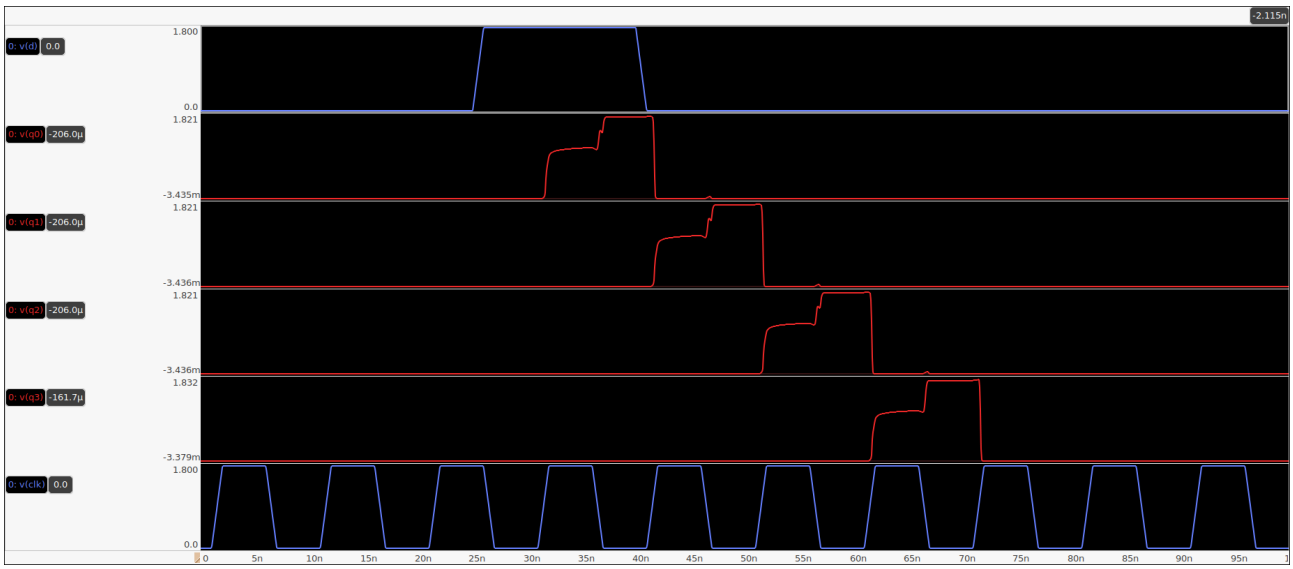

Figure 4: TT Model Simulation Strength Ratio 1 Transistors

However, we will find that through corner analysis this circuit does not function as expected using the SF and SS models. The output waveform shown below demonstrates the write-ability issue mentioned by Sivilotti with the SS models,

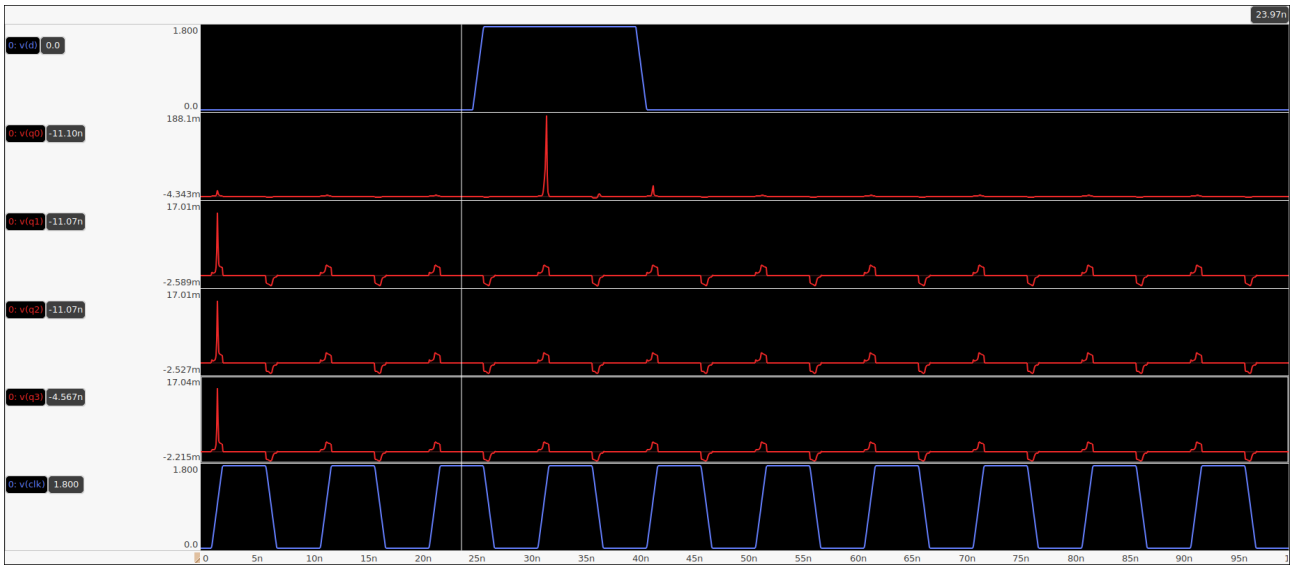

Figure 5: SS Model Simulation Strength Ratio 1 Transistors

For the output waveforms in each of the cases please refer to the following link, https://github.com/ThomasJagielski/MADVLSI-MP2/tree/main/images/width_1_simulations.

As a result of the write-ability issue demonstrated above, the pass transistors were sized with a strength ratio of $\frac{1}{2}$ transistors to ensure robust designs that are run invariant.

4 Layout

4.1 Single Flip-Flop Cell

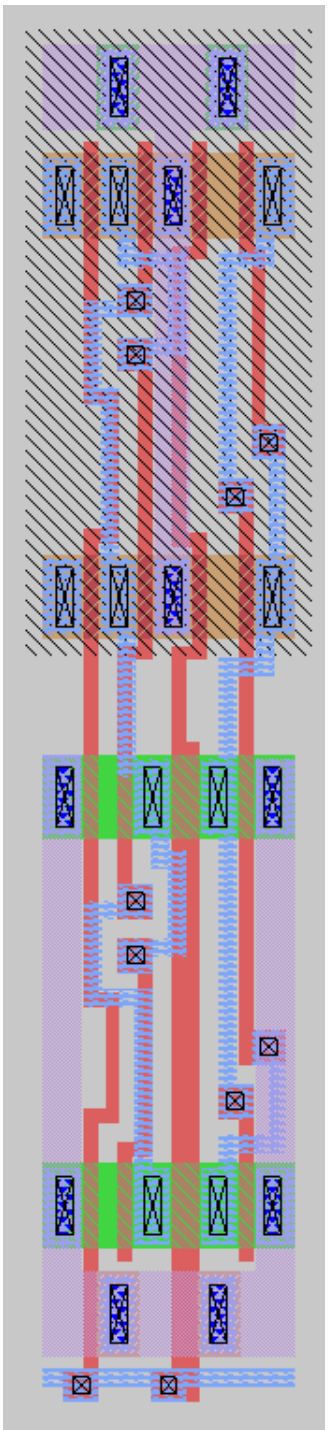

Figure 6: Single Positive Edge Triggered Flip-Flop Cell

4.2 Inverter

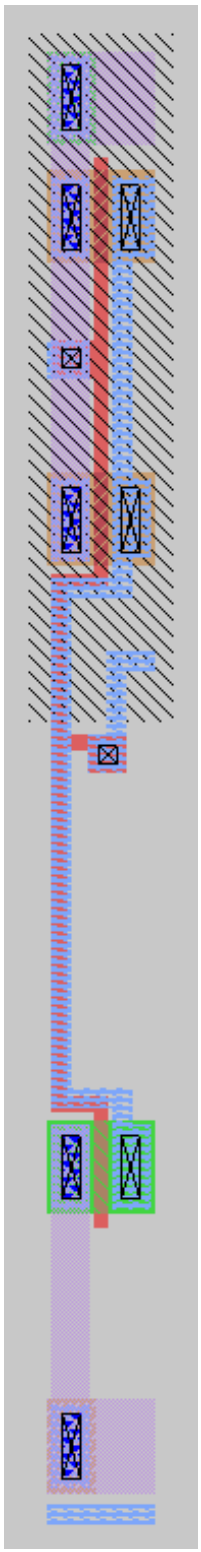

Figure 7: Inverter Cell for Dn Input from D

4.3 4-Bit Shift Register

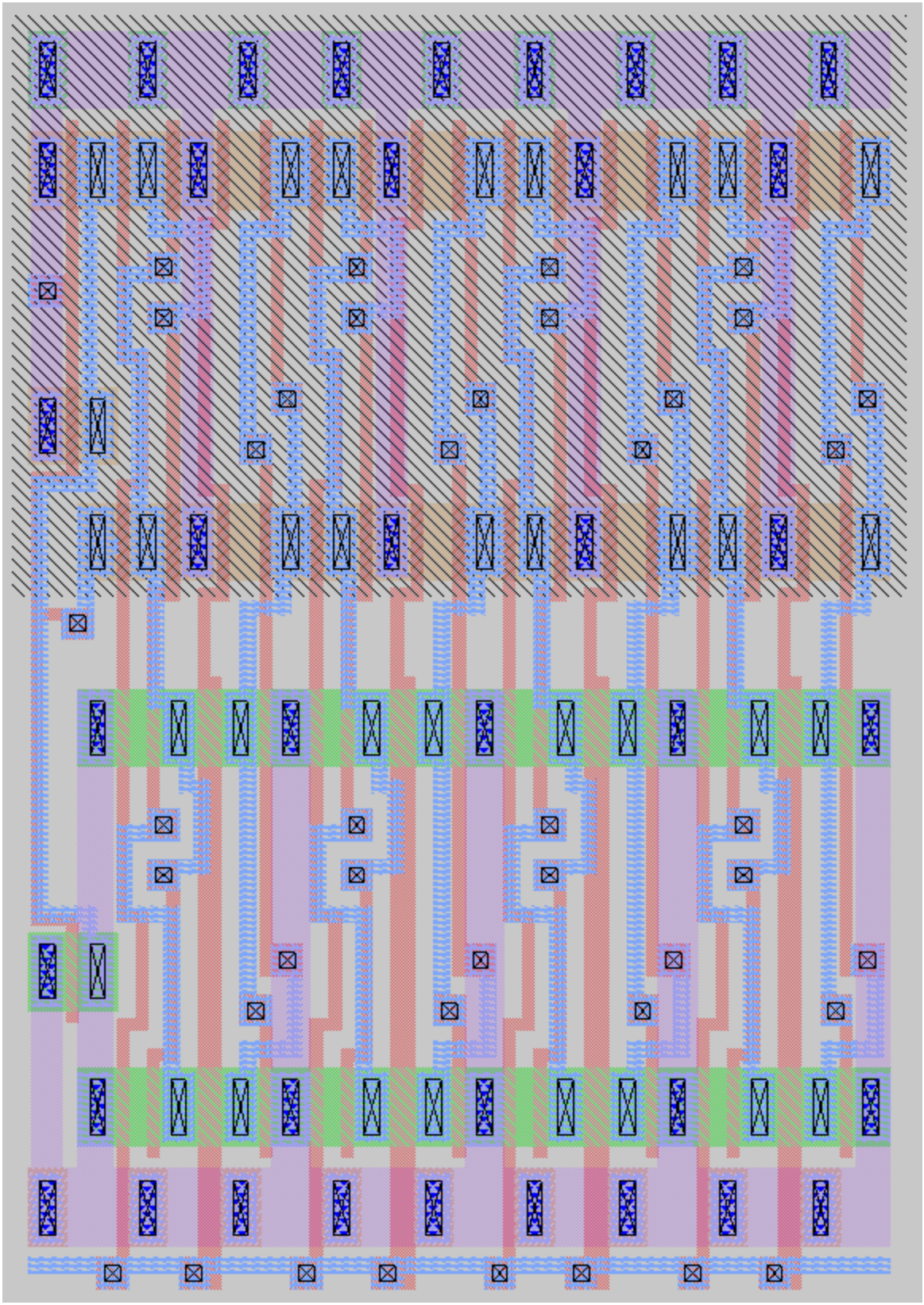

Figure 8: 4-Bit Shift Register Comprised of Latches Shown in Figure 6 and an Inverter as Shown in Figure 7

This 4-bit shift register with the inverter as an input to the Dn input has the following dimensions,

Cell Dimensions	
Width [Microns]	**Height [Microns]**
11.15	16.25.05

5 Layout Verses Schematic

The following comp.out file shows the LVS output for circuit shown in Figure 1 (schematic) and Figure 8 (layout). The "mismatches" at the top refer to the use of VP and VDD as well as VN and GND. We find at the end that when checking for net equalities the schematic and layout match.

```
Flattening unmatched subcell CSRL_D_FF in circuit shift_register_xschem_lvs.spice (0)(4 instances)
Flattening unmatched subcell D_latch in circuit shift_register.spice (1)(4 instances)
Equate elements:  no current cell.
Equate elements:  no current cell.

Cell inverter disconnected node: CLK
Class inverter:  Merged 1 devices.

Cell inverter disconnected node: CLK

Subcircuit summary:
Circuit 1: inverter                        |Circuit 2: inverter
-------------------------------------------|-------------------------------------------

sky130_fd_pr__pfet_01v8 (1)                |sky130_fd_pr__pfet_01v8 (1)
sky130_fd_pr__nfet_01v8 (1)                |sky130_fd_pr__nfet_01v8 (1)
Number of devices: 2                       |Number of devices: 2
Number of nets: 4                          |Number of nets: 4
-----------------------------------------------------------------------------------------

Circuits match uniquely.
Netlists match uniquely.

Subcircuit pins:
Circuit 1: inverter                        |Circuit 2: inverter
-------------------------------------------|-------------------------------------------

Y                                          |Y
A                                          |A
VDD                                        |VP **Mismatch**
GND                                        |VN **Mismatch**
(no matching pin)                          |CLK
-----------------------------------------------------------------------------------------

Cell pin lists for inverter and inverter altered to match.

Subcircuit summary:
Circuit 1: shift_register_xschem_lvs.spice |Circuit 2: shift_register.spice
-------------------------------------------|-------------------------------------------

sky130_fd_pr__pfet_01v8 (32)               |sky130_fd_pr__pfet_01v8 (32)
sky130_fd_pr__nfet_01v8 (32)               |sky130_fd_pr__nfet_01v8 (32)
inverter (1)                               |inverter (1)
Number of devices: 65                      |Number of devices: 65
Number of nets: 37                         |Number of nets: 37
```

```
--------------------------------------------------------------------------------

Circuits match uniquely.
Netlists match uniquely.
Cells have no pins;  pin matching not needed.
Device classes shift_register_xschem_lvs.spice and shift_register.spice are
   equivalent.
Circuits match uniquely.
```