

MADVLSI: Miniproject 2

Thomas Jagielski

February 2021

1 Design Files

GitHub link to design files: <https://github.com/ThomasJagielski/MADVLSI-MP2>.

2 Schematic

For this miniproject two conditions were considered. The first used transistors all with strength 1, and the second used strength 2 transistors in the pull down network. As shown in the simulation results section later, the strength 1 transistor circuit does not propagate the signal through the shift register properly. Thus, as discussed by Massimo Antonio Sivilotti in *Wiring Considerations in Analog VLSI Systems, with Application to Field-Programmable Networks*, the write-ability problem is present under slow transistor conditions. As a result, transistors with strength 2 in the pull down network were used in the design for increased robustness, as demonstrated through corner analysis in the simulation section. Unless indicated otherwise, the circuit being shown uses pull-down transistors of strength 2 as shown in Figure 1.

The following image shows a layout driven schematic for the CSRL positive-edge triggered D flip-flop with a ratio of 2 between the strength of the pull down transistors and the pass transistors.

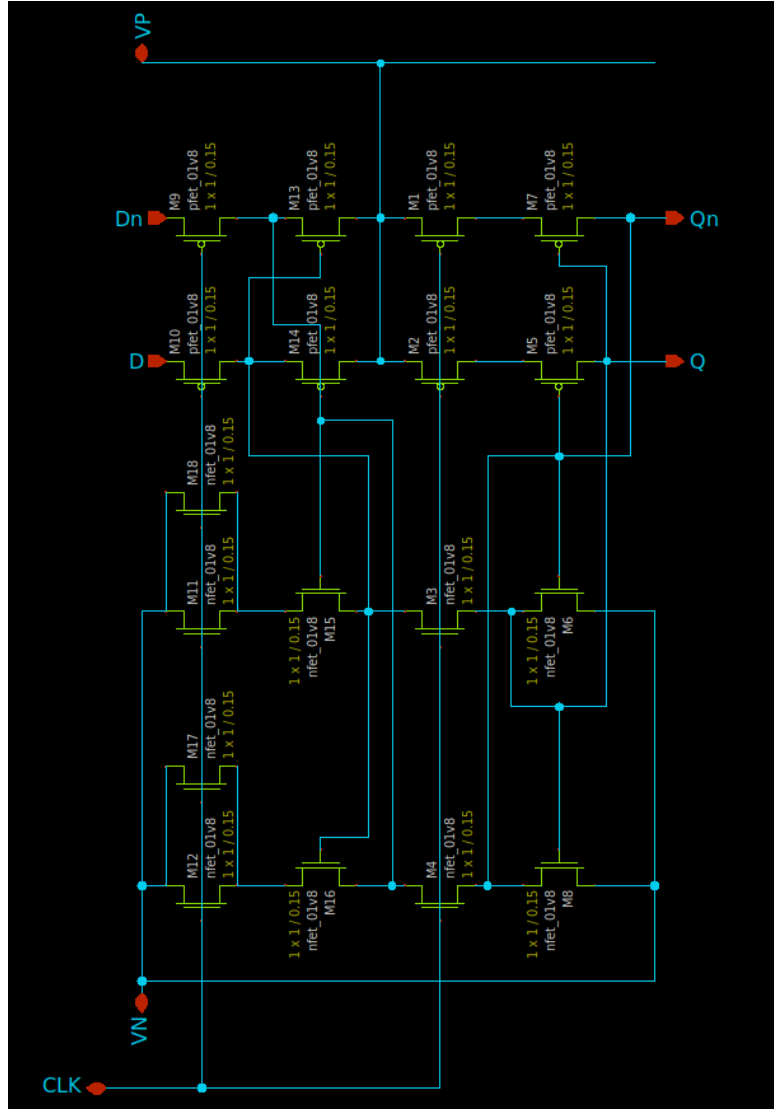


Figure 1: CSRL Positive Edge Triggered D Flip-Flop Layout Driven Schematic

3 Xschem Simulation

3.1 Schematic

The following image shows the test schematic and configuration used to simulate the circuit's function.

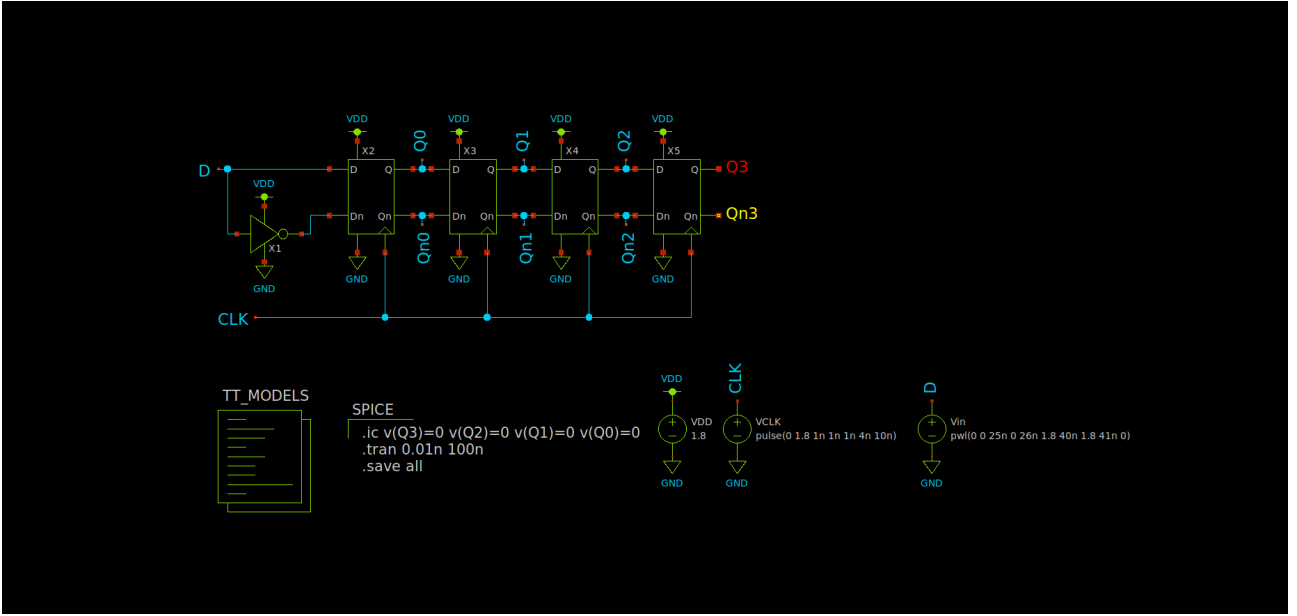


Figure 2: Simulation Schematic for Width 1 and Width 2 Cases

3.2 Simulation Results

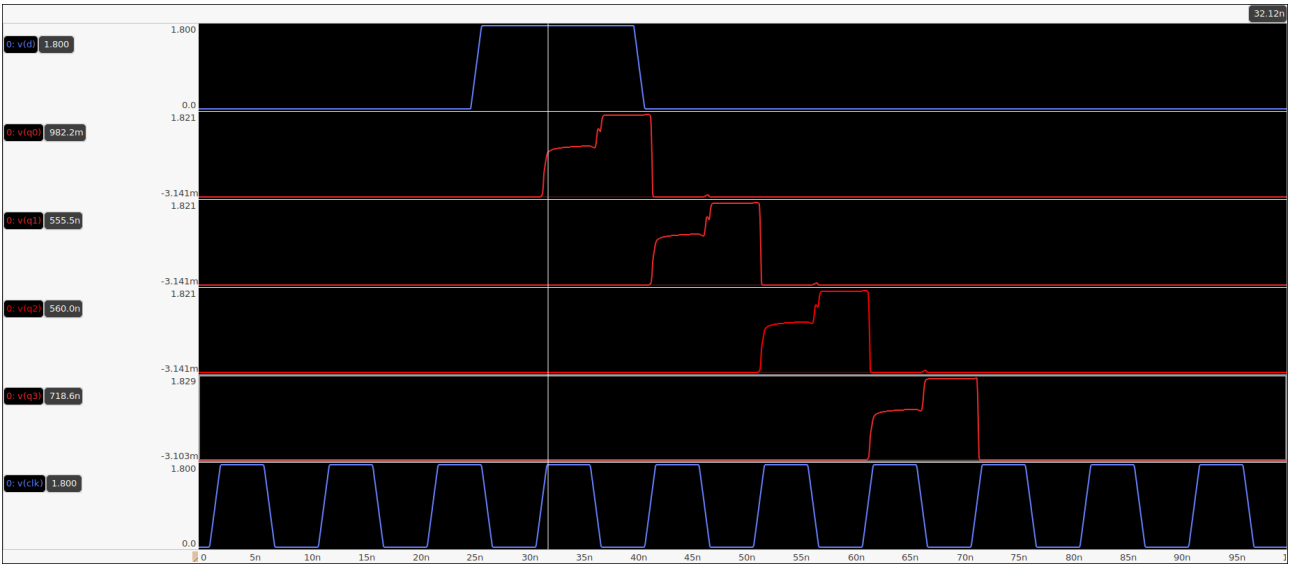


Figure 3: TT Model Simulation for Circuit Shown in Figure 1

We find that through corner analysis that the circuit functions as expected and similarly to what is shown in the figure above under all edge case considerations. Figures showing each of the corner case results can be seen at the following link https://github.com/ThomasJagielski/MADVLSI-MP2/tree/main/images/width_2_simulations.

3.2.1 Simulation with All Strength 1 Transistors

We will find that under the TT model, a circuit configuration with all transistors being strength 1 works as we expect. The output waveform for this model is shown below.

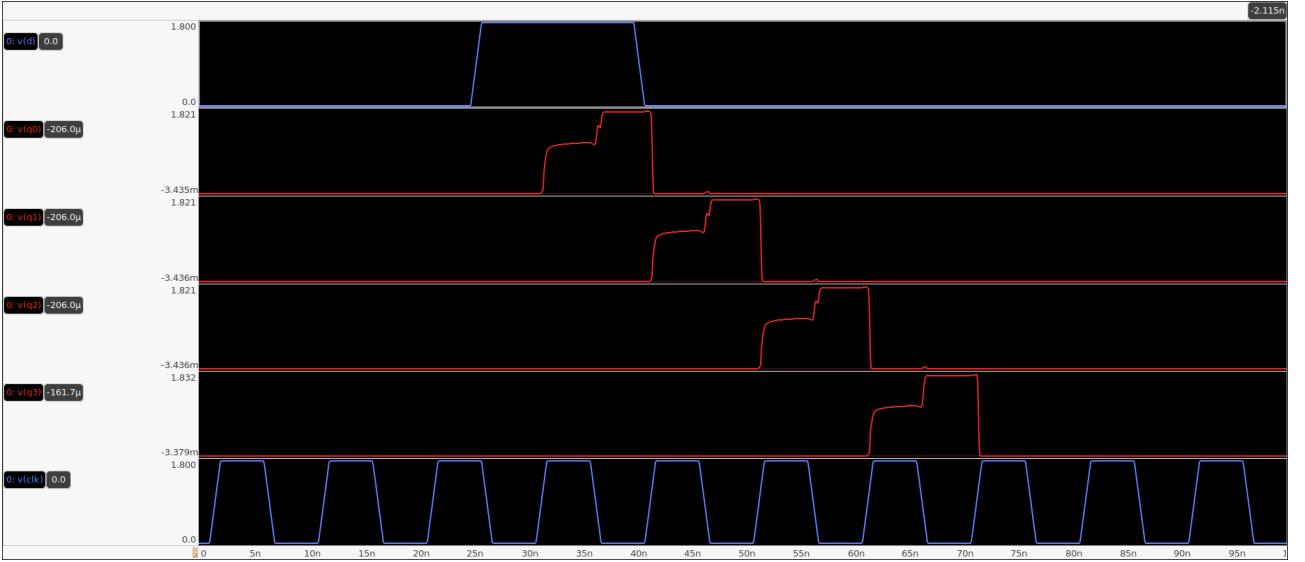


Figure 4: TT Model Simulation Strength Ratio 1 Transistors

However, we will find that through corner analysis this circuit does not function as expected using the SF and SS models. The output waveform shown below demonstrates the write-ability issue mentioned by Sivilotti with the SS models,

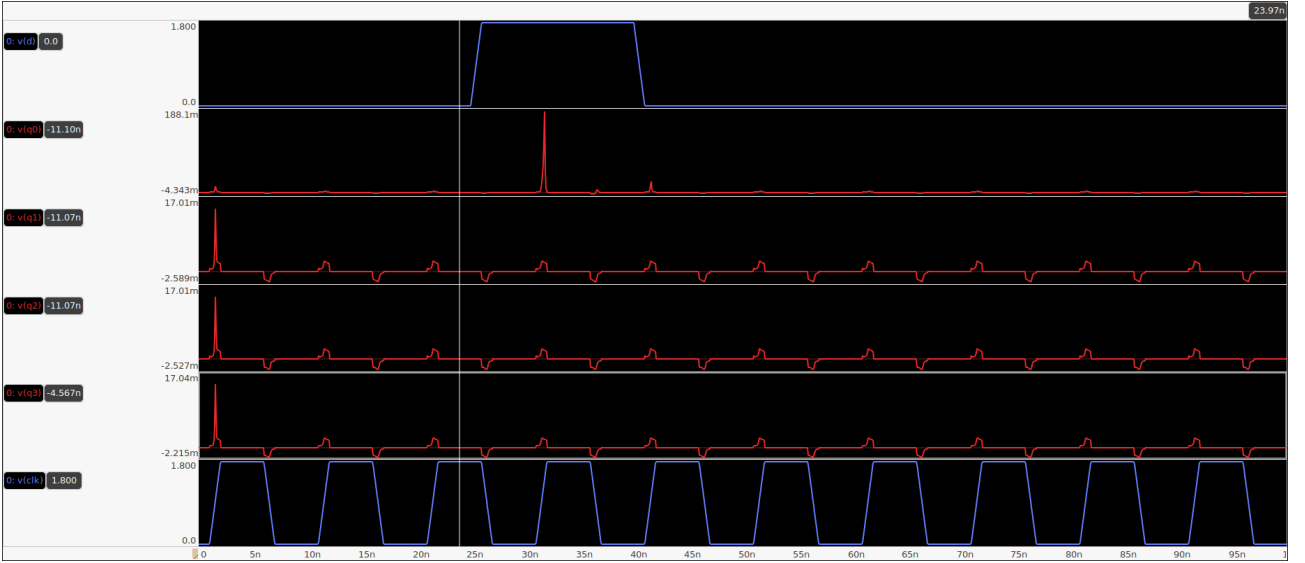


Figure 5: SS Model Simulation Strength Ratio 1 Transistors

For the output waveforms in each of the cases please refer to the following link, https://github.com/ThomasJagielski/MADVLSI-MP2/tree/main/images/width_1_simulations.

As a result of the write-ability issue demonstrated above, the pull down network was sized with a strength ratio of 2 transistors to ensure robust designs that are run invariant.

4 Layout

4.1 Single Flip-Flop Cell

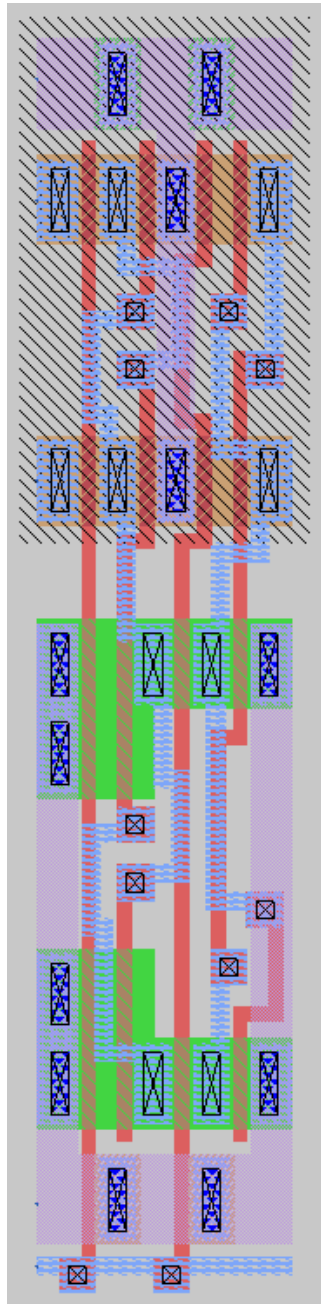


Figure 6: Single Positive Edge Triggered Flip-Flop Cell

4.2 Inverter

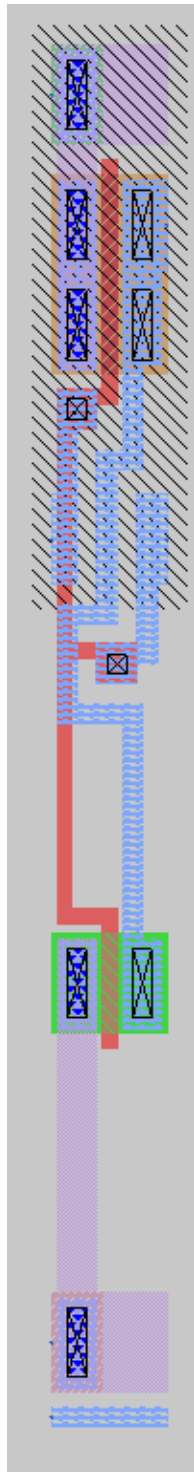


Figure 7: Inverter Cell for Dn Input from D

4.3 4-Bit Shift Register

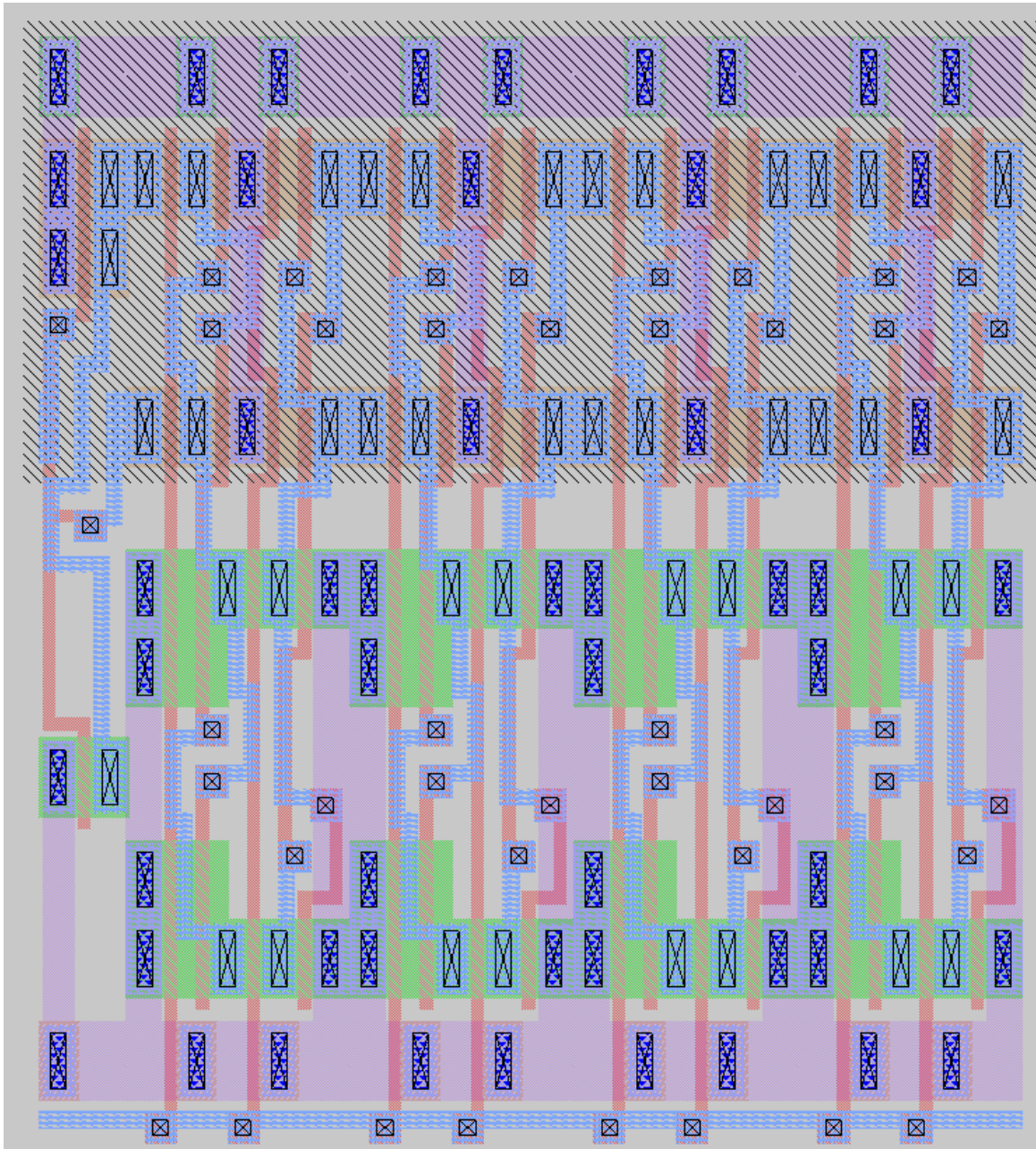


Figure 8: 4-Bit Shift Register Comprised of Latches Shown in Figure 6 and an Inverter as Shown in Figure 7

Cell Dimensions		
Case	Width [Microns]	Height [Microns]
Without Inverter	11.40	14.05
With Inverter	12.50	14.05

5 Layout Verses Schematic

The following comp.out file shows the LVS output for the width 2 pull-down transistor schematic and layout. The “mismatches” at the top refer to the use of VP and VDD as well as VN and GND. We find at the end that when checking for net equalities the schematic and layout match.

```

1 Equate elements:  no current cell.
2 Equate elements:  no current cell.
3
4 Cell inverter disconnected node: CLK
5
6 Subcircuit summary:
7 Circuit 1: inverter                      |Circuit 2: inverter
8 -----|-----
9 sky130_fd_pr__pfet_01v8 (1)             |sky130_fd_pr__pfet_01v8 (1)
10 sky130_fd_pr__nfet_01v8 (1)            |sky130_fd_pr__nfet_01v8 (1)
11 Number of devices: 2                    |Number of devices: 2
12 Number of nets: 4                      |Number of nets: 4
13 -----|-----
14 Circuits match uniquely.
15 Netlists match uniquely.
16
17 Subcircuit pins:
18 Circuit 1: inverter                      |Circuit 2: inverter
19 -----|-----
20 Y                                         |Y
21 A                                         |A
22 VP                                       |VDD **Mismatch**
23 VN                                       |GND **Mismatch**
24 -----|-----
25 Cell pin lists are equivalent.
26 Device classes inverter and inverter are equivalent.
27 Class CSRL_D_FF:  Merged 2 devices.
28
29 Subcircuit summary:
30 Circuit 1: CSRL_D_FF                    |Circuit 2: CSRL_D_FF
31 -----|-----
32 sky130_fd_pr__pfet_01v8 (8)             |sky130_fd_pr__pfet_01v8 (8)
33 sky130_fd_pr__nfet_01v8 (8)            |sky130_fd_pr__nfet_01v8 (8)
34 Number of devices: 16                    |Number of devices: 16
35 Number of nets: 13 **Mismatch**         |Number of nets: 15 **Mismatch**
36 -----|-----
37 NET mismatches: Class fragments follow (with fanout counts):
38 Circuit 1: CSRL_D_FF                    |Circuit 2: CSRL_D_FF
39 -----|-----
40 -----|-----
41 Net: CLK                                |Net: CLK
42   sky130_fd_pr__nfet_01v8/2 = 4         |   sky130_fd_pr__pfet_01v8/2 = 4
43   sky130_fd_pr__pfet_01v8/2 = 4         |   sky130_fd_pr__nfet_01v8/2 = 4
44                                           |
45 (no matching net)                       |Net: VDD
46                                           |   sky130_fd_pr__pfet_01v8/4 = 8
47                                           |
48 (no matching net)                       |Net: GND
49                                           |   sky130_fd_pr__nfet_01v8/4 = 8
50 -----|-----
51

```



```

52 -----
53 (no matching net) | Net: VN
54 | sky130_fd_pr__nfet_01v8/(1|3)
55 |
56 (no matching net) | Net: VP
57 | sky130_fd_pr__pfet_01v8/(1|3)
58 |
59 -----
60 -----
61 Net: D | (no matching net)
62 sky130_fd_pr__pfet_01v8/(1|3) = 1 |
63 |
64 Net: Dn | (no matching net)
65 sky130_fd_pr__pfet_01v8/(1|3) = 1 |
66 -----
67 -----
68 -----
69 (no matching net) | Net: Dn
70 | sky130_fd_pr__pfet_01v8/(1|3)
71 |
72 (no matching net) | Net: D
73 | sky130_fd_pr__pfet_01v8/(1|3)
74 |
75 -----
76 -----
77 Net: a_30_1320# | (no matching net)
78 sky130_fd_pr__nfet_01v8/(1|3) = 2 |
79 sky130_fd_pr__pfet_01v8/2 = 1 |
80 sky130_fd_pr__pfet_01v8/(1|3) = 2 |
81 sky130_fd_pr__nfet_01v8/2 = 1 |
82 |
83 Net: a_30_1950# | (no matching net)
84 sky130_fd_pr__pfet_01v8/(1|3) = 2 |
85 sky130_fd_pr__pfet_01v8/2 = 1 |
86 sky130_fd_pr__nfet_01v8/(1|3) = 2 |
87 sky130_fd_pr__nfet_01v8/2 = 1 |
88 -----
89 -----
90 -----
91 (no matching net) | Net: net3
92 | sky130_fd_pr__nfet_01v8/(1|3)
93 | sky130_fd_pr__pfet_01v8/(1|3)
94 | sky130_fd_pr__pfet_01v8/2 = 1
95 | sky130_fd_pr__nfet_01v8/2 = 1
96 |

```

```

97 (no matching net) | Net: net4
98 | sky130_fd_pr__nfet_01v8/(1|3)
99 | sky130_fd_pr__pfet_01v8/(1|3)
100 | sky130_fd_pr__pfet_01v8/2 = 1
101 | sky130_fd_pr__nfet_01v8/2 = 1
102 -----
103
104 -----
105 Net: VN | (no matching net)
106 sky130_fd_pr__nfet_01v8/4 = 8 |
107 sky130_fd_pr__nfet_01v8/(1|3) = 4 |
108 |
109 Net: VP | (no matching net)
110 sky130_fd_pr__pfet_01v8/4 = 8 |
111 sky130_fd_pr__pfet_01v8/(1|3) = 4 |
112 -----
113
114 -----
115 Net: a_290_1950# | (no matching net)
116 sky130_fd_pr__pfet_01v8/(1|3) = 2 |
117 |
118 Net: a_290_1320# | (no matching net)
119 sky130_fd_pr__pfet_01v8/(1|3) = 2 |
120 -----
121
122 -----
123 Net: a_30_710# | (no matching net)
124 sky130_fd_pr__nfet_01v8/(1|3) = 2 |
125 |
126 Net: a_30_n30# | (no matching net)
127 sky130_fd_pr__nfet_01v8/(1|3) = 2 |
128 -----
129
130 -----
131 (no matching net) | Net: net5
132 | sky130_fd_pr__pfet_01v8/(1|3)
133 |
134 (no matching net) | Net: net6
135 | sky130_fd_pr__pfet_01v8/(1|3)
136 |
137 -----
138 -----
139 (no matching net) | Net: net1
140 | sky130_fd_pr__nfet_01v8/(1|3)
141 |

```

```

142 (no matching net) |Net: net2
143 | sky130_fd_pr__nfet_01v8/(1|3)
    = 2
144 -----
145
146 -----
147 Net: Qn | (no matching net)
148 sky130_fd_pr__pfet_01v8/(1|3) = 1 |
149 sky130_fd_pr__nfet_01v8/2 = 1 |
150 sky130_fd_pr__pfet_01v8/2 = 1 |
151 sky130_fd_pr__nfet_01v8/(1|3) = 2 |
152 |
153 Net: Q | (no matching net)
154 sky130_fd_pr__pfet_01v8/2 = 1 |
155 sky130_fd_pr__nfet_01v8/(1|3) = 2 |
156 sky130_fd_pr__pfet_01v8/(1|3) = 1 |
157 sky130_fd_pr__nfet_01v8/2 = 1 |
158 -----
159
160 -----
161 (no matching net) |Net: Q
162 | sky130_fd_pr__nfet_01v8/(1|3)
    = 2
163 | sky130_fd_pr__pfet_01v8/(1|3)
    = 1
164 | sky130_fd_pr__pfet_01v8/2 = 1
165 | sky130_fd_pr__nfet_01v8/2 = 1
166 |
167 (no matching net) |Net: Qn
168 | sky130_fd_pr__nfet_01v8/(1|3)
    = 2
169 | sky130_fd_pr__pfet_01v8/2 = 1
170 | sky130_fd_pr__nfet_01v8/2 = 1
171 | sky130_fd_pr__pfet_01v8/(1|3)
    = 1
172 -----
173 DEVICE mismatches: Class fragments follow (with node fanout counts):
174 Circuit 1: CSRL_D_FF |Circuit 2: CSRL_D_FF
175
176 -----
177 Instance: sky130_fd_pr__nfet_01v83 | (no matching instance)
178 (1,3) = (12,2) |
179 2 = 8 |
180 4 = 12 |
181 |
182 |
183 Instance: sky130_fd_pr__nfet_01v85 | (no matching instance)
184 (1,3) = (12,2) |
185 2 = 8 |
186 4 = 12 |
187 |
188 -----
189

```

```

190 -----
191 Instance: sky130_fd_pr__nfet_01v81      |(no matching instance)
192   (1,3) = (6,5)                        |
193   2 = 8                                |
194   4 = 12                                |
195                                         |
196                                         |
197 Instance: sky130_fd_pr__nfet_01v811     |(no matching instance)
198   (1,3) = (6,5)                        |
199   2 = 8                                |
200   4 = 12                                |
201                                         |
202 -----
203
204 -----
205 Instance: sky130_fd_pr__nfet_01v813     |(no matching instance)
206   (1,3) = (6,2)                        |
207   2 = 6                                |
208   4 = 12                                |
209                                         |
210                                         |
211 Instance: sky130_fd_pr__nfet_01v814     |(no matching instance)
212   (1,3) = (6,2)                        |
213   2 = 6                                |
214   4 = 12                                |
215                                         |
216 -----
217
218 -----
219 Instance: sky130_fd_pr__nfet_01v86      |(no matching instance)
220   (1,3) = (12,5)                       |
221   2 = 5                                |
222   4 = 12                                |
223                                         |
224                                         |
225 Instance: sky130_fd_pr__nfet_01v815     |(no matching instance)
226   (1,3) = (12,5)                       |
227   2 = 5                                |
228   4 = 12                                |
229                                         |
230 -----
231
232 -----
233 (no matching instance)                  | Instance:
234   sky130_fd_pr__nfet_01v8M3            |   (1,3) = (6,5)
235                                         |   2 = 8
236                                         |   4 = 8
237                                         |
238                                         |
239 (no matching instance)                  | Instance:
240   sky130_fd_pr__nfet_01v8M4            |   (1,3) = (6,5)

```

```

241 | 2 = 8
242 | 4 = 8
243 |
244 -----
245
246 -----
247 (no matching instance) | Instance:
    sky130_fd_pr__nfet_01v8M6
248 | (1,3) = (5,4)
249 | 2 = 5
250 | 4 = 8
251 |
252 |
253 (no matching instance) | Instance:
    sky130_fd_pr__nfet_01v8M8
254 | (1,3) = (5,4)
255 | 2 = 5
256 | 4 = 8
257 |
258 -----
259
260 -----
261 (no matching instance) | Instance:
    sky130_fd_pr__nfet_01v8M11
262 | (1,3) = (4,2)
263 | 2 = 8
264 | 4 = 8
265 |
266 |
267 (no matching instance) | Instance:
    sky130_fd_pr__nfet_01v8M12
268 | (1,3) = (4,2)
269 | 2 = 8
270 | 4 = 8
271 |
272 -----
273
274 -----
275 (no matching instance) | Instance:
    sky130_fd_pr__nfet_01v8M15
276 | (1,3) = (6,2)
277 | 2 = 6
278 | 4 = 8
279 |
280 |
281 (no matching instance) | Instance:
    sky130_fd_pr__nfet_01v8M16
282 | (1,3) = (6,2)
283 | 2 = 6
284 | 4 = 8
285 |
286 -----
287

```

```

288 -----
289 Instance: sky130_fd_pr__pfet_01v84      |(no matching instance)
290     (1,3) = (12,2)                       |
291     2 = 8                                |
292     4 = 12                               |
293                                           |
294                                           |
295 Instance: sky130_fd_pr__pfet_01v88      |(no matching instance)
296     (1,3) = (12,2)                       |
297     2 = 8                                |
298     4 = 12                               |
299                                           |
300 -----
301
302 -----
303 Instance: sky130_fd_pr__pfet_01v80      |(no matching instance)
304     (1,3) = (5,2)                        |
305     2 = 5                                |
306     4 = 12                               |
307                                           |
308                                           |
309 Instance: sky130_fd_pr__pfet_01v89      |(no matching instance)
310     (1,3) = (5,2)                        |
311     2 = 5                                |
312     4 = 12                               |
313                                           |
314 -----
315
316 -----
317 Instance: sky130_fd_pr__pfet_01v82      |(no matching instance)
318     (1,3) = (12,6)                       |
319     2 = 6                                |
320     4 = 12                               |
321                                           |
322                                           |
323 Instance: sky130_fd_pr__pfet_01v810     |(no matching instance)
324     (1,3) = (12,6)                       |
325     2 = 6                                |
326     4 = 12                               |
327                                           |
328 -----
329
330 -----
331 Instance: sky130_fd_pr__pfet_01v87      |(no matching instance)
332     (1,3) = (6,1)                        |
333     2 = 8                                |
334     4 = 12                               |
335                                           |
336                                           |
337 Instance: sky130_fd_pr__pfet_01v812     |(no matching instance)
338     (1,3) = (6,1)                        |
339     2 = 8                                |
340     4 = 12                               |

```

```

341 |
342 -----
343
344 -----
345 (no matching instance) | Instance:
    sky130_fd_pr__pfet_01v8M1
346 | (1,3) = (4,2)
347 | 2 = 8
348 | 4 = 8
349 |
350 |
351 (no matching instance) | Instance:
    sky130_fd_pr__pfet_01v8M2
352 | (1,3) = (4,2)
353 | 2 = 8
354 | 4 = 8
355 |
356 -----
357
358 -----
359 (no matching instance) | Instance:
    sky130_fd_pr__pfet_01v8M5
360 | (1,3) = (5,2)
361 | 2 = 5
362 | 4 = 8
363 |
364 |
365 (no matching instance) | Instance:
    sky130_fd_pr__pfet_01v8M7
366 | (1,3) = (5,2)
367 | 2 = 5
368 | 4 = 8
369 |
370 -----
371
372 -----
373 (no matching instance) | Instance:
    sky130_fd_pr__pfet_01v8M9
374 | (1,3) = (6,1)
375 | 2 = 8
376 | 4 = 8
377 |
378 |
379 (no matching instance) | Instance:
    sky130_fd_pr__pfet_01v8M10
380 | (1,3) = (6,1)
381 | 2 = 8
382 | 4 = 8
383 |
384 -----
385
386 -----

```



```

387 (no matching instance) | Instance:
    sky130_fd_pr__pfet_01v8M13
388 | (1,3) = (6,4)
389 | 2 = 6
390 | 4 = 8
391 |
392 |
393 (no matching instance) | Instance:
    sky130_fd_pr__pfet_01v8M14
394 | (1,3) = (6,4)
395 | 2 = 6
396 | 4 = 8
397 |
398 -----

399 Netlists do not match.
400 Flattening non-matched subcircuits CSRL_D_FF CSRL_D_FF
401 Subcircuit summary:
402 Circuit 1: shift_register_final.spice | Circuit 2:
    shift_register_lvs_xschem.spice
403 -----|-----

404 inverter (1) | inverter (1)
405 sky130_fd_pr__pfet_01v8 (32) | sky130_fd_pr__pfet_01v8 (32)
406 sky130_fd_pr__nfet_01v8 (32) | sky130_fd_pr__nfet_01v8 (32)
407 Number of devices: 65 | Number of devices: 65
408 Number of nets: 37 | Number of nets: 37
409 -----

410 Circuits match uniquely.
411 Property errors were found.
412 Netlists match uniquely.
413 There were property errors.
414 CSRL_D_FF_3/sky130_fd_pr__nfet_01v813 vs. CSRL_D_FF5/
    sky130_fd_pr__nfet_01v8M15:
415 w circuit1: 2 circuit2: 1 (delta=66.7%, cutoff=1%)
416 CSRL_D_FF_3/sky130_fd_pr__nfet_01v814 vs. CSRL_D_FF5/
    sky130_fd_pr__nfet_01v8M16:
417 w circuit1: 2 circuit2: 1 (delta=66.7%, cutoff=1%)
418 CSRL_D_FF_2/sky130_fd_pr__nfet_01v813 vs. CSRL_D_FF4/
    sky130_fd_pr__nfet_01v8M15:
419 w circuit1: 2 circuit2: 1 (delta=66.7%, cutoff=1%)
420 CSRL_D_FF_2/sky130_fd_pr__nfet_01v814 vs. CSRL_D_FF4/
    sky130_fd_pr__nfet_01v8M16:
421 w circuit1: 2 circuit2: 1 (delta=66.7%, cutoff=1%)
422 CSRL_D_FF_1/sky130_fd_pr__nfet_01v813 vs. CSRL_D_FF3/
    sky130_fd_pr__nfet_01v8M15:
423 w circuit1: 2 circuit2: 1 (delta=66.7%, cutoff=1%)
424 CSRL_D_FF_1/sky130_fd_pr__nfet_01v814 vs. CSRL_D_FF3/
    sky130_fd_pr__nfet_01v8M16:
425 w circuit1: 2 circuit2: 1 (delta=66.7%, cutoff=1%)
426 CSRL_D_FF_0/sky130_fd_pr__nfet_01v813 vs. CSRL_D_FF2/
    sky130_fd_pr__nfet_01v8M15:
427 w circuit1: 2 circuit2: 1 (delta=66.7%, cutoff=1%)
428 CSRL_D_FF_0/sky130_fd_pr__nfet_01v814 vs. CSRL_D_FF2/
    sky130_fd_pr__nfet_01v8M16:
429 w circuit1: 2 circuit2: 1 (delta=66.7%, cutoff=1%)
430 Cells have no pins; pin matching not needed.
431 Device classes shift_register_final.spice and shift_register_lvs_xschem.
    spice are equivalent.

```

```
432 Circuits match uniquely.  
433 Property errors were found.  
434 The following cells had property errors: shift_register_final.spice
```