MADVLSI: Miniproject 3

Thomas Jagielski

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1 Design Files

GitHub link to design files: https://github.com/ThomasJagielski/MADVLSI-MP3.

- Layout = https://github.com/ThomasJagielski/MADVLSI-MP3/tree/main/layout
- Schematic = https://github.com/ThomasJagielski/MADVLSI-MP3/tree/main/schematic
- LVS = https://github.com/ThomasJagielski/MADVLSI-MP3/tree/main/LVS

2 Grook the Circuit

Please refer to the attached document at the end or at https://github.com/ThomasJagielski/MADVLSI-MP3/blob/main/Grook%20the%20Circuit%20-%20Thomas%20Jagielski.pdf.

3 Schematics

The following images show the layout-driven schematics for the differential pair with cascode transistors, the cascode bias voltage generation circuit, and the folded-cascode differential amplifier.

3.1 Cascode Differential Pair Layout-Driven Schematic

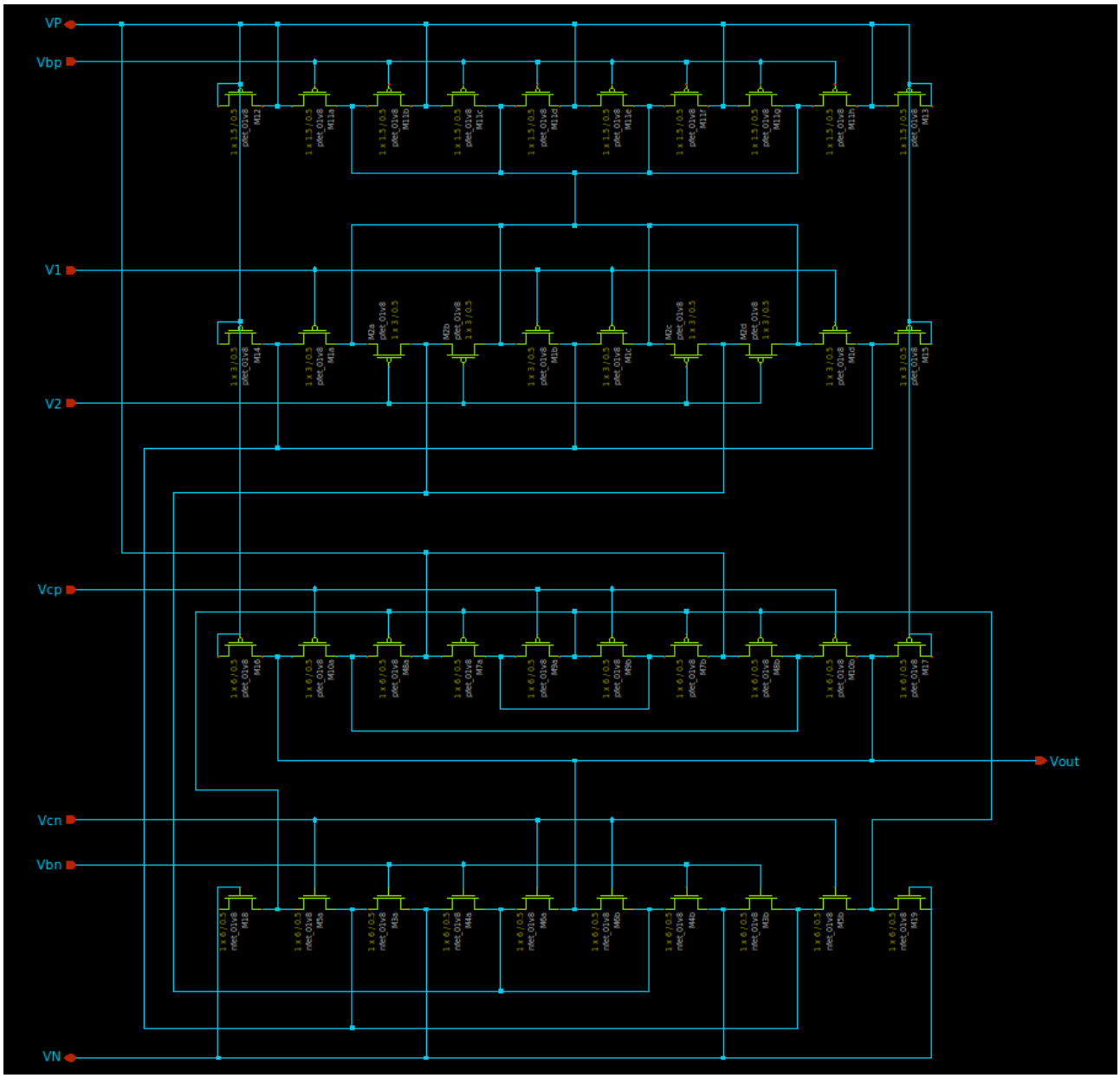


Figure 1: Layout-Driven Schematic for Cascode Differential Pair

3.2 Bias Circuit Layout-Driven Schematic

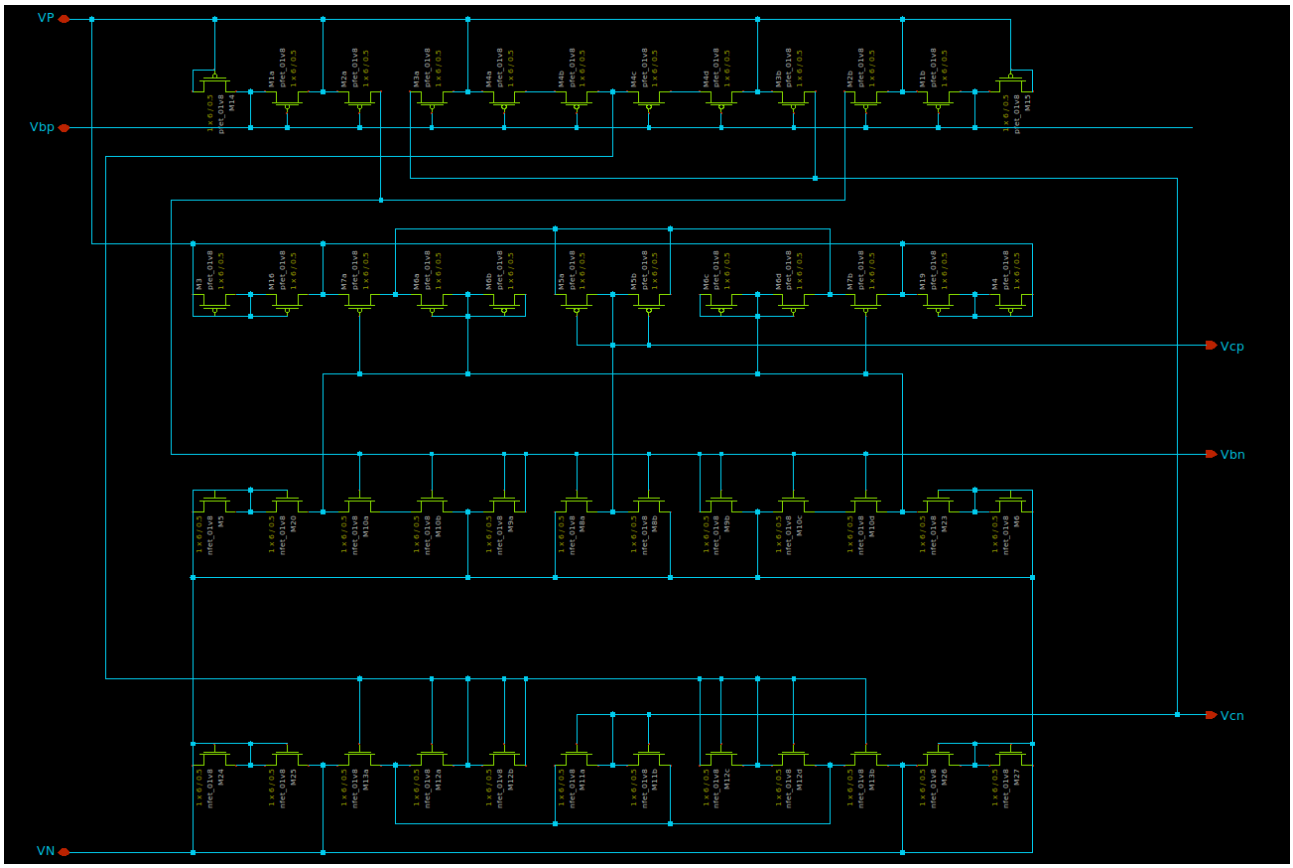


Figure 2: Layout-Driven Schematic for Cascode Transistor Biasing

3.3 Folded-Cascode Differential Pair Schematic

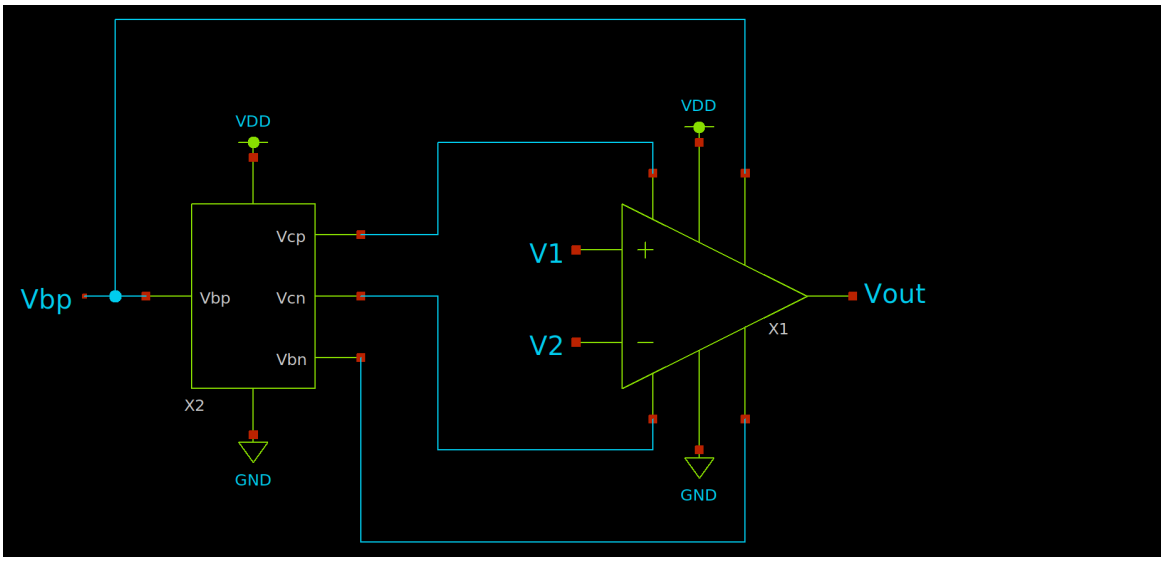


Figure 3: Layout-Driven Schematic for Folded-Cascode Differential Amplifier with Bias Circuitry

4 Xschem Simulation and Analysis

4.1 Voltage Transfer Characteristics

We first considered the voltage transfer characteristics of the amplifier. To do this, we swept noninverting input at various inverting input voltages.

4.1.1 Simulation Configuration

The following image shows the simulation configuration used to find the voltage transfer characteristics.

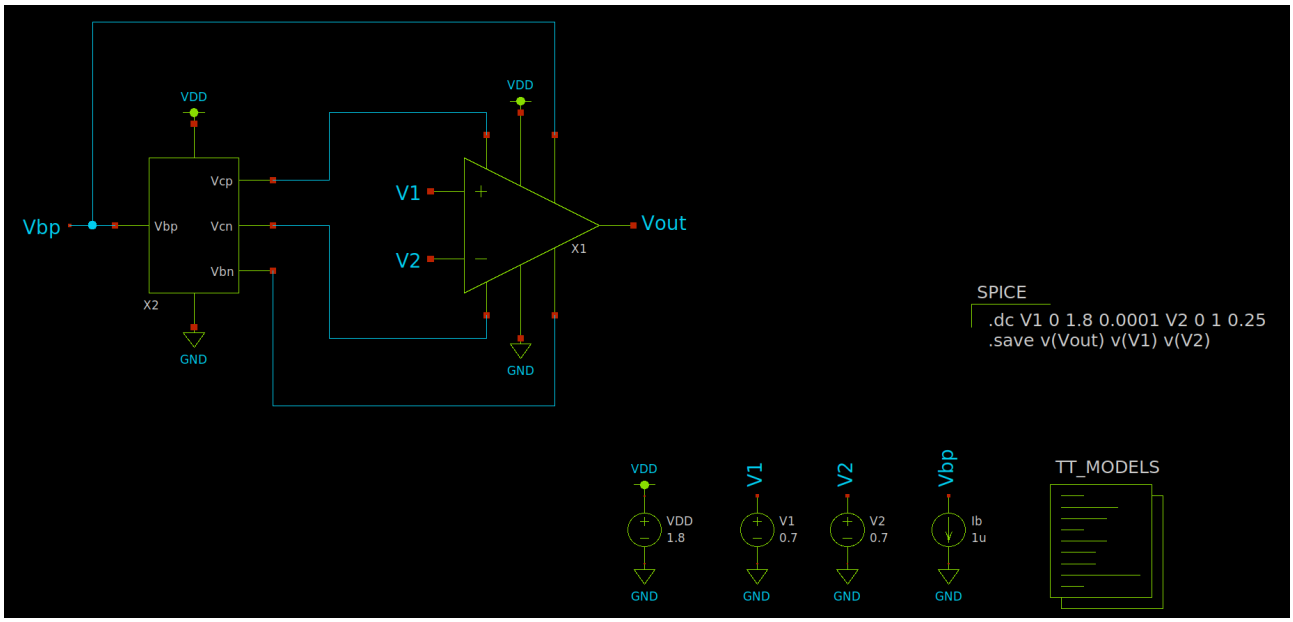


Figure 4: Configuration for Voltage Transfer Characteristics Simulation

4.1.2 Plots and Discussion

The following figure shows the simulated voltage transfer characteristics for the amplifier.

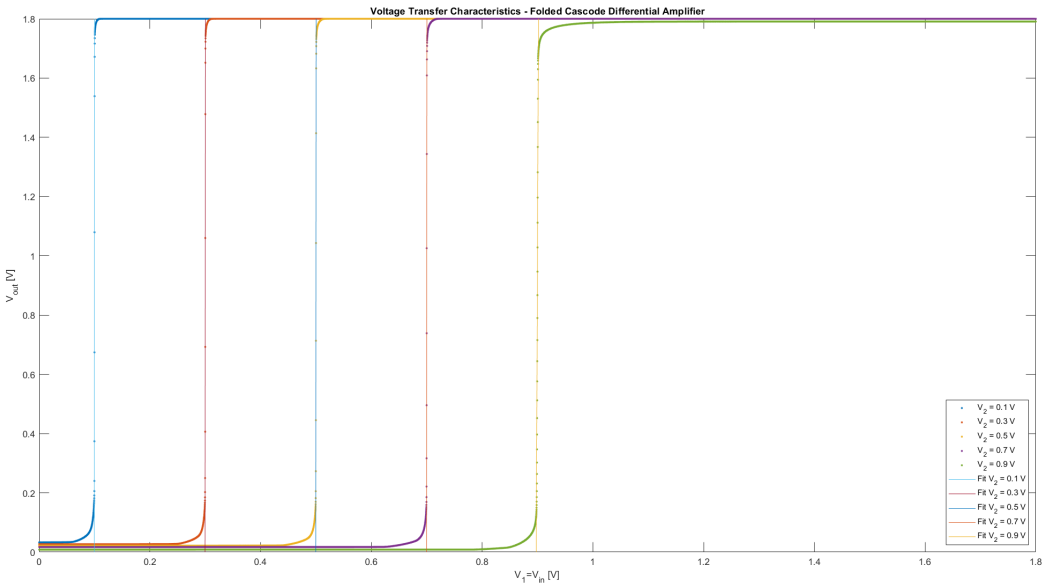


Figure 5: Voltage Transfer Characteristics for a Folded-Cascode Differential Amplifier

Fitting Data		
V_2 Value [V]	Slope of Fit	Line of Best Fit
0.1	$3.3026 * 10^3$	y = $3.3026 * 10^3 * V_{in} - 329.1507$
0.3	$2.1581 * 10^3$	y = $2.1581 * 10^3 * V_{in} - 646.4727$
0.5	$2.2351 * 10^3$	y = $2.2351 * 10^3 * V_{in} - 1.1165 * 10^3$
0.7	$1.8775 * 10^3$	y = $1.8775 * 10^3 * V_{in} - 1.3132 * 10^3$
0.9	451.3016	y = $451.3016 * V_{in} - 405.1626$

We can see that, in general, the DC gain of the circuit decreases as the common mode input increases. To consider the DC gain of the circuit in regions we would likely operate within, I averaged the gain values for when $V_2 = 0.1, 0.3, 0.5,$ and 0.7. This yields an average gain of $2.3933 * 10^3$ during DC operation of the Folded-Cascode Differential Amplifier when $V_2 \leq 0.7V$.

4.2 Voltage-to-Current Transfer Characteristics

We then found the voltage-to-current transfer characteristics. This was found by fixing the output voltage in the middle of the rails such that all of the transistors were saturated. Then the noninverting input was swept about a single value for the inverting input and the output current was measured.

4.2.1 Simulation Configuration

The following image shows the simulation configuration used.

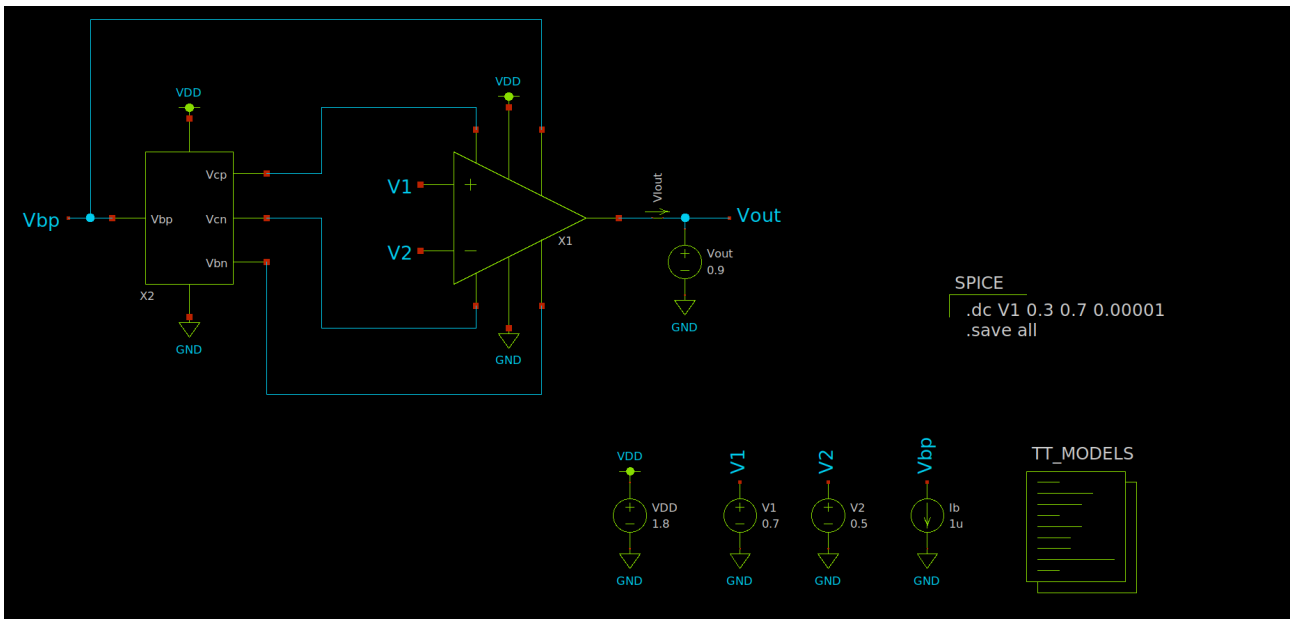


Figure 6: Configuration for Voltage-to-Current Transfer Characteristics Simulation

4.2.2 Plots and Discussion

The following image shows the simulated results for the voltage-to-current transfer characteristics.

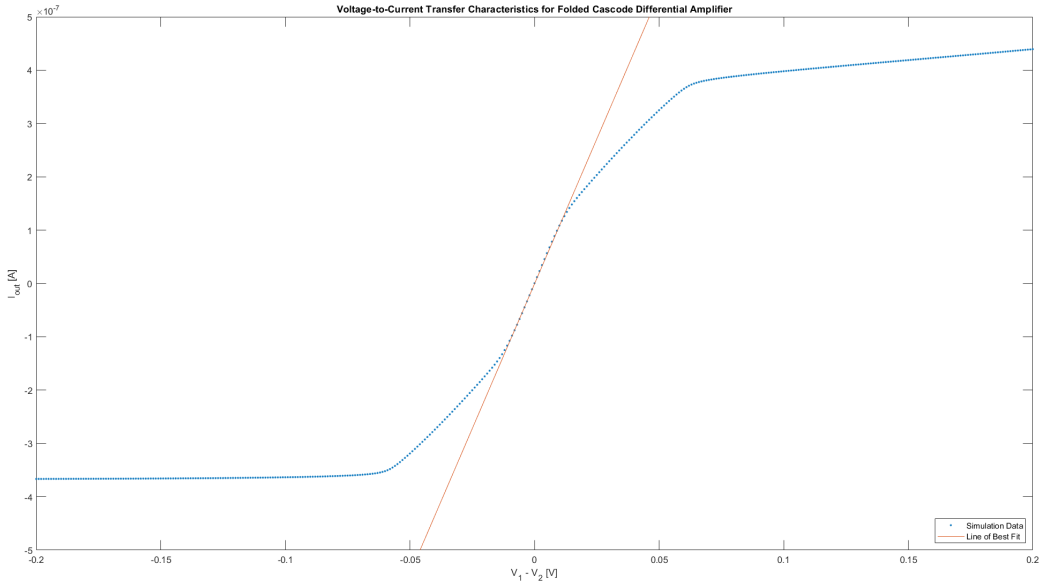


Figure 7: Voltage-to-Current Transfer Characteristics for a Folded-Cascode Differential Amplifier

The line of best fit shown in the figure above has the equation $y = 1.0868 * 10^{-5} * (V_1 - V_2) - 7.5064^{-10}$. From this, we extract the slope to be $1.0868 * 10^{-5}$ S or $\frac{A}{V}$ which represents the incremental transconductance gain of the circuit. We can further identify the limiting values of the output current to be approximately $-3.67 * 10^{-7}$ A and $4.5 * 10^{-7}$ A. The lower bound indicates the current that is pulled in from the output through the circuit, and the higher bound expresses the maximum current that can come from the circuit through the output. We will also note that there is a slight incline on the

upper-bound current limit that the lower bound does not contain, which may yield a higher maximum current level than noted above.

4.3 Loopgain

To find the loopgain of the amplifier, the Ochoa Z method was used.

4.3.1 Simulation Configuration

The following image shows the simulation configuration used.

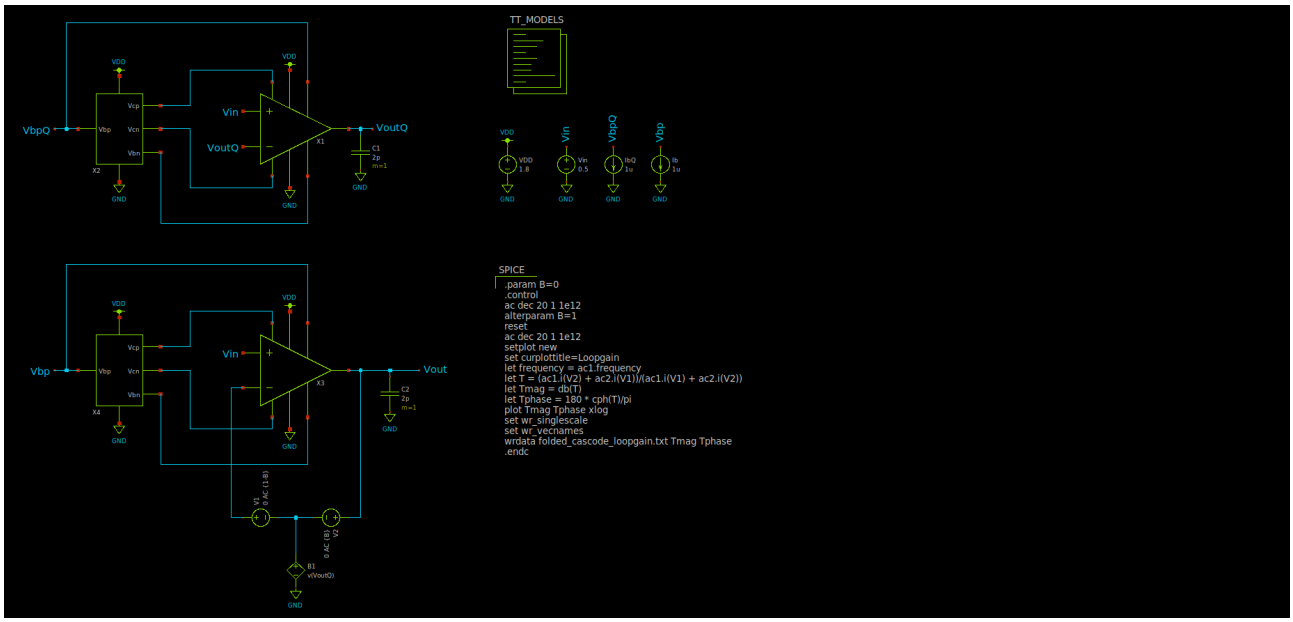


Figure 8: Configuration for Loopgain Simulation

4.3.2 Plots and Discussion

The following image shows the simulated results for the loopgain simulation.

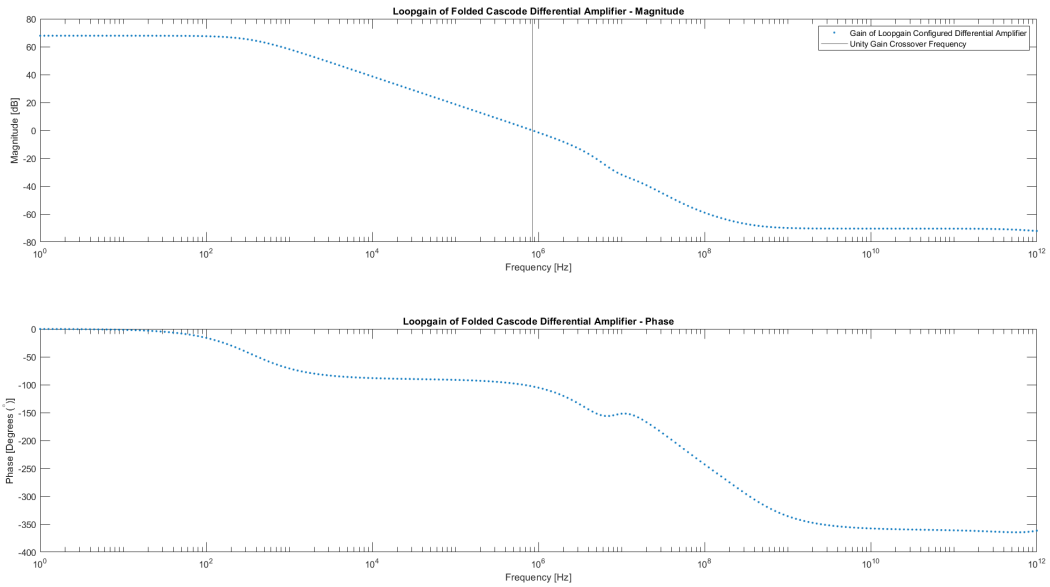


Figure 9: Loopgain Response of Folded-Cascode Differntial Amplifier

The conversion from gain to dB can be computed using the following formula,

$$dB = 20 * log(\frac{V_{out}}{V_{in}}) \tag{1}$$

We found the DC gain of the circuit to be $2.3933 * 10^3$ which is equal to 67.58 dB. The gain found in the low frequency region (1 Hz to 100 Hz) we find to be 67.878 dB. This yields an absolute percent error between the DC gain found through the voltage transfer characteristics and the loopgain simulation to be $\approx 0.5\%$.

We find the unity-gain crossover frequency to be approximately 845,480 Hz. Furthermore, we find a theoretical unity-gain crossover frequency through,

$$\text{Unity-Gain Crossover Frequency} = \frac{G_m}{C * 2\pi} \tag{2}$$

By considering the incremental transconductance gain found through the voltage-to-current characteristics, we find a theoretical unity-gain crossover frequency of 864,847 Hz. This is quite close to the experimentally found value, with an absolute percent error of 2.2% between them.

4.4 Unity-Gain Follower Frequency Response

We connected our amplifier as a unity-gain follower to consider the frequency response of the circuit.

4.4.1 Simulation Configuration

The following image shows the simulation configuration used.

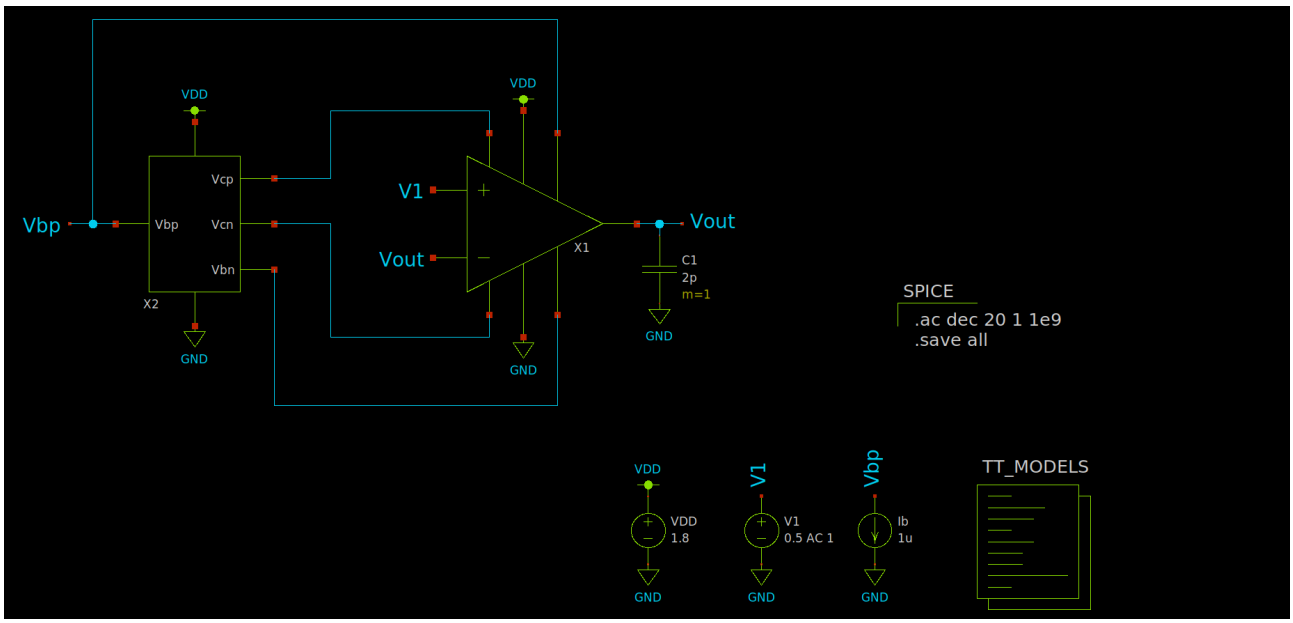


Figure 10: Configuration for Unity-Gain Simulation

4.4.2 Plots and Discussion

The following image shows the frequency response for the unity-gain follower configuration.

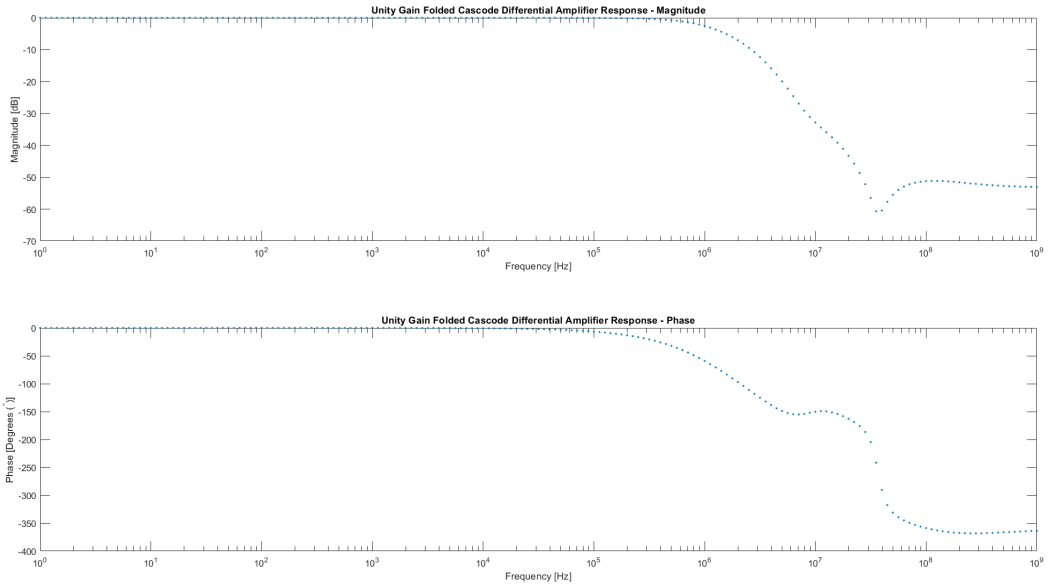


Figure 11: Unity-Gain Frequency Response

The corner frequency in the unity-gain configuration is defined as the point when the gain of the circuit reduces to -3 dB. We find that this point is at approximately 1,050,000 Hz for our circuit. Considering the unity-gain crossover frequency stated above and the corner frequency found through this simulation, we find an absolute percent error of approximately 14%.

4.5 Small-Signal Step Response

With the circuit configured as a unity-gain follower, we input a small-signal transient to find the small-signal step response.

4.5.1 Simulation Configuration

The following image shows the simulation configuration used.

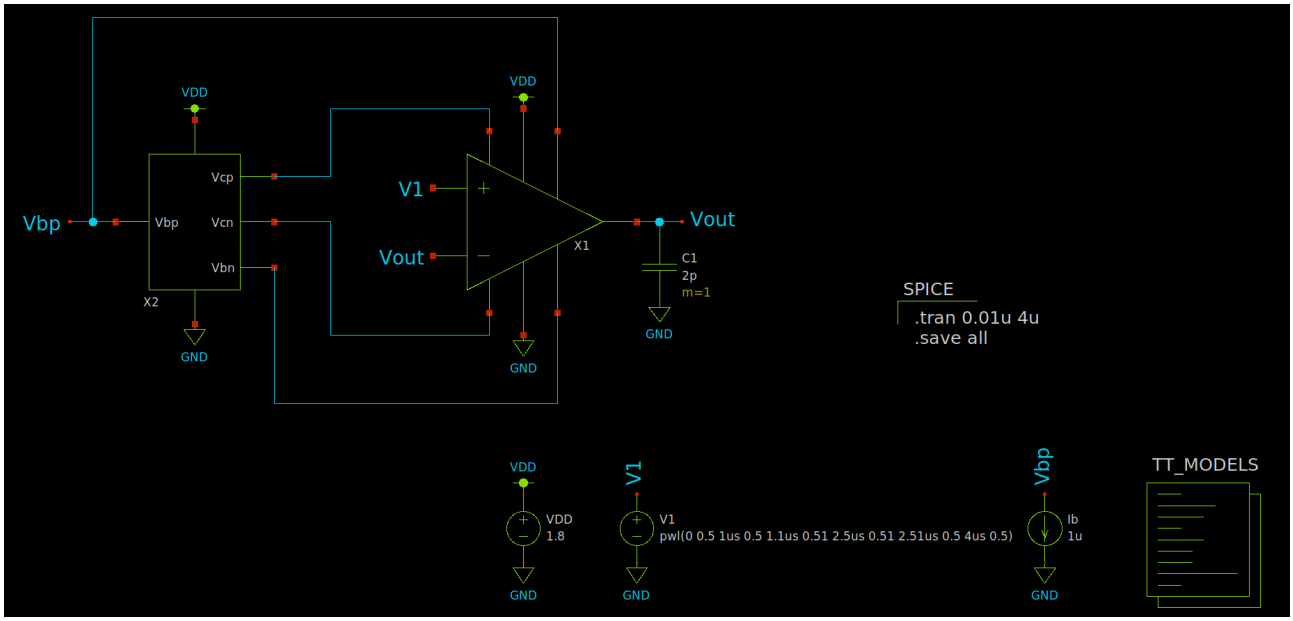


Figure 12: Configuration for Small-Signal Step Response Simulation

4.5.2 Plots and Discussion

The following image shows the up-going and down-going transient response of the amplifier for a small-signal step input.

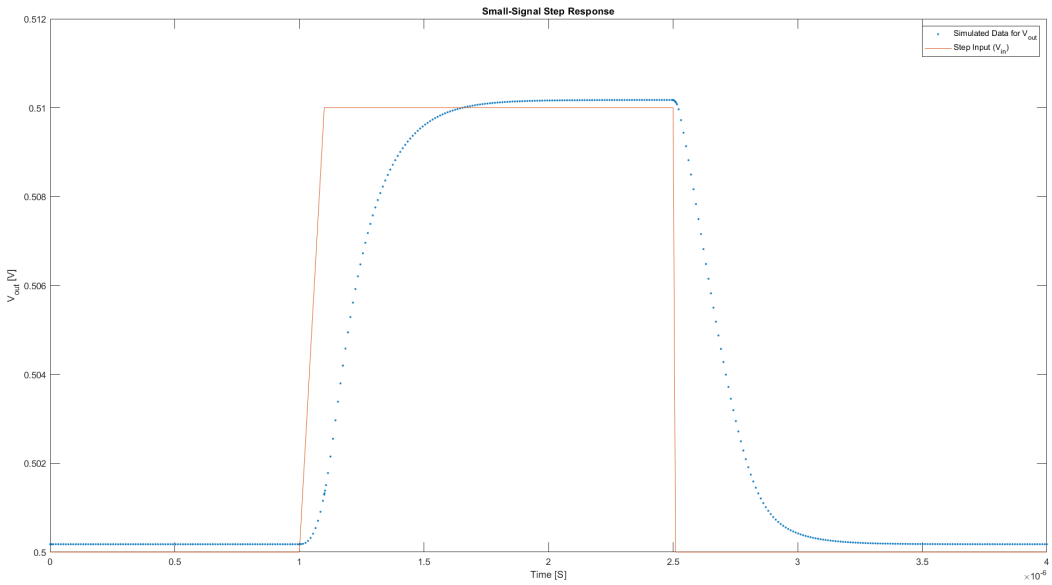


Figure 13: Small-Signal Step Response for Folded-Cascode Differential Amplifier

The following image shows the lines of best fit with the transient responses, which were used to extract the time constant for the up-going and down-going response.

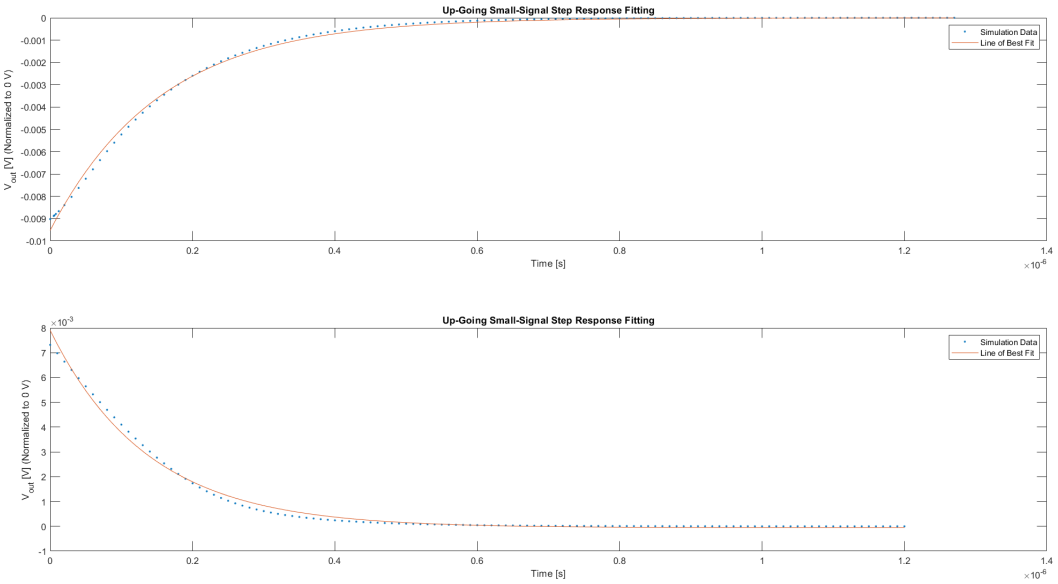


Figure 14: Small-Signal Response Up- and Down-Going Step Response Fitting

When deciding how small to make the input step, we must ensure that the differential pair transistors remain in saturation. We also must ensure that the output does not saturate such that the output voltage response does not slew in the output voltage response to a small-signal input.

We find that the up-going and down-going responses for a small-signal step change in this circuit respond symmetrically. Since the response is similar to a RC circuit (which is a linear system), we find that the amplifier exhibits linear behavior.

We find an up-going time constant to be $1.546 * 10^{-7}$ seconds and a down-going time constant $1.372 * 10^{-7}$ seconds. Between the two, there is an absolute percent error of 11.2%. This implies the values are quite similar since the time constants are on the order of $\frac{1}{10^7}$ seconds. The error can likely be accounted for through unmatched fitting ranges between the the up-going and down-going responses. Specifically, we can see that the line of best fit matches the up-going response better than the down-going response line of best fit.

Conversion from the time constant to an effective corner frequency for the circuit can be found through the following equation,

$$\text{Cutoff Frequency} = \frac{1}{\tau * 2\pi} \tag{3}$$

Thus, the corner frequency obtained from the up-going time constant is 1,029,462 Hz and the down-going time constant yields 1,160,021 Hz. These values fall on either side of the cutoff frequency obtained from the unity-gain follower frequency response as the unity-gain follower method yielded a corner frequency of 1,050,000 Hz. This results in an absolute percent error of $\sim 2\%$ and $\sim 9\%$ between the corner frequency computed with τ and the unity-gain follower extracted corner frequency for the up-going and down-going responses respectively. As stated before, the line of best fit matches the up-going response better than the down-going response, which is consistent with the difference in absolute percent errors found above.

4.6 Large-Amplitude Step Response

With the circuit configured as a unity-gain follower, we input a large-amplitude transient to find the large-amplitude step response.

4.6.1 Simulation Configuration

The following image shows the simulation configuration used.

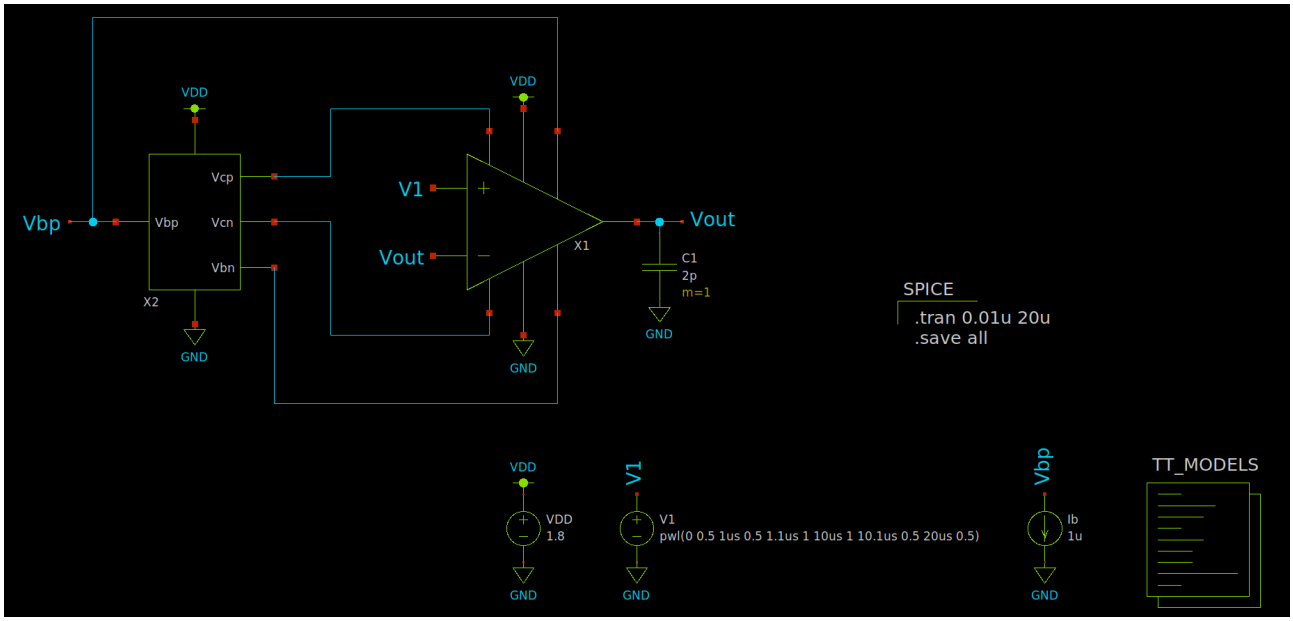


Figure 15: Configuration for Large-Amplitude Step Response Simulation

4.6.2 Plots and Discussion

The following image shows the up-going and down-going transient response of the amplifier for a large-amplitude step input.

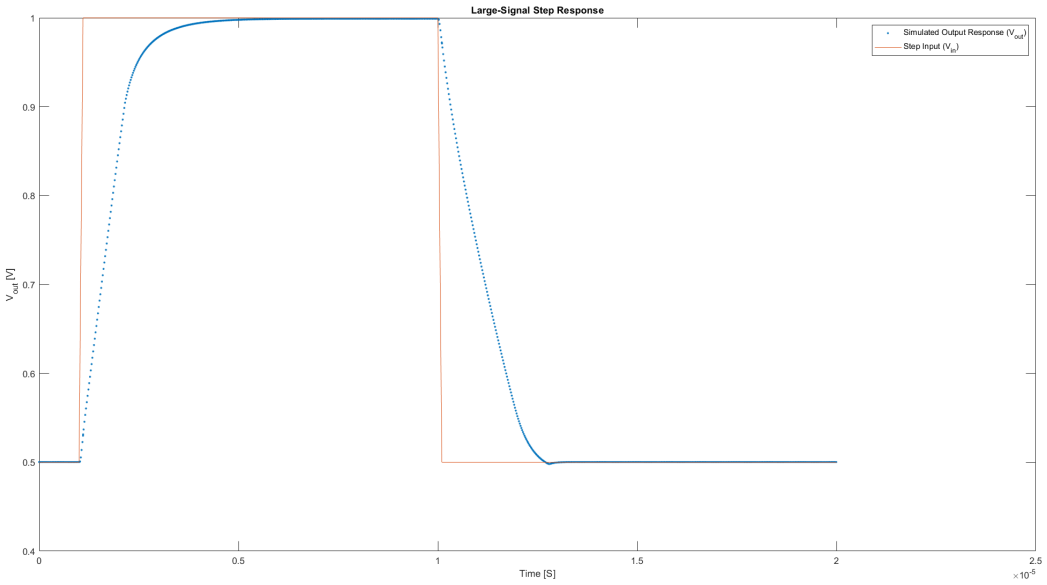


Figure 16: Large-Signal Step Response for Folded-Cascode Differential Amplifier

The following figure adds the lines of best fit used to extract the slew rates.

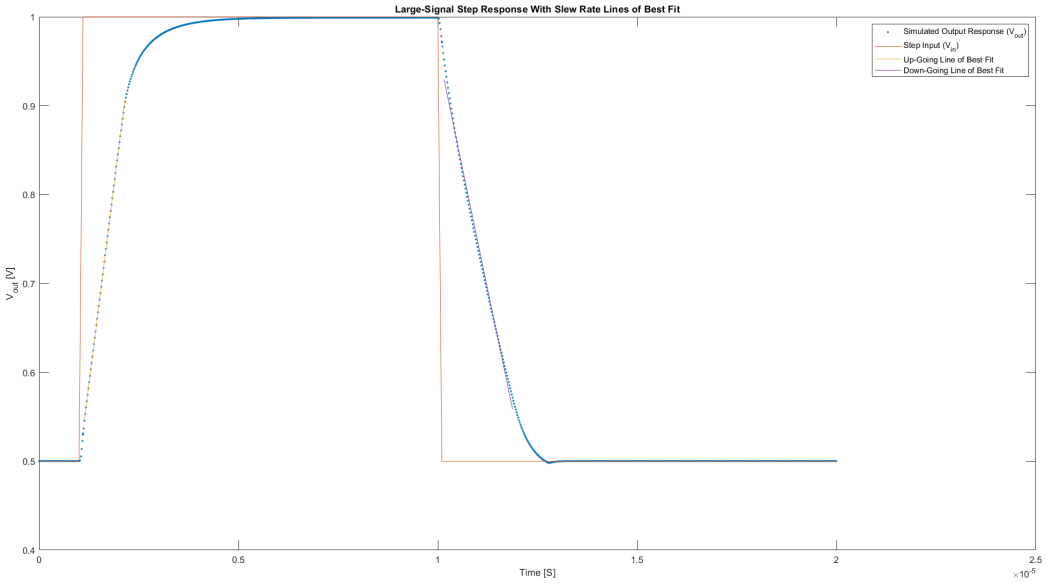


Figure 17: Large-Signal Step Response for Folded-Cascode Differential Amplifier With Slew Rate Lines of Best Fit

Considering the large-amplitude step response of the folded-cascode differential amplifier, we find that the response is not symmetric between the up-going and down-going responses. However,

they are close to symmetric. We find that the down-going response is slightly quicker and yields minimal overshoot when approaching the final value. The up-going response does not demonstrate these features.

We extract an up-going slew rate as the slope of the line of best fit to be $3.5439 * 10^5$ V/s. Similarly, we find the down-going slew rate to be $-2.1572 * 10^5$ V/s. Between both values there is an absolute percent error of 160.87%. This would indicate that the response of the system is asymmetric for the up-going and down-going response.

The expected slew rates of the circuit can be considered through the load capacitance and limiting output current values as

$$\text{Slew Rate} = \pm\frac{I_b}{C} \tag{4}$$

Thus, we find a theoretical up-going slew rate as 225,000 V/s and a theoretical down-going slew rate of -185,000 V/s. We will note that the theoretical slew rate for the up-going response is approximately 125,000 V/s lower than the extracted slew rate. This likely could be a result of the increasing output current in the voltage to current transfer characteristic plot. I used a maximum output current of $4.5 * 10^{-7}$ A; however, this current changes based on the differential between V1 and V2. The values that we find for the theoretical and extracted down-going responses are much closer, and the difference could potentially be explained by a slightly inaccurate output current level on the lower bound.

5 Layout

The following images show the layout of the Folded-Cascode Differential Amplifier.

5.1 Cascode and Differential Pair Layout

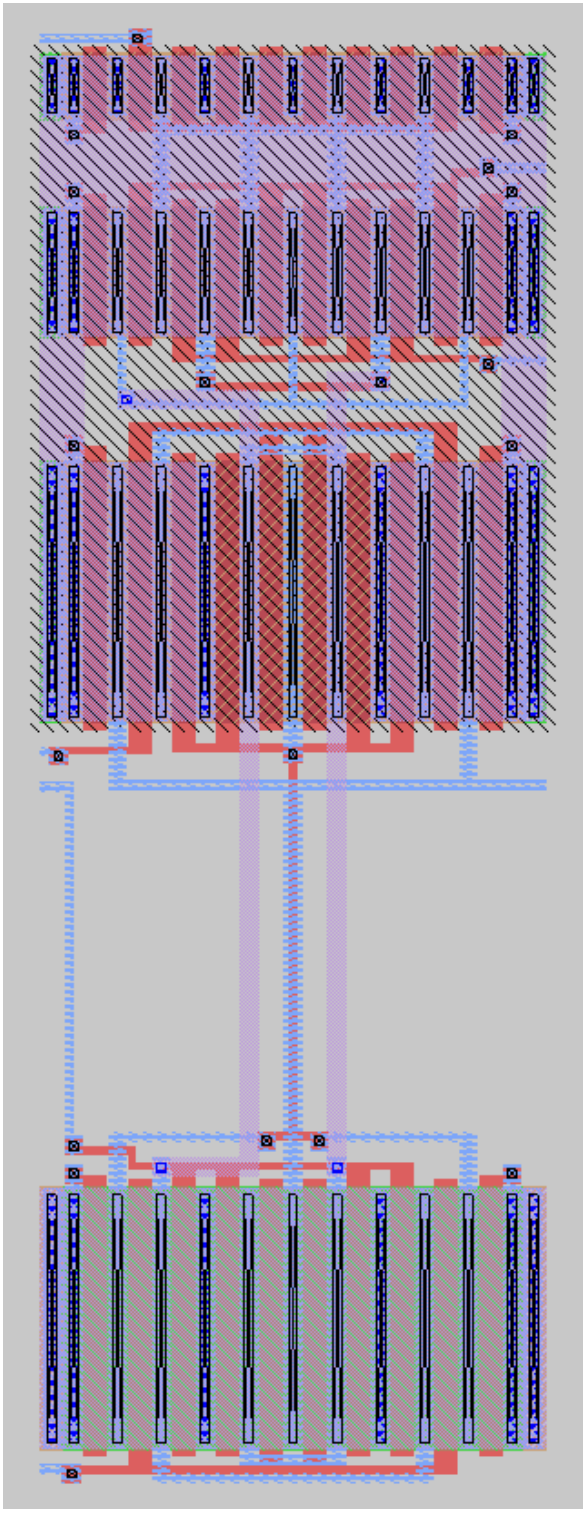


Figure 18: Cascode and Differential Pair Layout

5.2 Cascode Bias Circuit Layout

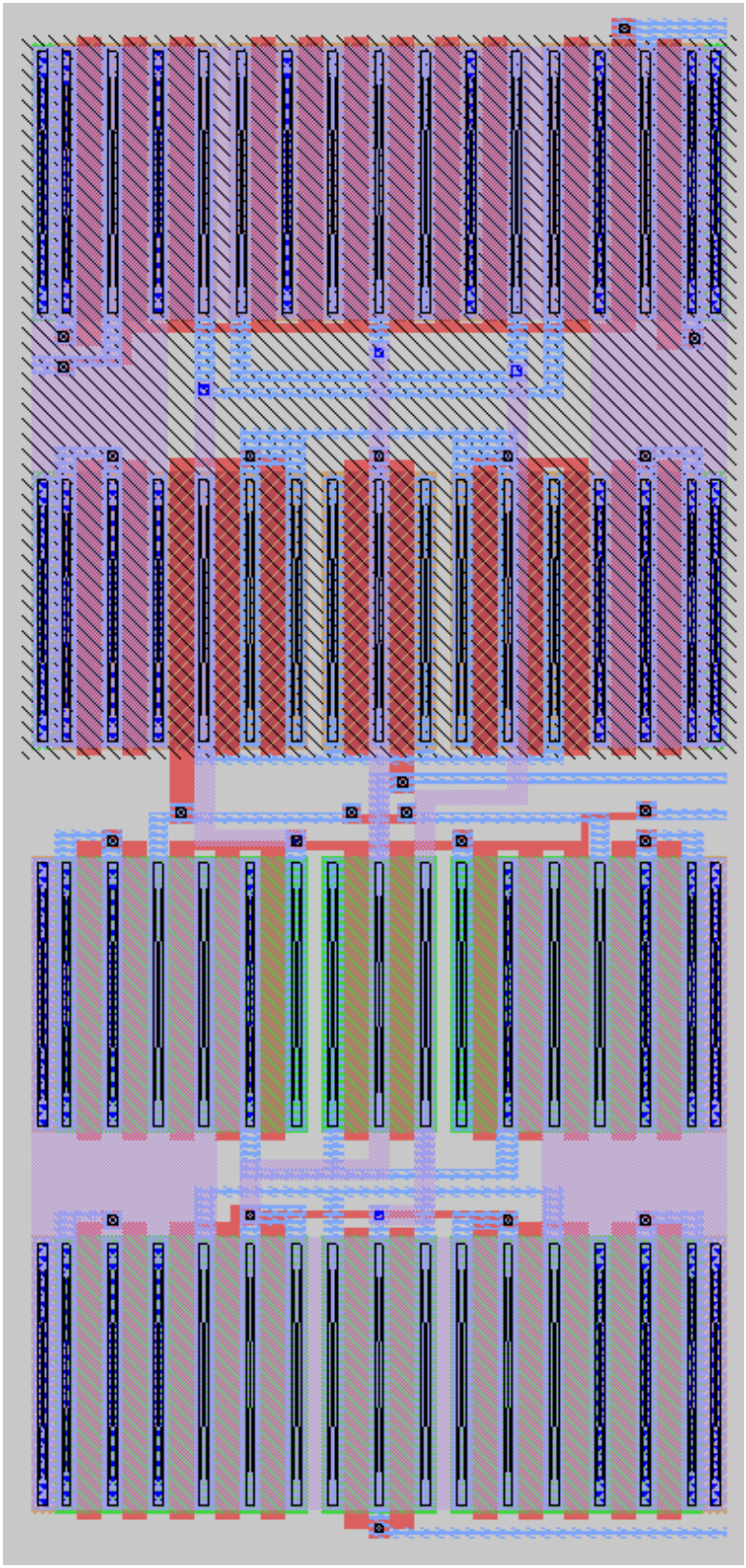


Figure 19: Cascode Bias Circuit Layout

5.3 Folded-Cascode Differential Amplifier Layout

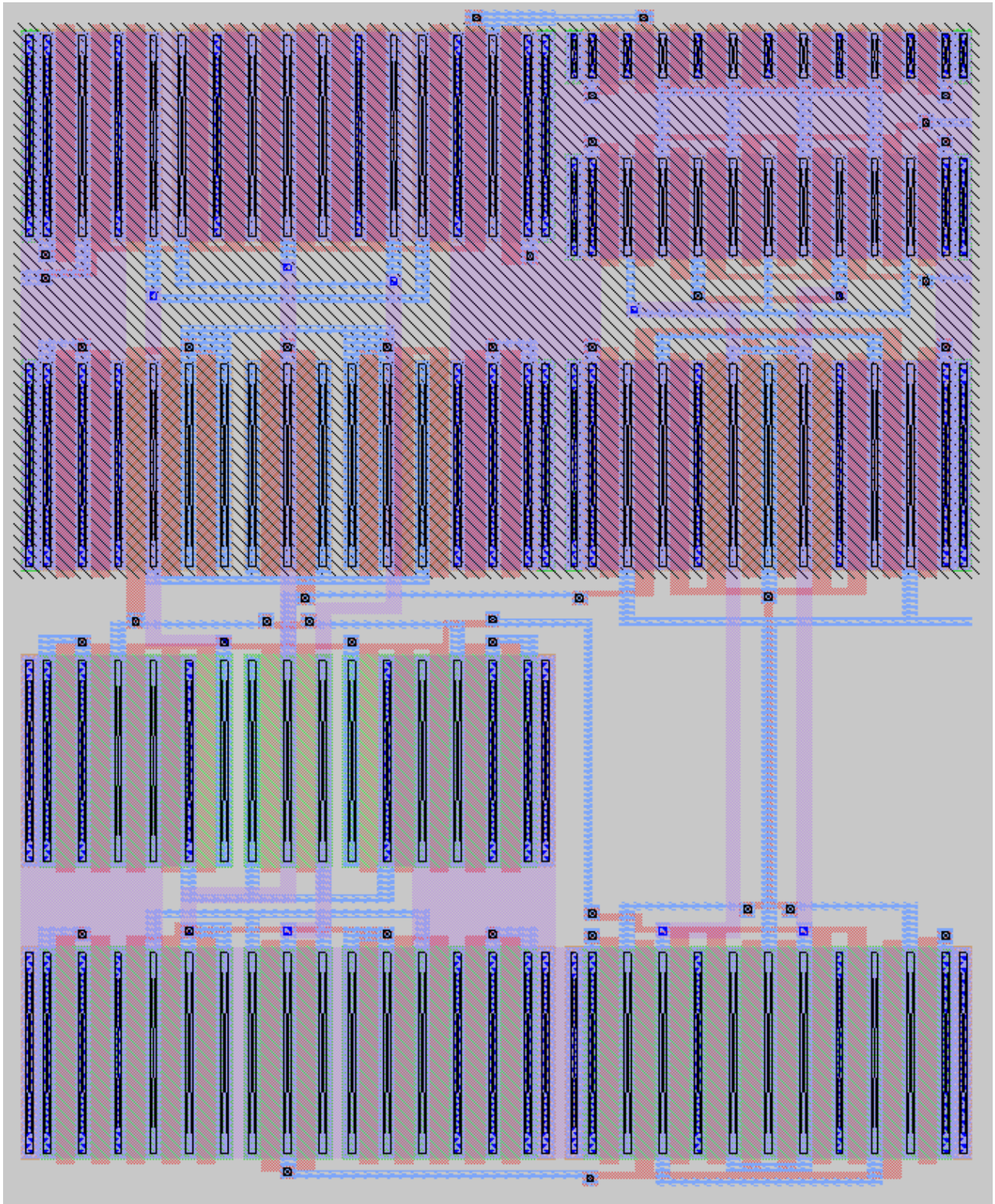


Figure 20: Layout of Folded-Cascode Differential Amplifier

6 Layout Verses Schematic

6.1 Cascode Differential Pair

The following comp.out file shows the LVS for the cascode differential pair layout and schematic.

```
Equate elements:  no current cell.
Equate elements:  no current cell.
Class differential_pair.spice:  Merged 25 devices.
Class differential_pair_xschem.spice:  Merged 25 devices.

Subcircuit summary:
Circuit 1: differential_pair.spice         |Circuit 2: differential_pair_xschem.
    spice
-------------------------------------------|-------------------------------------------

sky130_fd_pr__pfet_01v8 (10)               |sky130_fd_pr__pfet_01v8 (10)
sky130_fd_pr__nfet_01v8 (5)                |sky130_fd_pr__nfet_01v8 (5)
Number of devices: 15                      |Number of devices: 15
Number of nets: 15                         |Number of nets: 15
-----------------------------------------------------------------------------------------

Circuits match uniquely.
Netlists match uniquely.
Cells have no pins;  pin matching not needed.
Device classes differential_pair.spice and differential_pair_xschem.spice are
    equivalent.
Circuits match uniquely.
```

6.2 Cascode Bias

The following comp.out file shows the LVS for the cascode bias voltage generation circuit layout and schematic.

```
Equate elements:  no current cell.
Equate elements:  no current cell.
Class cascode_bias.spice:  Merged 23 devices.
Class cascode_bias_xschem.spice:  Merged 23 devices.

Subcircuit summary:
Circuit 1: cascode_bias.spice              |Circuit 2: cascode_bias_xschem.spice
-------------------------------------------|-------------------------------------------

sky130_fd_pr__pfet_01v8 (13)               |sky130_fd_pr__pfet_01v8 (13)
sky130_fd_pr__nfet_01v8 (12)               |sky130_fd_pr__nfet_01v8 (12)
Number of devices: 25                      |Number of devices: 25
Number of nets: 14                         |Number of nets: 14
-----------------------------------------------------------------------------------------

Resolving automorphisms by property value.
Resolving automorphisms by pin name.
Netlists match with 6 symmetries.
Circuits match correctly.
Cells have no pins;  pin matching not needed.
Device classes cascode_bias.spice and cascode_bias_xschem.spice are equivalent.
Circuits match uniquely.
```

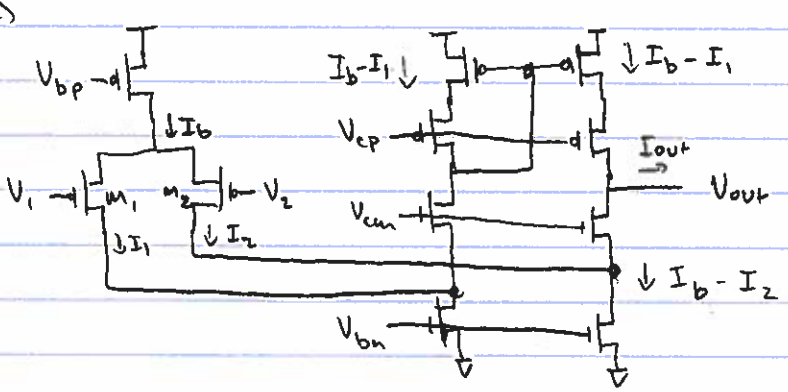
6.3 Folded-Cascode Differential Amplifier

The following comp.out file shows the LVS for the full folded-cascode differential amplifier layout and schematic.

```
Flattening unmatched subcell differential_pair in circuit
    folded_cascode_differential_amplifier.spice (0)(1 instance)
Flattening unmatched subcell cascode_bias in circuit
    folded_cascode_differential_amplifier.spice (0)(1 instance)
Flattening unmatched subcell folded_cascode_differential_amplifier_LDS in
    circuit folded_cascode_differential_amplifier_xschem.spice (1)(1 instance)
Flattening unmatched subcell cascode_bias_LDS in circuit
    folded_cascode_differential_amplifier_xschem.spice (1)(1 instance)
Equate elements:  no current cell.
Equate elements:  no current cell.
Class folded_cascode_differential_amplifier.spice:  Merged 49 devices.
Class folded_cascode_differential_amplifier_xschem.spice:  Merged 49 devices.

Subcircuit summary:
Circuit 1: folded_cascode_differential_amp |Circuit 2:
    folded_cascode_differential_amp
-------------------------------------------|-------------------------------------------

sky130_fd_pr__pfet_01v8 (22)               |sky130_fd_pr__pfet_01v8 (22)
sky130_fd_pr__nfet_01v8 (17)               |sky130_fd_pr__nfet_01v8 (17)
Number of devices: 39                      |Number of devices: 39
Number of nets: 23                         |Number of nets: 23
-------------------------------------------------------------------------------------

Resolving automorphisms by property value.
Resolving automorphisms by pin name.
Netlists match with 6 symmetries.
Circuits match correctly.
Cells have no pins;  pin matching not needed.
Device classes folded_cascode_differential_amplifier.spice and
    folded_cascode_differential_amplifier_xschem.spice are equivalent.
Circuits match uniquely.
```

Miniproject 3 — Thomas Jagielski

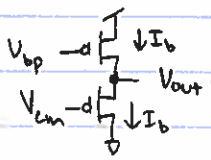
1) a)



$$I_{out} = (I_b - I_1) - (I_b - I_2) \Rightarrow \boxed{I_{out} = I_2 - I_1}$$

Since the differential pair is pMOS an increase in voltage will decrease the current. Thus if we increase V_1, then I_1 will decrease yielding a larger I_{out}. Conversely, if we increase V_2, then I_2 will decrease yielding a smaller I_{out}. Therefore V_1 is the noninverting input and V_2 is the inverting input as explained above.

b) Assume all transistors of strength 1 in pMOS drain follower



$$I_b = 5I_s \log^2\left(1 + e^{(\kappa((V_{dd} - V_{bp}) - V_{T0}) - (V_{dd} - V_{dd})/2u_T}\right)$$
$$= 5I_s \log^2\left(1 + e^{\kappa((V_{dd} - V_{cm}) - V_{T0}) - (V_{dd} - V_{out})/2u_T}\right)$$

$$\Rightarrow \kappa(V_{dd} - V_{bp} - V_{T0}) = \kappa(V_{dd} - V_{cm} - V_{T0}) - (V_{dd} - V_{out})$$
$$\kappa V_{dd} - \kappa V_{bp} - \kappa V_{T0} = \kappa V_{dd} - \kappa V_{cm} - \kappa V_{T0} - V_{dd} + V_{out}$$
$$-\kappa V_{bp} = -\kappa V_{cm} - V_{dd} + V_{out}$$
$$V_{out} = V_{dd} + \kappa V_{cm} - \kappa V_{bp}$$
$$V_{out} = V_{dd} - \kappa(V_{bp} - V_{cm})$$

$$\therefore V_{dd} - V_{sosat} \geq V_{dd} - \kappa(V_{bp} - V_{cm}) \Rightarrow \frac{V_{sosat}}{\kappa} \leq V_{bp} - V_{cm} \Rightarrow -V_{cm} \geq \frac{V_{sosat}}{\kappa} - V_{bp}$$

$$\Rightarrow V_{cm} \leq V_{bp} - \frac{V_{sosat}}{\kappa}$$

1) b) (continued) we know that for M_b to remain in saturation and conduct I_b the node voltage between M_b, M_1, and M_2 needs to be at least V_{sdsat} below V_{dd}. Following the PMOS drain follower calculations before, this is the case when

$$V_{cm} \leq V_{bp} - \frac{V_{osat}}{K}$$

Thus, this is the maximum common mode voltage the circuit can handle, since this is a PMOS differential pair the minimum V_{cm} is 0 V. It is important to note that this is a conservative estimate since only $\frac{W}{L} = 1$ transistors. If we were to consider the differential pair as $\frac{W}{L} = 2$, we would find a slightly higher allowable range for V_{cm}.

c) Please refer to 1-a for explaination $I_{out} = I_2 - I_1$

d) The currents sunk by M_3 and M_4 need to be equal to I_b. If M_3 or M_4 were to sink less than I_b then if $I_1 = I_b$ current would need to flow upwards through the M_7, M_9, and M_5 branch. This would break the diode connection yielding a circuit that does not function properly. Similarly, if M_3 and M_4 were to sink more than I_b then small changes in I_1 and I_2 will not affect the output current as much (ie $2I_b - \frac{I_b}{2}$ is a smaller change than $I_b - \frac{I_b}{2}$). This would, therefore, decrease the change in output current as well as the gain of the circuit for that reason. Thus, M_3 and M_4 must sink I_b.

1) e)