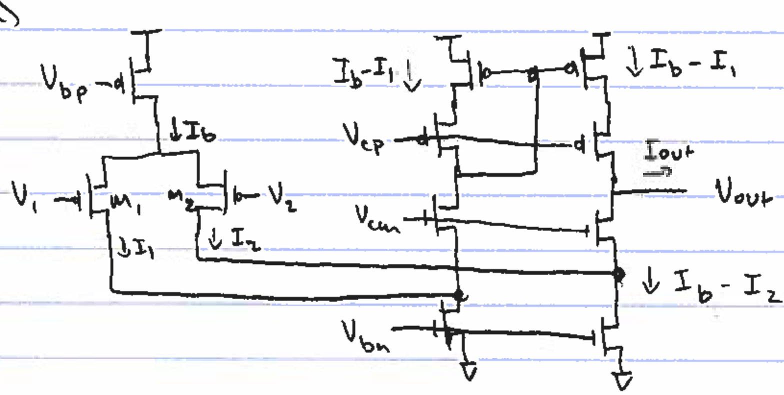
Miniproject 3 Thomas Jagielski

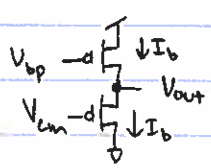
1) a)



$$I_{out} = (\cancel{I_b} - I_1) - (\cancel{I_b} - I_2) \Rightarrow \boxed{I_{out} = I_2 - I_1}$$

Since the differential pair is pMOS an increase in voltage will decrease the current. Thus if we increase V_1, then I_1 will decrease yielding a larger I_{out}. Conversely, if we increase V_2, then I_2 will decrease yielding a smaller I_{out}. Therefore V_1 is the noninverting input and V_2 is the inverting input as explained above.

b) Assume all transistors of strength 1 in pmos drain follower



$$I_b = SI_s \log^2\left(1 + e^{(\kappa((V_{dd} - V_{bp}) - V_{T0}) - (\cancel{V_{dd}} \overset{0}{V_{dd}}))/2U_T}\right)$$

$$= SI_s \log^2\left(1 + e^{\kappa((V_{dd} - V_{cn}) - V_{T0}) - (V_{dd} - V_{out}))/2U_T}\right)$$

$$\Rightarrow \kappa(V_{dd} - V_{bp} - V_{T0}) = \kappa(V_{dd} - V_{cn} - V_{T0}) - (V_{dd} - V_{out})$$

$$\cancel{\kappa V_{dd}} - \kappa V_{bp} - \cancel{\kappa V_{T0}} = \cancel{\kappa V_{dd}} - \kappa V_{cn} - \cancel{\kappa V_{T0}} - V_{dd} + V_{out}$$

$$-\kappa V_{bp} = -\kappa V_{cn} - V_{dd} + V_{out}$$

$$V_{out} = V_{dd} + \kappa V_{cn} - \kappa V_{bp}$$

$$V_{out} = V_{dd} - \kappa(V_{bp} - V_{cn})$$

$$\therefore \cancel{V_{dd}} - V_{SDsat} \geq \cancel{V_{dd}} - \kappa(V_{bp} - V_{cn}) \Rightarrow \frac{V_{SDsat}}{\kappa} \leq V_{bp} - V_{cn} \Rightarrow -V_{cn} \geq \frac{V_{SDsat}}{\kappa} - V_{bp}$$

$$\Rightarrow V_{cn} \leq V_{bp} - \frac{V_{SDsat}}{\kappa}$$

1) b) (continued) we know that for m_b to remain in saturation and conduct I_b the node voltage between M_b, M_1, and M_2 needs to be at least V_{SDsat} below V_{dd}. Following the PMOS drain follower calculations before, this is the case when

$$V_{cm} \leq V_{bp} - \frac{V_{SOsat}}{K}$$

Thus, this is the maximum common mode voltage the circuit can handle. Since this is a PMOS differential pair the minimum V_{cm} is 0 V. It is important to note that this is a conservative estimate since only $\frac{W}{L} = 1$ transistors. If we were to consider the differential pair as $\frac{W}{L} = 2$, we would find a slightly higher allowable range for V_{cm}.

c) Please refer to 1-a for explaination $\underline{I_{out} = I_2 - I_1}$

d) The currents sunk by M3 and M4 need to be equal to I_b. If M_3 or M_4 were to sink less than I_b then if $I_1 = I_b$ current would need to flow upwards through the m7, m9, and M5 branch. This would break the diode connection yielding a circuit that does not function properly. Similarly, if M_3 and M_4 were to sink more than I_b then small changes in I_1 and I_2 will not affect the output current as much (ie $2I_b - \frac{I_b}{2}$ is a smaller change than $I_b - \frac{I_b}{2}$). This would, therefore, decrease the change in output current as well as the gain of the circuit for that reason. Thus, M3 and M4 must sink I_b.

1) e)