Mixed Analog-Digital VLSI Mini-Project IV: 7-Bit Digital-to-Analog Converter

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Contents

Project Links

We created a unified GitHub repository for collaborating on this project. This section includes the relevant links to access the Schematics, Layouts, and Analysis scripts.

1 Circuit Analysis and Bias Voltage Generation

1.1 M-2M Ladder

We created a MOS analog of the M-2M ladder circuit (from Circuits), as represented in the figure below:

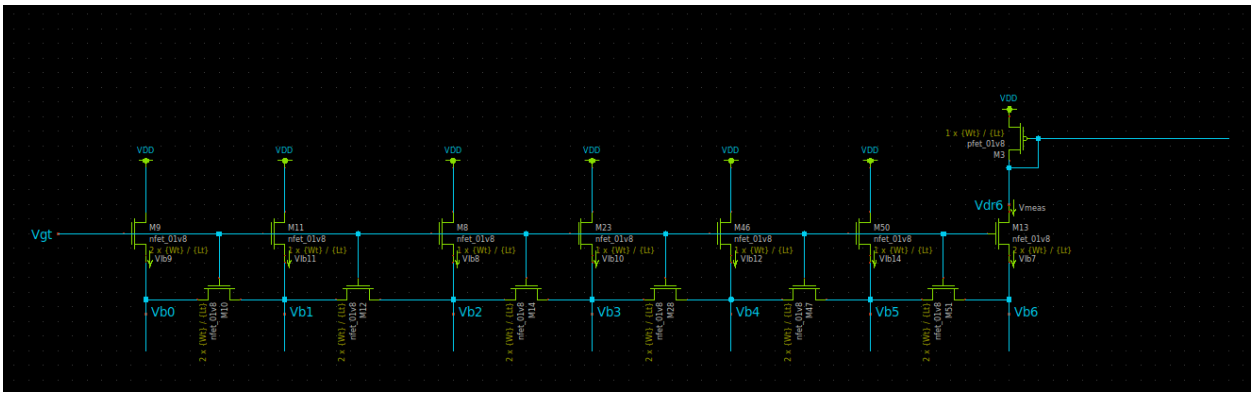

Figure 1: M-2M ladder MOS design capture in Xschem

As is required by the circuit, we size and source the transistors in order for the vertical transistors to remain in saturation, and for the Early effect to be minimized in our simulations. The ladder circuit can be analyzed using the method of superposition for each leg of current sink. In this method, we treat all but one current sink as absent. This allows us to reduce the M-2M ladder into three unit transistors in parallel at the node of present current sink. The gates of the vertical transistors are generated through this observation and controlled by a CMOS differential amplifier circuit as represented below.

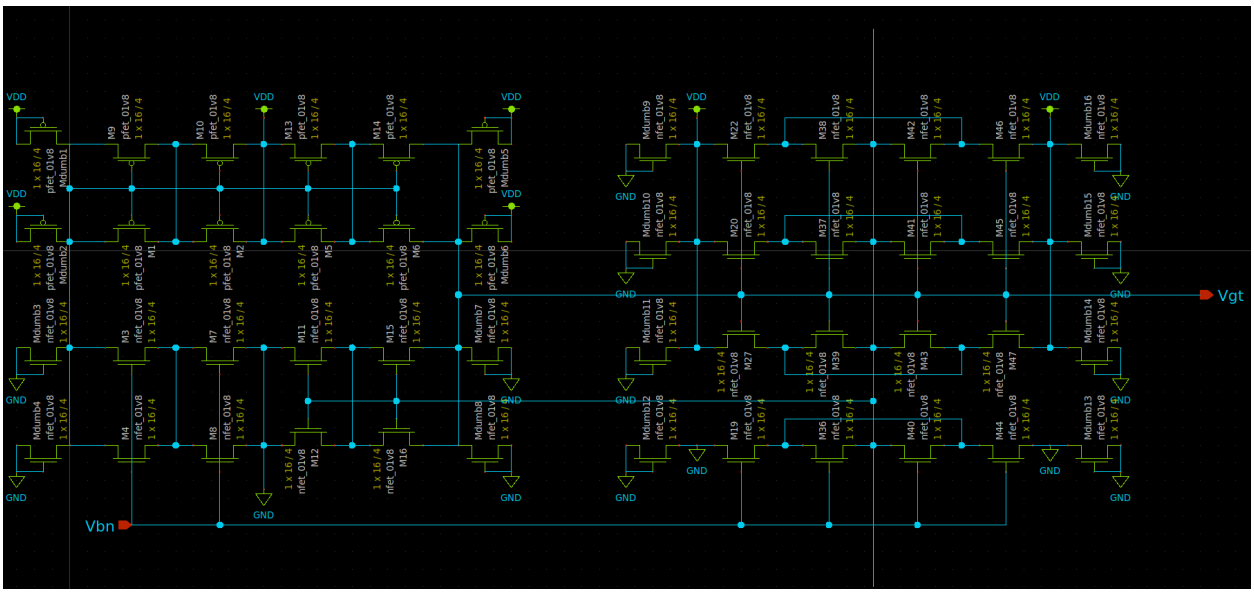

Figure 2: Vg generator differential amplifier circuit

The output current (I_{out}) for our 7-bit DAC (Passing through M3 transistor) would ideally equal

$$I_{out} = \frac{1}{96} I_{ref}(b_0 + 2b_1 + 4b_2 + 8b_3 + 16b_4 + 32b_5 + 64b_6) \tag{1}$$

provided we observe negligible transfer error through the mirroring process (explained later) and negligible Early effect.

1.2 Digital Input Logic

In order to set the state of the ladder based on digital input bits, we used 2:1 multiplexers, one for each leg of the ladder, to switch between "on" or "off" state. Each of these multiplexers drives the gate of an nMOS transistor, which in turn, lets current pass through or blocks it. The structure of the multiplexer is as follows:

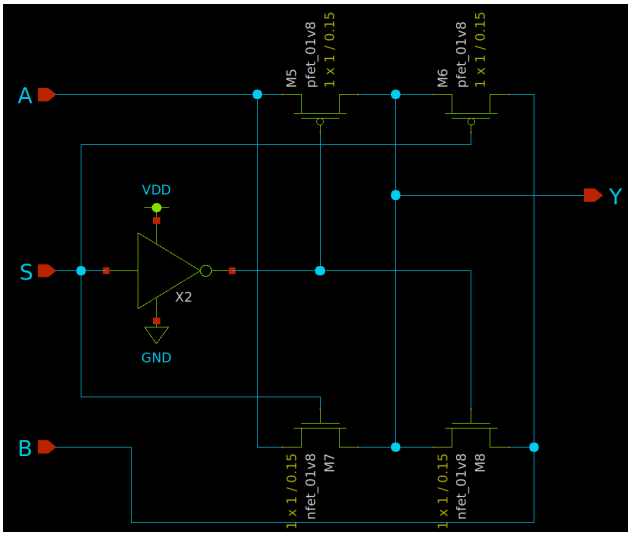

Figure 3: Mux circuit

1.3 Bias Current and Gate Voltage Generation

For generating the proper bias voltage for the reference current, we used the "magic" variant of the boot-strap circuit that Professor Bradley Minch introduced in one of the content videos. The circuit uses an external resistor to set the desired current level and invokes the idea of a simple four-transistor differential amplifier to generate a pMOS and nMOS gate voltage to allow for the bias current.

Observing the fact that the M-2M ladder reduces to three unit transistors in parallel with superposition analysis, we treat them as in series with the current sink nMOS and proposed the idea of using a cascode bias voltage generating circuit to generate the gate voltage for the transistors in the M-2M ladders. However, by doing transient simulations in the early stages of our circuit design process, we notice that such a configuration would consistently result in the current sinks in the ladder sinking less current that what the bias current generating circuit has intended. This mismatch is attributed to the different drain voltages at the current sinks and at the bias current generator and the Early effect of the nMOS transistors. Thus, we decided to pursue a different approach. We built a reference device that is three parallel nMOS in series with one nMOS to mimic the reduced structure of the M-2M ladder and similarly used a four transistor differential amplifier with feedback to drive the gate voltage of the three parallel transistors such that the drain voltage is the same for nMOS in both the bias current generator and the ladder current sinks. While this approach does not account for the variations and voltage drops across different legs of the M-2M ladder, it allows to much more closely match the drain voltages and pass the intended current better than the approach of cascode bias voltage generation.

1.4 Low-voltage Super-Wilson Current Mirror

In order to mirror the current between the M-2M network and the output, we conducted experiments with a variety of simple current mirrors, and observed some transfer error in the mirroring process. To combat this, we applied the Wilson mirror topology. Specifically, we used the Low-Voltage Super-Wilson design to achieve operation over a wider voltage swing across the power rails. We achieved this through the addition of a diode connected nMOS transistor in the input branch (reduces the systematic gain error) and one additional input branch (which approximately passes half the current (I_b), compared to the diode connected input branch ($2I_b$). This topology requires a minimum supply voltage of only $V_{diode} + 2V_{DSsat}$.

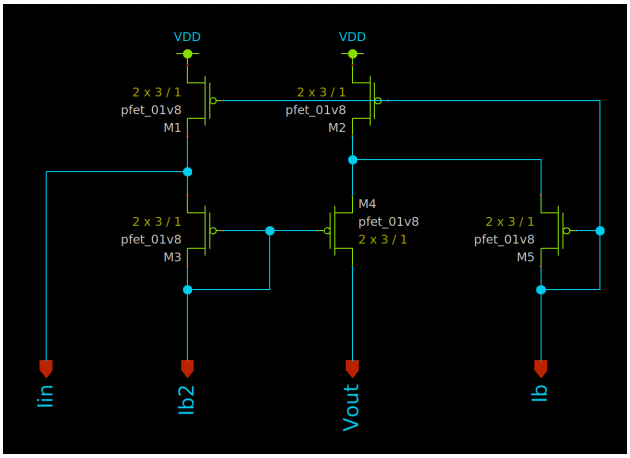

Figure 4: Low-Voltage Super-Wilson design capture in Xschem

Furthermore, to generate the bias currents for the Low-Voltage Super-Wilson design (I_b, $2I_b$), we used an M-2M ladder network. This ladder is identical to the standard cell we developed as part of our 7-bit M-2M ladder network.

2 Schematic Capture and Simulation

The layout driven schematics we created can be found at the following link: https://github.com/ThomasJagielski/MADVLSI-MP4/tree/main/schematic/LDS.

2.1 Schematic Capture

The design of our 7-bit DAC is shown in Figure 5. Viewing the circuit after a 90 clockwise rotation, we can roughly divide up the circuits into three parts. On the bottom left is the bias current generating circuit and the ladder gate voltage generating circuit. In the middle is our M-2M networks with nMOS acting as current sinks with digitally controlled 2-input MUX that switches the gate voltage between bias-current voltage and ground. On the top right is the low voltage super-wilson current mirror that serves as the output stage of the M-2M ladder. The current mirror is biased with an nMOS network identical to the M-2M used for digital-to-analog conversion, except that the gates of all but the LSB current sink is switched off.

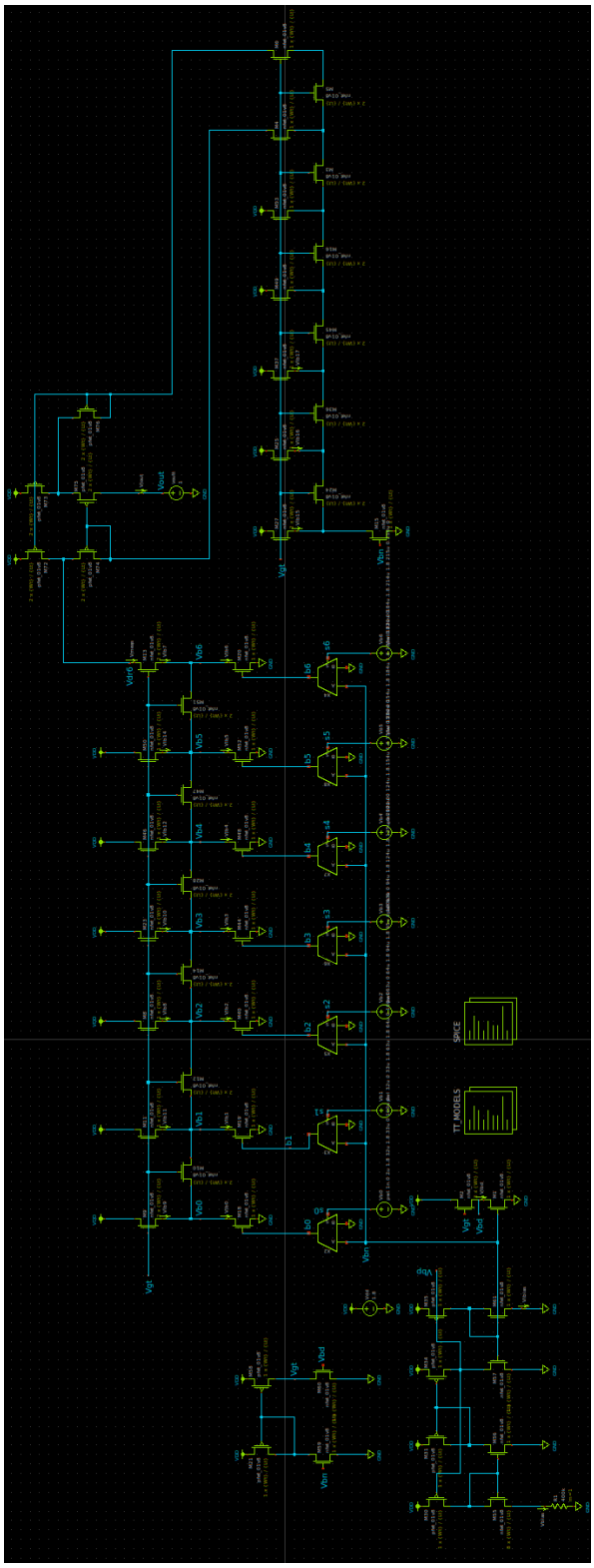

Figure 5: Human-readable schematic of our 7-bit DAC.

2.2 Layout Driven Schematic

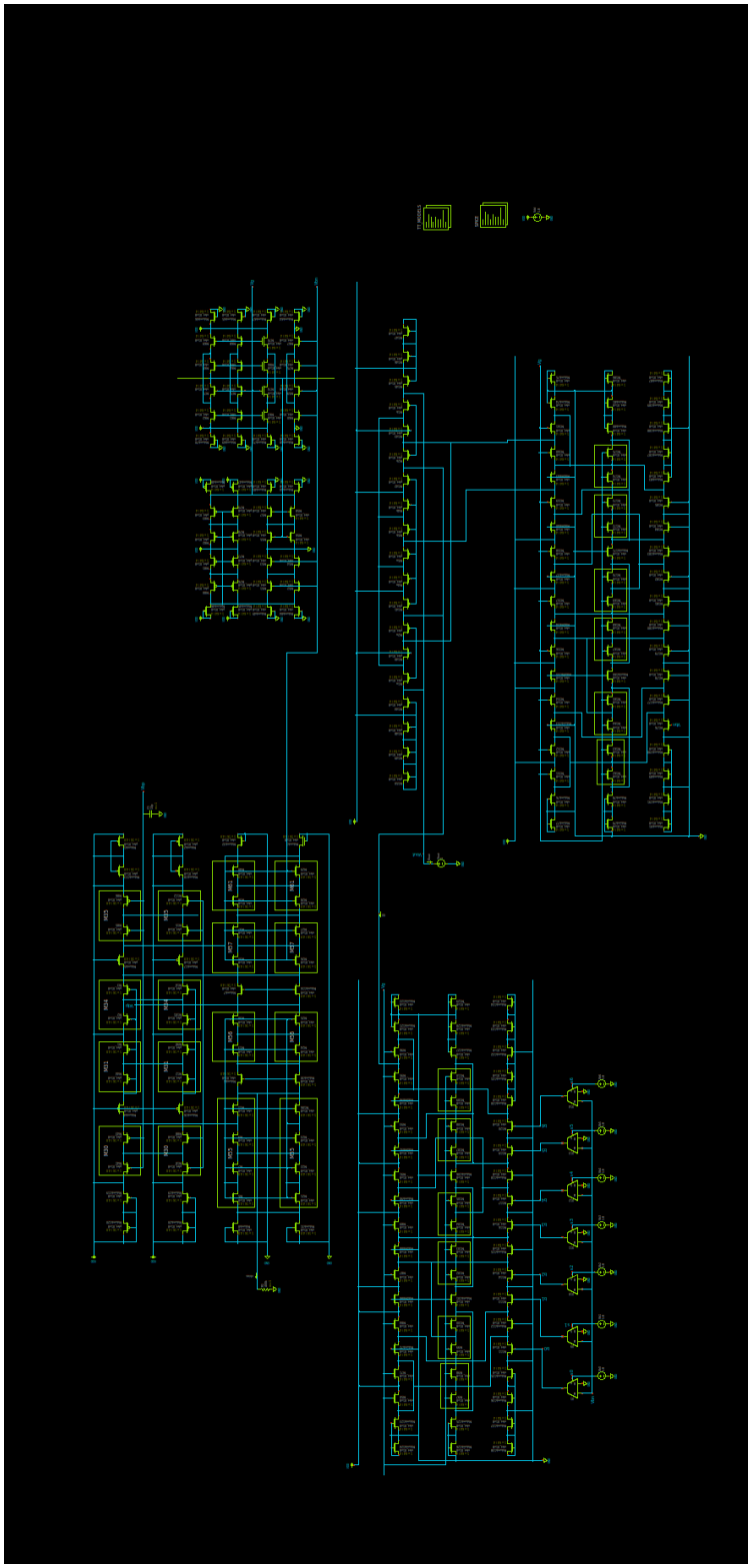

Figure 6: Layout driven schematic of our 7-bit DAC.

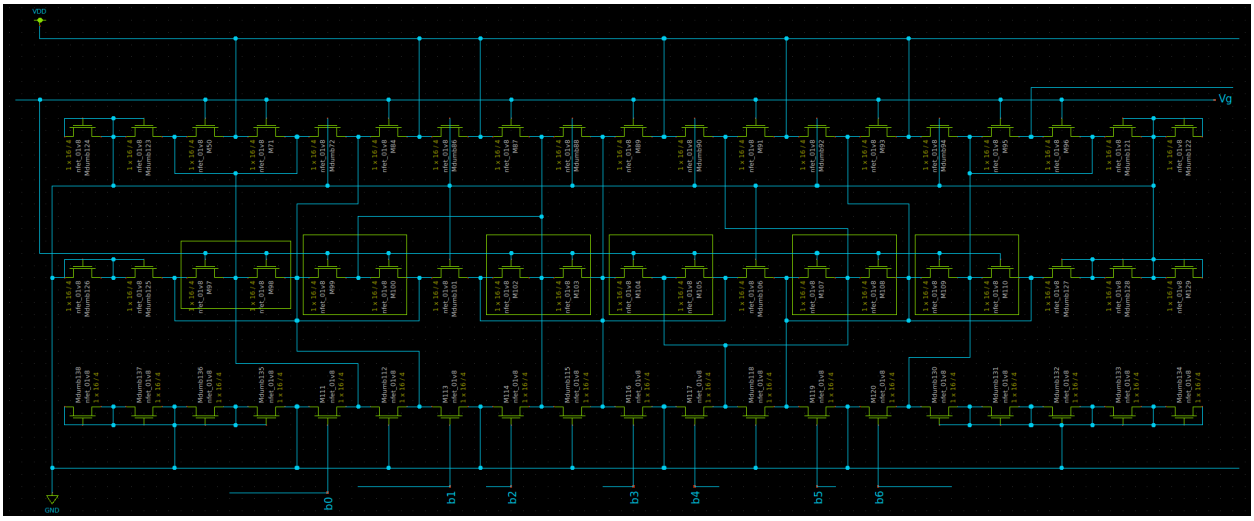

Figure 7: Layout driven schematic of our 7-bit M-2M ladder.

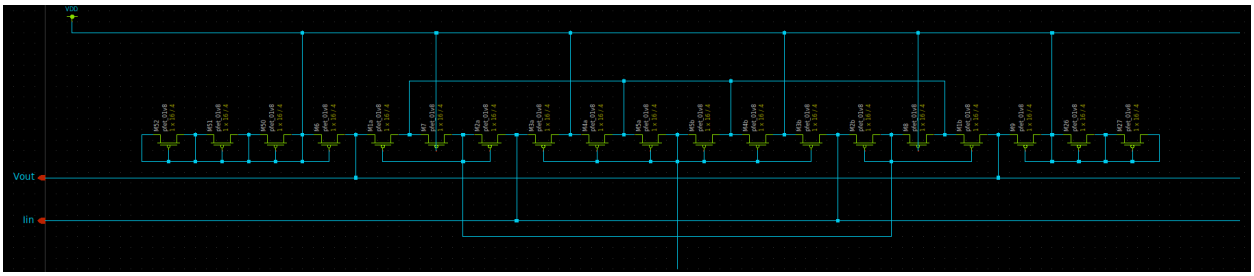

Figure 8: Layout driven schematic of the pMOS section of our Super-Wilson current mirror.

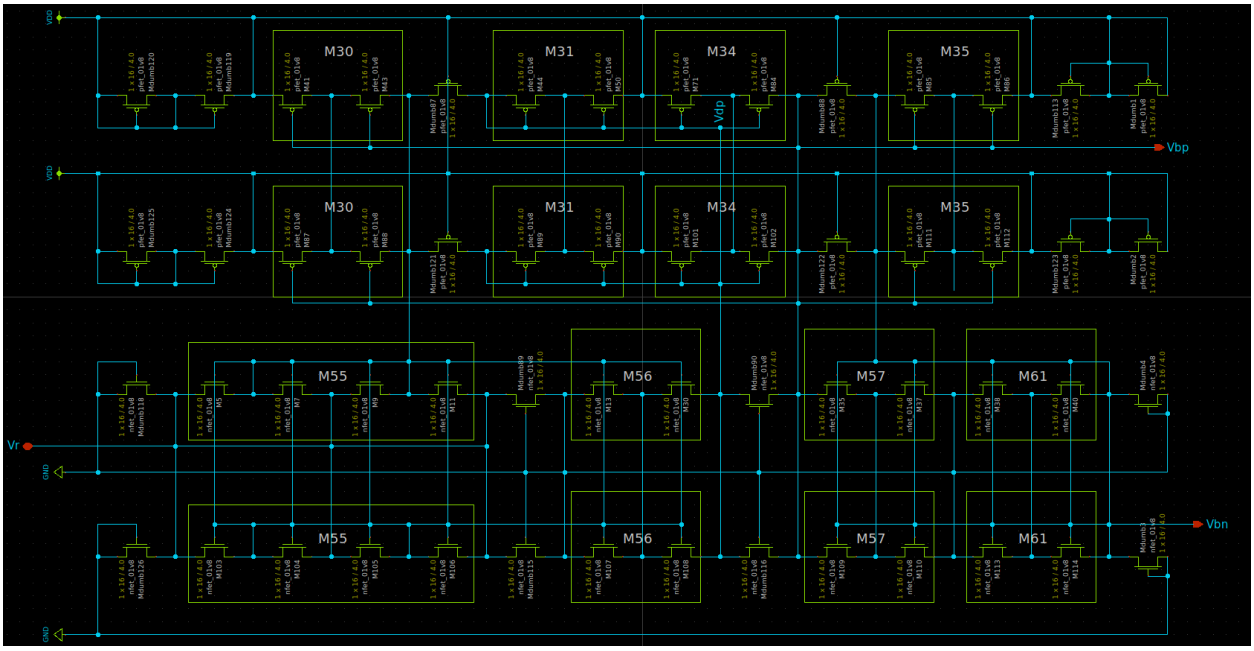

Figure 9: Layout driven schematic of the bias current generating circuit.

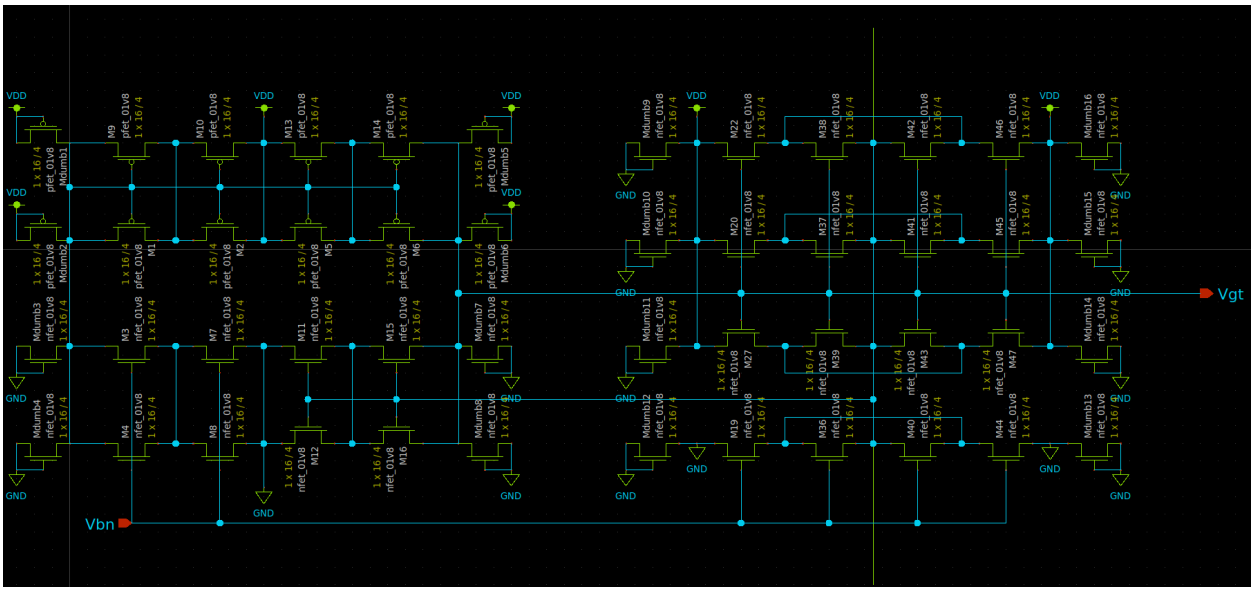

Figure 10: Layout driven schematic of the ladder gate voltage generating circuit.

2.3 Test Harness

The initial project requirements were provided as follows: Firstly, the output current should be available as a current source or sink that changes by no more than 0.5%/V over at least 80% of the power supply range. Secondly, the output current should not change by more than 0.5%/V with the power supply voltage. Lastly, the DAC must have differential and integral nonlinearity (DNL/INL) of no more than one least-significant bit (LSB).

In order to verify the output current generation capability of our circuit, we performed the operating point and DC sweep simulations that let us examine the linearity and the variation per unit supply/output voltage.

In order to verify the differential nonlinearity (DNL) and integral nonlinearity (INL) of our circuit, we performed analysis using the script linked here. The DNL specifies the difference between two successive voltage levels that a DAC produces. It characterizes this difference in the form of deviation of the output from the ideal LSB value. Utilizing the calculated DNL values, we can arrive at the INL of the DAC through a simple summation as follows:

$$INL_n = \sum_{i=0}^{n} DNL_i \tag{2}$$

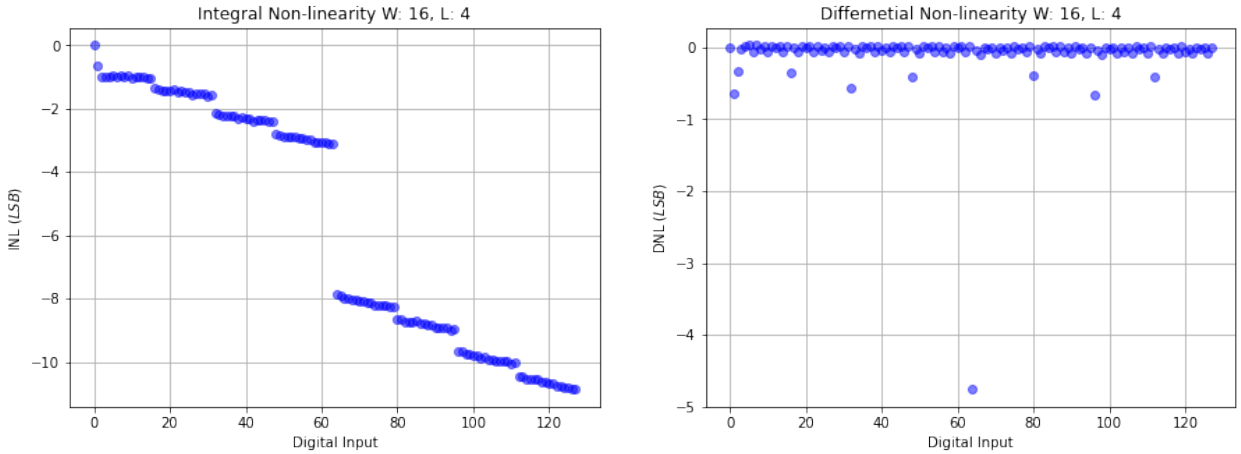

Figure 11: Mismatch-Free DNL and INL for our DAC Layout Driven Schematic

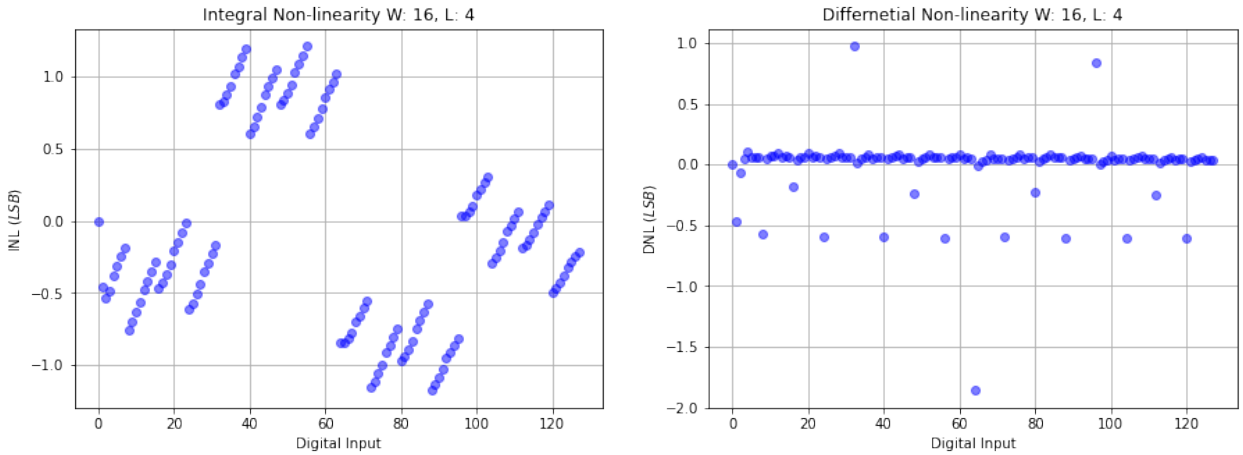

Figure 12: Mismatch-Free DNL and INL for our DAC Human-Readable schematic.

The results from our analysis are presented in the following graphs:

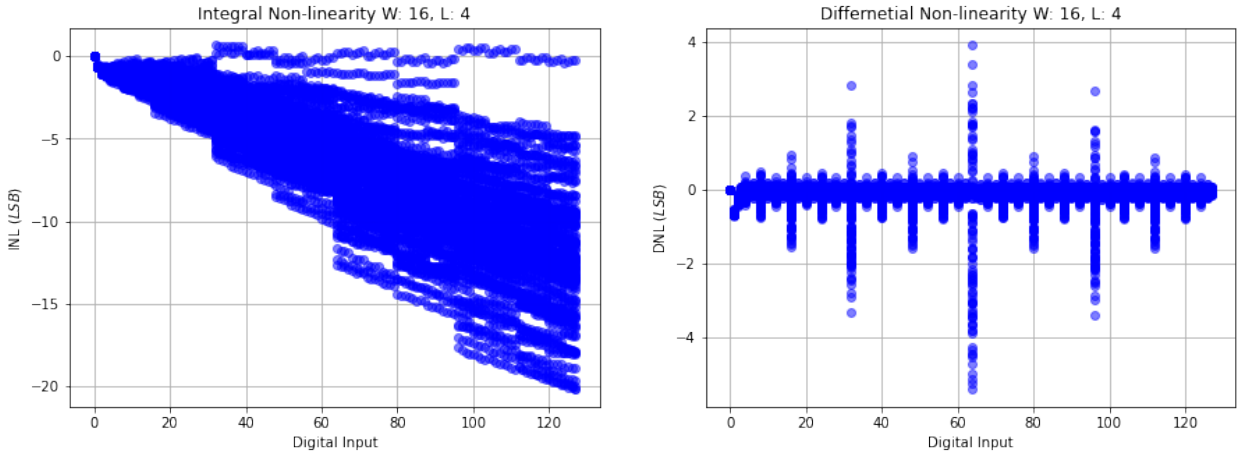

Figure 13: DNL and INL for our DAC Layout Driven Schematic

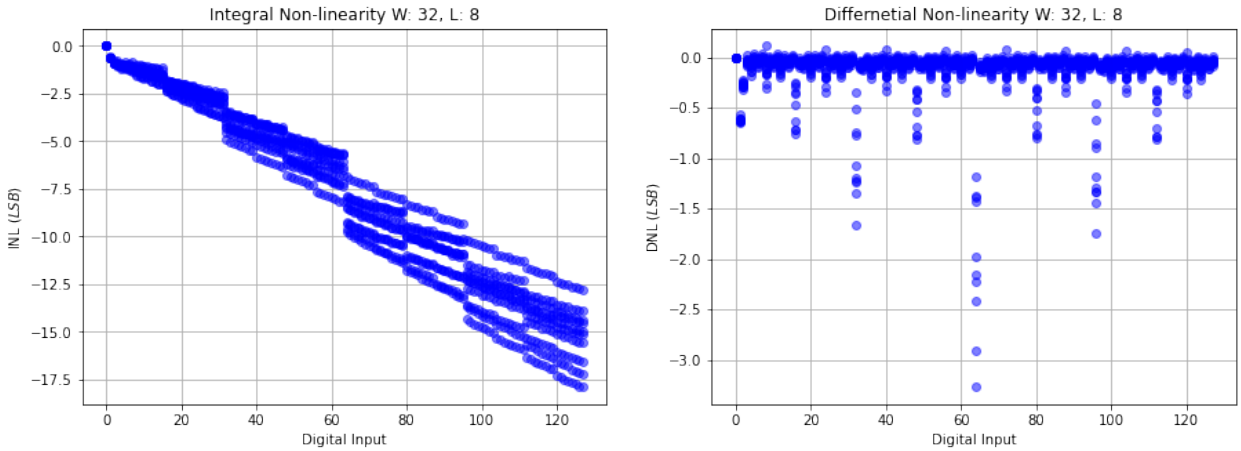

Figure 14: DNL and INL for our DAC Layout Driven Schematic for 32/8 transistors

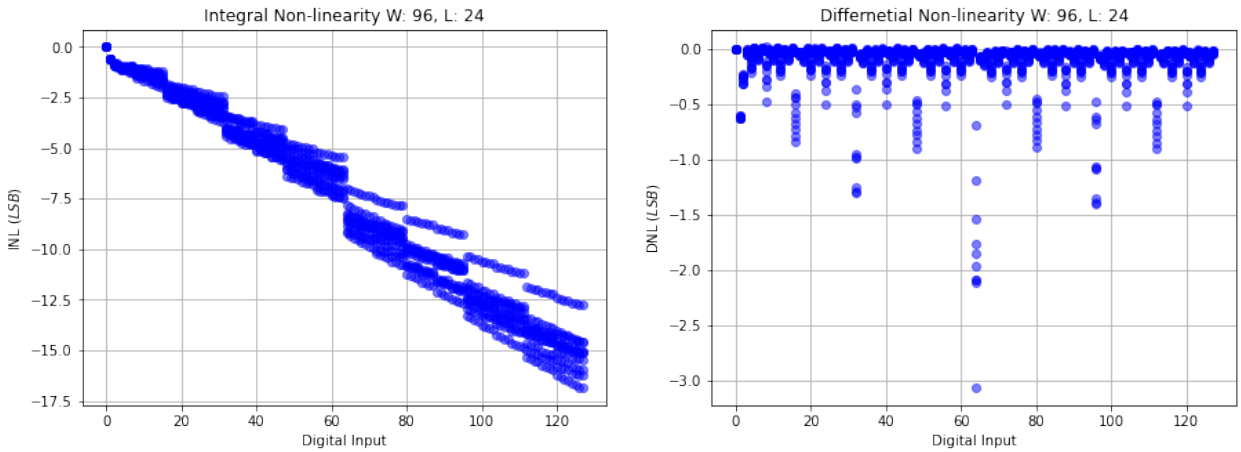

Figure 15: DNL and INL for our DAC Layout Driven Schematic 32/8 transistors

We observe that the DNL is centered on 0 LSB line, with minor outliers at the 17-,32-, 48-, 64-, 80-, 97-, and 112-bit marks. The pattern we observe here is there seem to be the most outliers around the duration we switch from or to multiples of the number 16 in bits, between 1 (0000001) and 127 (1111111): (16, 32, 48, 64, 80, 96, 112). The maximum absolute DNL is observed at the 64-bit mark, where it reaches about 5.8 LSB's.

Looking at the INL plot, we observe a systematic error as we get lower analog output than we expected overall. This accumulates to the maximum allowable limit of 20 LSB at around the 122 bit mark.

We have also done a large number of testing on the size of the transistors. Our final choice is 16μm-wide and 4μm-long transistor. Smaller transistors results in more prominent Early effect that leads to less reliable INL and DNL outcomes and more variable DC sweeps on V_{out} and V_{dd}, while larger transistors, as large as 96-by-24, does not offer any noticeable performance increase, if they don't worsen the results to begin with. As you may see in Figure 14 AND 15 that are 10 Monte Carlo mismatch simulations, the Therefore, we settle on 16-by-4 as a reasonably size transistor to both perform and implement.

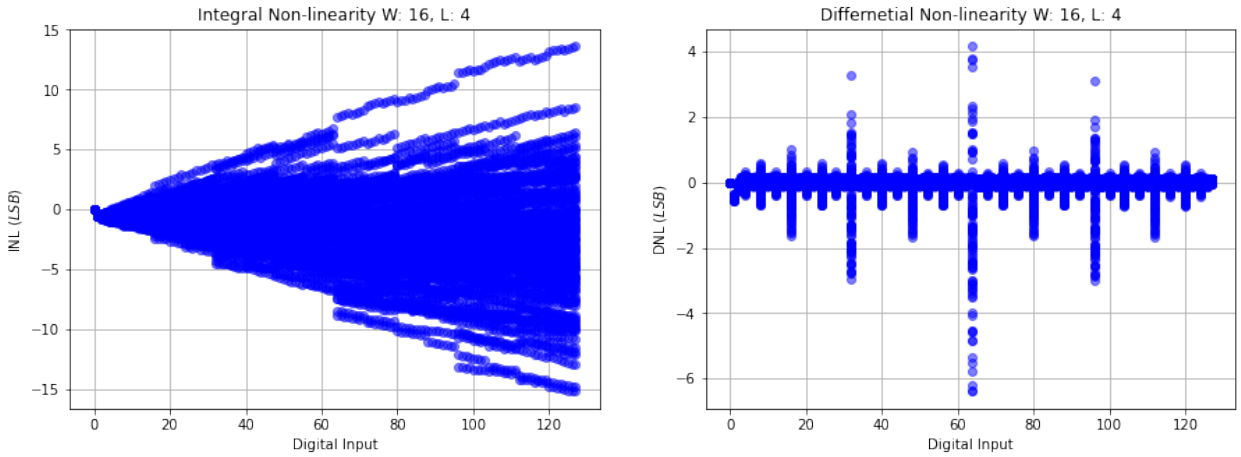

Figure 16: DNL and INL for the human-readable schematic

Referring to figure 13, we can observe that the DNL plots look nearly identical. The largest deviation in the DNL for the human-readable schematic is around the 64-bit mark, where the absolute DNL is about 6.8 LSB's. This is different from the case of layout driven schematic by roughly 17%.

The INL plot for the human-readable schematic has a more symmetric profile, and a better overall INL (15 LSB's at the 122-bit mark). This is approximately 0.25% better compared to the case of layout driven schematic.

Part of the difference can be attributed to added devices due to common centroiding the transistors in the layout driven schematic. To maximize the matching through common unit transistor sizes, we added two unit devices in series on each side of the common centroid to maintain the proper transistor sizing. As a result of this, there could be added parasitic capacitances or resistances due to the added devices. Similarly, we know that simulations differ when we use two devices as opposed to a single device with an equivalent effective size. Thus, these reasons may account of the variation between the human readable and layout driven schematic simulations of the circuit. Finally, another reason is more devices yields more opportunity for mismatch when running Monte Carlo simulations.

We next considered the sensitivity of the output current on the output voltage. The following image shows the percentage change in the output current over 80% of the power supply as we sweep V_{out}.

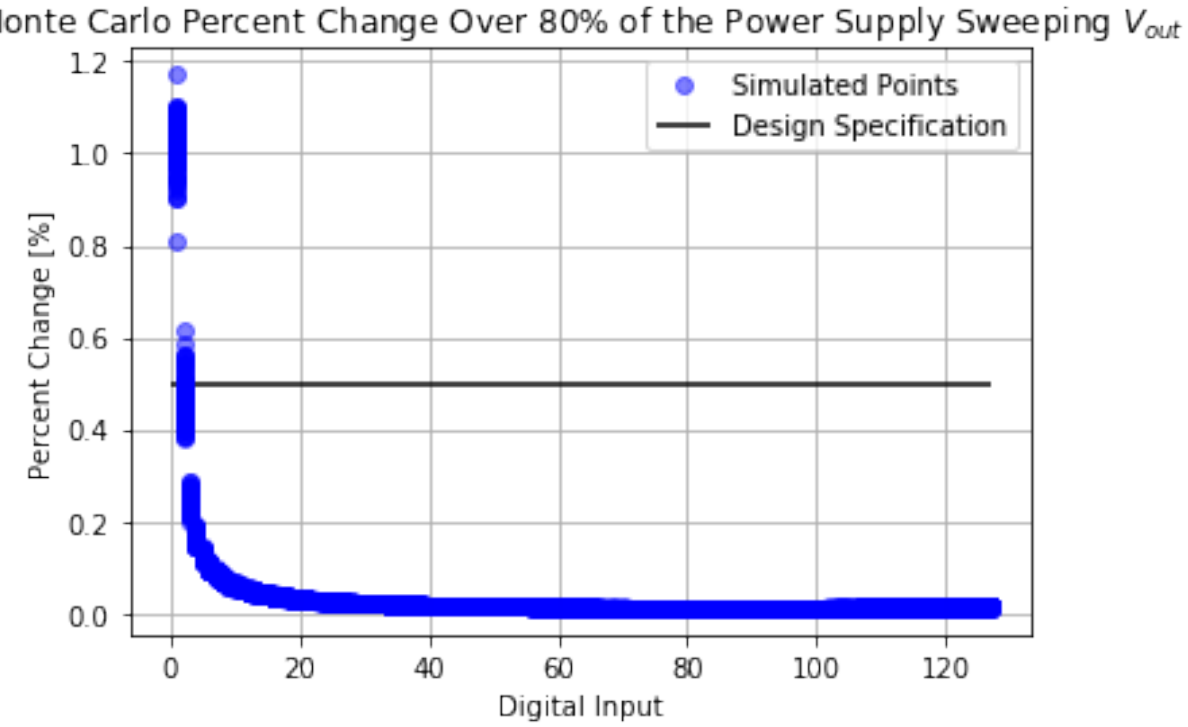

Figure 17: Figure depicting percentage change in output current per volt as we sweep V_{out} for 80% of the power supply

We find that our design for nearly all of the digital inputs is substantially less than 0.2% change per volt during the sweep. Through Monte Carlo simulations, we find that all binary inputs greater than 3 fall under the 0.5% / volt design specification. Across all Monte Carlo simulations and binary input values, we find the average percent change in current at 80% of the power supply to be 0.035% / V.

We also considered the change in output current due to changes in Vdd. For this analysis, we swept Vdd from 1.8 V $\pm$ 0.05 V to consider a change in Vdd in either direction. As we expected when Vdd was slightly higher than 1.8 V, our circuit performed with a flat line output. However, there was a significant decrease as we reduced Vdd to lower than 1.8 V. The following figure shows the percent change per volt as a result of changes in the power supply.

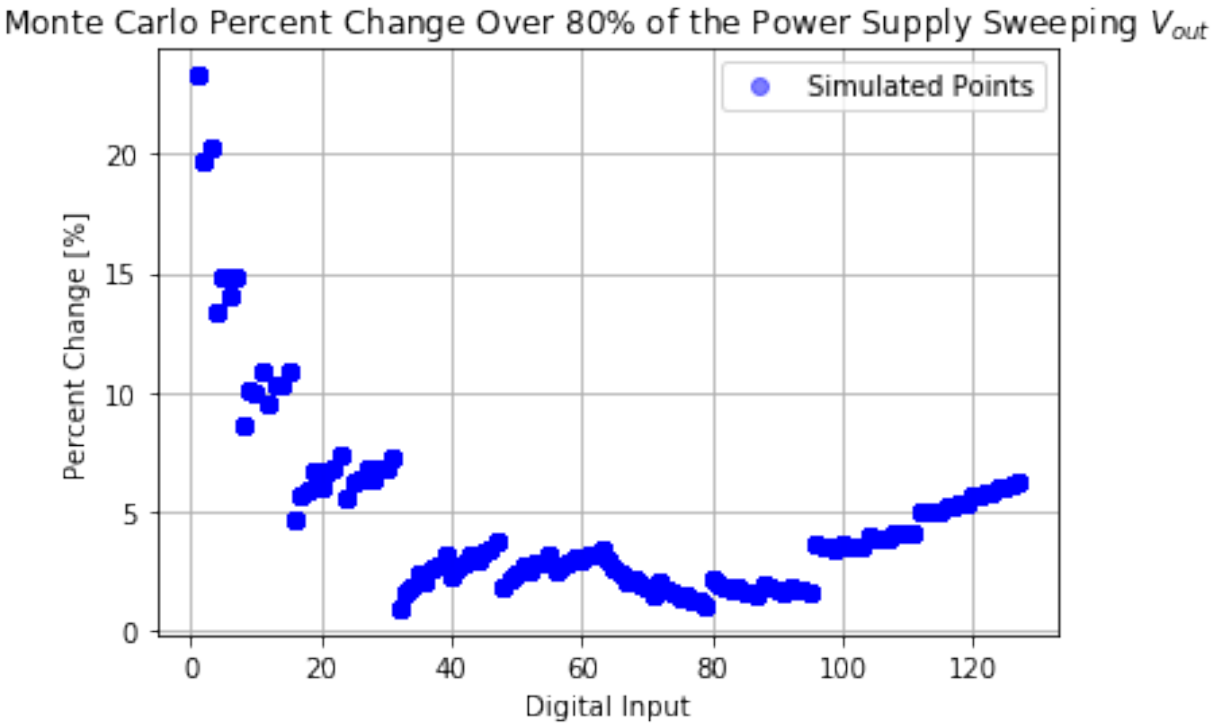

Figure 18: Figure depicting percentage change in output current per volt as we sweep Vdd

We can see that our circuit yields a higher percent change in output current per volt than the design specification for all binary input values. Taking into account all of the simulations and binary inputs, we found an average percent change in output current per volt to be 4.68% / V.

For further improvements to decrease this value, we could increase the length of our transistors, make voltage references to ground instead of Vdd, and add cascode stages to portions of the circuit such as the bias current generating circuit.

3 Layout Design

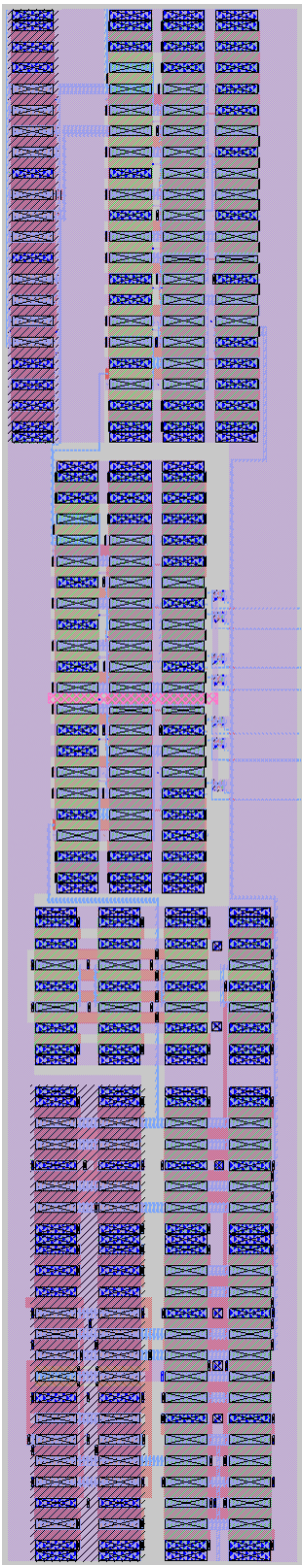

Figure 19: Layout of our 7-bit DAC.

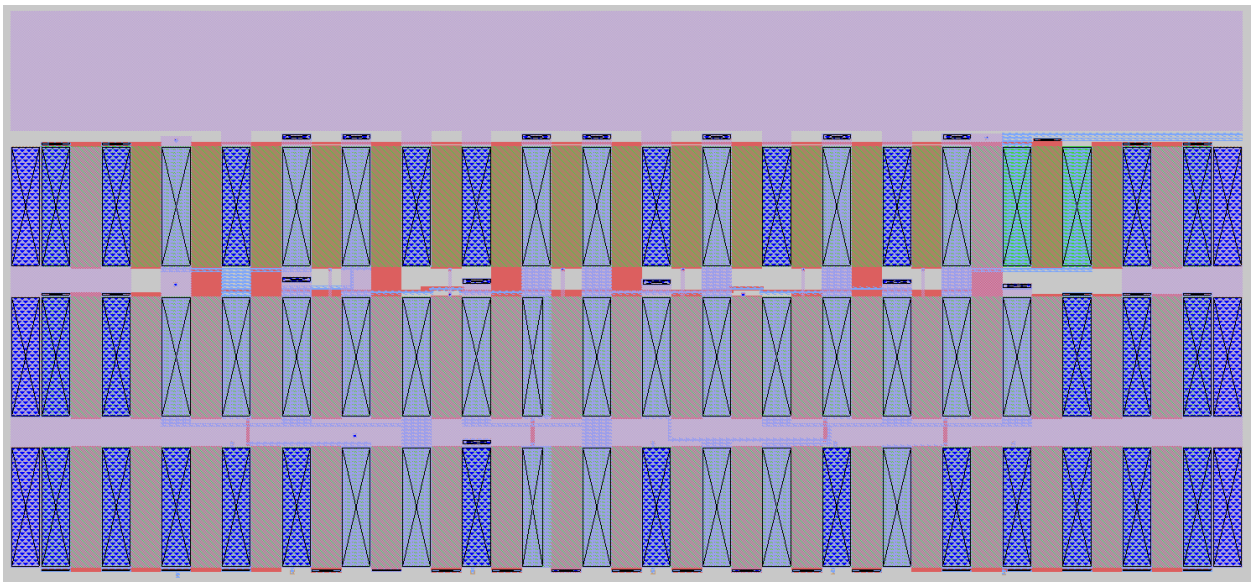

Figure 20: Layout of our 7-bit M-2M ladder.

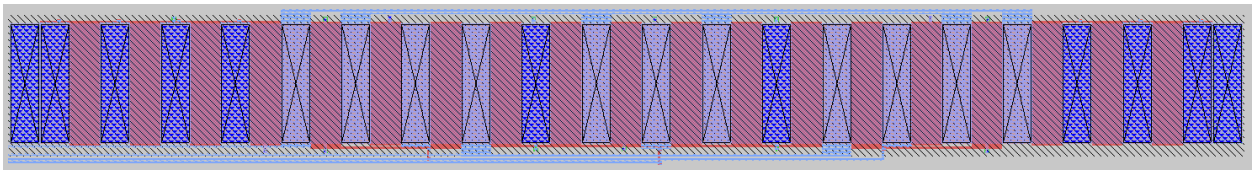

Figure 21: Layout of the pMOS section of our Super-Wilson current mirror.

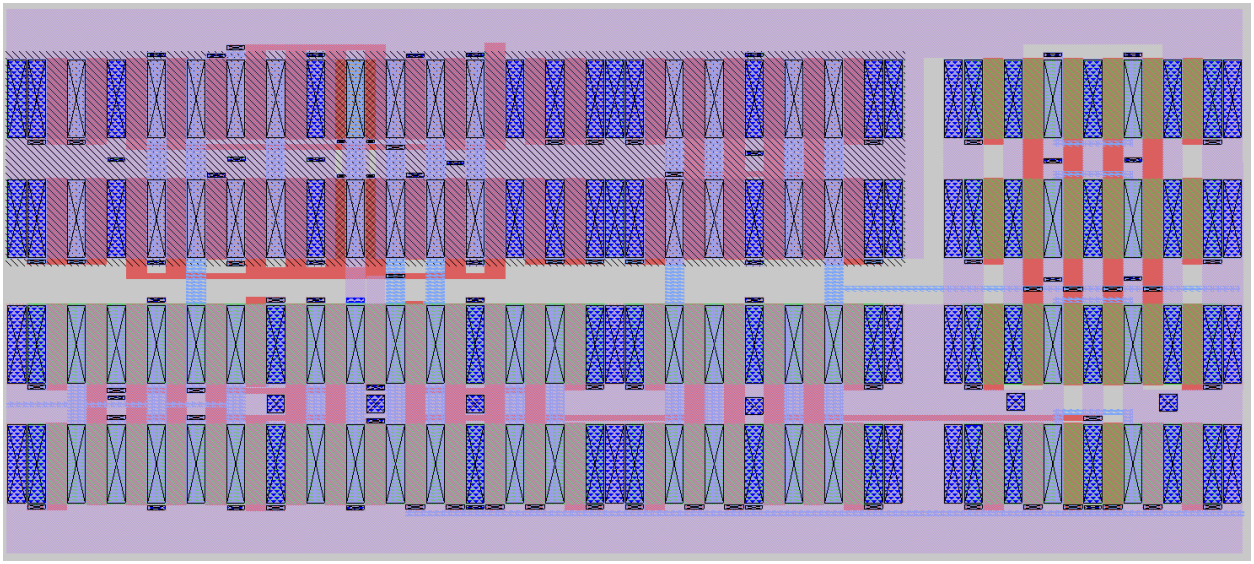

Figure 22: Layout of the bias current generating circuit and ladder gate voltage generating circuit.

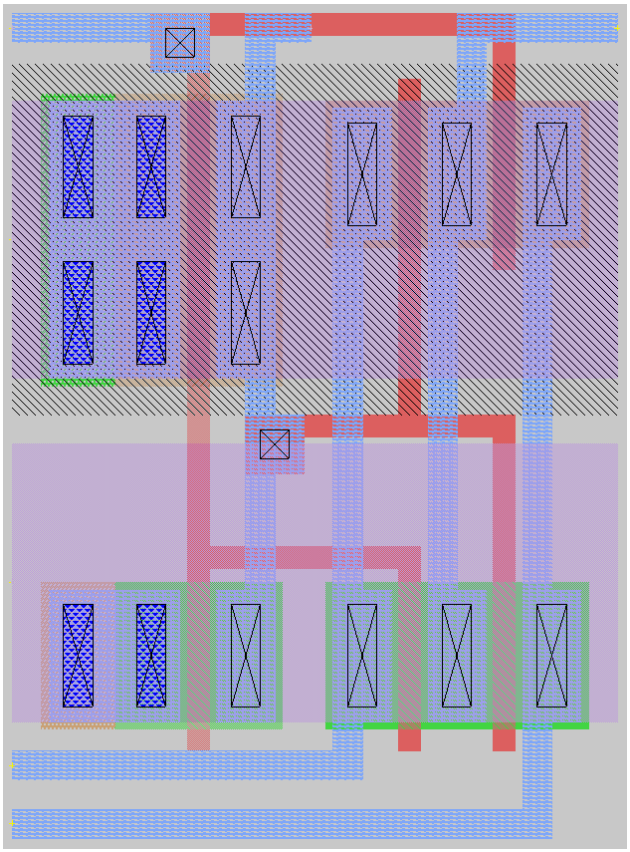

Figure 23: Layout of the multiplexer circuit.

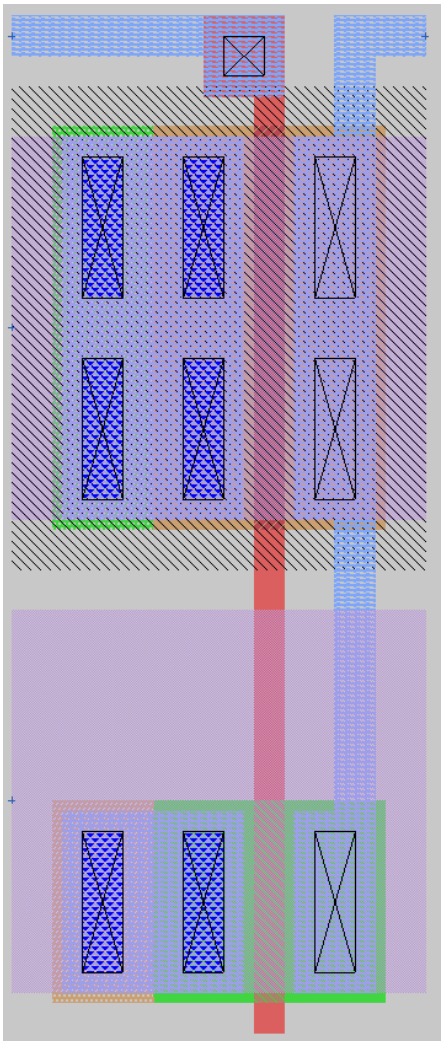

Figure 24: Layout of the inverter circuit.

4 Layout versus Schematic

Finally, we performed Layout-versus-Schematic comparison at all levels of the 7-bit digital-to-analog converter. There are three LVS listings below:

1. Layout versus Schematic for Bias Current and Ladder Gate Voltage Generating Circuits
2. Layout versus Schematic for Seven-bit M-2M Ladder
3. Layout versus Schematic for the pMOS section of the Low-Voltage Super-wilson

Listing 1: **Layout versus Schematic for Bias Current and Ladder Gate Voltage Generating Circuits**

```
Equate elements:  no current cell.
Equate elements:  no current cell.
Class layout/ibias_vg.spice:  Merged 61 devices.
Class schematic/LDS/ibias_vg_lvs.spice:  Merged 61 devices.
```

```
Subcircuit summary:
Circuit 1: layout/ibias_vg.spice|Circuit 2: schematic/LDS/ibias_vg_lvs.spice
--------------------------------|------------------------------------------
sky130_fd_pr__nfet_01v8 (26)    |sky130_fd_pr__nfet_01v8 (26)
sky130_fd_pr__pfet_01v8 (17)    |sky130_fd_pr__pfet_01v8 (17)
Number of devices: 43           |Number of devices: 43
Number of nets: 25              |Number of nets: 25
-----------------------------------------------------------------------------

Resolving automorphisms by property value.
Resolving automorphisms by pin name.
Netlists match uniquely.
Circuits match correctly.
Cells have no pins;  pin matching not needed.
Device classes layout/ibias_vg.spice
and schematic/LDS/ibias_vg_lvs.spice are equivalent.
Circuits match uniquely.
```

Listing 2: **Layout versus Schematic for Seven-bit M-2M Ladder**

```
Equate elements:  no current cell.
Class layout/dac_ladder.spice:  Merged 23 devices.
Class LVS/LVS/ladder/ladder_lds.spice:  Merged 23 devices.

Subcircuit summary:
Circuit 1: layout/dac_ladder.spice  |Circuit 2: LVS/LVS/ladder/ladder_lds.spice
------------------------------------|-------------------------------------------
sky130_fd_pr__nfet_01v8 (34)        |sky130_fd_pr__nfet_01v8 (34)
Number of devices: 34               |Number of devices: 34
Number of nets: 18                  |Number of nets: 18
-----------------------------------------------------------------------------

Circuits match uniquely.
Netlists match uniquely.
Cells have no pins;  pin matching not needed.
Device classes layout/dac_ladder.spice
and LVS/LVS/ladder/ladder_lds.spice are equivalent.
Circuits match uniquely.
```

Listing 3: **Layout versus Schematic for the pMOS section of the Low-Voltage Super-wilson**

```
Equate elements:  no current cell.
Class low-voltage_super-wilson_layout.spice:  Merged 11 devices.
Class low-voltage_super-wilson_LDS_pmos.spice:  Merged 11 devices.

Subcircuit summary:
Circuit 1: Layout               |Circuit 2: LDS
--------------------------------|-------------------------
sky130_fd_pr__pfet_01v8 (8)     |sky130_fd_pr__pfet_01v8 (8)
```

```
Number of devices: 8          |Number of devices: 8
Number of nets: 6             |Number of nets: 6
-------------------------------------------------------

Circuits match uniquely.
Netlists match uniquely.
Cells have no pins;  pin matching not needed.
Device classes low-voltage_super-wilson_layout.spice and
low-voltage_super-wilson_LDS_pmos.spice are equivalent.
Circuits match uniquely.
```

Listing 4: **Layout versus Schematic for the full seven bit DAC with biasing and output circuity**

```
Flattening unmatched subcell low-voltage_super-wilson in circuit dac7.spice (0)(1 i
Flattening unmatched subcell dac_ladder in circuit dac7.spice (0)(1 instance)
Flattening unmatched subcell dac_ladder_wilson in circuit dac7.spice (0)(1 instance
Flattening unmatched subcell ibias_vg in circuit dac7.spice (0)(1 instance)
Equate elements:  no current cell.
Equate elements:  no current cell.
Class inverter:  Merged 1 devices.

Subcircuit summary:
Circuit 1: inverter                       |Circuit 2: inverter
------------------------------------------|-----------------------------------------
sky130_fd_pr__nfet_01v8 (1)               |sky130_fd_pr__nfet_01v8 (1)
sky130_fd_pr__pfet_01v8 (1)               |sky130_fd_pr__pfet_01v8 (1)
Number of devices: 2                      |Number of devices: 2
Number of nets: 4 **Mismatch**            |Number of nets: 6 **Mismatch**
-------------------------------------------------------------------------------

NET mismatches: Class fragments follow (with fanout counts):
Circuit 1: inverter                       |Circuit 2: inverter


-------------------------------------------------------------------------------
Net: VN                                   |Net: VP
  sky130_fd_pr__nfet_01v8/(1|3) = 1       |  sky130_fd_pr__pfet_01v8/(1|3) = 1
  sky130_fd_pr__nfet_01v8/4 = 1           |
                                          |
Net: VP                                   |Net: VDD
  sky130_fd_pr__pfet_01v8/(1|3) = 1       |  sky130_fd_pr__pfet_01v8/4 = 1
  sky130_fd_pr__pfet_01v8/4 = 1           |
                                          |
(no matching net)                         |Net: VN
                                          |  sky130_fd_pr__nfet_01v8/(1|3) = 1
                                          |
(no matching net)                         |Net: GND
                                          |  sky130_fd_pr__nfet_01v8/4 = 1
-------------------------------------------------------------------------------

Netlists do not match.
```

```
  Flattening non-matched subcircuits inverter inverter
Subcircuit summary:
Circuit 1: mux2                                 |Circuit 2: mux2
------------------------------------------------|------------------------------------------------
sky130_fd_pr__nfet_01v8 (3)                     |sky130_fd_pr__nfet_01v8 (3)
sky130_fd_pr__pfet_01v8 (3)                     |sky130_fd_pr__pfet_01v8 (3)
Number of devices: 6                            |Number of devices: 6
Number of nets: 7                               |Number of nets: 7
------------------------------------------------------------------------------------------------
Circuits match uniquely.
Netlists match uniquely.

Subcircuit pins:
Circuit 1: mux2                                 |Circuit 2: mux2
------------------------------------------------|------------------------------------------------
B                                               |B
A                                               |A
muxout                                          |Y **Mismatch**
VP                                              |VDD **Mismatch**
S                                               |S
VN                                              |GND **Mismatch**
------------------------------------------------------------------------------------------------
Cell pin lists are equivalent.
Device classes mux2 and mux2 are equivalent.
Class dac7.spice:  Merged 125 devices.
Class dac_7_final_xschem.spice:  Merged 125 devices.

Subcircuit summary:
Circuit 1: dac7.spice                           |Circuit 2: dac_7_final_xschem.spice
------------------------------------------------|------------------------------------------------
sky130_fd_pr__pfet_01v8 (24)                    |sky130_fd_pr__pfet_01v8 (24)
sky130_fd_pr__nfet_01v8 (88)                    |sky130_fd_pr__nfet_01v8 (88)
mux2 (7)                                        |mux2 (7)
Number of devices: 119                          |Number of devices: 119
Number of nets: 58                              |Number of nets: 58
------------------------------------------------------------------------------------------------
Resolving automorphisms by property value.
Resolving automorphisms by pin name.
Netlists match uniquely.
Circuits match correctly.
Cells have no pins;  pin matching not needed.
Device classes dac7.spice and dac_7_final_xschem.spice are equivalent.
Circuits match uniquely.
```

Please note that the mismatch in the inverter portion of the LVS is due to differences in the difference between VDD and VP and GND and VN. This is apparent due to the use of three terminal devices, but is resolved at a higher level when we connect VP to VDD and VN to GND. The property mismatch shown at the very bottom of the listing is trivial because it is only in regards

to the size of a dummy transistor between two equivalent versions of the current bias generating circuits.