Lab 8: A Simple MOS Differential Amplifier

Thomas Jagielski and Sparsh Bansal

April 2020

1 Experiment 1: Voltage Transfer Characteristics

1.1 Background, Procedure and Model Expectations

For this experiment, we constructed a differential amplifier with a nMOS differential pair and a pMOS current mirror. We set the bias voltage so that the bias current was just at threshold. Then we connected V_2 to a constant voltage source and sweep V_1 from one rail to the other, measuring V_{out} for $V_2 = 2V, 3V,$ and $4V$ that are above the bias voltage. The following figure shows the schematic used for this experiment.

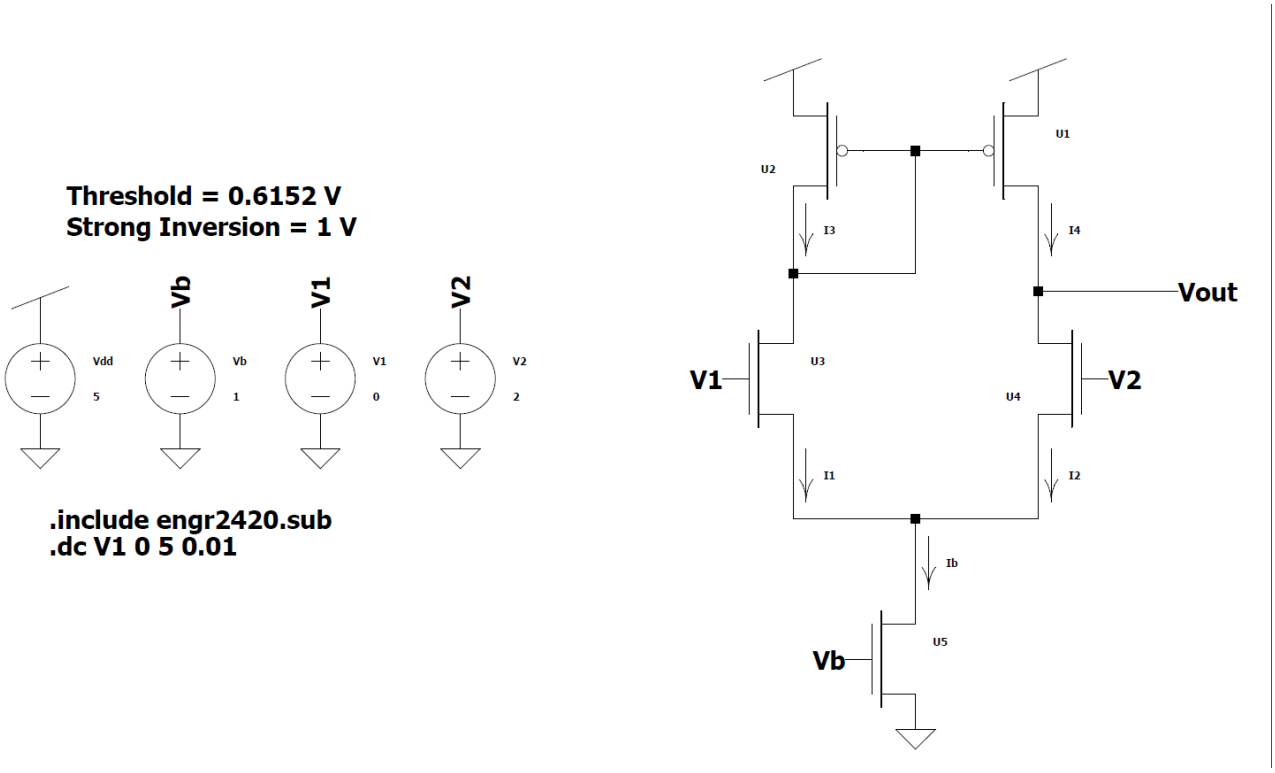

Figure 1: Circuit Schematic for Experiment 1

We then repeated these directions for an above threshold bias current.

1.2 Results

1.2.1 I_b at Threshold

The following figure shows the voltage transfer characteristics when sweeping V_1 from rail-to-rail and I_b is at threshold.

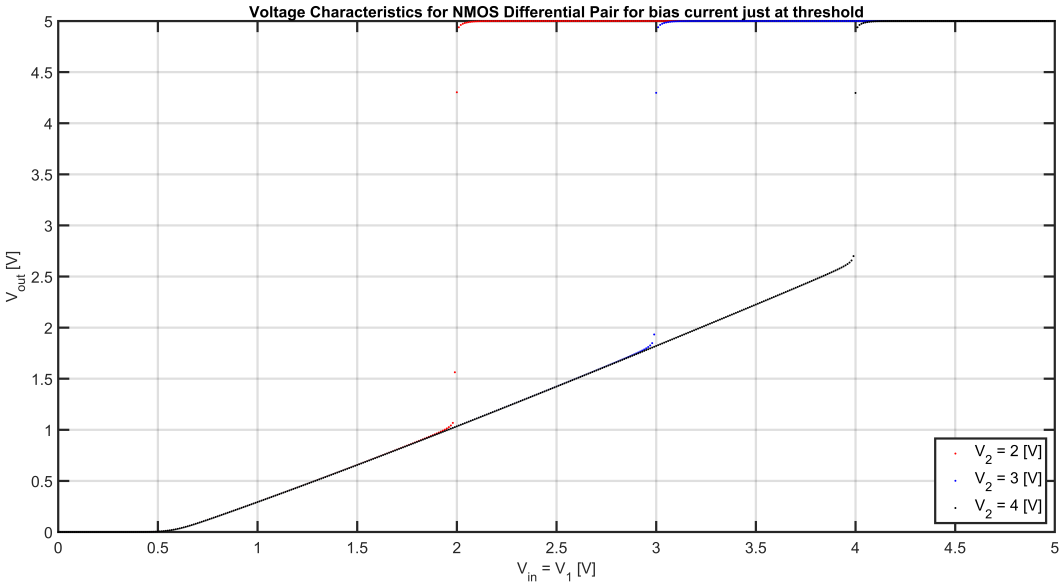

Figure 2: Voltage transfer characteristics for I_b at threshold

1.2.2 I_b Above Threshold

The next figure shows the voltage transfer characteristics when I_b is above threshold.

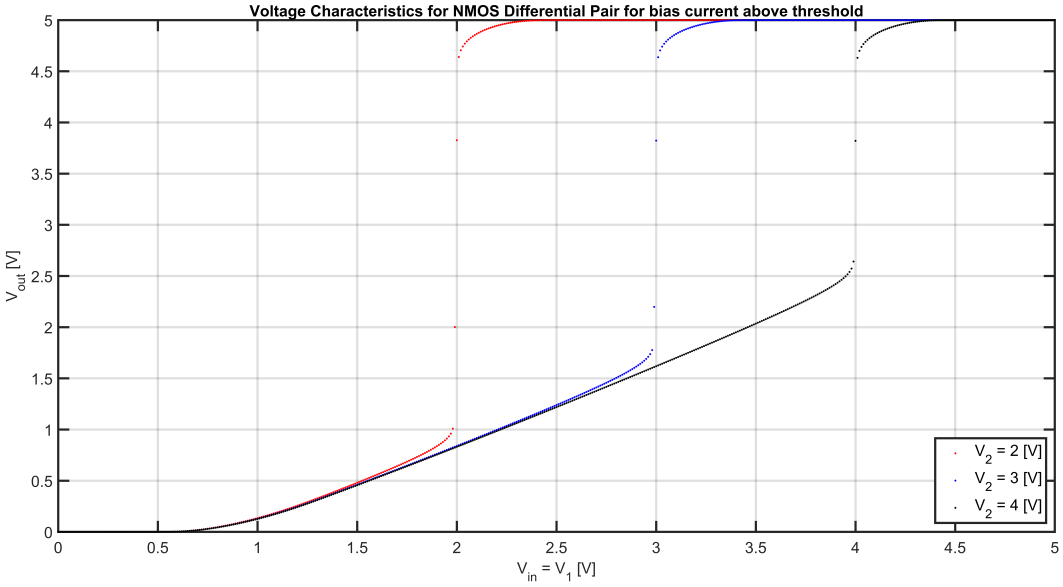

Figure 3: Voltage transfer characteristics for I_b above threshold

From this we can see that the voltage transfer characteristics are quite similar for when I_b is at threshold and in strong inversion. The differences include a larger slope when $V_{in} < V_2$ and the output voltage begins to transition to the gain region more gradually when I_b is above threshold. The transistion phase spans across a $\sim$100mV for the case when I_b is at threshold, whereas this span increases to $\sim$500mV for the case when I_b is above threshold.

2 Experiment 2: Transconductance, Output Resistance, and Gain

2.1 Background, Procedure and Model Expectations

For this experiment, we sweep V_1 around V_2 in fine increments, while measuring V_{out}, for a single value of V_2. We then fit a straight line to the steep part of the curve in order to determine the differential-mode voltage gain of the circuit.

Next, we set the differential-mode input voltage to zero and measure the current flowing into the output of the amplifier as we sweep V_{out} from one rail to the other. In order to determine the incremental output resistance of the circuit, we fit a straight line to the shallow part of this output current–voltage characteristic, which corresponds to the range of output voltages over which the gain of the circuit is large.

In the end, we fix the output voltage in the middle of the range of output voltages for which the circuit's gain is large and measure the current flowing out of the amplifier as we sweep V_1 around V_2. We then fit a straight line to the curve around where $V_1 = V_2$ and extract a value of the incremental transconductance gain of the circuit with the output voltage fixed from the slope of the best-fit line.

The incremental differential-mode voltage gain of the circuit can be written as

$$A_{dm} = \frac{\partial V_{out}}{\partial V_{dm}} = \frac{\partial V_{out}}{\partial I_{out}} . \frac{\partial I_{out}}{\partial V_{dm}} = R_{out} . G_m \tag{1}$$

The following figure shows the schematic of the circuit used during this experiment.

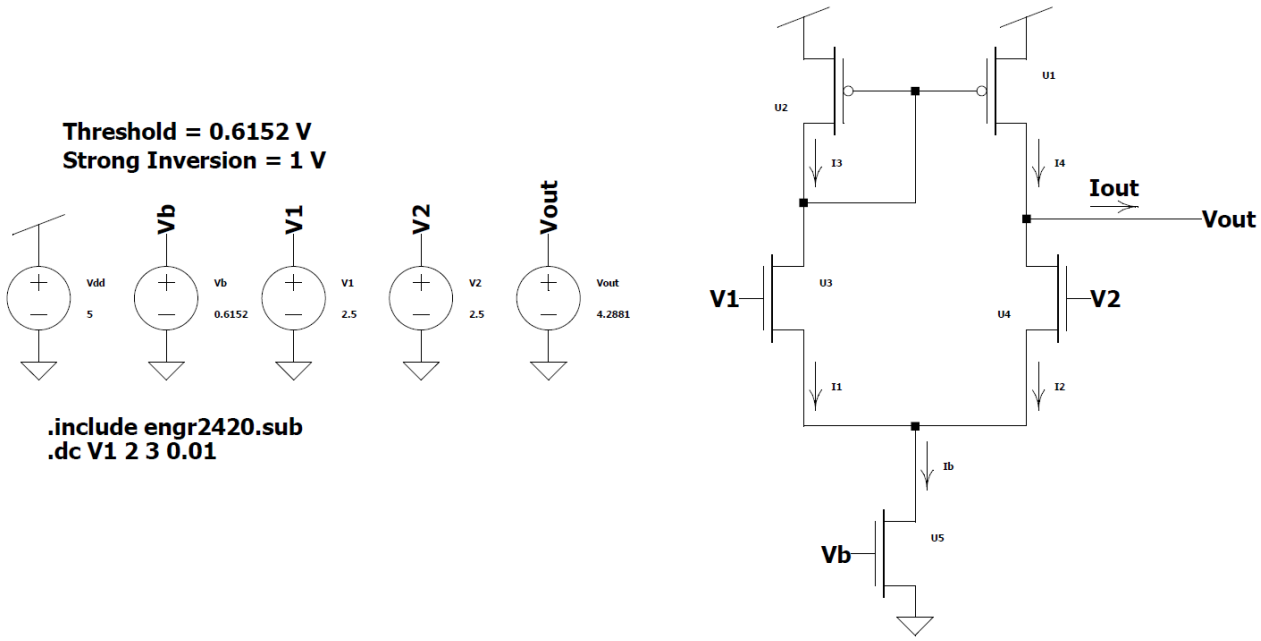

Figure 4: Schematic for Circuit Used in Experiment 2

2.2 Results

2.2.1 I_b at Threshold

Within this section, all results have the bias current set to threshold.

The following plot shows the output voltage of the differential amplifier when V_1 is near to $V_2 = 2.5V$.

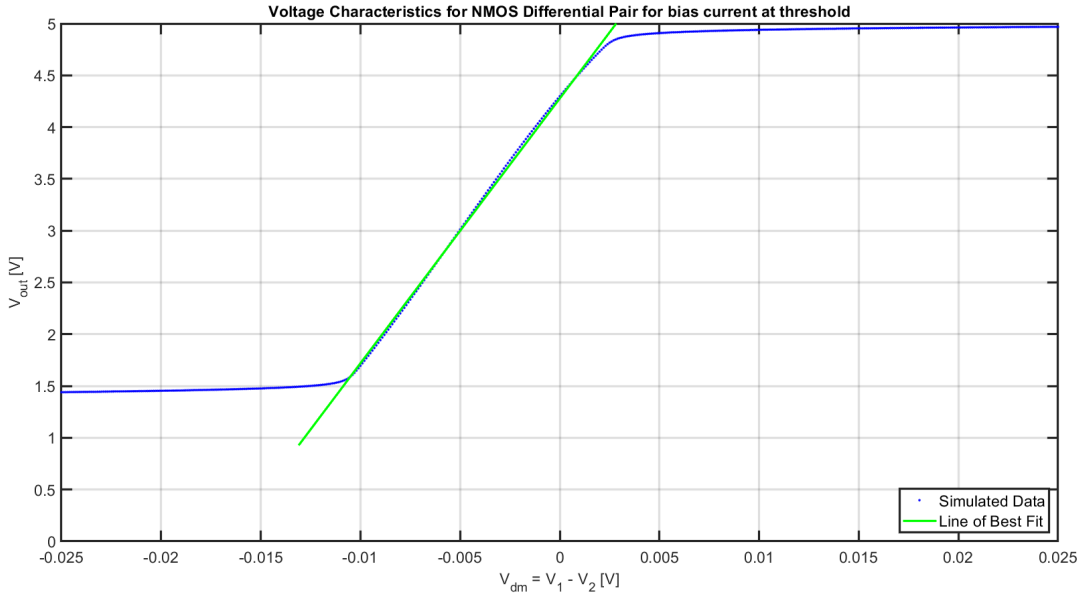

Figure 5: Voltage Transfer Characteristics for the NMOS Differential Pair with V_1 near $V_2 = 2.5V$

By finding the slope of the line when $V_1 \approx V_2$ we can find the differential-mode voltage gain to be 255.681.

The following figure shows the current flowing into the output of the amplifier while we sweep V_{out} from one rail to the other.

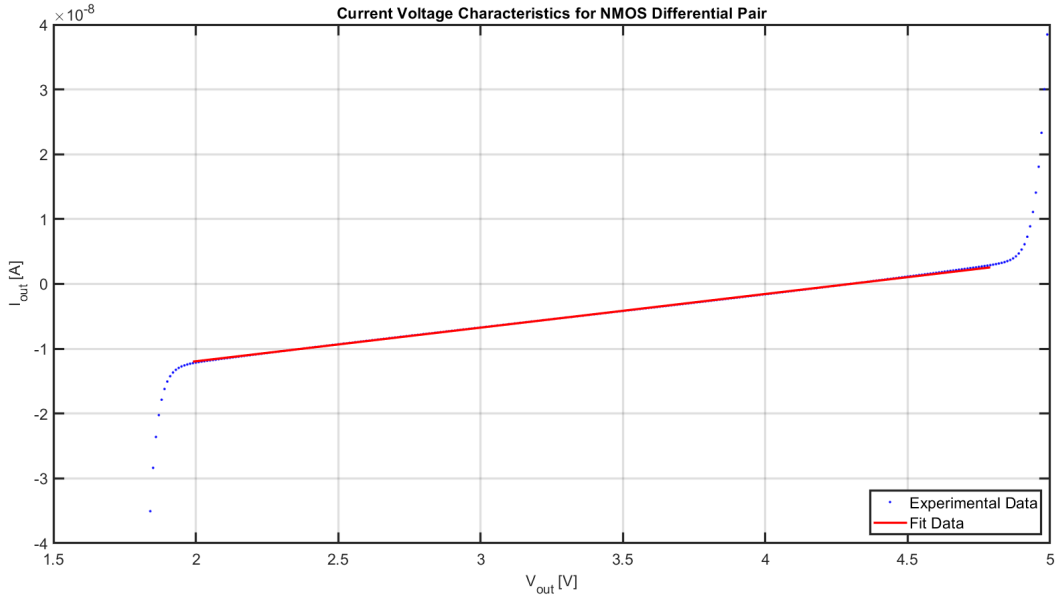

Figure 6: Current Voltage Characteristics for the NMOS Differential Pair While Sweeping V_{out}

Within this figure, we can find the slope of the line of best fit to be $5.1921 * 10^{-9}$ S or A/V. Which can be used to extract the incremental output resistance as $\frac{1}{Slope}$. Using this, we extract $R_{out} = 192.6M\Omega$. Additionally, we find the x-intercept to define the output voltage for finding the incremental transconductance gain of the circuit. We find the x-intercept to be 4.2984 V.

The following figure shows the current flowing out of the amplifier when sweeping V_1 close to V_2. From this we can extract the incremental transconductance gain of the circuit.

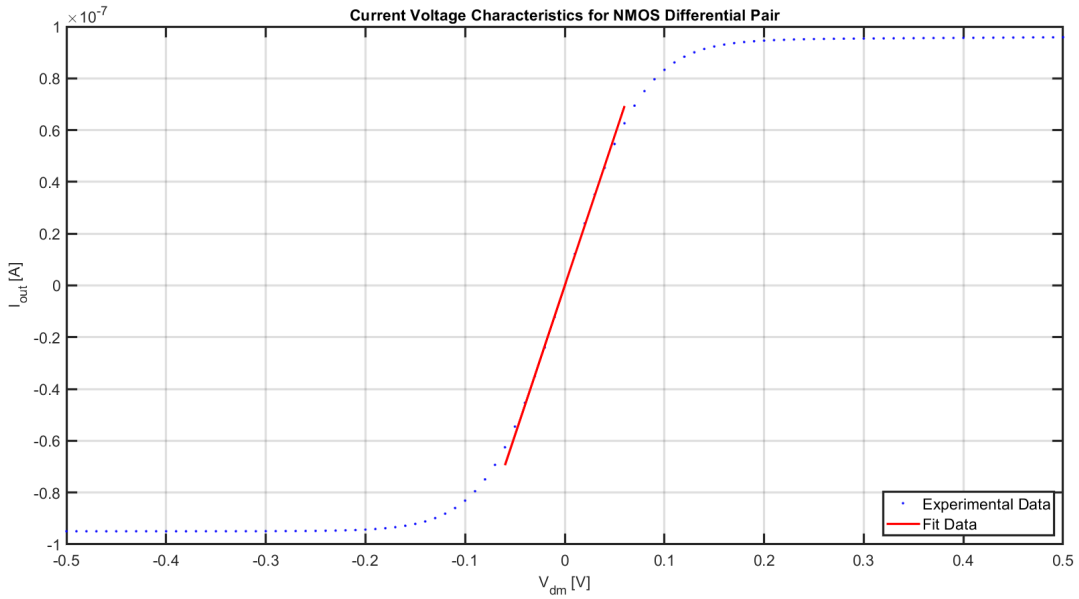

Figure 7: Current Voltage Characteristics for the NMOS Differential Pair While $V_{out} = 4.2984V$

By finding a line of best fit to the straight part of the curve, we can find the slope to be $1.157 * 10^{-6}$ S or A/V.

The following table shows the extracted parameters from each of the plots and the percent difference between the two extraction techniques for the differential-mode voltage gain of the differential pair circuit.

Differential-Mode Voltage Gain of Differential Pair Circuit with I_b at Threshold	
Parameter	Value
A_{dm} from V_{out} verses V_{dm} slope	255.681
Incremental Output Resistance (R_{out})	$192.6M\Omega$
Incremental Transconductance Gain (G_m)	$1.157 * 10^{-6}$ S or A/V
$A_{dm} = R_{out} * G_m$	222.7499
Absolute Percent Difference between A_{dm} from V_{out} verses V_{dm} slope and $A_{dm} = R_{out} * G_m$	12.8798 %

From this, we find that using $A_{dm} = R_{out} * G_m$ to find the differential-mode voltage gain does not match the A_{dm} value extracted from the slope of the V_{out} verses V_{dm} plot. There was an absolute percentage difference of 12.8798 %. When looking at the plots and extracting the values of R_{out} and G_m, our lines of best fit does not encapsulate all of the dynamics of the plots. We can see that the data does not perfectly following a linear fit which would account for some of this error.

2.2.2 I_b Above Threshold

Within this section, all results have the bias current set above threshold.

The following plot shows the output voltage of the differential amplifier when V_1 is near to $V_2 = 2.5V$.

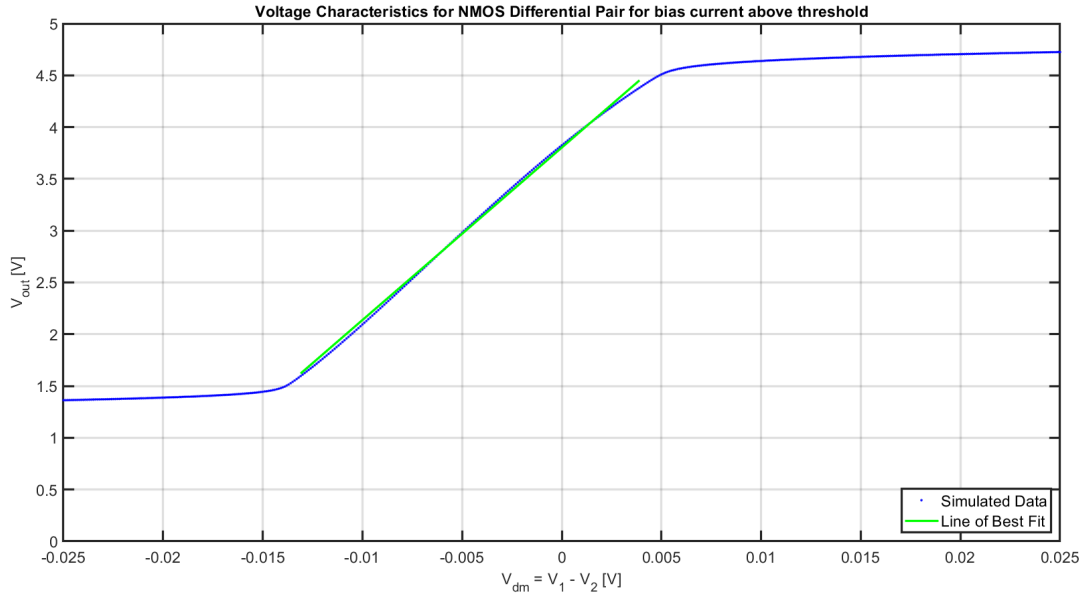

Figure 8: Voltage Transfer Characteristics for the NMOS Differential Pair with V_1 near $V_2 = 2.5V$

By finding the slope of the line when $V_1 \approx V_2$ we can find the differential-mode voltage gain to be $A_{dm} = 166.498$.

The following figure shows the current flowing into the output of the amplifier while we sweep V_{out} from one rail to the other.

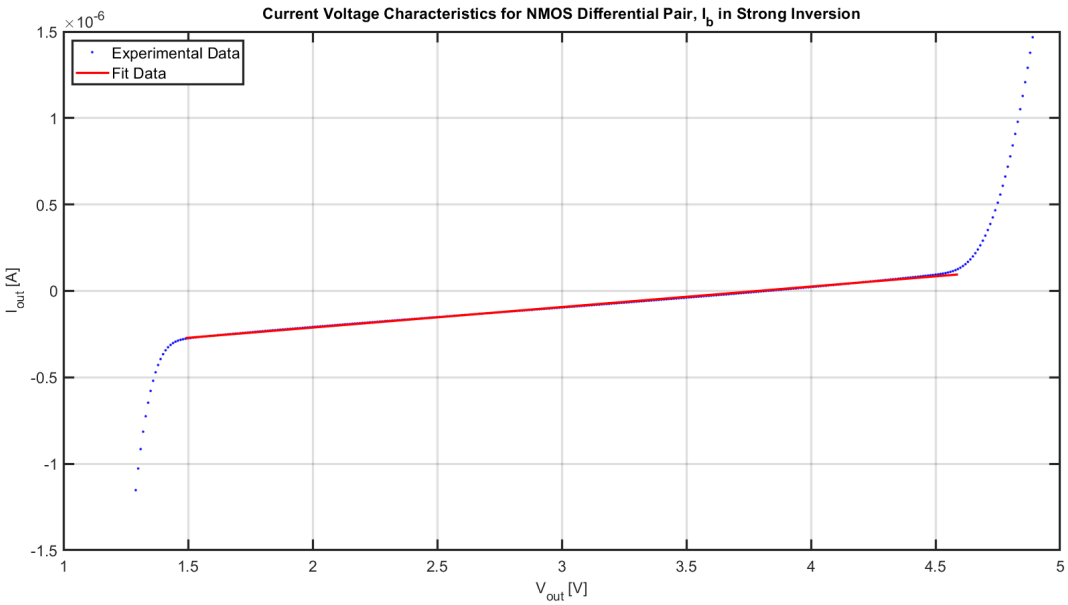

Figure 9: Current Voltage Characteristics for the NMOS Differential Pair While Sweeping V_{out}

Within this figure, we can find the slope of the line of best fit to be $1.1857 * 10^{-7}$ S. Which can be used to extract the incremental output resistance as $\frac{1}{Slope}$. Using this, we extract $R_{out} = 8.434M\Omega$. Additionally, we find the x-intercept to define the output voltage for finding the incremental transconductance gain of the circuit. We find the x-intercept to be 3.787 V.

The following figure shows the current flowing out of the amplifier when sweeping V_1 close to V_2. From this we can extract the incremental transconductance gain of the circuit.

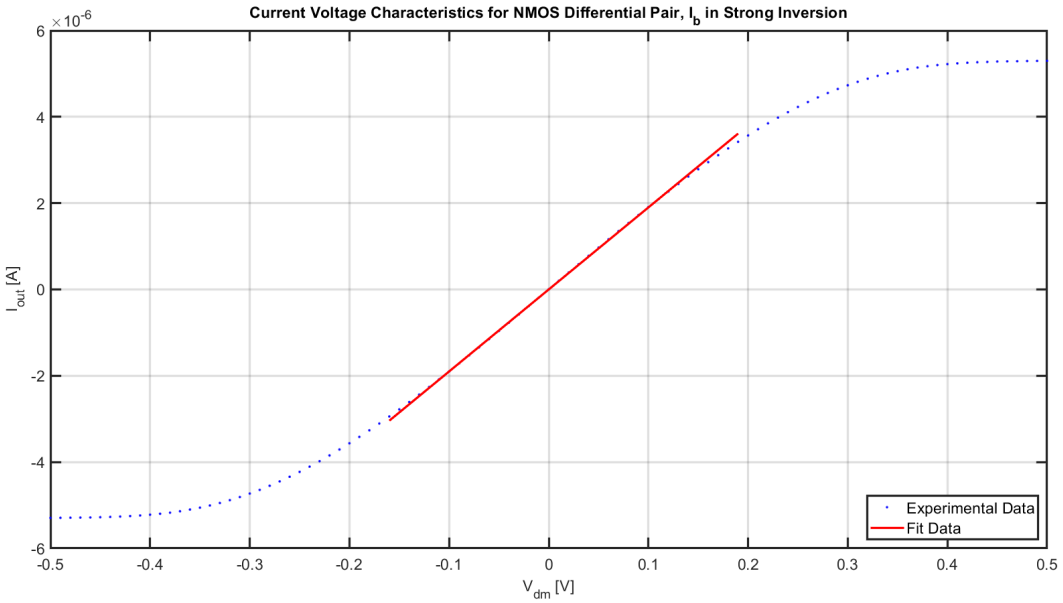

Figure 10: Current Voltage Characteristics for the NMOS Differential Pair While $V_{out} = 3.7870V$

By finding a line of best fit to the straight part of the curve, we can find the slope to be $1.9011 * 10^{-5}$ S or A/V.

Differential-Mode Voltage Gain of Differential Pair Circuit with I_b in Strong Inversion	
Parameter	Value
A_{dm} from V_{out} verses V_{dm} slope	166.498
Incremental Output Resistance (R_{out})	$8.434M\Omega$
Incremental Transconductance Gain (G_m)	$1.9011 * 10^{-5}$ S or A/V
$A_{dm} = R_{out} * G_m$	160.3321
Absolute Percent Difference between A_{dm} from V_{out} verses V_{dm} slope and $A_{dm} = R_{out} * G_m$	3.7033 %

From this, we find that the using $A_{dm} = R_{out} * G_m$ to find the differential-mode voltage gain matches the A_{dm} value extracted from the slope of the V_{out} verses V_{dm} plot quite well. There was an absolute percentage difference of 3.7033 %. Therefore, we find that both methods to find A_{dm} are quite similar to one another.

3 Experiment 3: Unity-Gain Follower

3.1 Background, Procedure and Model Expectations

In this experiment, we configure the NMOS differential pair amplifier as a unity-gain follower by connecting the output to the inverting input terminal. We then measure V_{out} as we sweep V_{in} from one rail to the other. We then can consider the offset voltage of the amplifier by plotting $V_{out} - V_{in}$ verses V_{in}.

For this experiment, the following schematic was used,

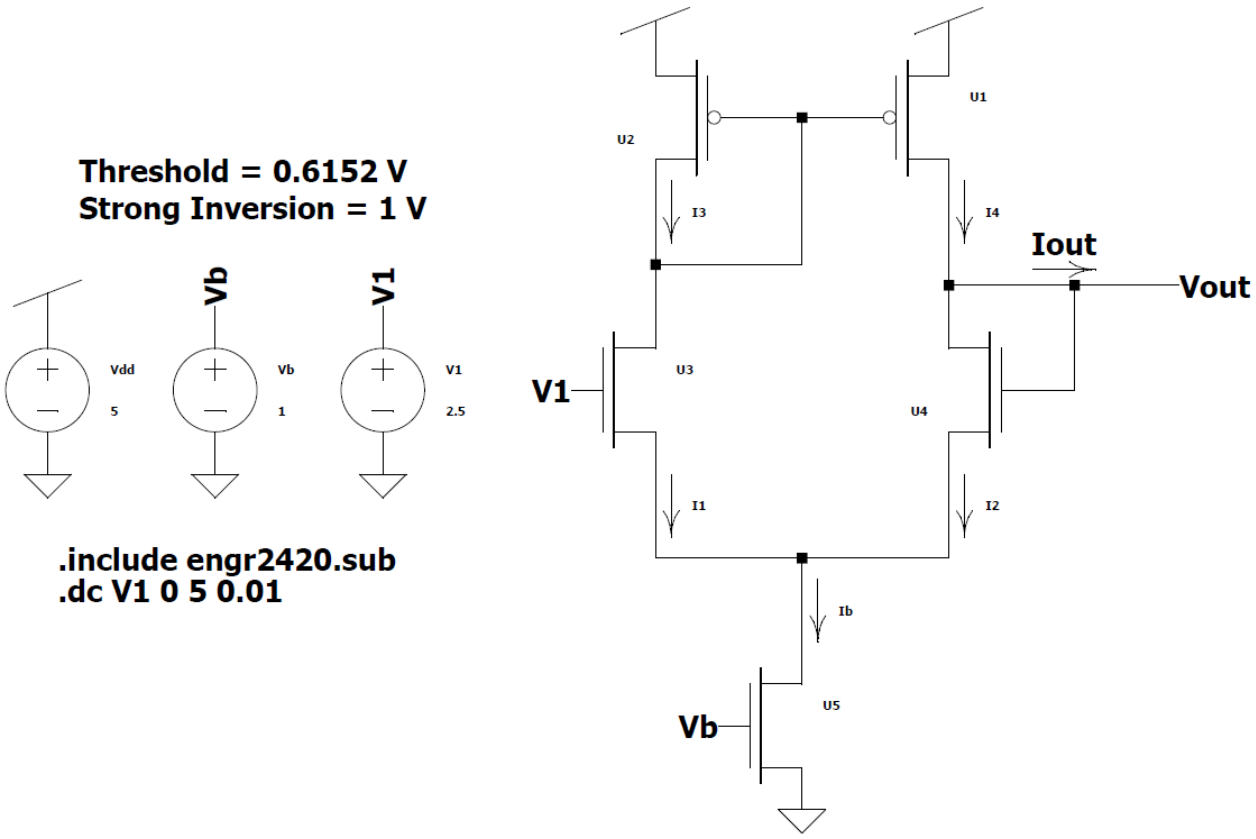

Figure 11: Schematic of Circuit Used in Experiment 3

Please note that if using the SMU we could measure $V_{out} - V_{in}$ directly by putting a current source across V_{out} and V_1 and measure the voltage across the terminals.

3.2 Results

3.2.1 I_b at Threshold

Within this section, all results have the bias current set to threshold.

The following plot shows the voltage transfer characteristics for a unity gain follower circuit when we sweep V_{in} from one rail to the other.

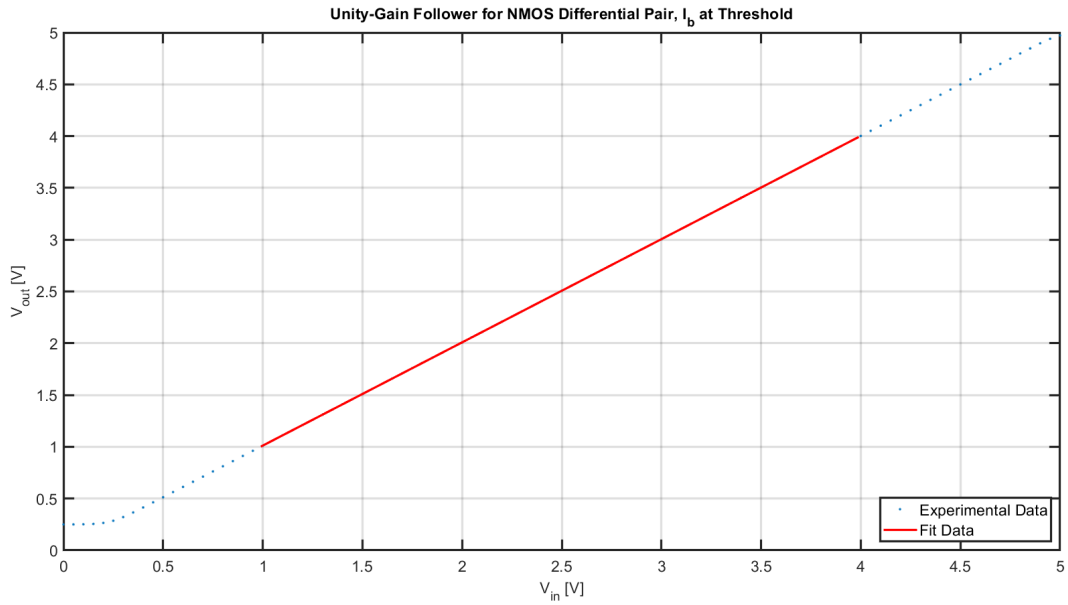

Figure 12: Voltage Transfer Characteristics for Unity-Gain Follower

By fitting a line of best fit to the data we can extract the slope (the gain of the circuit) to be 0.9968. Being a unity-gain follower, we expected this value to be 1. However, these two values are quite close to one another. Our simulated data has an absolute percentage error from the expected value of ~ 0.32 %.

The following plot shows the offset voltage of the amplifier.

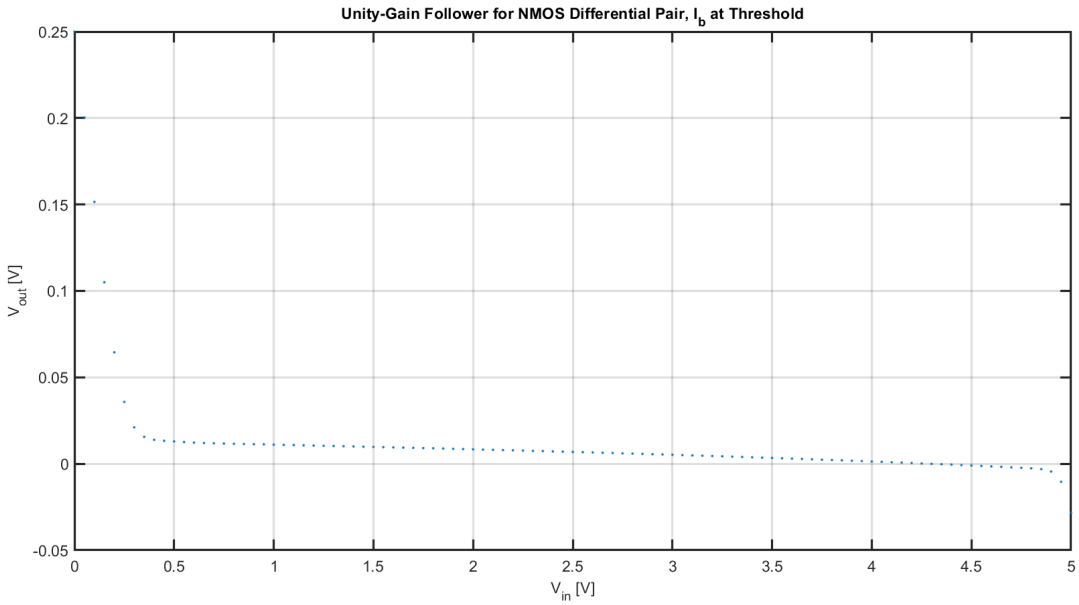

Figure 13: Offset Voltage of Amplifier ($V_{out} - V_{in}$ verses V_{in})

From this, we can see that the offset voltage of the amplifier decreases as we increase V_{in}. Within the range of 0.5 V and 4.5 V, we find the offset voltage decreases with a linear relationship. However, as V_{in} increases to near the positive rail, the offset voltage drops significantly more rapidly than the linear relationship. Similarly, we find that when V_{in} is near the bottom power rail, the offset voltage decreases more rapidly than the linear relationship. This could

be a result of the turn on voltage of the devices. We find that the offset voltage is above zero when $V_{in} <\sim 4.3V$. Beyond this, the offset voltage is negative.

3.2.2 I_b Above Threshold

Within this section, all results have the bias current set above threshold.

The following plot shows the voltage transfer characteristics for a unity gain follower circuit when we sweep V_{in} from one rail to the other.

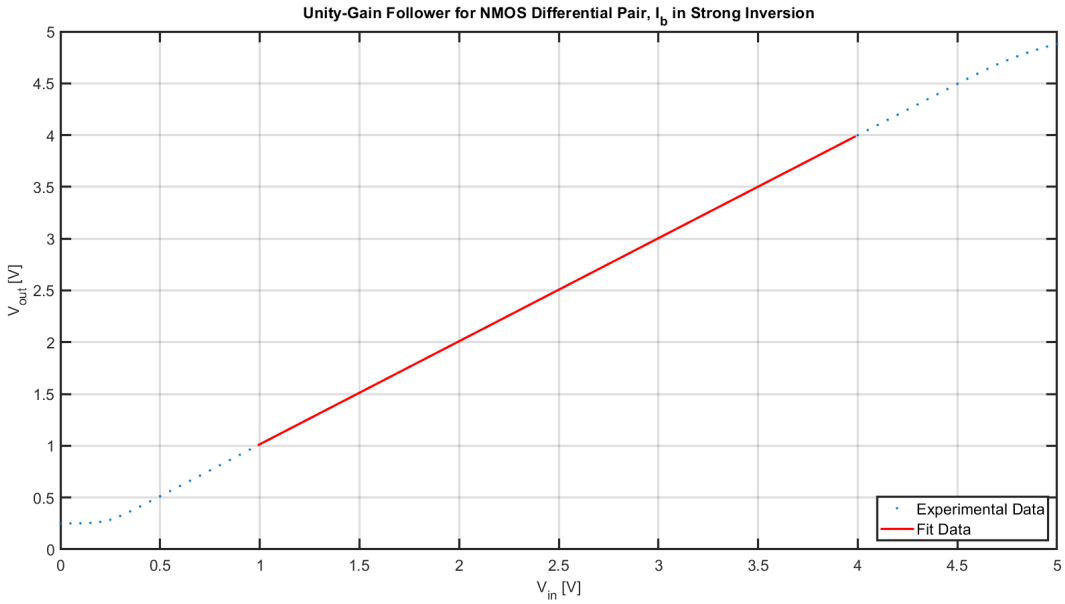

Figure 14: Voltage Transfer Characteristics for Unity-Gain Follower

By finding a line of best fit, we can extract the gain of the circuit as the slope of this line. We find this value to be 0.9950. Being a unity-gain follower, we expect this value to be one. However, there is only an absolute percentage difference between the extracted value and the theoretical value of 0.4961 %. So this is a quite accurate incremental gain compared to what we expect.

The following figure shows the offset voltage of the unity-gain follower when I_b is above threshold.

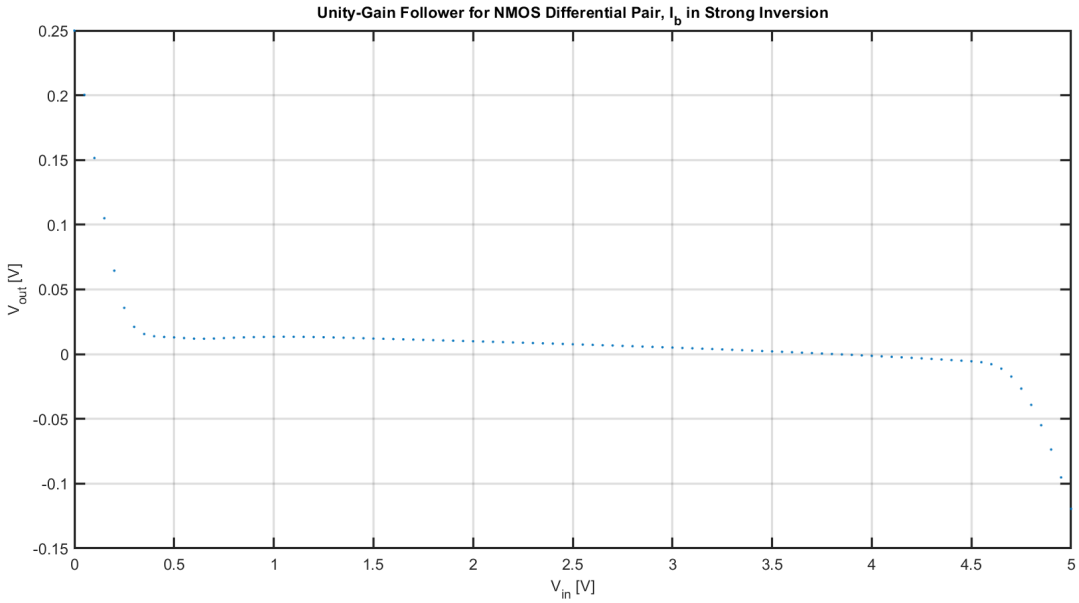

Figure 15: Offset Voltage of Amplifier ($V_{out} - V_{in}$ verses V_{in})

Similar to when the bias current was at threshold, the offset voltage of the unity-gain follower circuit when the bias current is above threshold behaves similarly. We find there to be a fairly linear relationship when $0.3V < V_{in} < 4.5V$. We find the offset to be positive when $V_{in} <\sim 3.8V$. Beyond this, the offset voltage is negative. This matches with Figure 14 as we can see V_{out} begin to bend downwards and break the linear relationship around this value. Further, we can see the initial offset in the voltage as a result of the turn on characteristics of the devices.