Lab 7: The MOS Differential Pair

Thomas Jagielski and Sparsh Bansal

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1 Experiment 1: Differential Pair I-V Characteristics

1.1 Background, Procedure and Model Expectations

For this lab, we made a nMOS differential pair (as shown in the circuit below).

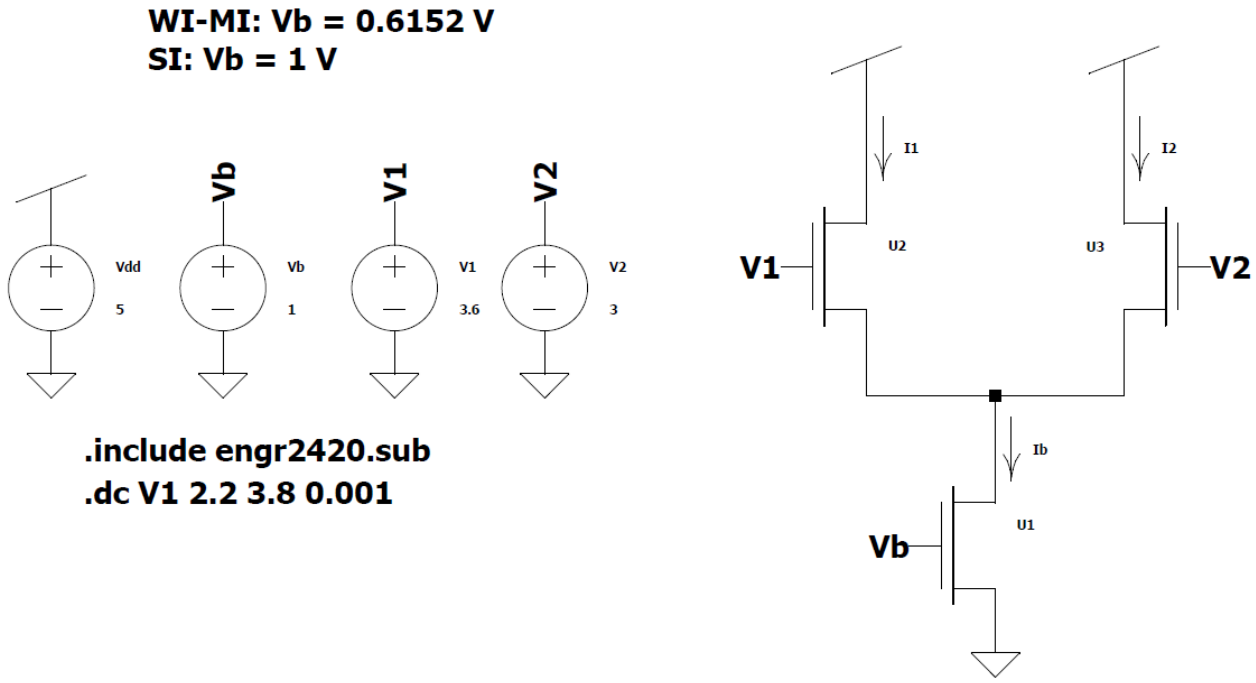

Figure 1: nMOS Differential Pair Schematic

We set the bias voltage (V_b), so the bias current is at or just below threshold. We then set V_2 to ensure the bias transistor is saturated, and sweep V_1 from a few tenths of a volt below V_2 to a few tenths of a volt above V_2. We then repeat the measurements for other values of V_2.

For analysis we looked at the value of I_1, I_2, $I_1 - I_2$, an $I_1 + I_2$ as a function of the difference in V_1 and V_2. We also looked at the common node voltage as a function of the difference in V_1 and V_2.

The incremental differential-mode transconductance gain of the differential pair can be given by,

$$G_{dm} = \frac{\partial I_{dm}}{\partial V_{dm}}\Big|_{V_{dm}=0} = \frac{\partial I_1 - I_2}{\partial V_1 - V_2}\Big|_{V_1=V_2} \tag{1}$$

However, we approximated the incremental differential-mode transconductance gain, by fitting a straight line to the plot of $I_1 - I_2$ as a function of $V_1 - V_2$ around the region where $V_1 \approx V_2$.

We repeated parts of the analysis for when the bias voltage was set above threshold.

The V_b we used in the threshold/sub-threshold region was $V_b = 0.6152V$. We used V_2 values of 2 V, 3 V, and 4 V and swept V_1 from $V_2 \pm 0.4V$.

When V_b was above threshold, we used $V_b = 1V$. We set $V_2 = 3V$ and swept V_1 from $V_2 \pm 0.8V$.

1.2 Results and Discussion

The following figure shows the results for the various current-voltage characteristics for the nMOS differential pair with I_b set at threshold or just below. The plot shows the results for the three values of V_2 that we used (2 V, 3 V, and 4 V).

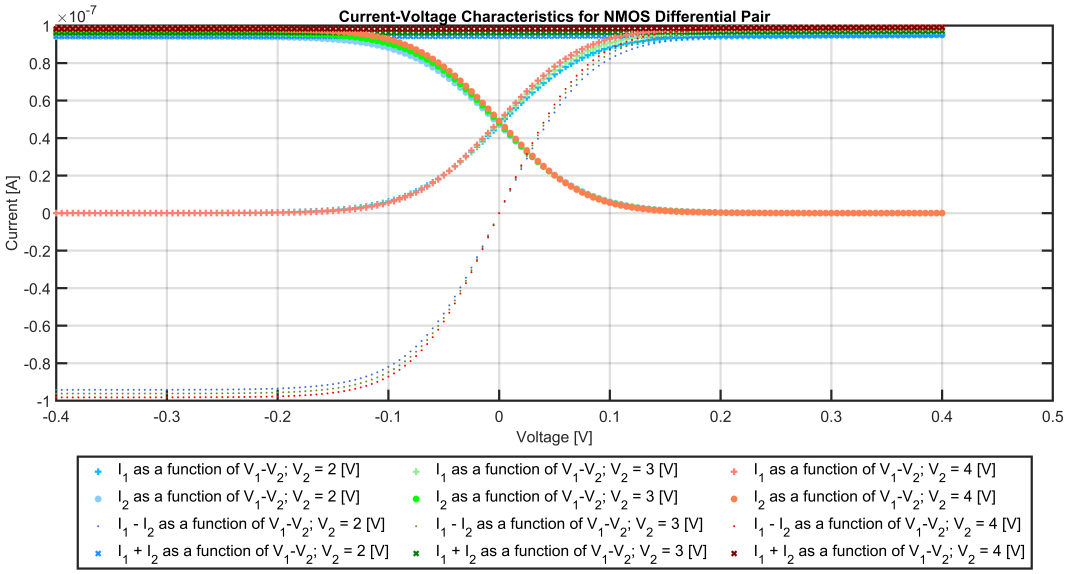

Figure 2: Current-Voltage Characteristics for nMOS Differential Pair, with the bias current just at threshold

In this plot, we can see that the current-voltage characteristics in each situation do no differ much. In general, when V_2 is set higher, the current level is also slightly higher by a visible difference (of $\sim$ 10 nA for all cases when V_1 and V_2 are far apart). When $V_1 \approx V_2$, the current levels converge to very similar magnitudes.

We found the slope in the region when $V_1 \approx V_2$, for the $I_1 - I_2$ characteristics as a function of $V_1 - V_2$, to find an approximate incremental differential-mode transconsuctance gain. The following table shows the slope for each of the values of V_2.

Extracted Incremental Differential-Mode Transconductance Gain		
V_2 Value [V]	Incremental Differential-Mode Transconductance Gain [S]	Absolute Error from the Mean [%]
$V_2 = 2$ V	$1.12 * 10^{-6}$ S	4.07 %
$V_2 = 3$ V	$1.17 * 10^{-6}$ S	0.33 %
$V_2 = 4$ V	$1.21 * 10^{-6}$ S	3.73 %

We can see that the slope slightly increases as we increase the value of V_2. However, the overall characteristics and slope does not change much for the different values of V_2. There is less than 5% error for each value of V_2 when considering the the error as the percent deviation from the averaged value of slope.

The next figure shows the node voltage as a function of the difference in the voltages $(V_1 - V_2)$.

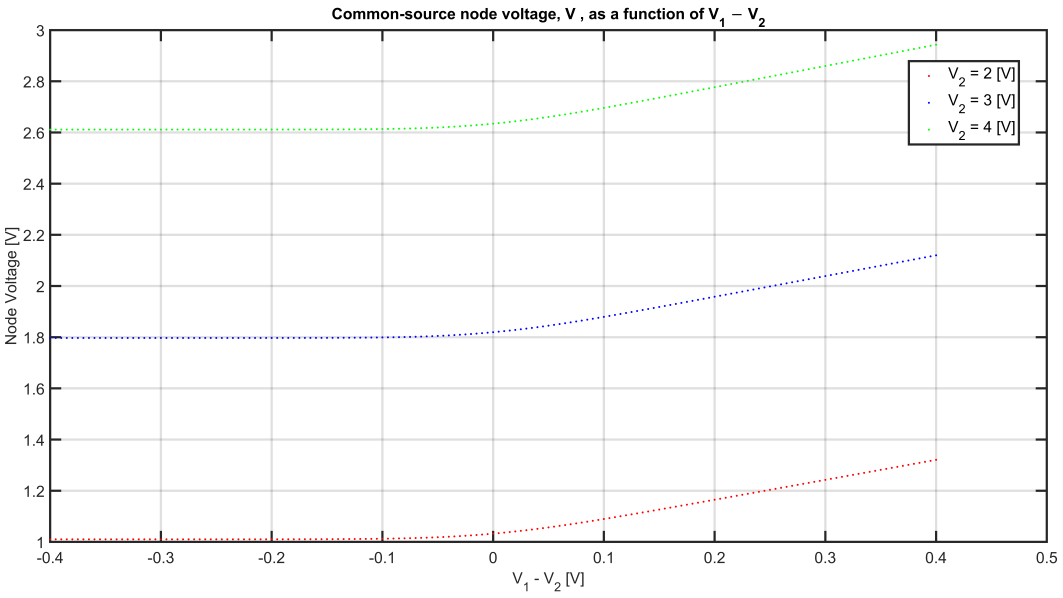

Figure 3: Common-Source node voltage (V) as a function of $V_1 - V_2$

From this figure, we can see that the node voltage is constant when $V_2 > V_1$. As the values of V_1 and V_2 approach one another (V_1 is less than V_2 by 0.5 V), the node voltage begins to slightly increase. We find, that there is a difference of $U_T * log(2)$ between the value of $V_1 - V_2$ and the constant voltage level from when $V_2 > V_1$. As we continue and V_1 becomes greater than V_2, we can see that the node voltage begins to increase as we increase V_1 and hold V_2 constant. We can find the slope of this line to be κ. There is also an offset in the initial node voltage value based on the voltage of V_2. For an increase of 1 V in V_2, the node voltage level (when $V_2 > V_1$) will increase by 0.8 V. Further, the level at which the node voltage will start at can be given by $\kappa(V_2 - V_1)$

The next figure shows the current-voltage characteristics for the nMOS differential pair when I_b is above threshold.

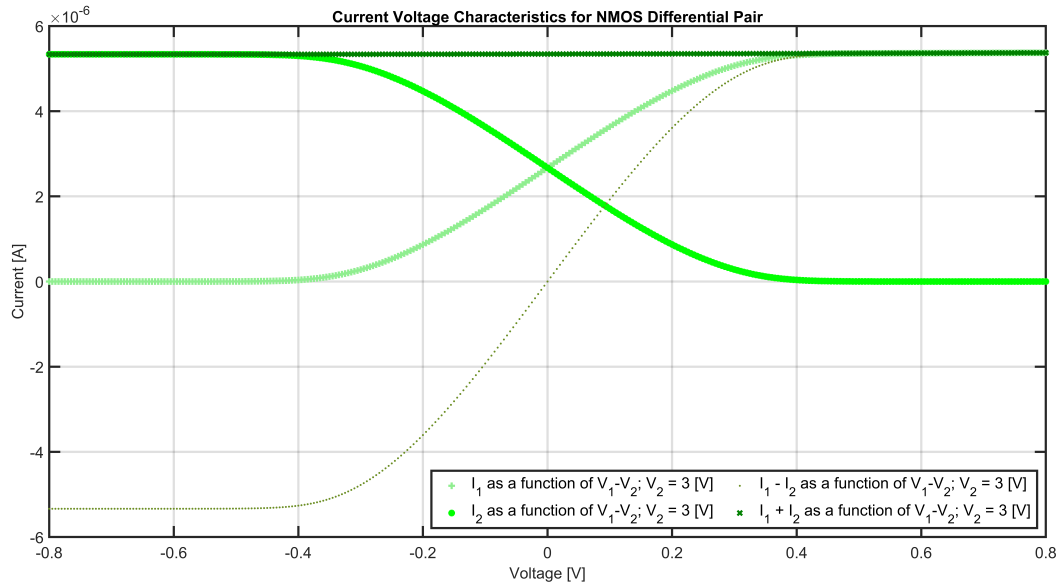

Figure 4: Current-Voltage Characteristics for nMOS Differential Pair, with the bias current over threshold

We can see that qualitatively, the current-voltage characteristics are similar to that of when I_b was at or slightly below threshold. The major difference is the range of current levels we are operating at. There is much more current, and a much larger current (~ 60 times the current), as we sweep V_1. However, we find the y-intercepts to be the same for both graphs. I_1 and I_2, both have an intercept of $\frac{I_b}{2}$. $I_1 - I_2$ has a y-intercept of 0 V. This is what we found when V_b was set to threshold.

The next figure shows the node voltage as a function of the difference in V_1 and V_1 $(V_1 - V_2)$ when I_b is above threshold.

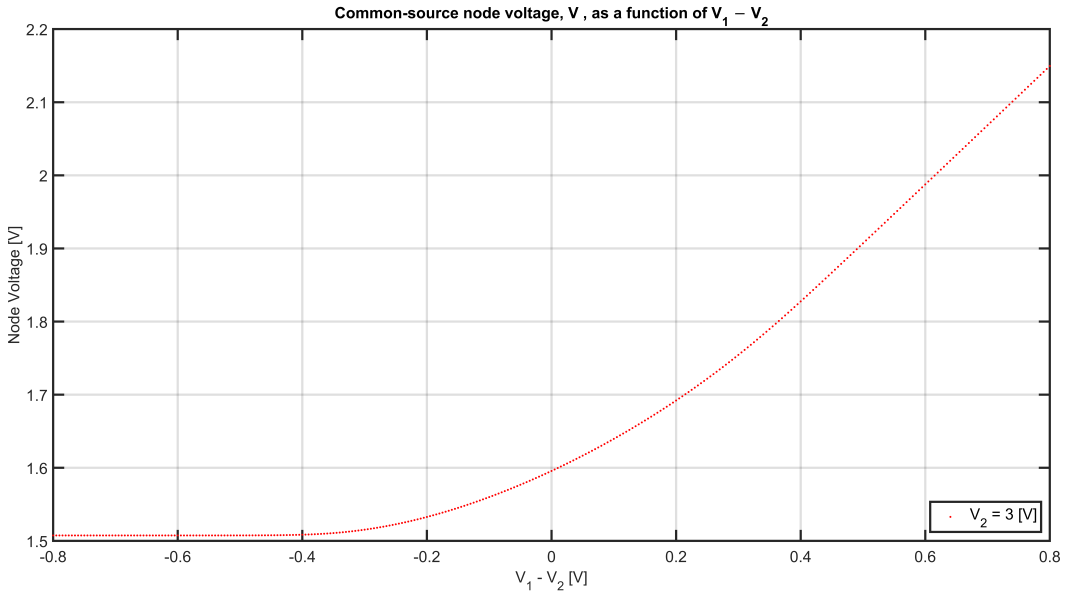

Figure 5: Common-Source node voltage (V) as a function of $V_1 - V_2$

Qualitatively, the graph does not differ much from when I_b was at threshold. There are two qualitative differences, the node voltage begins to increase when the difference in V_1 and V_2 is

much larger (V_2 is 0.4 V above V_1), and the rate by which the node voltage increases is slightly more than when I_b was at threshold.