

Lab 5: MOS Transistor Characteristics

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1 Experiment 1: Gate Characteristics

1.1 Background, Procedure and Model Expectations

For this experiment, we ran a DC simulation for an nMOS transistor, specifically one on an ALD1106 transistor array to obtain channel current as a function of gate voltage. We controlled the source voltage to be at ground and the drain voltage sufficiently far enough above ground to guarantee that the transistor remains in saturation.

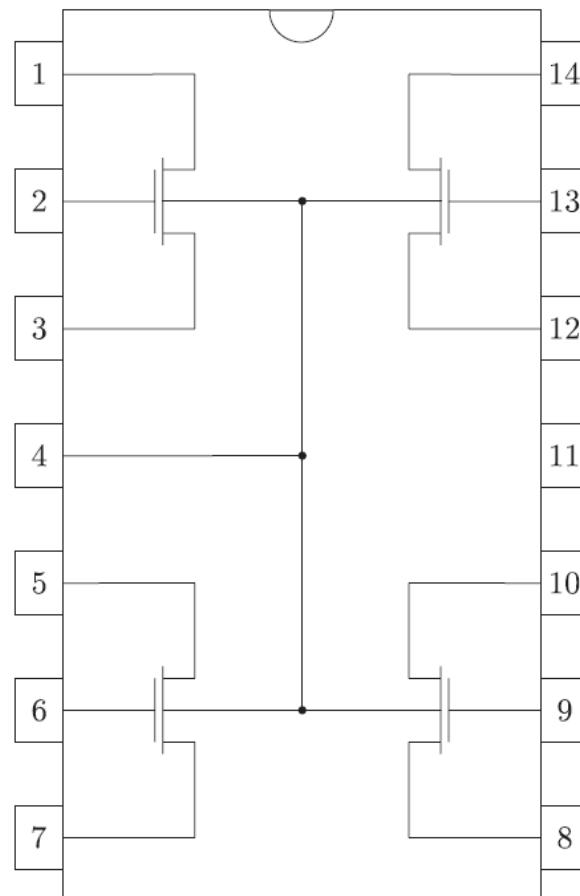


Figure 1: ALD1106 Array of nMOS Transistor in n-well technology

The circuit schematic that we used for the simulation is also presented below.

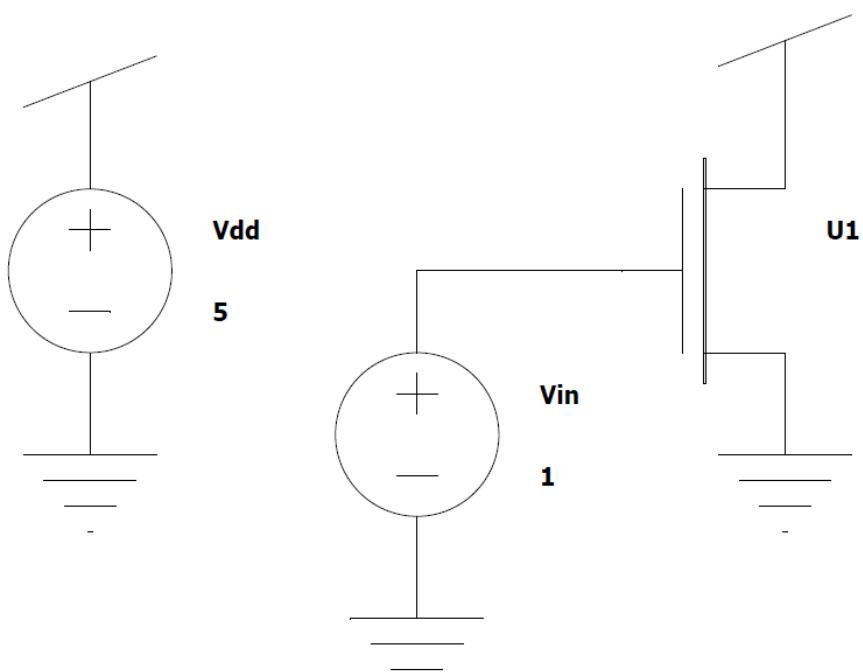


Figure 2: Circuit Schematic for experiment 1 with the nMOS transistor

To observe the analog of this data on a pMOS transistor, we conducted a similar DC simulation for a pMOS transistor, specifically one on an ALD1107 transistor array to obtain channel current as a function of gate voltage with the source voltage set to V_{dd} and the drain voltage sufficiently far enough below V_{dd} to guarantee that the transistor remains in saturation.

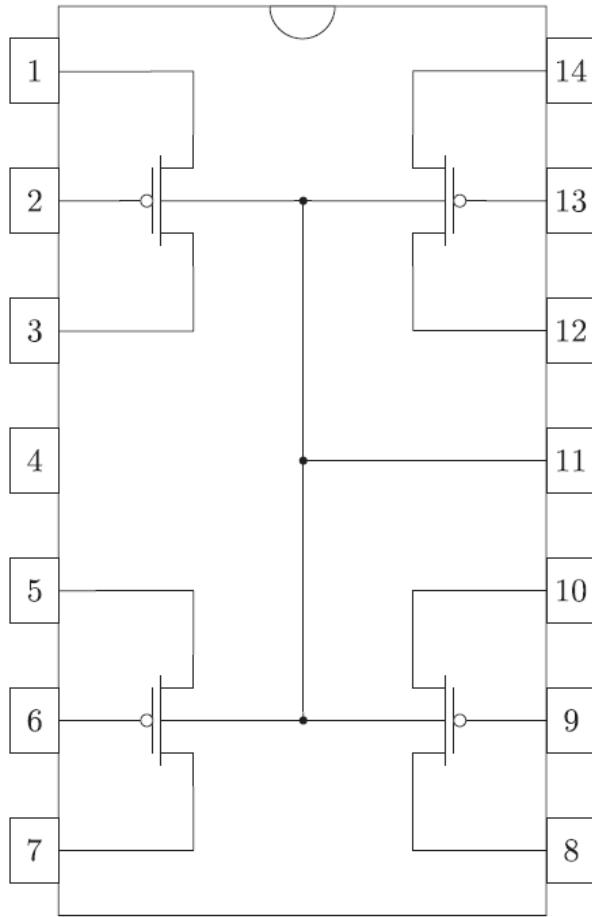


Figure 3: ALD1107 Array of pMOS Transistor in n-well technology

The circuit schematic that we used for the simulation is also presented below.

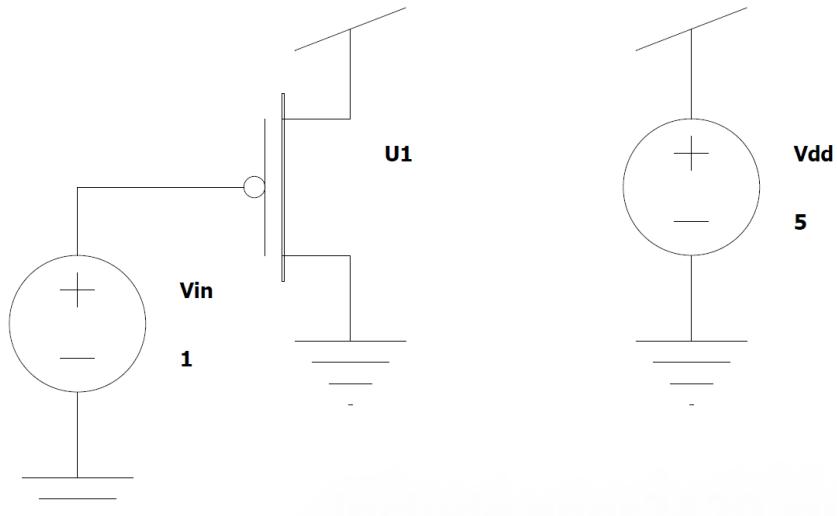


Figure 4: Circuit Schematic for experiment 1 with the pMOS transistor

We then used MATLAB to fit the EKV model to each of the simulated current-voltage characteristics, and extracted the values of Specific Current (I_s), Reciprocal subthreshold slope

factor (κ), and Zero-bias threshold voltage (V_{TO}). According to the EKV model, the relationship between the saturation current and the gate voltage is presented in the following equations.

$$I_{sat-nMOS} = I_s \left(\log \left(1 + e^{\left(\frac{\kappa(V_G - V_{TO}) - V_S}{2U_T} \right)} \right) \right)^2 \quad (1)$$

$$I_{sat-pMOS} = I_s \left(\log \left(1 + e^{\left(\frac{\kappa((V_{DD} - V_G) - V_{TO}) - (V_{DD} - V_S)}{2U_T} \right)} \right) \right)^2 \quad (2)$$

Additionally, we extracted each transistor's incremental transconductance gain (g_m) for both, the weak and the strong inversion regions.

$$g_m = \kappa \frac{\sqrt[2]{I_s I_{sat}}}{U_T} \left(1 - e^{-\sqrt[2]{\frac{I_{sat}}{I_s}}} \right) \quad (3)$$

For the case of weak inversion, using the approximation $I_{sat} \ll I_s$, we can derive the incremental transconductance gain to be

$$g_m = \kappa \frac{I_{sat}}{U_T} \quad (4)$$

For the case of strong inversion, using the approximation $I_{sat} \gg I_s$, we can derive the incremental transconductance gain to be

$$g_m = \kappa \frac{\sqrt[2]{I_s I_{sat}}}{U_T} \quad (5)$$

1.2 Results and Discussion

The following figure shows the channel current characteristics for varying gate voltage for both a NMOS and PMOS transistor. In order to extract parameters using the EKV model with the PMOS transistor, we defined the gate voltage as,

$$V_G = V_{DD} - V_{in} \quad (6)$$

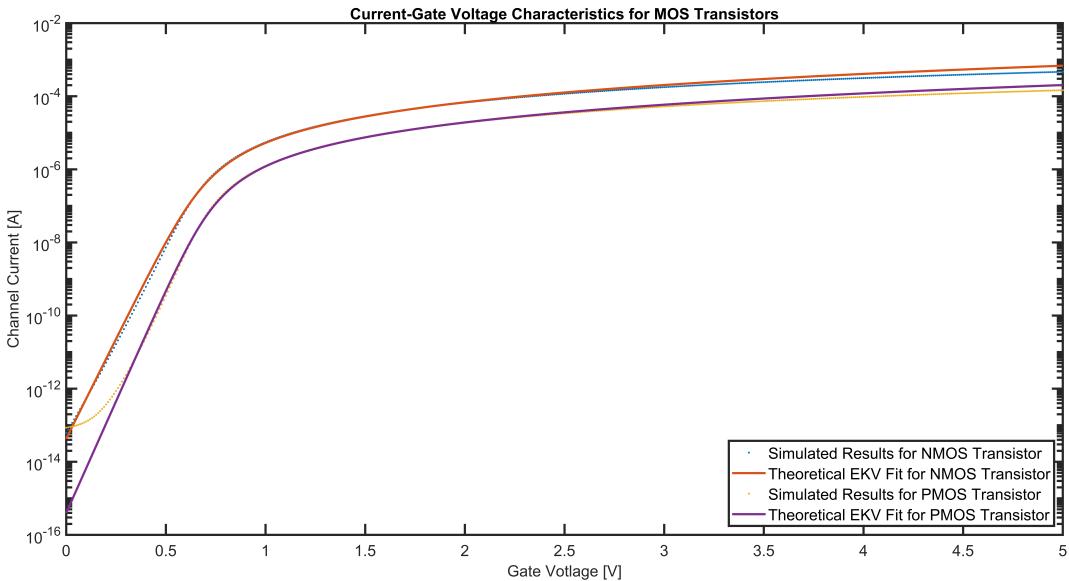


Figure 5: Saturation Current vs. Gate Voltage plot for MOS transistors

The following table shows extracted parameters for both the NMOS and PMOS devices from the EKV model fit.

Extracted Parameter Values			
Simulation Run	I_s [A]	κ	V_{TO} [V]
NMOS Transistor	$2.247 * 10^{-7}$ A	0.6492	0.6152 V
PMOS Transistor	$5.4363 * 10^{-8}$ A	0.7259	0.6659 V

Next, we considered the incremental transconductance gain of the MOS transistors. The gain with respect to the current through the transistor is shown below for both a NMOS and PMOS device.

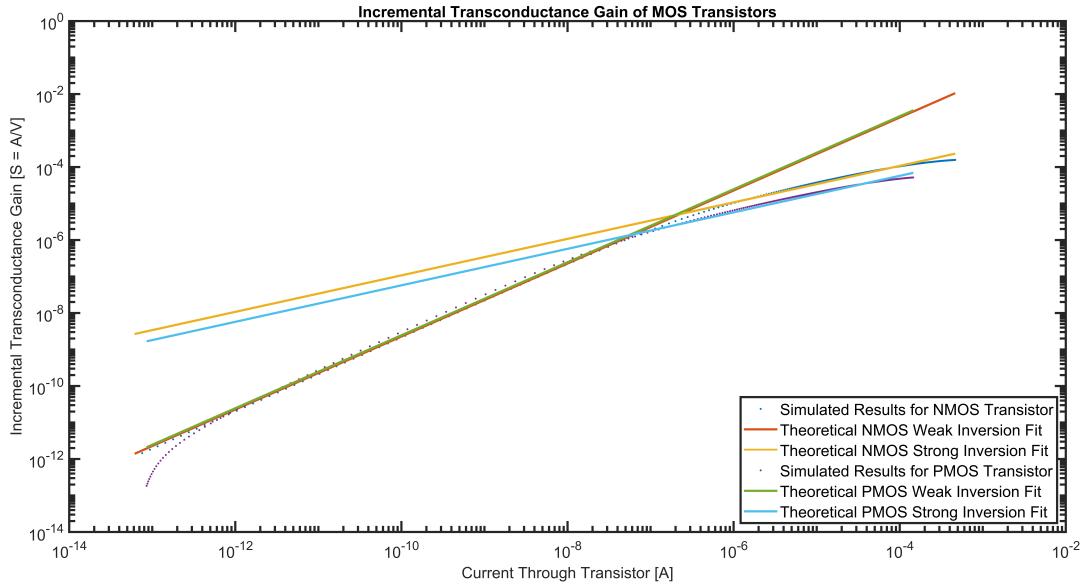


Figure 6: Incremental Transconductance Gain of MOS Transistors

For the theoretical fit, we used Equation 3 to fit for all regions and transitions. In doing this, we used the extracted device parameters from the EKV model fit. And we used $U_T = 0.0286V$ for the NMOS transistor. This value was extracted during Experiment 2. For the PMOS transistor we used $U_T = 0.0295V$.

We can see that the fits match the simulated data quite well. The NMOS weak inversion model fits the data quite well when the current through the transistor is between $10^{-13}A$ to $10^{-7}A$. In the strong inversion region the model fits moderately well when the current through the transistor is between $10^{-6}A$ and $10^{-4}A$. The linear model seems to average out the slight bend of the intrinsic gain characteristics. For the PMOS transistor, the theoretical model in the strong inversion region fits better than the weak inversion region. It seems the strong inversion region simulated data tends towards $-\infty S$ for small current levels (less than $10^{-12}A$ of current through the transistor). This could be a result of the slop in the calculations in LTspice. The weak inversion model fits the simulated data pretty well when the current through the transistor is between $10^{-12}A$ to $10^{-7}A$. However, there is a slight bend in the simulated data that is not accounted for in the fit of the model. The characteristics are similar in for the strong inversion fit. The fit matches the data fairly well when the current through the transistor is between $10^{-6}A$ to $10^{-4}A$ region. Slight changes in values for U_T can cause significant changes in the theoretical fits.

2 Experiment 2: Source Characteristics

2.1 Background, Procedure and Model Expectations

For this experiment we simulated the channel current as a function of source voltage with the gate and drain voltages both set at V_{dd} , for an NMOS transistor, and correspondingly for a PMOS transistor with the gate and drain voltages both set at ground.

The circuit schematics that we used for the simulation are also presented below.

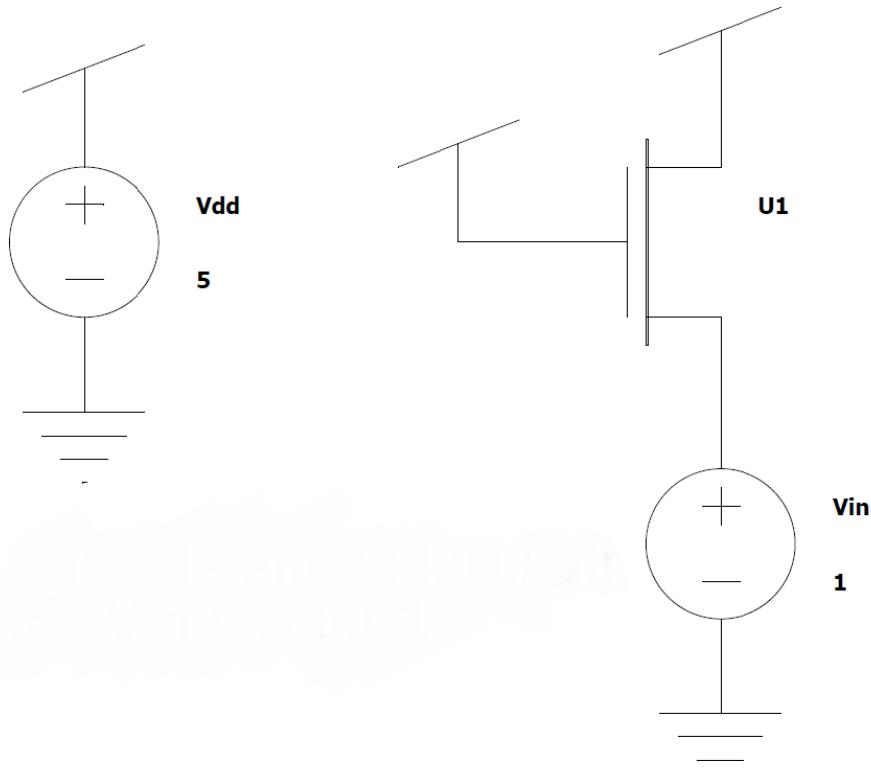


Figure 7: Circuit Schematic for experiment 2 with the nMOS transistor

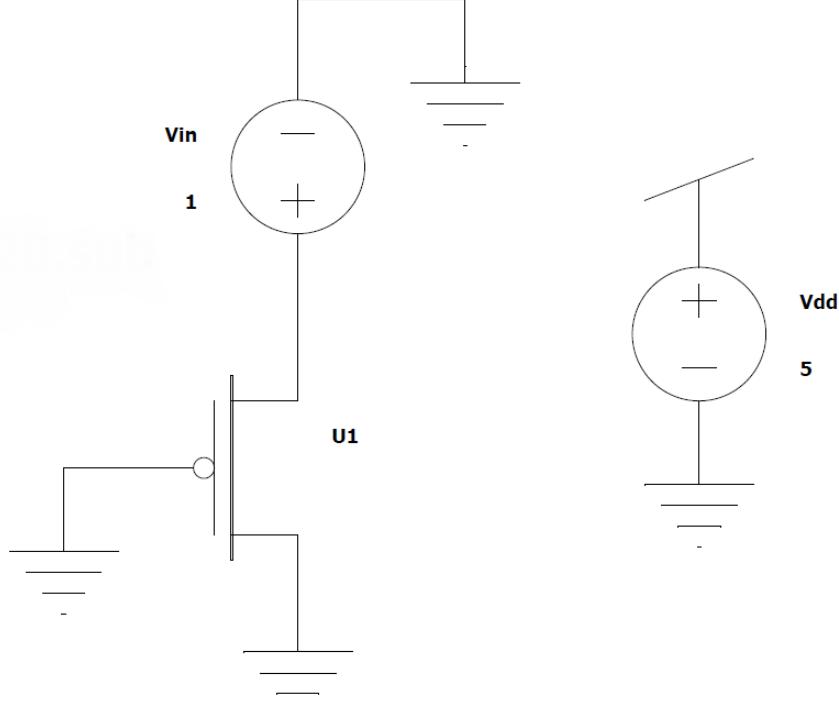


Figure 8: Circuit Schematic for experiment 2 with the pMOS transistor

Using these characteristics, we extracted each transistor's incremental source conductance (g_s).

$$g_s = \frac{(\sqrt[2]{I_s I_{sat}})}{U_T} (1 - e^{-\sqrt[2]{\frac{I_{sat}}{I_s}}}) \quad (7)$$

For operation in the weak inversion region, we can derive the incremental source conductance of the transistors to be:

$$g_s = \frac{I_{sat}}{U_T} \quad (8)$$

For this experiment, we use the value of the thermal voltage as extracted in experiment 1.

For operation in the strong inversion region, we can derive the incremental source conductance to be:

$$g_s = \frac{(\sqrt[2]{I_s I_{sat}})}{U_T} \quad (9)$$

2.2 Results and Discussion

The following plot shows the current though a NMOS transistor when we sweep the source voltage. We also found a best fit line in the weak inversion region, which is also shown on the figure below.

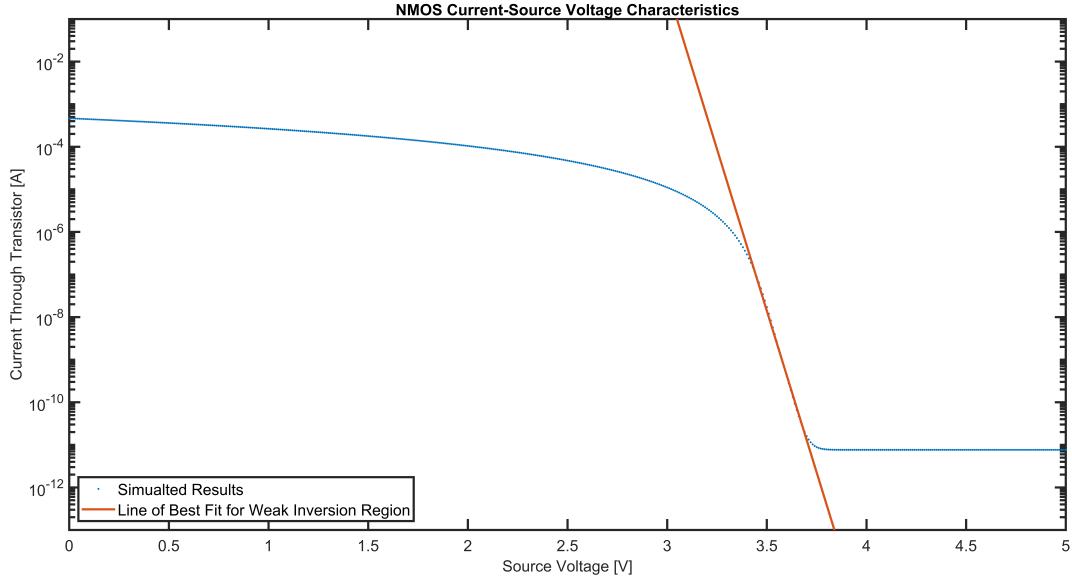


Figure 9: Current-Source Characteristics for NMOS Transistor

From this we can extract the slope of the exponential to be -34.9659 S or $\frac{A}{V}$. We can extract U_T as the negative reciprocal of the slope. We can extract $U_T = 0.0286V$ for the NMOS transistor.

The following figure shows the current through a PMOS transistor as we sweep the source voltage. We found the best fit line in the weak inversion region, which is also shown in the figure below. Please note, that in order to reference the voltages to ground we said,

$$V_S = V_{DD} - V_S \quad (10)$$

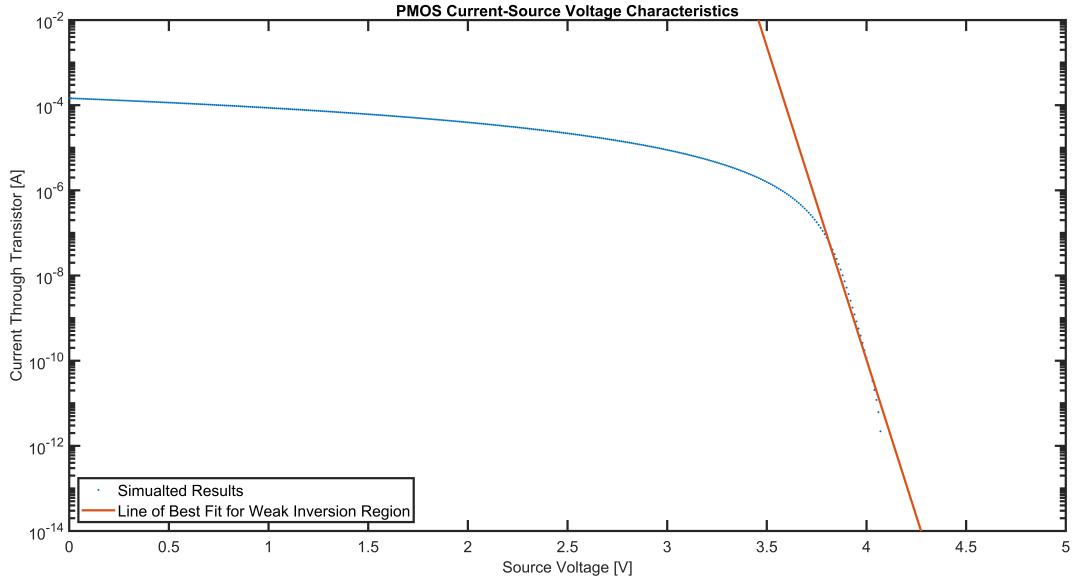


Figure 10: Current-Source Characteristics for PMOS Transistor

In doing this, we found the slope of the exponential to be -33.8468 S or $\frac{A}{V}$. We can extract U_T as the negative reciprocal of the slope. We can extract $U_T = 0.0295V$ for the PMOS transistor.

These characteristics seem to be the inverse of the gate characteristics from Experiment 1. The NMOS transistor is saturated when the source voltage is small (less than ~ 2.5 V) in Experiment 2. Whereas, for Experiment 1, the transistor was saturated when the gate voltage was greater than ~ 1 V. Similarly, the PMOS transistor is saturated in similar regions (when referenced to ground and the input voltages were defined as $V_{DD} - V_{in}$).

The next plot shows the incremental source conductance for both types of MOS transistors along with theoretical fits for the weak and strong inversion regions. The weak inversion region was modeled with Equation 8, and the strong inversion region was modeled with Equation 9.

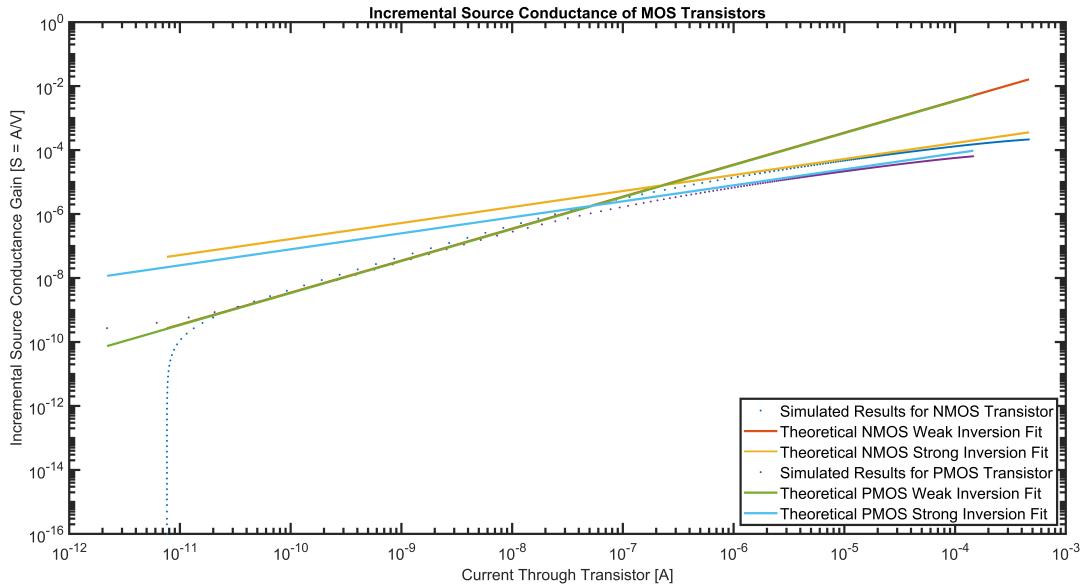


Figure 11: Incremental Source Conductance for NMOS and PMOS Transistors

The theoretical fits match the data fairly well. Similar to the previous experiment, the theoretical fits fail to account for the slight bend in the simulated data. For the NMOS transistor the weak inversion model matches the data fairly well when the current through the transistor is between $\sim 10^{-11} A$ and $10^{-7} A$. The strong inversion model matches the data fairly well when the current through the transistor is $10^{-6} A$ to $10^{-4} A$. For the PMOS transistor the weak inversion model matches the data fairly well when the current through the transistor is between $10^{-11} A$ and $10^{-7} A$. The strong inversion model matches the data fairly well when the current through the transistor is between $10^{-6} A$ and $10^{-5} A$. It does seem that there is a slight offset where the theoretical fit predicts a higher incremental source conductance than the experimental data shows. This could be a result of a slightly different extracted U_T value than the simulator used.

3 Experiment 3: Drain Characteristics

3.1 Background, Procedure and Model Expectations

In this experiment, we measured the channel current for each of the transistors as a function of drain voltage for three values of gate voltage, as mentioned in the table below.

Drain Characteristics Simulation Parameters			
Transistor Type	Weak Inversion	Moderate Inversion	Strong Inversion
NMOS	0.5152 [V]	0.6152 [V]	5 [V]
PMOS	4.4341 [V]	4.3341 [V]	0 [V]

The circuit schematics that we used for the simulation are also presented below.

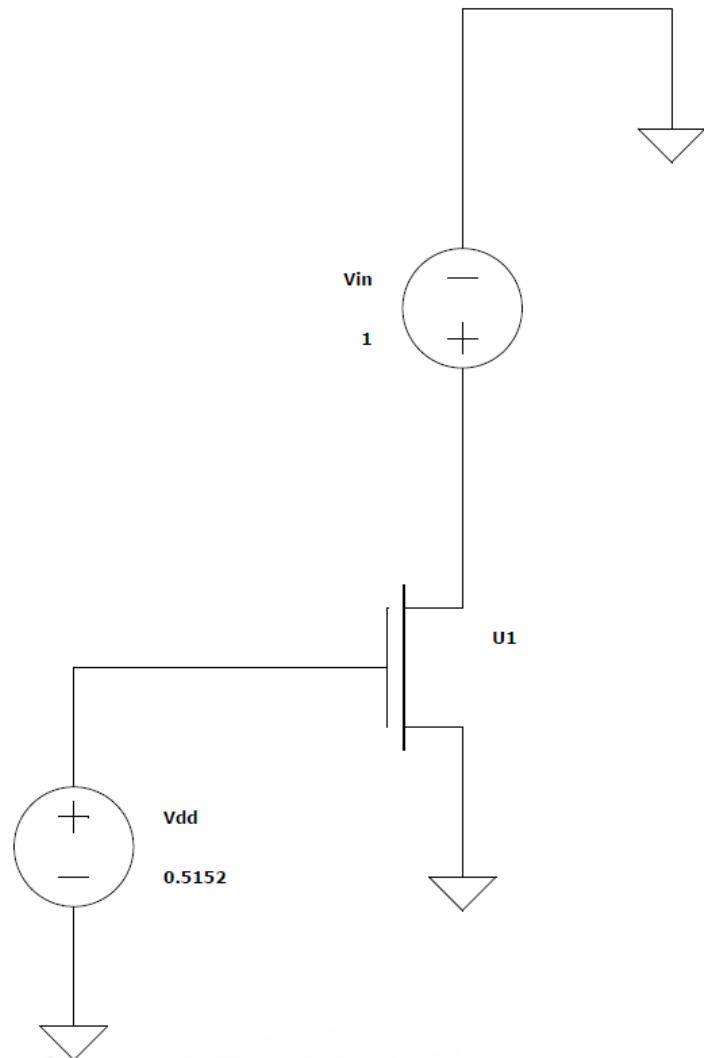


Figure 12: Circuit Schematic for experiment 3 with the nMOS transistor

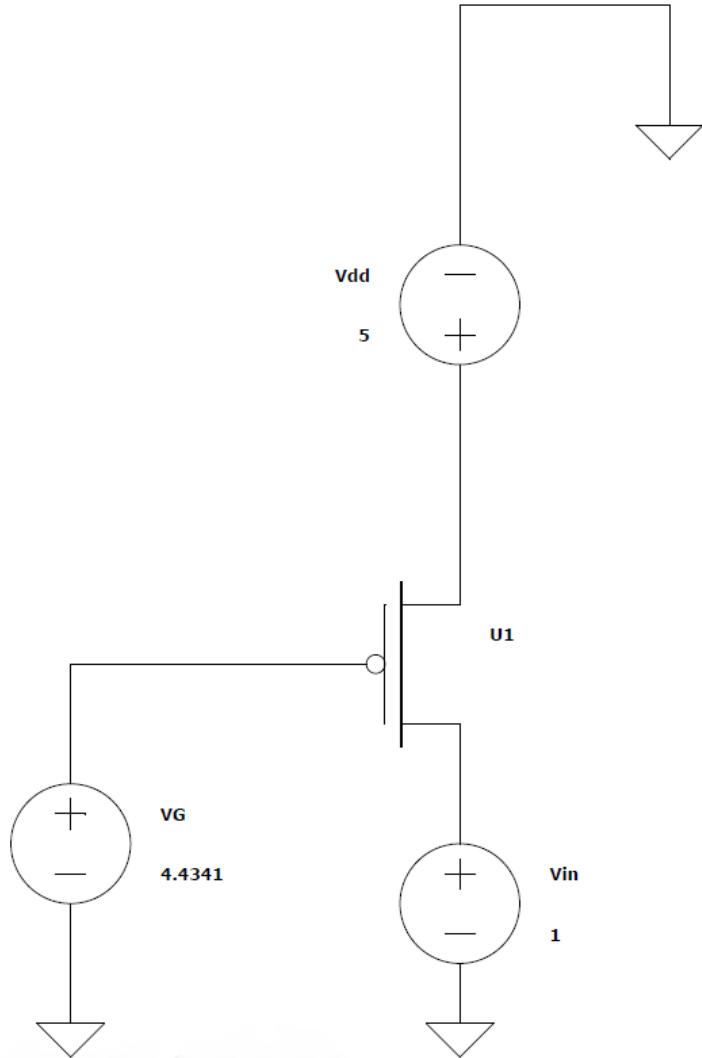


Figure 13: Circuit Schematic for experiment 3 with the pMOS transistor

Using the drain characteristics, we extracted values of the Early voltage (V_A), saturation current (I_{sat}), and the transistor's intrinsic gain ($g_s r_o$).

To extract the Early Voltage (V_A) from the data, we use the equation:

$$V_A = r_o I_{sat} \quad (11)$$

Here, r_o denotes the incremental output resistance of the MOS transistor in saturation. It can be extracted from the characteristics through inverting the slope of the data in the saturation region.

In order to extract the saturation current (I_{sat}), we use the y-intercept of the theoretical fit for the saturation region of the gate characteristics.

To extract the incremental source conductance (g_s), we use the slope of the theoretical fit to the ohmic region of the gate characteristics. We then used to calculate the intrinsic gains for each transistor as follows:

$$\text{Intrinsic Gain} = g_s r_o \quad (12)$$

3.2 Results and Discussion

The following plot shows the current-source voltage characteristics for a NMOS transistor. We found the characteristics with the gate voltage set at regions of weak, moderate, and strong inversion.

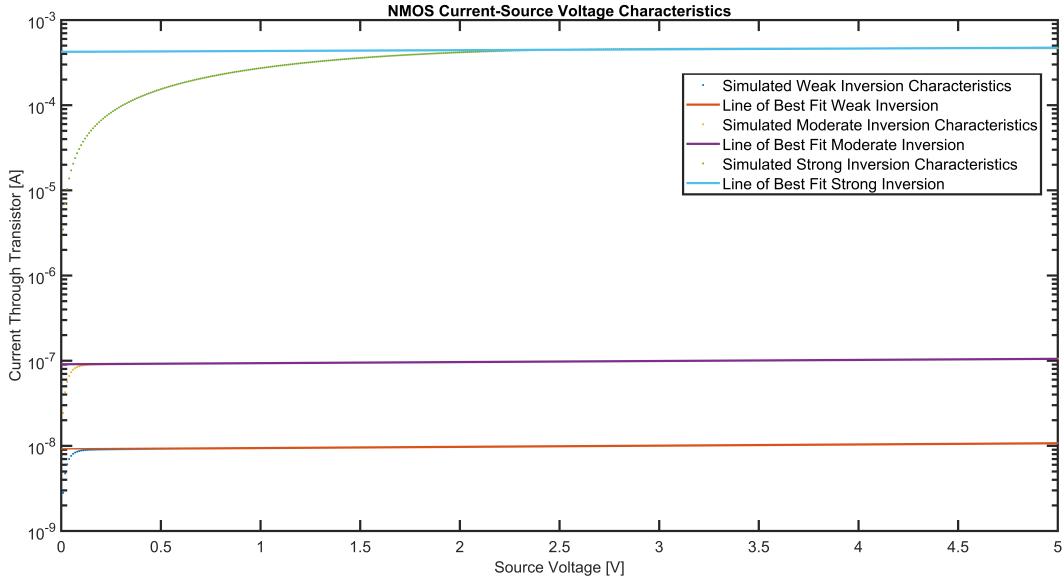


Figure 14: Current-Source voltage Characteristics for the nMOS transistor

By finding a line of best fit in the saturation region, we can calculate the Incremental Output Resistance (r_o) as the reciprocal of the slope. We can also find the saturation current of the transistor as the y-intercept. The Incremental Transconductance (g_m) can be found as the slope of the line in the deep ohmic region. These values can be found in the table below.

Parameter Values for the nMOS transistor			
Gate Voltage	Saturation Current (I_{sat})	Incremental Output Resistance (r_o)	Incremental Transconductance (g_m)
0.5152 [V]	9.1196e-9 [A]	3.1597e9 [Ω]	1.5279e-6 [S]
0.6152 [V]	9.0842e-8 [A]	3.5452e8 [Ω]	2.1824e-5 [S]
5 [V]	4.2319e-4 [A]	1.011e5 [Ω]	0.0334 [S]

The following plot shows the current-source voltage characteristics of a PMOS transistor. We defined the source voltage as

$$V_s = V_{DD} - V_S \quad (13)$$

in order to reference the voltages to ground.

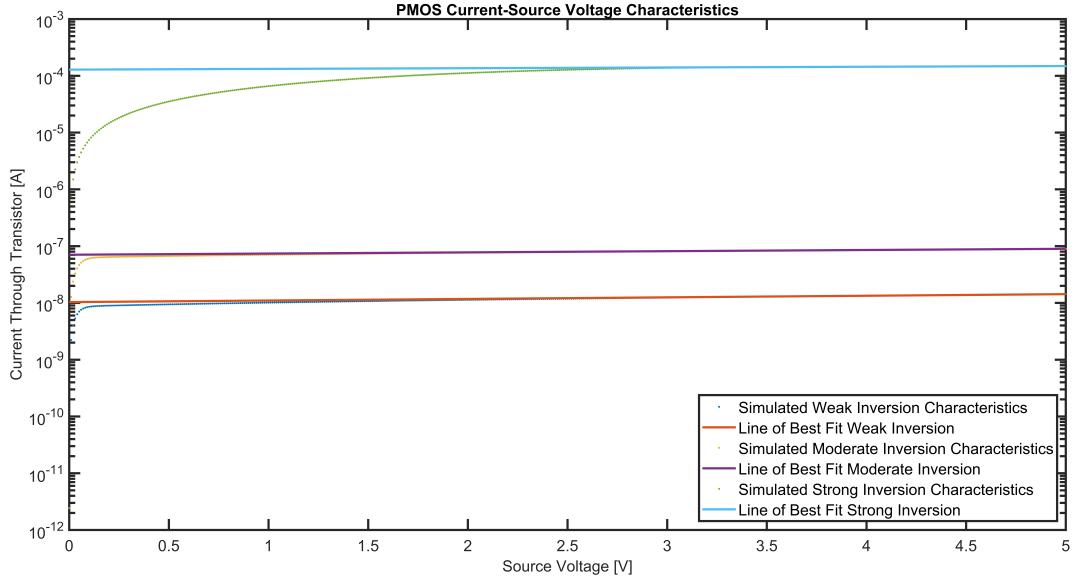


Figure 15: Current-Source voltage Characteristics for the pMOS transistor

By finding a line of best fit in the saturation region, we can calculate the Incremental Output Resistance (r_o) as the reciprocal of the slope. We can also find the saturation current of the transistor as the y-intercept. The Incremental Transconductance (g_m) can be found as the slope of the line in the deep ohmic region. These values can be found in the table below.

Parameter Values for the pMOS transistor				
Gate Voltage	Saturation Current (I_{sat})	Incremental Output Resistance (r_o)	Incremental Transconductance (g_m)	
4.4341 [V]	1.0330e-8 [A]	1.1937e9 [Ω]	8.2927e-6 [S]	
4.3341 [V]	7.0553e-8 [A]	2.4887e8 [Ω]	9.6182e-5 [S]	
0 [V]	1.2847e-4 [A]	2.4211e5 [Ω]	0.0239 [S]	

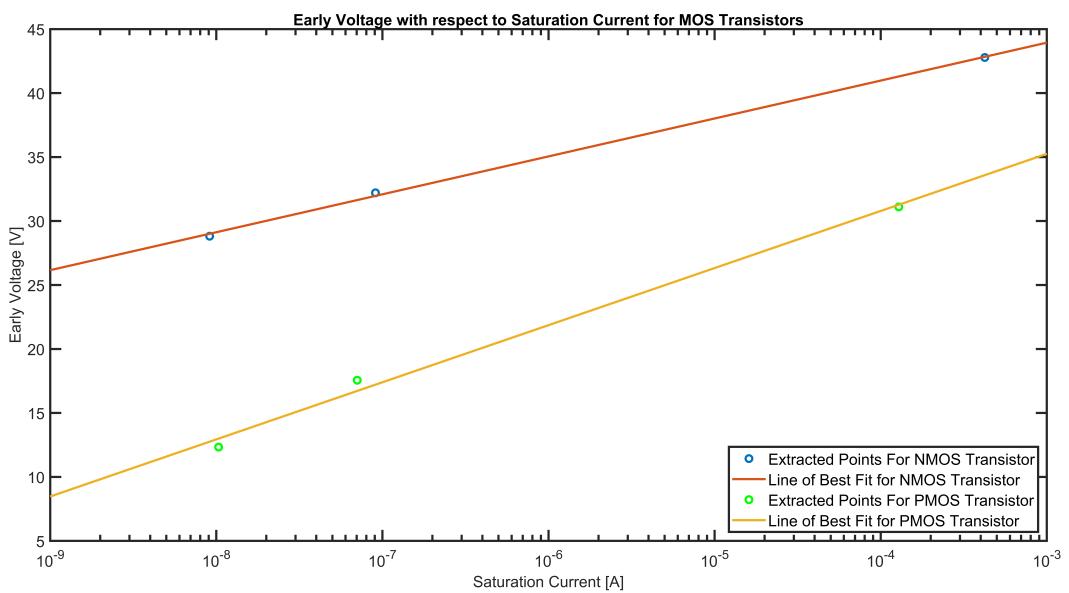


Figure 16: Early Voltage (V_A) with respect to Saturation Current (I_{sat}) for MOS transistors

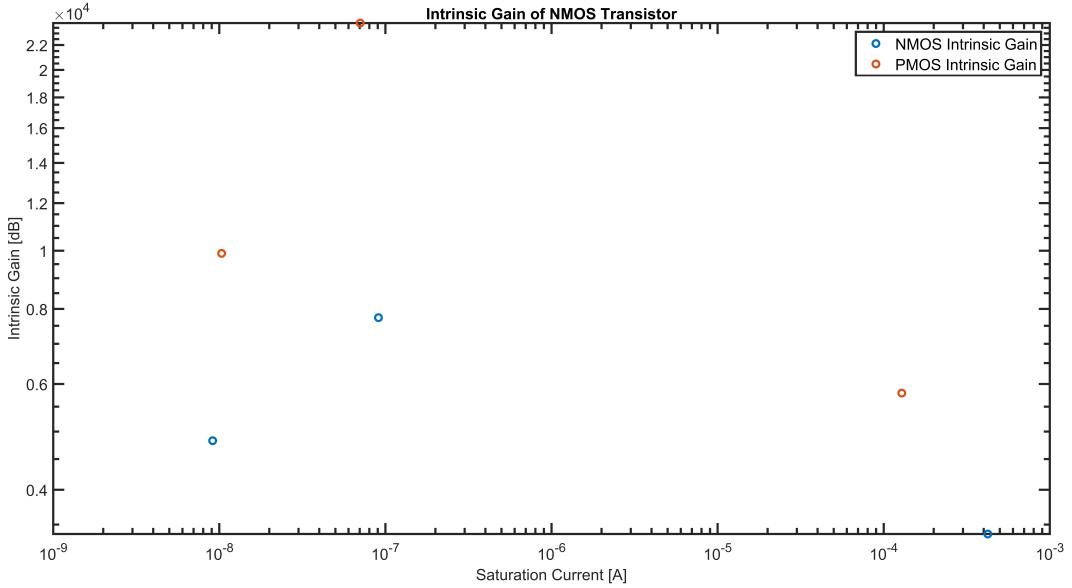


Figure 17: Intrinsic Gain ($g_s * r_0$) of MOS transistors

In this graph, we can observe that the intrinsic gain values for both the transistors are much greater than unity. We can conclude that the assumption for CMOS circuits is a valid one, generally.

Parameter Values for the nMOS transistor		
Gate Voltage	Early Voltage (V_A)	Intrinsic Gain ($g_s r_o$)
0.5152 [V]	28.8147 [V]	4.8275e3 [dB]
0.6152 [V]	32.2055 [V]	7.731e3 [dB]
5 [V]	42.7822 [V]	3.3758e3 [dB]

Parameter Values for the pMOS transistor		
Gate Voltage	Early Voltage (V_A)	Intrinsic Gain ($g_s r_o$)
4.4341 [V]	12.3308 [V]	9.8993e3 [dB]
4.3341 [V]	17.5587 [V]	2.3937e4 [dB]
0 [V]	31.1033 [V]	5.7947e3 [dB]

We can find the theoretical maximum incremental voltage gain of the transistor configured as a common-source amplifier, $g_m r_0$, by multiplying $\kappa * (g_s * r_0)$. From Experiment 1, we found that the κ value of a NMOS transistor to be 0.6492 and 0.7259 for the PMOS transistor. As κ is less than one, we know that $g_m r_0$ will be less than $g_s * r_0$. This indicates that the gain when a MOS transistor is configured as a common-gate amplifier will have more gain than when it is configured as a common-source amplifier.