

Lab 6: Series/Parallel MOS Networks and MOS Current Dividers

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1 Experiment 1: Transistor Matching

1.1 Background, Procedure and Model Expectations

For this experiment, we measure channel current as a function of gate voltage with the source voltage at ground and the drain voltage at V_{dd} for each of the four transistors on the ALD1106 chip. Then, we fit the EKV model to each of these characteristics using the MATLAB function *ekvfit.m* and extract a value of I_s , κ , and V_{T0} .

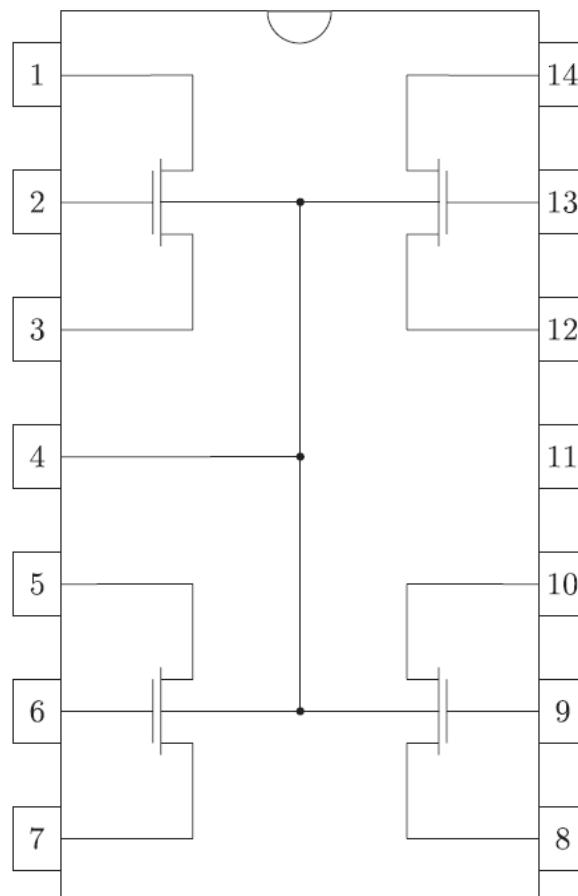


Figure 1: ALD1106 Array of nMOS Transistor in n-well technology

For this experiment, the transistors are numbered counterclockwise around the chip starting with pin 1. All data for this experiment was sent by Brad.

1.2 Results and Discussion

Below is a table showing these extracted parameter values for all four transistors.

Extracted Parameter Values			
Transistor	I_s [A]	κ	V_{TO} [V]
Q1 (Pins 1-3)	1.9999e-06 [A]	0.633	0.667 [V]
Q2 (Pins 5-7)	1.7934e-06 [A]	0.645	0.655 [V]
Q3 (Pins 8-10)	1.7976e-06 [A]	0.646	0.655 [V]
Q4 (Pins 12-14)	1.9534e-06 [A]	0.636	0.660 [V]

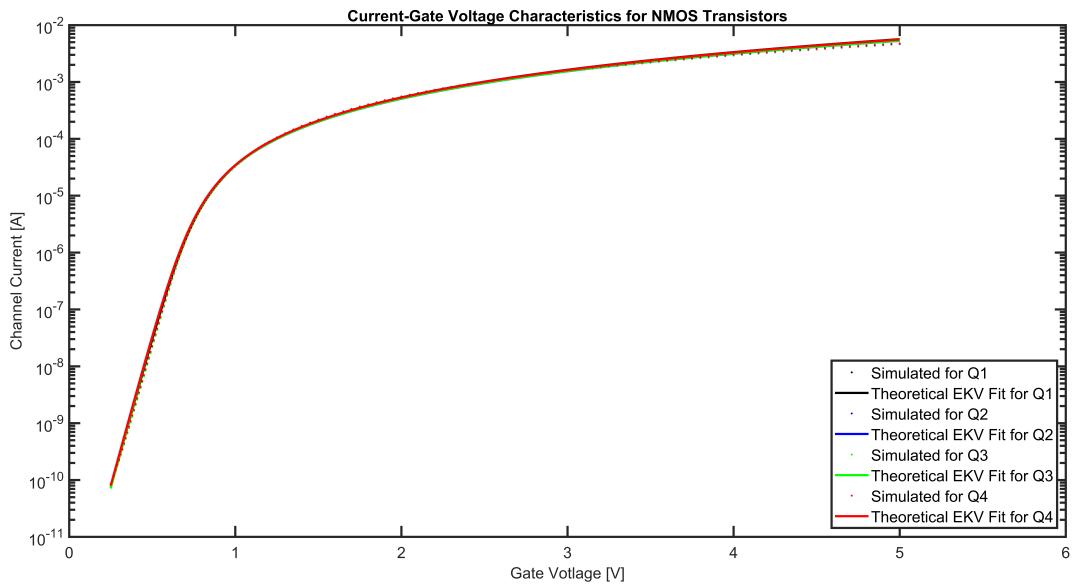


Figure 2: Current-Gate Voltage Characteristics for each of the four transistors on the ALD1106 transistor array

From the plot and table above, we can see that the transistors match one another quite well. In Figure 2, the current-voltage characteristics are fairly indistinguishable from one another. From the parameter values, we can see that transistors 2 and 3 match one another the best for each of the extracted values, but transistors 1 and 4 also seem to match one another quite well. Although there are the two groupings in terms of the parameter value matching, all of the parameter values are fairly close to one another for all transistors.

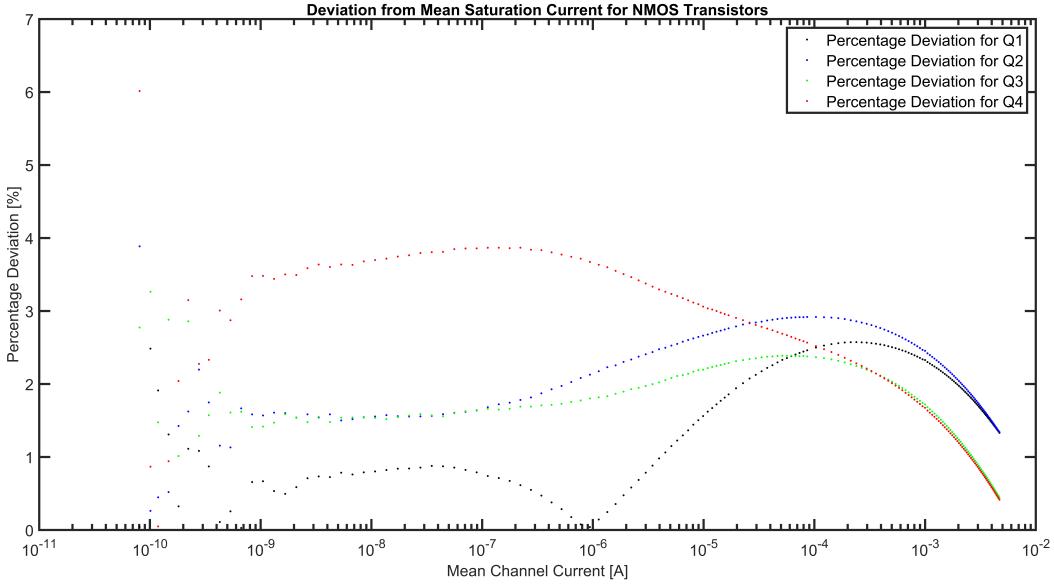


Figure 3: Deviation from Mean Saturation Current for each of the four transistors on the ALD1106 transistor array

From the plot above, we can see that the transistors are all mostly within 4% of the mean saturation current level across all saturation regions. This implies that all transistors are quite closely matched. Above, we can see that for channel current levels of 10^{-9} A to 10^{-7} A, transistors 2 and 3 are quite consistent with their deviation from the mean saturation current. However, as we begin to increase the channel current to 10^{-4} A, transistors 3 and 4 match one another quite well in terms of the deviation from the mean saturation current. At 10^{-3} A, transistors 1 and 2 begin to match one another quite well in terms of deviation from the mean. As we increase the channel current to above 10^{-4} A, we can see that all transistors seem to converge towards the mean saturation current level. Therefore, we can conclude that for strong inversion levels, the transistors all converge towards the mean saturation current.

2 Experiment 2: MOS Transistors in Series and Parallel

2.1 Background, Procedure and Model Expectations

For this experiment, we measure channel current as a function of gate voltage both for $V_{DS} = 10mV$ and for $V_{DS} = V_{dd}$. Next, we connect a matched pair of nMOS transistors in parallel with each other, and in a separate run, in series with each other, and repeat the measurements that we just did one of the devices by itself.

From the prelab, we can expect that by putting two transistors in series with one another, we expect the current to divide by two (assuming the transistors are matched). Similarly, we expect that by putting two transistors in parallel, the current should be twice as large as the current through a single transistor (assuming the transistors are matched).

For this experiment, the second (pins 5-7) and third (pins 8-10) transistors were used. The second transistor was used as the individual transistor. When in series, the top transistor was the third transistor and the bottom transistor was the second transistor. All data for this experiment was sent by Brad.

2.2 Results and Discussion

The following plot shows the current voltage characteristics for all configurations (series, parallel, and a single transistor) with $V_{DS} = 5V$ and $V_{DS} = 10mV$.

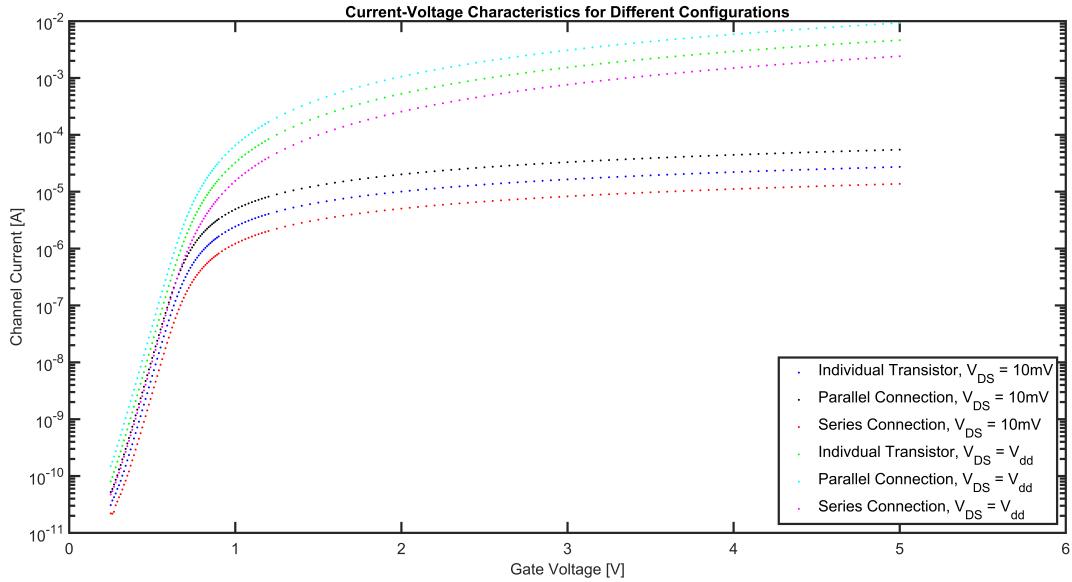


Figure 4: Semilog plot showing data from the individual transistor, the parallel connection, and the series connection, for each of the two experimental situations

The next plot shows the ratio of channel current for a parallel configuration to a single transistor.

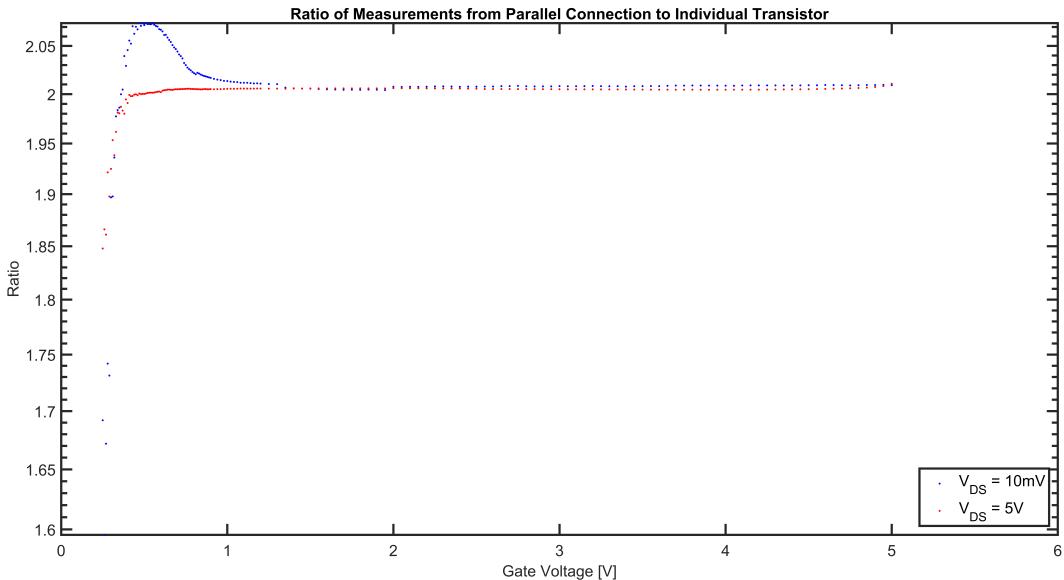


Figure 5: The ratio of the measurements from the parallel connection to those from the individual transistor

From this plot, we can see that when $V_{DS} = 5V$ the channel current is consistently 2 times the current of a single transistor (under the condition that the gate voltage is above the threshold voltage). Conversely, when $V_{DS} = 10mV$, the channel current is (for the most part) 2

times the current of a single transistor under the same region. However, we can see that when the gate voltage is under 1V, the current is just over 2 times the current of a single transistor (2.05 times). Although there is a slight spike under 1V in the gate voltage, this is still quite close to the expected value.

The next plot shows the ratio of channel current for a series configuration to a single transistor.

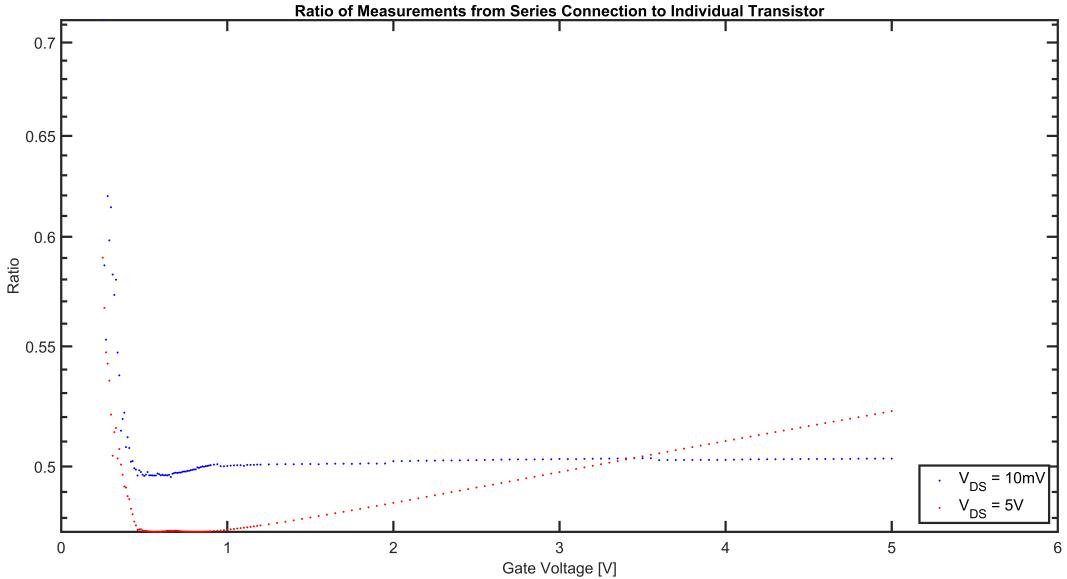


Figure 6: The ratio of the individual transistor measurements to those from the series connection

In this figure above, we can see that for $V_{DS} = 10mV$, the ratio of $\frac{1}{2}$ the current of a single transistor is quite consistently accurate. This is accurate when the gate voltage is above the threshold voltage. When $V_{DS} = 5V$, we can see that the ratio is not as accurate as it was for the $V_{DS} = 10mV$ case. However, this is still a quite good approximation as the series connection is 0.5 ± 0.03 when the gate voltage is above the threshold voltage and under 5 V. A reason that there may be a variable ratio between the series connection and an individual connection could be a result of the incremental output resistance of the transistors.

The parallel and series equivalences work quite well for the MOS transistors. We have found that the current through the parallel circuit was (for the most part) 2 times the current through a single MOS transistor. When the gate voltage was above 1 V, for both $V_{DS} = 10mV$ and $V_{DS} = 5V$, the ratio between a parallel connection and individual transistor was 2, which implies that a parallel equivalence of a transistor with 2 times the current flowing through it is quite good for all inversion levels. However, we find that in the saturation region in particular, the equivalence matched quite well for both V_{DS} values.

For the series connection we found that current through the transistors were consistently $\frac{1}{2}$ the current through a single transistor when $V_{DS} = 10mV$ and the gate voltage was above the threshold voltage. For this situation, the series equivalence of a single transistor with half the current flowing through it is quite good at all inversion levels. For $V_{DS} = 5V$, the equivalence is not quite as good. We find that the equivalence would match the best in the middle of the saturation region. With $V_{DS} = 5V$, the ratio between the series connection and a single transistor is 2 when the gate voltage is ~ 3.5 V. As there is a consistent slope to the line, we will find that the ratio will be closest to 2 when we near a gate voltage of 3.5 V. Thus, we can conclude that the equivalent circuit (a single transistor with half of the current flowing through it) will be best in the middle of the saturation region.

3 Experiment 3: MOS Current Dividers

3.1 Background, Procedure and Model Expectations

For this experiment, we constructed a two-way current divider (shown in Fig. 6.2a in the lab document) in which the divider ratio is a ratio of 2:1 from the nMOS transistors in the ALD1106 array by connecting them in series. We set the gate voltage to V_{dd} and the drain voltages to V_{dd} in order to guarantee that the transistors are saturated. We then measure the output current as a function of input current. Lastly, we fit a straight line to the divider's current transfer characteristic and extract the value of the divider ratio. To find the divider ratio we use,

$$\frac{I_i}{I_{in}} = \frac{S_i}{\sum S} \quad (1)$$

where i is the branch we are currently considering.

The schematic used in this experiment is shown below,

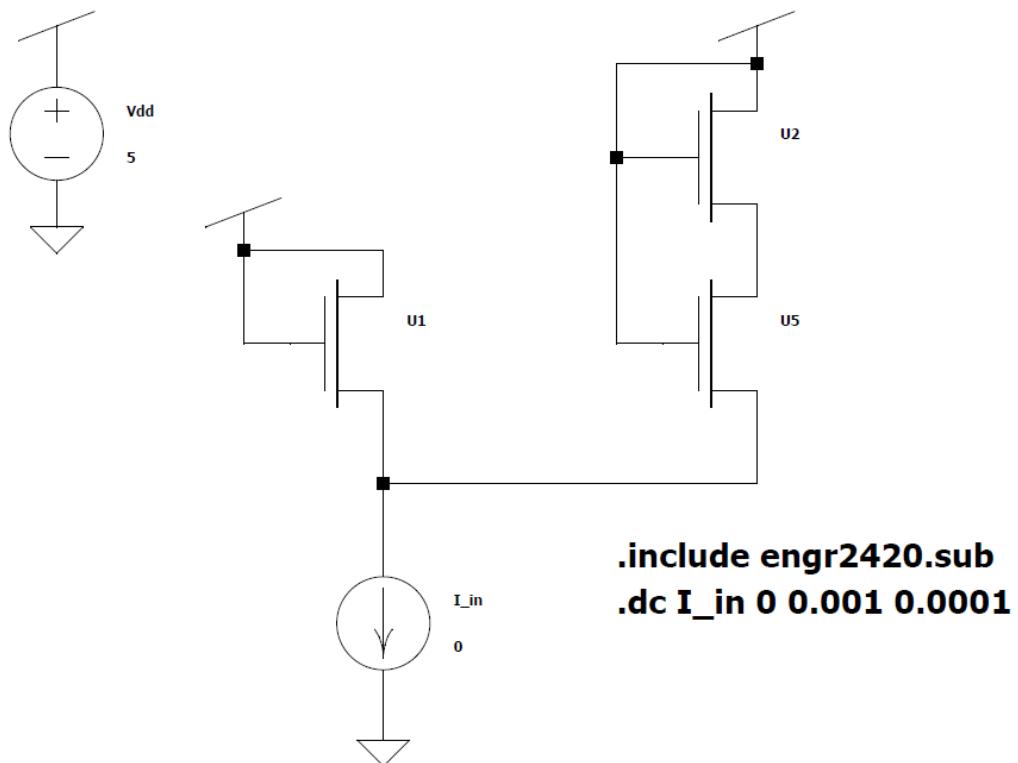


Figure 7: Schematic for two way current divider with current sink

For the second part of this experiment, we construct the two-way current divider (shown in Fig. 6.2b in the lab document) using the nMOS transistors in the ALD1106 array. We set the gate voltage to V_{dd} , sufficiently high that the transistors can accommodate the maximum input current that we use in the simulation and the source voltages to ground. We then measure the output current as a function of input current. Once again, we fit a straight line to the divider's current transfer characteristic and extract the value of the divider ratio. The following image shows the schematic used in this experiment,

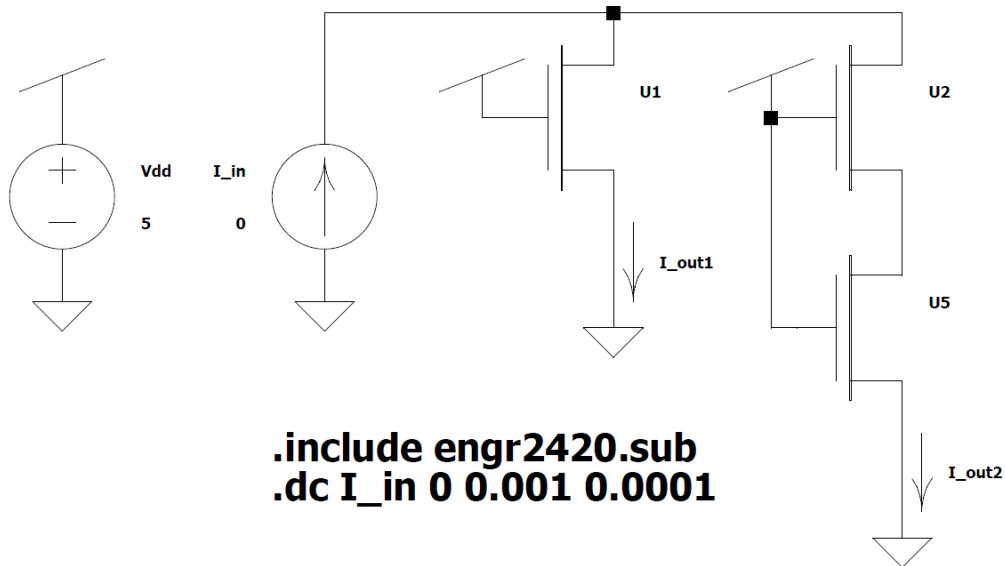


Figure 8: Schematic for two way current divider with current source

3.2 Results and Discussion

The following plot shows the output current for each branch as we vary the current sink value.

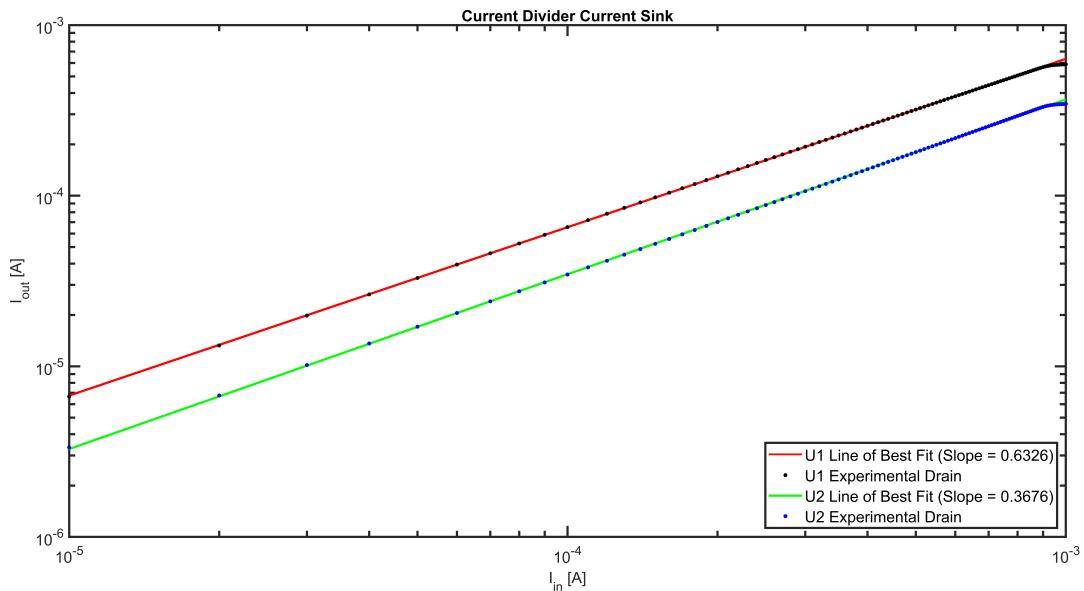


Figure 9: Output current with respect to input current for circuit in Figure 7

The following table shows the extracted and theoretical ratios of current division. The theoretical divider ratio is given in Equation 1, with the strength ratio of U1 as twice the effective strength ratio for the U2 and U5 series branch. This is because by adding two transistors in series, we are effectively increasing the length of the transistor by two.

Extracted Parameter Values			
Branch Current	Theoretical Current Division Ratio	Experimental Best Fit Ratio	Percent Difference
Current through U1	2/3	0.6326	5.11 %
Current through U2	1/3	0.3676	7.28 %

For the first circuit (shown in Figure 7), we can see that the experimental division ratios are quite close to the theoretical values. For the U1 transistor branch, the theoretical and extracted percent difference was 5.11 %, which is fairly accurate. Similarly, the current through the U2 branch was 7.28 % off in terms of the percentage difference between the theoretical and extracted ratios.

A reason for the slight error in simulated and theoretical ratios could be due to slop in the calculations for LTspice. Another influencing factor could be the distribution of points. We are favoring the higher input current region by taking a higher density of points in that region. We can see that as we approach $10^{-3} A$, the simulated output current levels off. This would result in pulling the slope of the line down. If we were collecting data from a physical set up, a contributing factor could be the resistance in the terminals of the transistors.

The following figure shows the output current through each branch as we vary the value of the current source.

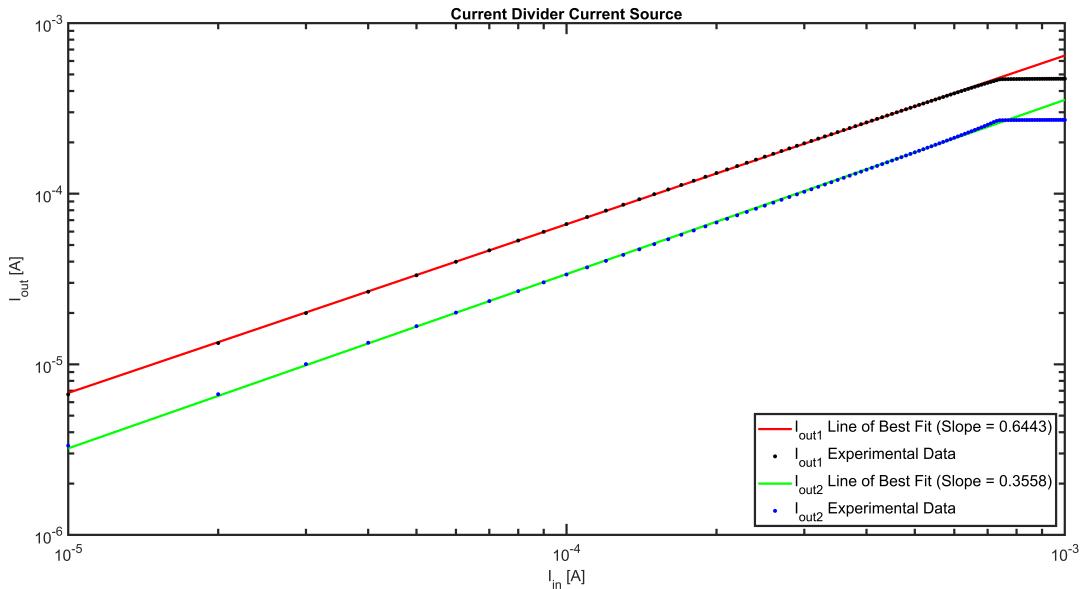


Figure 10: Output current with respect to input current for circuit in Figure 8

The following table shows the extracted and theoretical ratios of current division. The theoretical divider ratio is given in Equation 1, with the strength ratio of U1 as twice the effective strength ratio for the U2 and U5 series branch (by the same logic as the last circuit).

Extracted Parameter Values			
Branch Current	Theoretical Current Division Ratio	Experimental Best Fit Ratio	Percent Difference
I _{out1}	2/3	0.6443	3.355 %
I _{out2}	1/3	0.3558	6.74 %

For the second circuit (shown in Figure 8), we can see that the experimental division ratios are quite close to the expected values. This arrangement of a current divider seemed to more

closely match the theoretical results when extracting the current division ratio. For the I_{out1} branch, the percentage difference was 3.355 % error, which quite close. For the I_{out2} branch, we find the percentage difference was 6.74 %. Similar to the previous arrangement of the current divider, the error can be a result of similar effects.