

Final Project: Frequency Response of Class-AB Two-Stage CMOS Differential Amplifier

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1 Background Information

For this project, we are looking at the frequency response of a Class-AB Two-Stage CMOS Differential Amplifier. Specifically, we looked into the stability and the range of frequencies it operates as expected for. We used various compensation situations to improve circuit behavior, and compared the frequency responses.

A system is considered stable if the amplitude of the gain is less than unity when the phase reaches -180° . Negative feedback introduces 180° of phase shift, so when the phase angle is -180° the feedback signal adds in phase with the original signal and creates an oscillation. In doing this, the negative feedback loop turns into positive feedback, which creates conditions for an unstable system to arise. If, at this point, the gain is greater than one, the oscillation will grow in amplitude causing the system to go unstable; whereas, if the gain is less than one, the oscillation will diminish and the system will be restored to a stable condition.

We also know that connecting the circuit as a unity gain follower provides the least stable possibility for the circuit. This is because feedback is what causes the system to go unstable. As a unity gain follower, the feedback is maximum from the output into the inverting input. By considering the unity gain case, worst-case analysis is performed.

1.1 Theory

The *gain crossover point* is where the magnitude of the loop gain is equal to unity and the *phase crossover point* is where the phase of the loop gain is equal to -180° . A system is stable when the gain crossover point occurs before the phase crossover.

According to Razavi, for two-stage op-amps, each gain stage introduces a *dominant pole*. For this case, if we reduce the feedback of the system, then for a logarithmic vertical axis, the magnitude plot translates down vertically (assuming that the bode plot is graphed on a logarithmic scale). This moves the gain crossover point towards the origin while the phase crossover point remains constant, resulting in a more stable system. This is a trade off between the feedback strength and the stability of the circuit.

For three-stage systems, the *third pole* gives rise to additional phase shift possibly moving the phase crossover to frequencies lower than the gain crossover and leading to oscillation. It also decreases the magnitude of the loop gain at a greater rate. Hence, the additional poles impact the phase to a much greater extent than they do the magnitude.

At low frequencies, the closed-loop frequency exhibits a sharp peak in the vicinity of the first frequency. The system is near oscillation and its step response exhibits a very underdamped behaviour. Hence, a second-order system may suffer from *ringing* although it is stable. We can quantify this ringing effect by computing the *settling time*, which is the time elapsed from the

application of a step input to the amplifier, till the time at which the output of the amplifier has entered and is within a pre-determined error-band, which can be given in percentage terms. Settling time and ringing contribute to the *figures of merit* for amplifiers and other similar control-based devices.

If the gain crossover point precedes phase crossover point by a greater margin, then we could expect relatively less ringing, pointing us to our aim: to increase this gap to achieve higher stability systems. This gap is commonly known as *phase margin*. According to Razavi, a phase margin of 60° is considered an optimal value.

To ensure stability of the cascode topologies, a need for *compensation* arises if the phase margin is low (or negative, meaning that the phase crossover point precedes the gain crossover point). As postulated by Razavi, stability can be achieved by minimizing the overall phase shift, or dropping the gain. The first approach requires minimization of the number of poles in the signal path, and since each additional stage contributes at least one additional pole, this means that the number of stages must be minimized yielding low voltage gain and limited output swings. Compared to the second approach, which retains the low-frequency gain and output swings, but reduces the bandwidth by forcing the gain to fall at lower frequencies.

Pole splitting is the property of Miller Compensation which moves the inter-stage pole toward the origin and the output pole away from the origin, allowing a much greater bandwidth than that obtained by merely connecting the compensation capacitor from one node to the ground. In the experiments below, we have run iterations on choosing the compensation capacitor for best resultant phase margin.

As introduced by Thandri, the positive phase shift of the left half plane zeroes caused by a *feed-forward* path can be used to cancel the negative phase shift of poles to achieve a good phase margin and make the circuit faster. This technique, known as the *Feedforward Transconductance Compensation* has been used in order to achieve a high-gain wide-band amplifier, which was compromised due to the pole-splitting effect of Miller compensation technique. It is also suggested that the pole-zero cancellation should occur at high frequencies for best settling-time performance, and that the goal for this design strategy should be to maximize the transconductance of the feed-forward stage to push the poles to higher frequencies.

2 Experiment 1: Class-AB Two-Stage CMOS Differential Amplifier without Compensation

2.1 Background, Procedure and Model Expectations

For the first experiment, we considered an uncompensated Class-AB Two-Stage CMOS Differential Amplifier. We looked at the circuit configured as a unity-gain follower to consider the frequency response and stability of the system. A schematic of the circuit used is shown below,

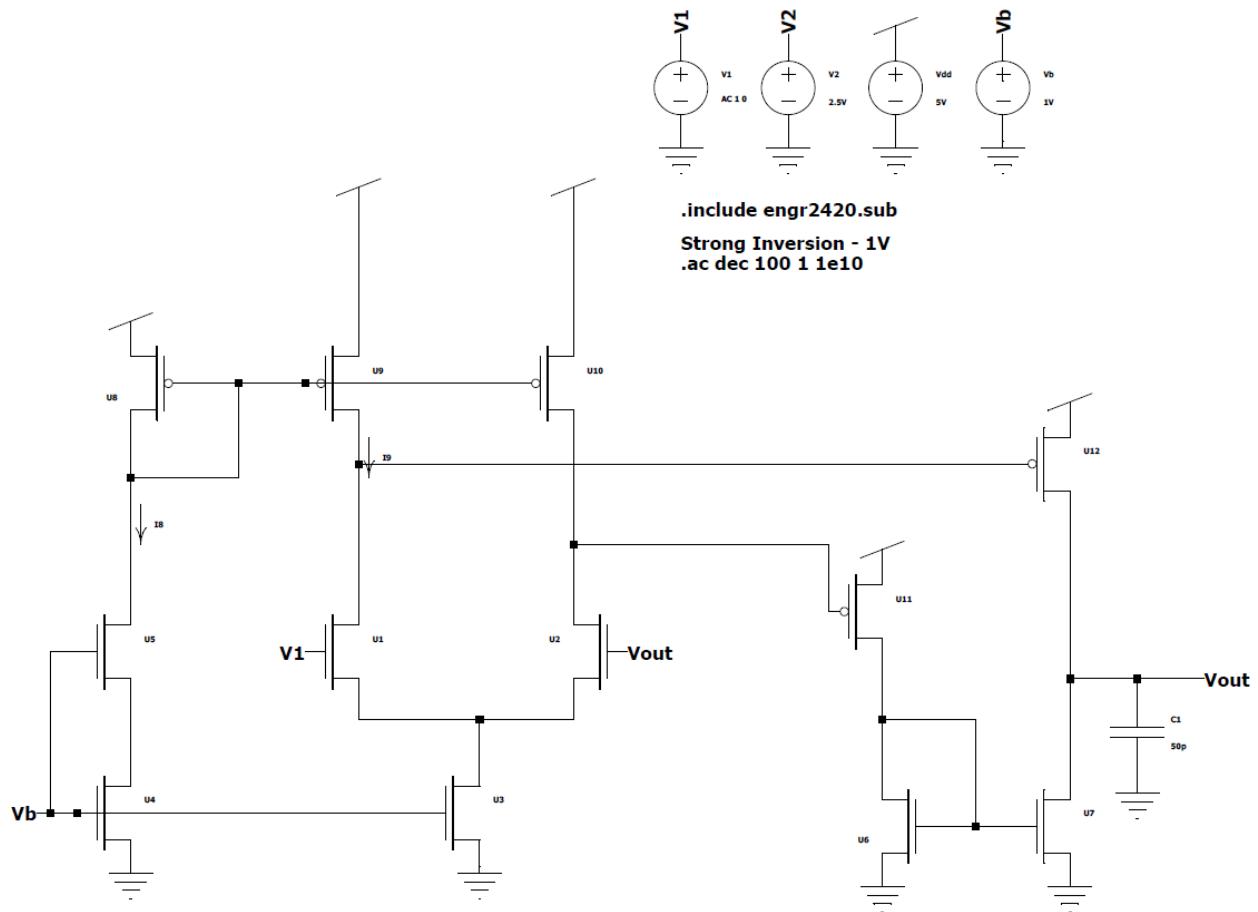


Figure 1: Uncompensated Two-Stage Differential Amplifier Schematic

2.2 Results

The figure below shows a Bode plot for the uncompensated amplifier shown in Figure 1.

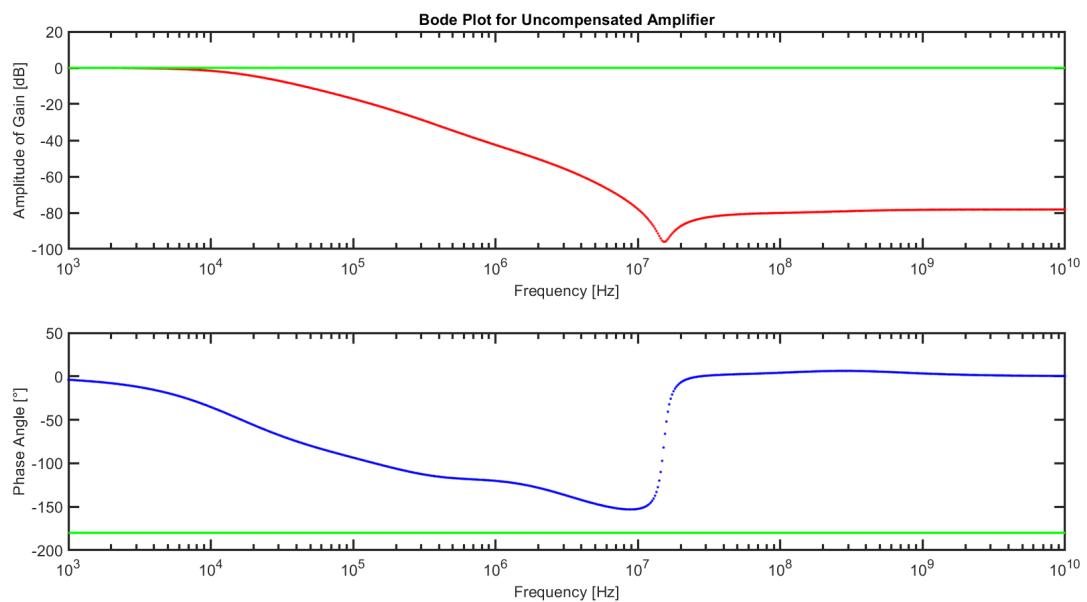


Figure 2: Bode Plot for Uncompensated Class-AB Two-Stage CMOS Differential Amplifier

We find that the circuit behaves as expected (specifically considering the gain) for input frequencies on the order of 10^4 Hz. We also find that the phase of the circuit never reaches -180° , and as a result the feedback loop will not go unstable for the range of frequencies we considered.

The next figure shows the output voltage response to a 1 MHz input frequency pulse.

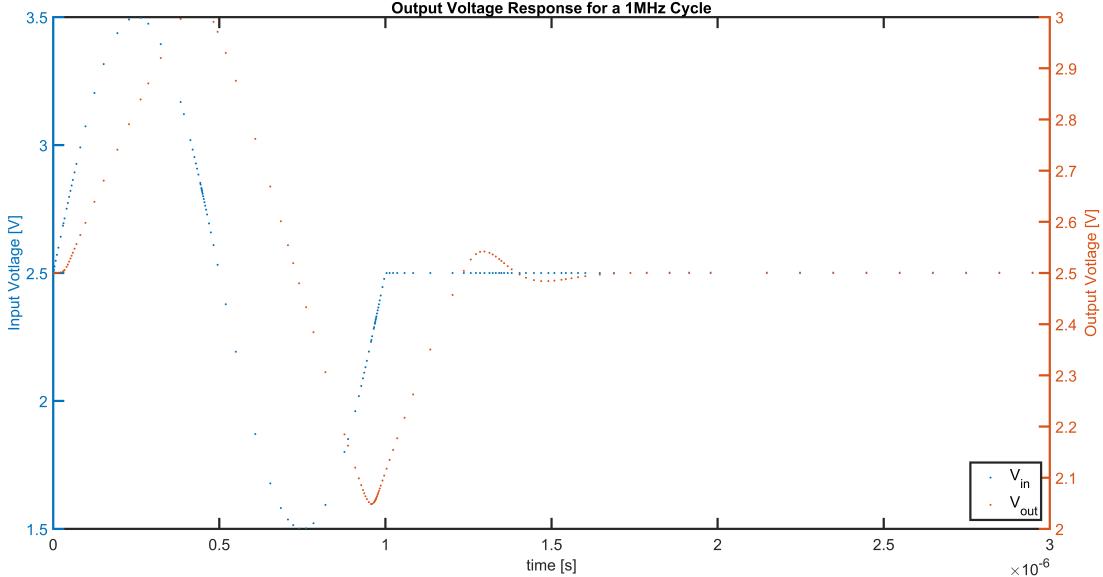


Figure 3: 1 MHz Input, V_{out} response

We find that the circuit took $\sim 1.5 * 10^{-6}$ s for the output signal to settle at the final value. From this, we know that a slight ringing of the circuit will occur.

3 Experiment 2: Two-Stage CMOS Differential Amplifier with Indirect Compensation

3.1 Background, Procedure and Model Expectations

For the second experiment, we considered a Class-AB Two-Stage CMOS Differential Amplifier with indirect compensation. We looked at the circuit configured as a unity-gain follower to consider the frequency response and stability of the system. A schematic of the circuit used is shown below,

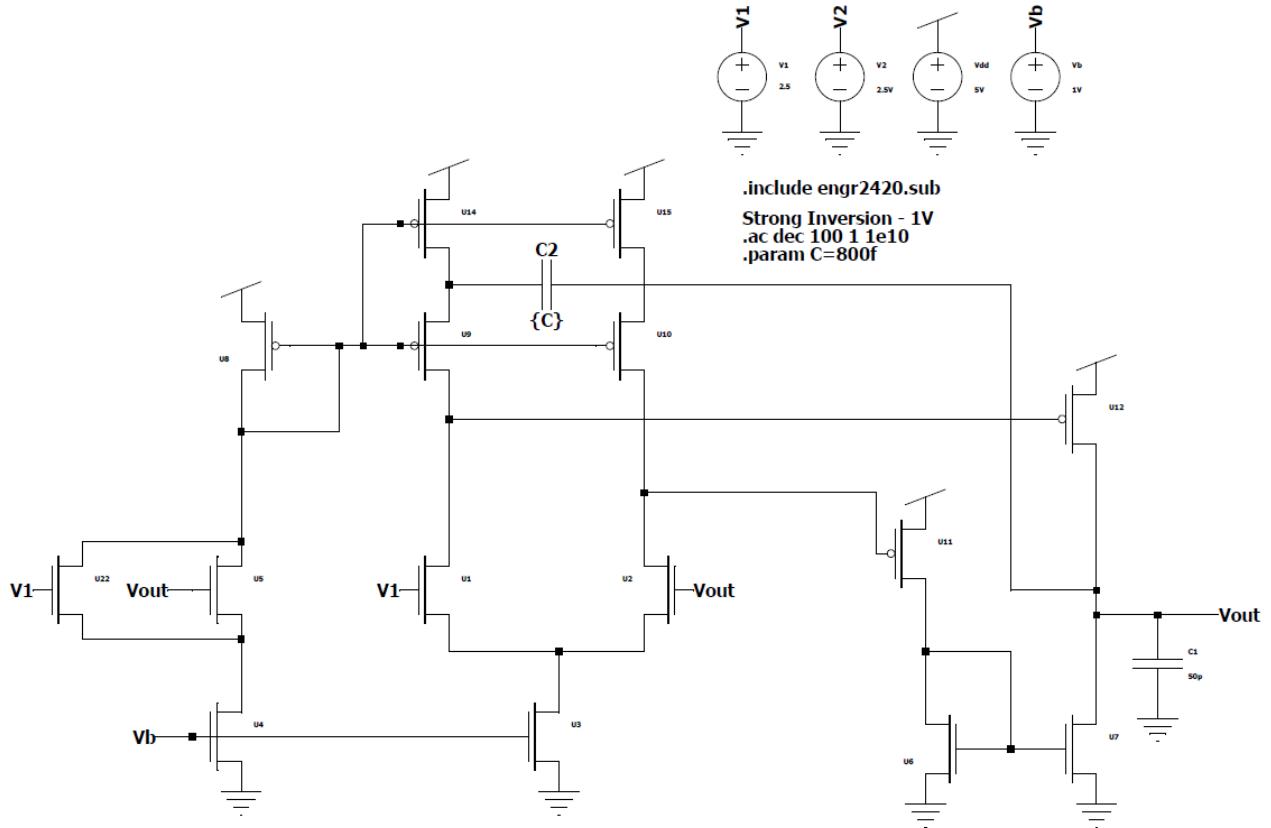


Figure 4: Indirectly Compensated Two-Stage Differential Amplifier Schematic

With this circuit, we used a capacitor (C_2) value of 80 fF, 800 fF, and 1200 fF.

We use two transistors on the left (U22 and U5) to provide feedback for the bias current level. This allows for the bias current to change in accordance to the differential input voltage. The capacitor (C_2) provides an indirect feedback connection between the output and the input, which is what provides compensation for this circuit.

After performing frequency response simulations, we also considered a transient analysis to look at the ringing of the system that occurs when a circuit is not critically damped. To do this, we input a wave at the frequency of the peak and simulated the output voltage. Post-simulation, we calculate the settling time for the circuit, within a range of 1% of the final voltage. We have maintained this range for all the ringing-based experiments.

3.2 Results

3.2.1 $C = 80 \text{ fF}$

The following results show the characteristics for a compensation capacitor value of 80 pF. We first considered the frequency response of the circuit.

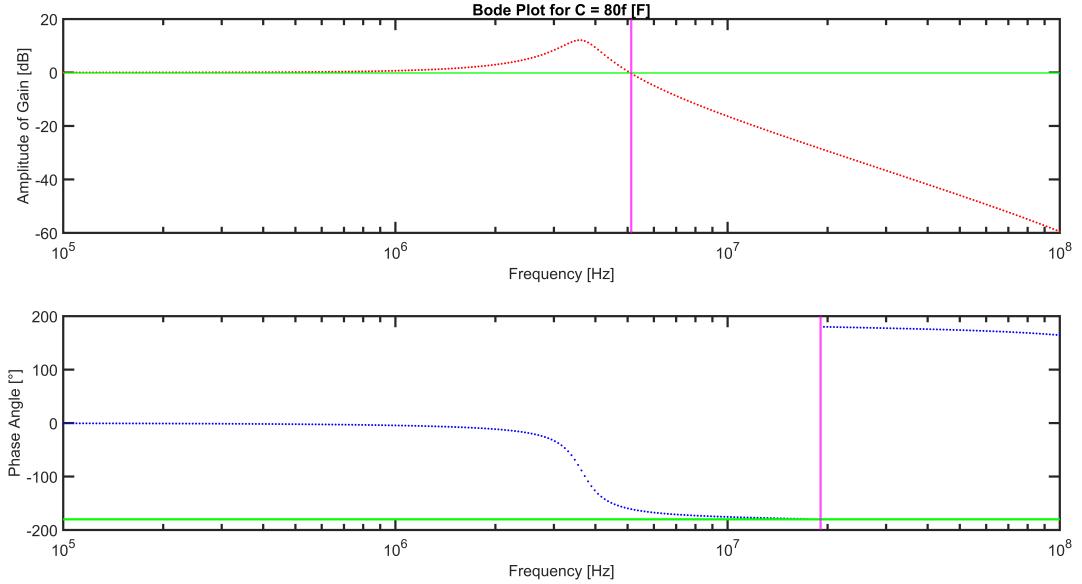


Figure 5: Bode Plot for $C = 80 \text{ fF}$

We found the circuit behaved as expected for higher frequencies. We find the circuit behaves with unity gain until $\sim 1 \text{ MHz}$. This is much higher compared to the case where there was no compensation. When considering the phase angle, we find that this circuit is stable for the regime we considered. We find a pulse in gain amplitude that occurs at 3.5 MHz . We find a value of $\sim 12 \text{ dB}$.

With a pulse here, we considered the ringing that would occur as a result of the pulse. The figure below shows these characteristics,

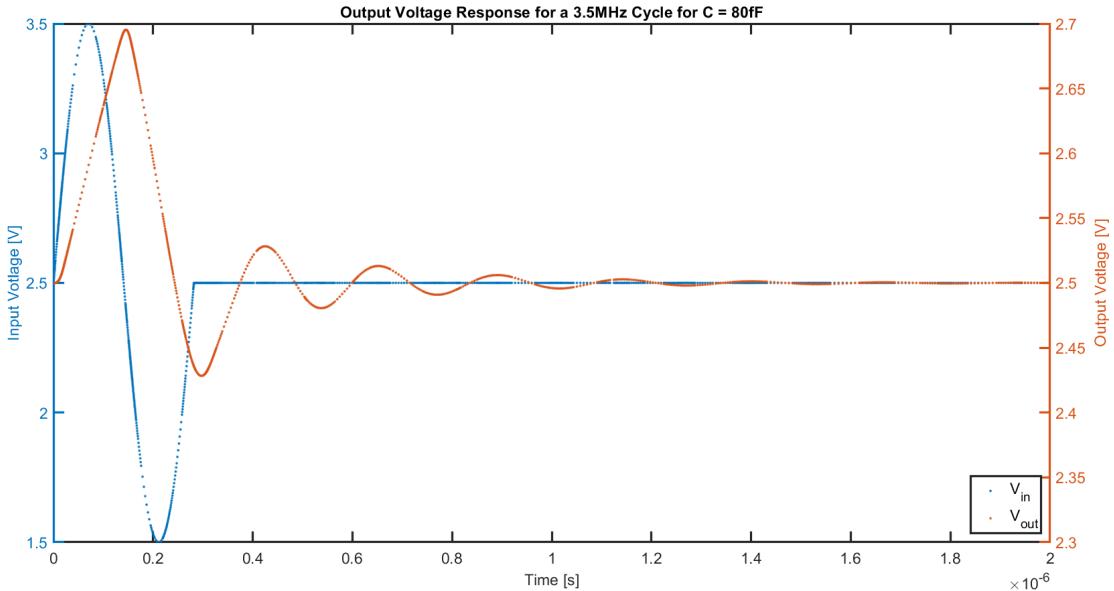


Figure 6: 3.5 MHz Input, V_{out} response

From this, we find that ringing occurs on the output for $\sim 1.6 * 10^{-6} \text{ s}$. The ringing has a peak-to-peak amplitude of $\sim 0.27V$.

3.2.2 $C = 800 \text{ fF}$

All of the results below show the characteristics for a compensation capacitor value of 800 fF.

The following figure shows a bode plot depicting the frequency response of the circuit.

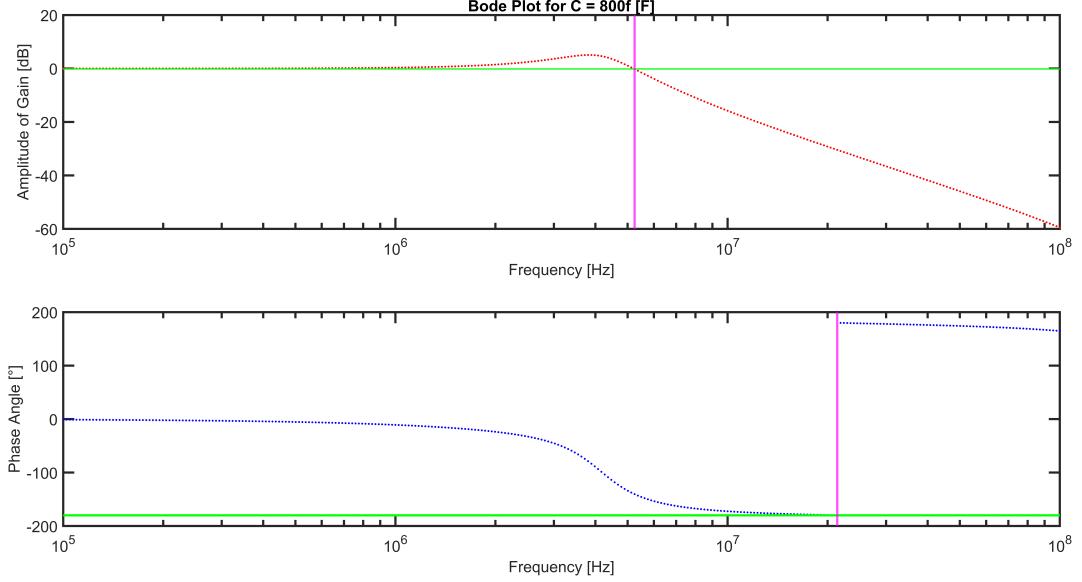


Figure 7: Bode Plot for $C = 800 \text{ fF}$

We found the circuit behaved similarly to the case with a compensation capacitor value of 80 fF. We find the circuit behaves with unity gain until $\sim 1 \text{ MHz}$, which was the same as the 80 fF case. When considering the phase angle as well as the gain, we find that this circuit is stable for the regime we considered. We find a pulse in gain amplitude that occurs at 3.8 MHz , which was the same frequency as the 80 fF case. We find a value of $\sim 5 \text{ dB}$.

With a pulse here, we considered the ringing that would occur as a result of the pulse. The figure below shows these characteristics,

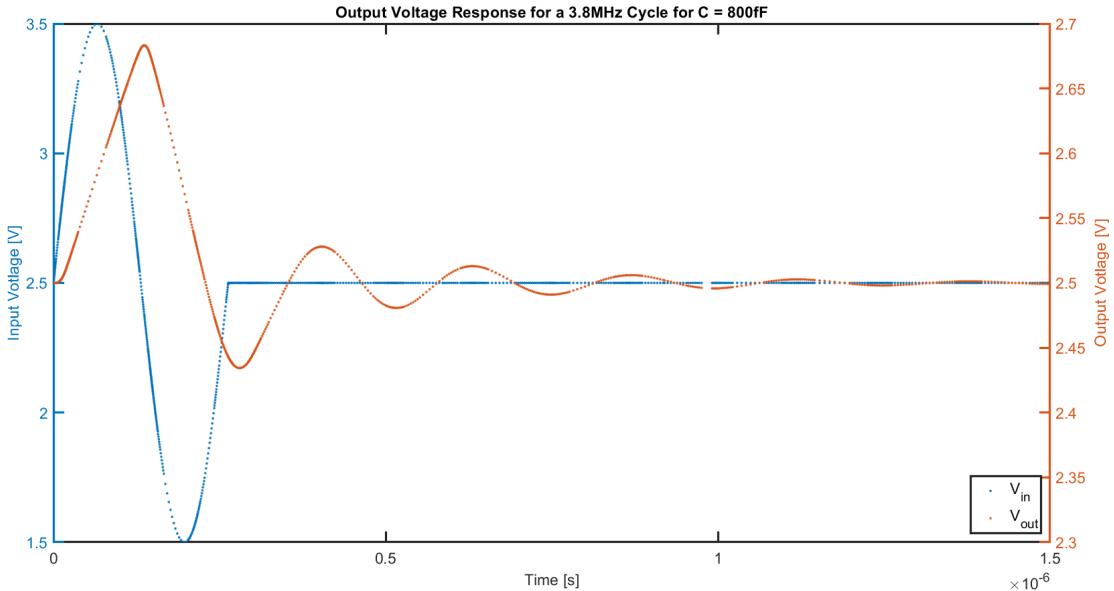


Figure 8: 3.8 MHz Input, V_{out} response

We find that the ringing response of the output behaves with a slightly smaller peak-to-peak amplitude as the 80 fF case (0.2 V); however, the main difference is in the time it takes for the ringing to settle. We find that the ringing in this case settles slightly quicker than the 80 fF case. It takes $\sim 1.25 * 10^{-6}$ s for the output ringing to settle with a compensation capacitor of 800 fF.

3.2.3 C = 1200 fF

All of the results below show the characteristics for a compensation capacitor value of 1200 fF.

The following figure shows a bode plot depicting the frequency response of the circuit.

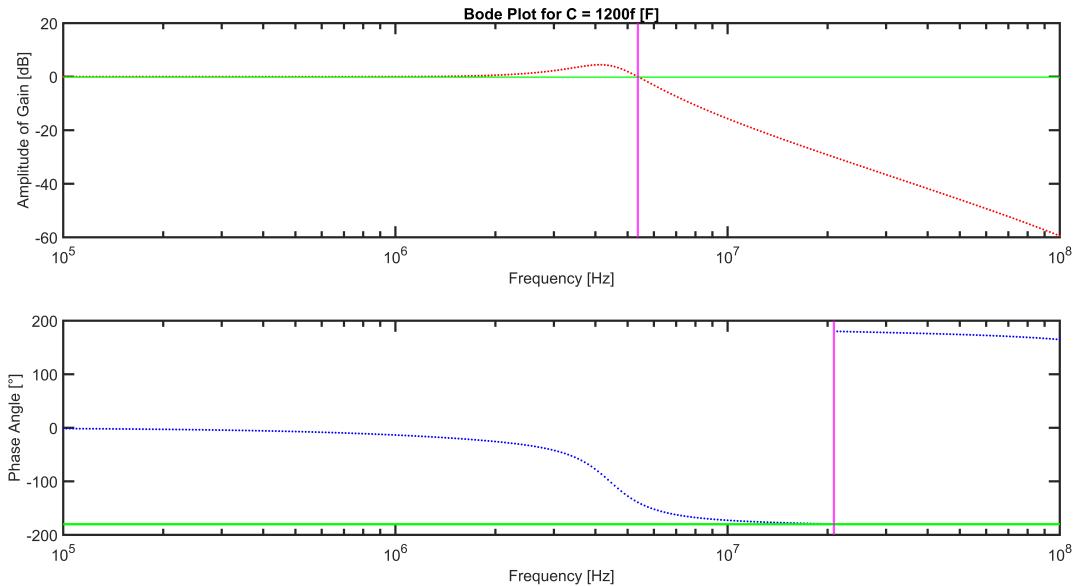


Figure 9: Bode Plot for C = 1200 fF

All in all, the characteristics are similar to the 800 fF characteristics. We find that the circuit behaves as expected for slightly higher frequencies - up to 2 MHz, which was 1 MHz higher than the 800 fF case. We find the spike occurs at ~ 4.2 MHz and has an amplitude of ~ 4.4 dB.

We also considered the ringing of the output as a result of the peak. The characteristics are shown below.

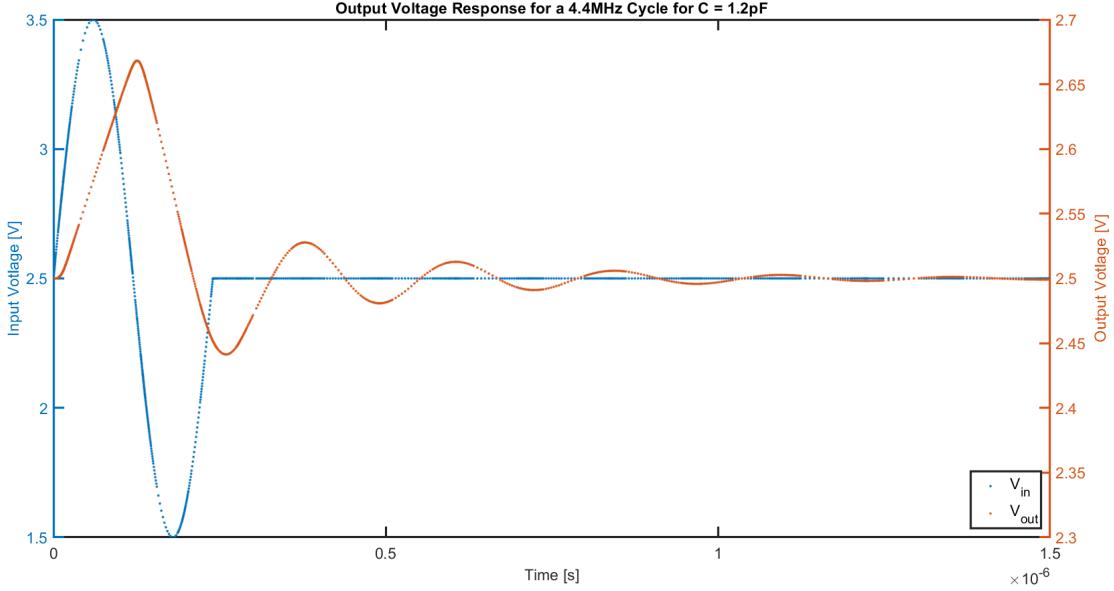


Figure 10: 4.4 MHz Input, V_{out} response

We find that the ringing has a peak-to-peak output voltage similar to that of the 80 fF and 800 fF cases (0.2 V) but is slightly smaller. The settling time of the ringing is the same as it was with the 800 fF capacitor ($\sim 1.25 * 10^{-6}$ s). However, if we were to design an integrated circuit, we would consider the layout as well. Since the behavior is comparable for the 800 fF and 1200 fF cases and since $C \propto W * L$, it would make sense to use the 800 fF capacitor as the compensation capacitor over the 1200 fF to take up less area on a integrated circuit die.

4 Experiment 3: Feedforward Compensation for Operational Transconductance Amplifiers without Miller Compensation

4.1 Background, Procedure and Model Expectations

For the third experiment, we considered a Class-AB Two-Stage CMOS Differential Amplifier with a feedforward transconductance compensation. We looked at the circuit configured as a two-input, one output circuit to consider the frequency response and stability of the system. A schematic of the circuit used is shown below,

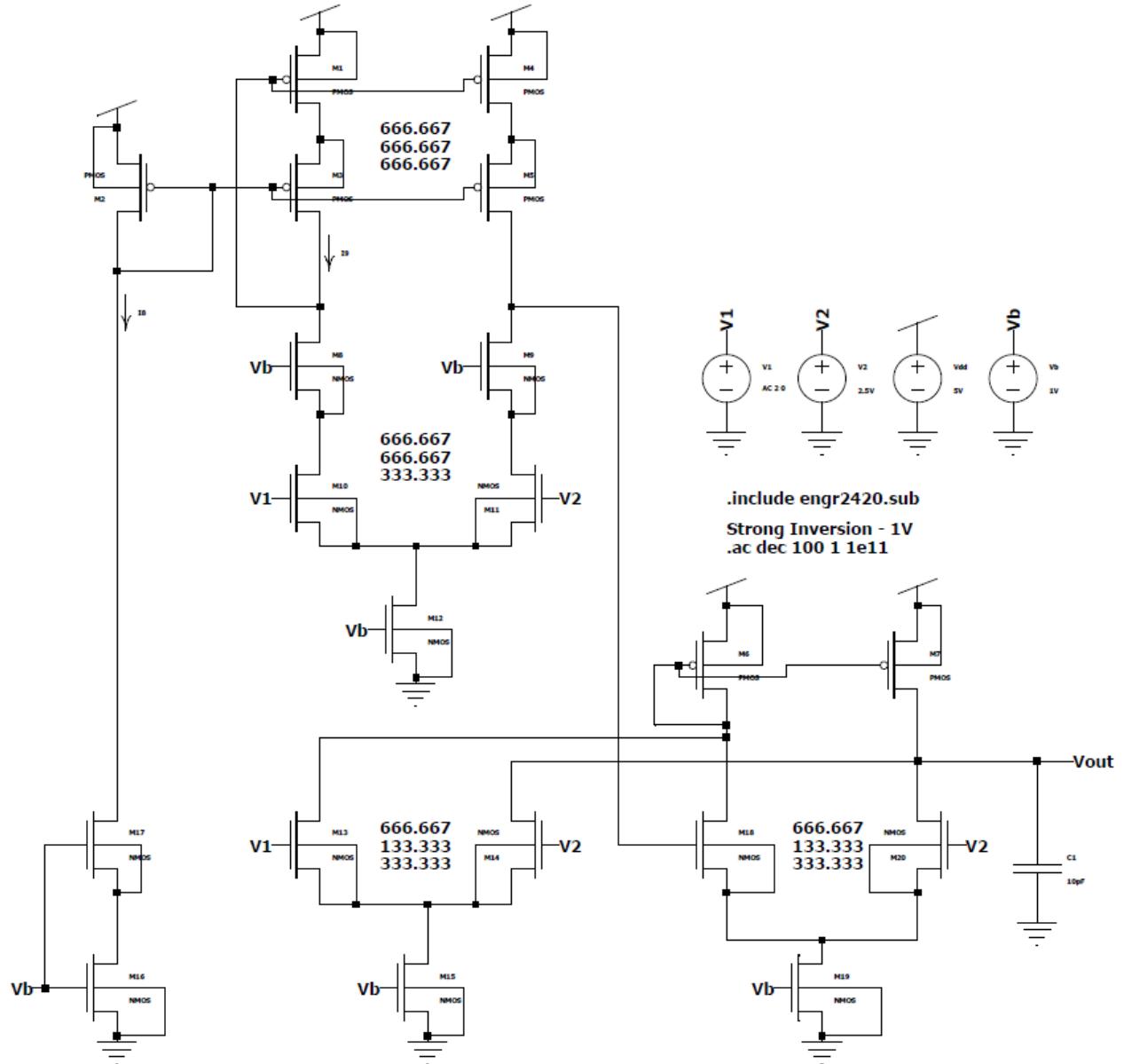


Figure 11: Feedforward Transconductance Compensated Two-Stage Differential Amplifier Schematic

With this circuit, we used strength ratio pairs for the differential pairs as shown in text form on the schematic. We varied the W/L ratio to change the relative strength of each of the transistors in order to observe the changes in the amplifier gain. After performing frequency response simulations, we also considered a transient analysis to look at the ringing of the system that occurs when a circuit is not critically damped. To do this, we input a wave at the frequency of the peak and simulated the output voltage.

The scheme of this compensation uses the positive phase shift of left-half plane zeros created by the feedforward path, to compensate the negative phase shift due to the poles. For the functionality, the scheme requires the second and third stages of the circuit to have a common pole. When the compensation occurs (frequency at which the left-half plane zero occurs), the amplifier phase margin is 90° .

Additionally, using a feed-forward system, we will observe a linearization effect to the bode plot curves from the previous experiments. The output gain would show a linear-device like

behavior, relative to the previously shown plots. *Linearity* contributes toward the figures of merit for an amplifier and other similar control-based devices.

4.2 Results

4.2.1 Matched Differential Pairs

The following results show the characteristics for a matched set of differential pairs. For our simulation, the W/L ratios are as follows:

Transistor Dimensions			
Transistor	W(nm)	L(nm)	Strength Ratio
M13-M14	600	0.9	666.67
M18-M20	600	0.9	666.67
M8-M9-M10-M11	600	0.9	666.67
M1-M3-M4-M5	600	0.9	666.67

We first considered the frequency response of the circuit, as follows:

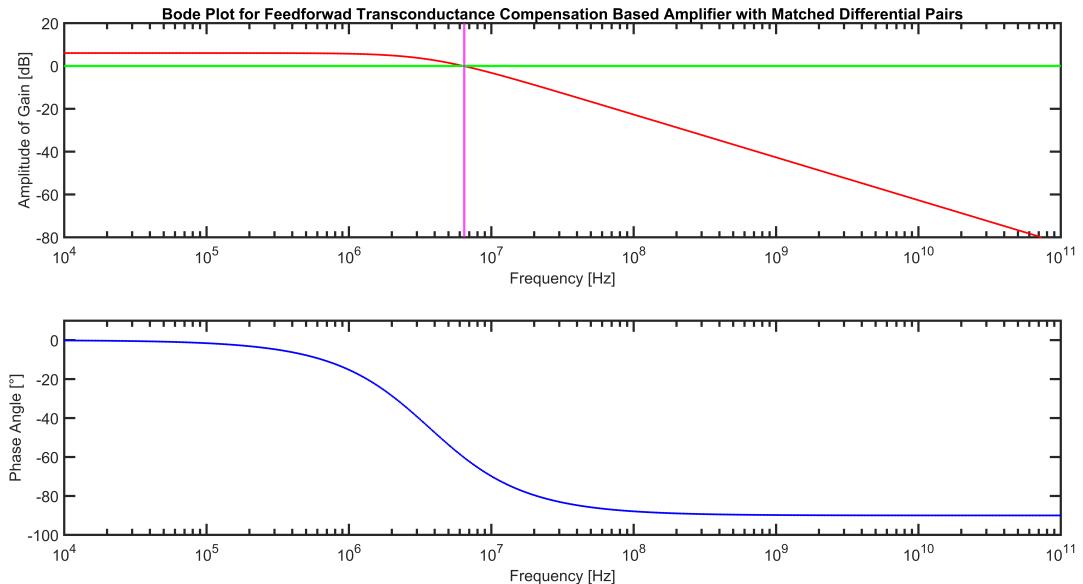


Figure 12: Bode Plot for identical strength ratios

We found the circuit behaved as expected for higher frequencies. We find the circuit behaves with unity gain only at ~ 6 MHz. This is much higher compared to the case where there was no compensation, or miller compensation. Hence, we get a higher bandwidth for feedforward transconductance compensated circuit. When considering the phase angle, we find that this circuit is stable for the regime we considered.

We also considered the ringing that would occur as a result of a pulse, which is shown in the figure below, along with the characteristics,

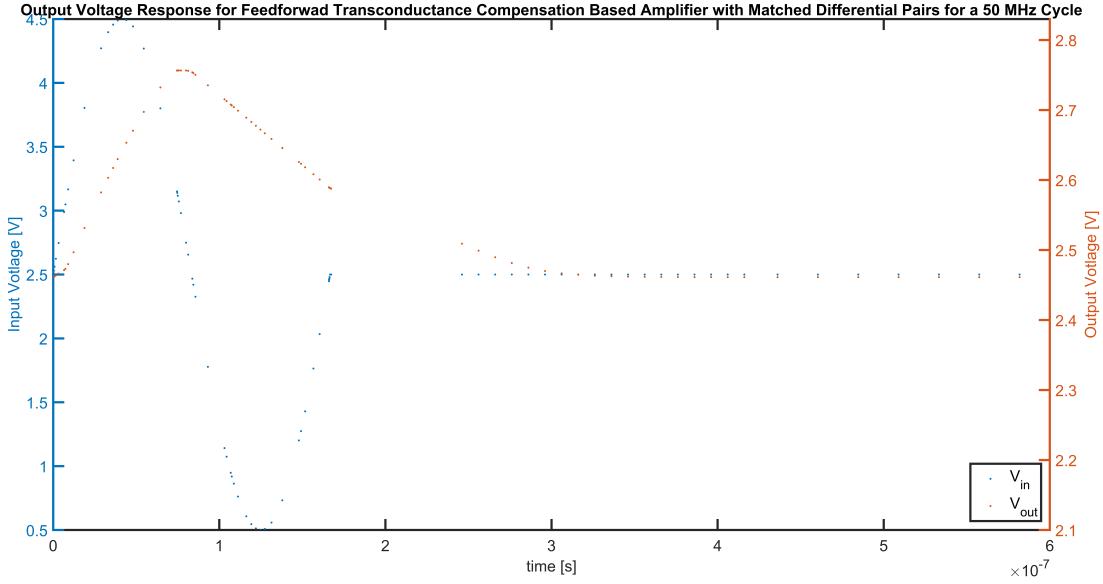


Figure 13: 50 MHz Input, V_{out} response

From this, we find that slight ringing occurs on the output for $\sim 6 \times 10^{-7}$ s. The ringing has a peak-to-peak amplitude of ~ 0.3 V. Considering the other types of compensation that we have considered for this lab, we find this technique to have the least ringing, and highest stability given the frequency of operation.

4.2.2 Unmatched Differential Pairs

The following results show the characteristics for an unmatched set of differential pairs. For our simulation, the W/L ratios are as follows:

Transistor Dimensions			
Transistor	W(nm)	L(nm)	Strength Ratio
M13-M14	120	0.9	133.33
M18-M20	120	0.9	133.33
M8-M9-M10-M11	600	0.9	666.67
M1-M3-M4-M5	600	0.9	666.67

We first considered the frequency response of the circuit, as follows:

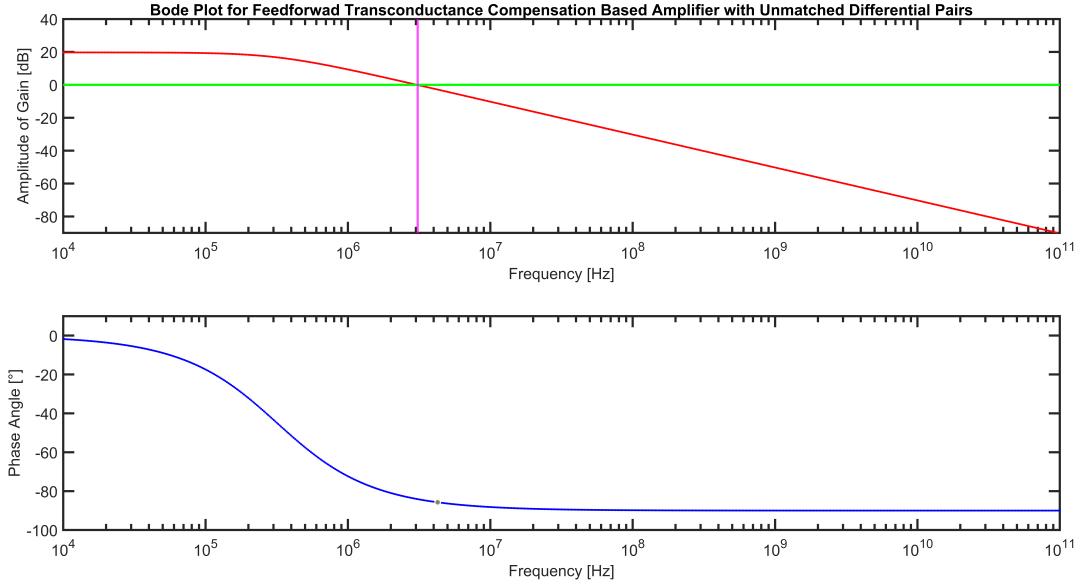


Figure 14: Bode Plot for nonidentical strength ratios

We found the circuit behaved as expected for higher frequencies. We find the circuit behaves with unity gain only at ~ 2 MHz. This is much higher compared to the case where there was no compensation, or miller compensation, but considerably lower compared to the case of matched differential pairs. Hence, we get a relatively lower bandwidth for feedforward transconductance compensated circuit. When considering the phase angle, we find that this circuit is stable for the regime we considered.

We also considered the ringing that would occur as a result of a pulse, which is shown in the figure below, along with the characteristics,

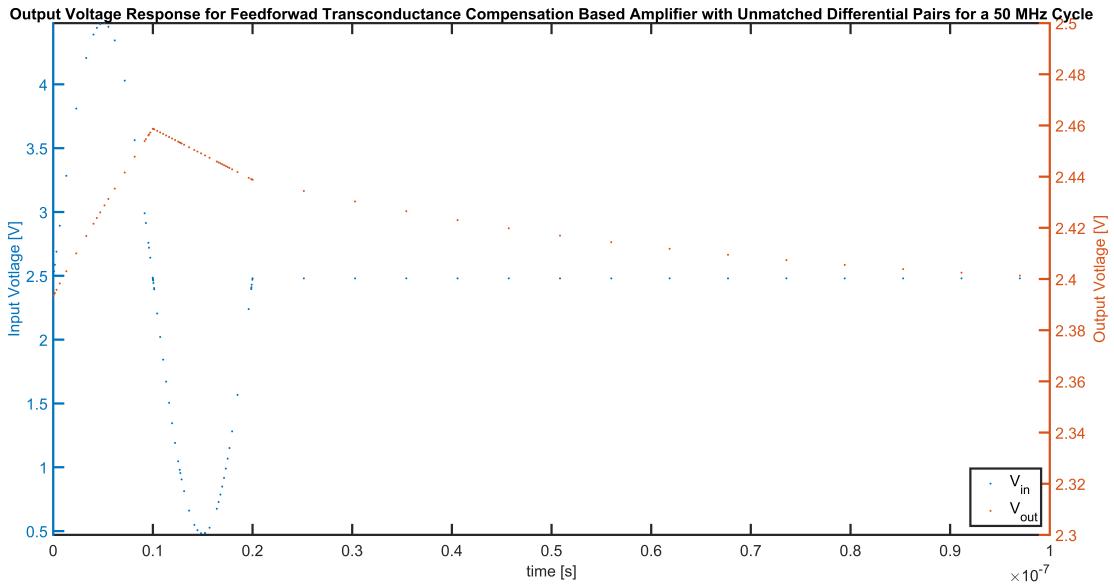


Figure 15: 50 MHz Input, V_{out} response

From this, we find that slight ringing occurs on the output for $\sim 1 * 10^{-7}$ s. The ringing has a peak-to-peak amplitude of ~ 0.06 V. As we observed in the previous circuit, the ringing is

minimal, compared with other compensation techniques. By far in the lab report, this circuit has the least peak-to-peak amplitude as well as settling-stabilizing time for the step response.

5 Summary

Using the circuit topology from experiment 3, we find that the ringing of the output is damped, and occurs over a shorter time period than the ones in experiment 2. It was roughly an order of magnitude quicker for the experiment 3 than it was for experiment 2. We also find the peak-to-peak amplitude of the ringing to be 4 times smaller for the circuit in experiment 3 than those in experiment 2.

Within experiment 2, a 800fF capacitor should be used as this provides great operation characteristics without taking up redundant space. We find that the 1200fF case performs slightly better; however, the improvements are minimal. As we continue to increase the size of the capacitor, we will find slight improvements in the behavior of the circuit. But, as we increase the capacitance, we also increase the area of the capacitor, which may become a concern depending on the application for an amplifier.

6 Bibliography

- Razavi, Behzad. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill Education, 2017
- Baker, Jacob, and Vishal Saxena. *High Speed Op-amp Design: Compensation and Topologies for Two and Three Stage Designs*. Boise State University.
- Thandri, Bharathkumar and Silva-Martínez, José. (2003). *A robust feedforward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors*. Solid-State Circuits, IEEE Journal of. 38. 237 - 243. 10.1109/JSSC.2002.807410.