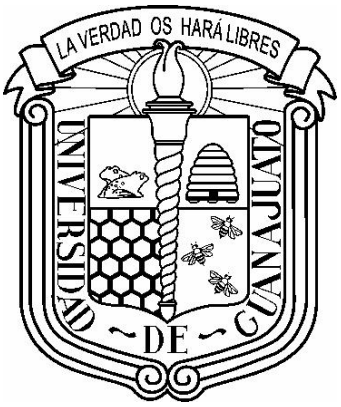

University of Guanajuato

Bachelor's Thesis

Study of Domain Wall Dynamics under Nonlocal Spin-Transfer Torque using heterogeneous computing

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A thesis to obtain the degree of Bachelor of Computacional Systems Engineering

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Abstract

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Study of Domain Wall Dynamics under Nonlocal Spin-Transfer Torque using heterogeneous computing

by Thomas Sanchez Lengeling

This work is an exploration of the role that Graphical Processing Units, also known as GPUs, can play in the acceleration of physical simulations. In particular, in the research of spintronic effects such as the dynamics of domain walls under nonlocal spin-transfer torque. Our study is relevant because it allows researchers to quantitatively test some of the effects of a phenomenon known as spin-diffusion on magnetic configurations at the nanoscale. Some of such configurations are known as domain walls. These magnetic configurations can be observed experimentally in NiFe soft nanostripes but they are really complicated to produce and image experimentally. Due to this, we use the massively parallel capabilities of a single GPU to numerically solve a mathematical equation, known as the Zhang-Li model. As a consequence of our implementation, we have observed a 7.5x speed-up in the solution of the Zhang-Li equation. This speed-up is obtained when we compare the time needed to obtain the result of a simulation in a GPU with that of a simulation with the same input parameters in a conventional processor e.g. Intel Xeon. The numerical method used for the solution is a the method known as Finite Differences in the Time Domain (FDTD) whose integration is done using a 4th order Runge - Kutta integration

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Introduction

Commodity graphics processing units (GPUs) are becoming increasingly popular to accelerate scientific applications due to their low cost and potential for high performance when compared with central processing units (CPUs). A large number of contemporary problems and scientific research are being benefit from this new technology .There has been considerable progress in implementing the hardware and the supporting infrastructure for GPUs programming and streaming architectures. This thesis is a exploration and study of the role of accelerator hardware like the use of the GPUs on physical computing, more specific in the area of spin-diffusion effects within a continuously variable magnetization distribution.

The work begins with a overview of the current trends in computing, focusing our attention specifically on GPUs, on how they differ from the CPUs and common programming practices that uses heterogeneous computing. The second chapter focus on the use of techniques of heterogeneous computing to gain more performance out the GPUs when applying to a specific task. Also the necessary means how to test the speed-up against the CPU. The next chapter is overview of the CUDA code implementation of Dr. Claudio's work "Domain Wall Dynamics under Non-local Spin-Transfer Torque". The forth chapter are the results collected by applying optimization techniques to the initial CUDA code implementation. The outcome is compared by launching the code in-to several GPUs nodes. Finally the last chapter of the thesis is a conclusion of the work and future research.

Chapter 1

Heterogeneous Computing

Heterogeneous computing refers a system that combines several processor types to gain more performance. Typically using a single or multi-core computer processing units (CPUs) and a graphics processing units (GPUs). Frequently GPUs are know for 3D graphics rendering, video games and video editing, but GPUs are becoming increasingly popular for accelerating computing applications and scientific research due to their low price, high performance and relatively low energy consumption per FLOPS (floating point operations per second) when compared with the CPUs. This chapter provides an overview of GPUs within the High Performance Computing (HPC) context, their advantages and disadvantages and how they can be integrated in to a scientific software and research.

1.1 Motivation

The GPU has been essential part of personal computer since the early use. Over the course of 30 years the graphics architecture has evolve form drawing a simple 3D scene to be able to program each part of the GPU graphics pipeline. Their role became more important in the 90s with the first-person shooting video game DOOM by id Software. The demanding video game industry has brought year by year more realistic 3D graphics. Consequently new innovated hardware capabilities has been developed to increase the graphics pipeline and the render output. This lead to a more sophisticated programming environment with a massive parallel capabilities.

The fixed graphics pipeline (fixed functions on the GPU) was introduced in the early 90s, allowed various customization of the rendering process. However only allowed some modifications of the GPU output. Specific adjustment were extremely complicated did

not allow custom algorithms. In 2001 NVIDIA and ATI (AMD) introduced the first programmability to the graphics pipeline. Which could control millions pixels and vertex output in a single frame, moreover it out-performed the CPU in rending video. In addition graphics shift from the CPU to the GPU. This was the beginning of GPU parallel capabilities.

At first the GPUs where only used for general-purpose computing like computer graphics, but in-till resent years the GPU has been used to accelerate scientific research, analytics, engineering, robotics and consumer applications.(GPGPU)[11].

GPUs are attractive for certain type of scientific computation as they offer potential seed-up of multi-processors devices with the added advantages of being low cost, low maintenance, energy efficient, and relative simple to program. Many algorithms in applied physics are using GPUs to improve their performance over the CPU. Some area of scientific research that obtain the benefit of heterogenous computing are: Molecular Dynamics, Quantum Chemistry, Computational Structural Mechanics and Computational Physics [16].

In any case, for a given simulation a compromise between speed and accuracy is always made. The current tendency of the CPU relies on increases the clock seeped, decreasing the size of transistor and finally adding more cores per unit and be able to work and a parallel manner, because of the there are some limitations[21]

Power Wall

The CPUs single core has not gone beyond the 4GHz barrier, a paradigm shift from a single core to a multi-core CPUs, also the power use of CPUs is very high per Watt. The figure 1.1 shows the comparison of performance between the GPU and CPU.

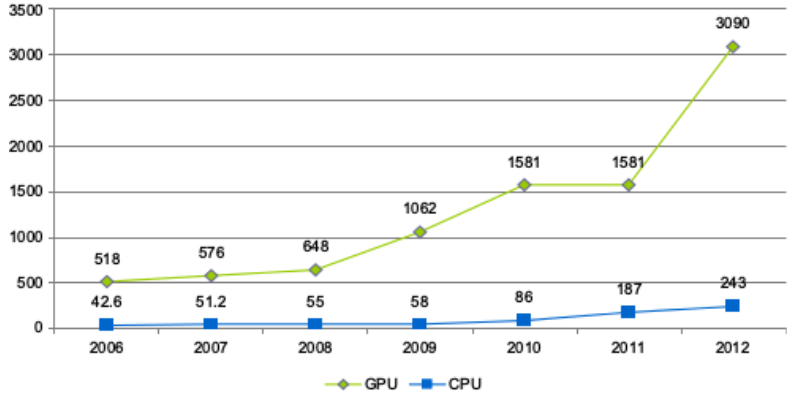

FIGURE 1.1: *GPU and CPU peak performance in gigaflops*

Memory Wall

This refers to the growing disparity of speed between CPU and the memory outside the CPU chip. Some applications have become memory bound, that is to say computing time is bounded by the transfer memory between the CPU and all the hardware devices connected to the CPU, commonly to the Peripheral Component Interconnect (PCI) chip. In conclusion the computing time is bounded by the memory not by the time calculations done on the CPU.

Parallelism Wall

This indicates a law that indicates the number of parallel processes. The number N parallel processes is never ideal and always depends on the problem. The seed-up can be described by Amdahl's Law in terms of the fraction of parallelized work (f). [21].

$$speedup \leq \frac{N}{f + N(1 - f)}$$

The current paradigm of using CPUs for computing is growth unsustainable. In 2012, Japan among the countries with elite supercomputers, builded the machine "K Computer", with 705,024 multi-core CPUs, it can achieve 11.3 petaflops (10^5 flops). Furthermore the computer is one of the most power efficient supercomputer in the world with a total of 12.66 megawatts (MW), in other words 830 Mflops/watt. This is this is enough to power a small town of 10,000 homes. If the current thread of power use continues, the next supercomputer would require 200 MW of power, this would require a nuclear power reactor to run it.[27]. However in 2013 Oak Ridge Nacional Laboratory (U.S) built a supercomputer that combines CPUs and GPUs, the Titan. It can archive an astonish 24 petaflops theoretical peak. Moreover with a power consumption of 8.2 MW. As showed is possible to built a supercomputers that combines CPUs and GPUs, which has a higher performance and lower power consumption compared to a CPU based supercomputer. [19]

As said the GPU exceeds the CPU in calculations per second FLOPS with a low energy consumption. However the GPU is designed to launch small amounts of data in parallel with only several instructions, in other words the GPU swap, switch threads very fast and they are extremely lightweight. In a typical system, thousands of threads are waiting to work. While the CPU only run up-to 24 threads on a hex-core processor. They can execute a single operation on comparatively large set of data with only one instruction. Although this can be extremely cost-wise operation on the GPU.

1.2 GPUs as computing units

A insight of the architecture of GPU can give a idea of why it outperforms the CPU on various benchmarking.

The GPU, unlike its CPU cousin, has thousands for registers per SM (streaming multiprocessor), this are arithmetic processing units. An SM can thought of like a multi-thread CPU core. On a typical CPU has two, four, six or eight cores. On a GPU as many as N SM core. We can see this in the figure 1.2. For a particular calculation, all the stream processors within a group execute exactly the same instruction on a particular data stream, then the data is sent to the upper level, the host (CPU). [5]

As commonly named CUDA cores are the number of processors in a single NVIDIA GPU chip. For example one of the first GPU capable of running CUDA code was the NVIDIA 9800 GT, which had 112 cores, while the latest high-end GPU GTX 980 has 2048 cores.

FIGURE 1.2: *Architecture of a NVIDIA GeForce GTX 580*

Each CUDA core can execute a sequential thread, just like a CPU thread, which NVIDIA calls it Single Instruction, Multiple Thread (SIMT). In addition all cores in the same group execute the same instruction at the same time, much like classical SIMD (Single instruction, multiple data) processors. SIMT handles conditionals somewhat differently than SIMD, though the effect is much the same, where some cores are disabled for conditional operations, in other word a single instruction is executed throughout the device.

Being able to efficiently use a GPU for an application requires to expose the inherent data-parallelism Optimized for low-latency, serial computation. This can be seen in contrast with a CPU, which is optimized for sequential code performance, fast switching registers and sophisticated control logic allowing to run single complex programs as fast as possible, which is not possible on the GPU. Memory management is very important

for GPUs. this refers how to allocate memory space and transfer data between host (CPU) and device (GPU). While the CPU memory hierarchy is almost non-existent, on the GPU inherent data is important. In figure 1.3 different levels of memory can be observer between the host and the device, which differs form the CPU [12].

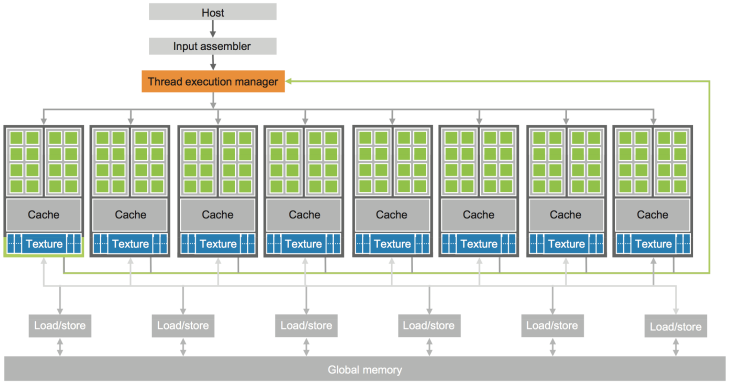

FIGURE 1.3: *Memory transfer between the host and device*

On the GPU precision and optimization are very important but there is a penalty for choosing performance or precession. All the GPUs are optimized for single precision floating operations, 24 bit size, Also provides double precision point, size of 53 bits. This is using the standard notation IEEE 754. Normally the GPU uses single precession(SP) by default, if chosen double precision (DP), normally there is a penalty of 2x - 4x seed-up. [30] Libraries such as CUBLAS and CUFFT provides useful information how NVIDIA handles floating point operations under the hood.

1.3 Programming on GPUs

There exist, among many, two main computing platforms, NVIDIA's Compute Unified Device Architecture (CUDA), and Khronos's Open Computing Language (OpenCL). NVIDIA's CUDA provides the necessary tools, frameworks and library to programs parallel computing, but for there GPUs. While OpenCL is a open standard framework meaning that is possible to do parallel computing on other GPUs, like on AMD cards. Programmers can easily port their code to others graphics cars. However CUDA has more robust debugging and profiling for GPGPU computing. This two frameworks are developed to be close to the hardware layer, using C programming language. CUDA provides both a low level API and a higher level API. Those who are familiar to OpenCL and CUDa, can easily modify their code to work on either platform.[12]

The CUDA programming model views the GPU as an accelerator processor which calls parallel programs throughout all the SMI. This programs are only called on the device and are called kernels, which launch a large amounts of threads to execute CUDA code. The basic idea of programming on a GPU is simple. We can observer this in the figure 1.4

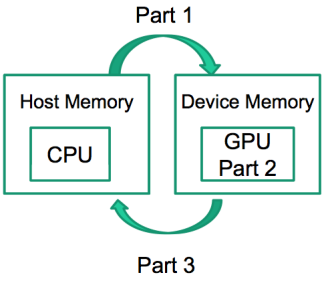

FIGURE 1.4: *Programming Cycle between the CPU and GPU*

- Create memory(data) for the host (CPU) and devices (GPUs)
- Send the data host memory to the highly parallel device.
- Do something with data on the device, e.g. matrix multiplication,calculation, parallel algorithm.
- Return the data from the device to the host.

The structure of CUDA reflects the coexistence of CPU and GPUs. The CUDA code is a mixture of both host code and device code. The CUDA C compiler is called NVCC. The host code is the standard low level ANSI C language. The device code is marked is CUDA keywords for identifying data-parallel functions and has a extension file .cu.

When a kernel is launched, executed by a large amount of threads, where they are organized as a one, two or three dimensional grid of thread blocks. A thread is the simplest executing process. It consists of the code of the program, the particular point where the code is being executed. [12]. Many threads form a block, and many blocks form a grid. CUDA handles the execution of the random-access threads, which take up-to very few clock cycles in comparison to CPU threads. The threads per block can be observer in figure 1.5. All the threads in a kernel can access the global memory, figure 1.3.

Each of the threads can be access by implicit variable that identifies its position within the thread block and its grid. In a case of 1-D block. [25]

$$blockIdx.x \times blockDim.x + threadId.x$$

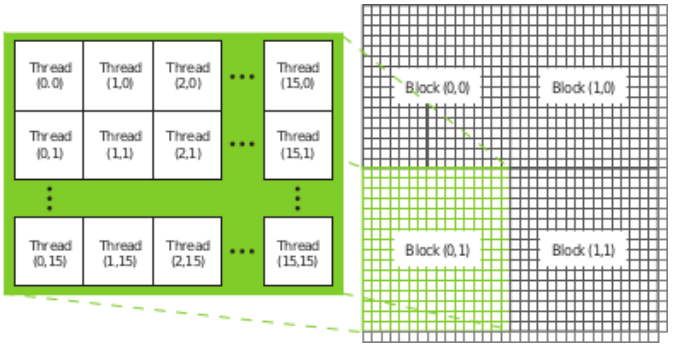

FIGURE 1.5: *Part of a 2D CUDA's thread grid, divided in blocks, each block with its own respective threads.*

In CUDA. host and device have separate memory spaces. This can bee seen on the host and device with the DRAM(Dynamic random-access memory) data. For example a NVIDIA GTX 660m comes with 2GB of memory, which is the global memory for the device. As told the host and device allocates data. The programmer needs to send data from the host memory to the device's global memory. We can see this in the figure **??**. Once the memory is transfer back to the host, is completely necessary to free the memory from the device and host. This is typically done with free or delete on C/C++. The CUDA's Application Programming Interface (API) functions performs this activities on behalf of the programmer. [12]

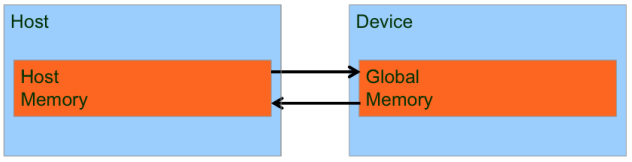

FIGURE 1.6: *Separate memory spaces for the CPU and GPU*

1.3.1 Vector Addition Example

A simple example of a vector addition to show the comparison between the GPU and CPU, input, two list of number which is sum up each corresponded element to produce a final output with the addition of both list. Figure 1.7 shows this process. [25]

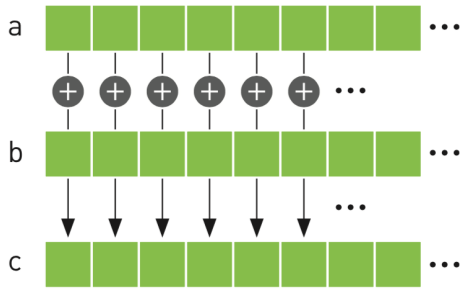

FIGURE 1.7: *Simple Vector Addition Example*

1.3.1.1 CPU Code

This first example illustrates the CPU code executed in a single thread. The code is straight forward to understand. First create the memory for each array, A, B and C with size N. Then calculate the sum of the two vectors with the function *add*. As we can see in the function *add*, we use the while loop to go through each element of the arrays A and B, which are added into a single array C.

```
#include <iostream>
#define N 100

void add( int *a, int *b, int *c );

int main()
{
    int A[N], B[N], C[N];

    //fill the arrays with values
    for(int i = 0; i < N; i++){
        A[i] = 1; B[i] = i;
    }

    add(A, B, C);

    //Display the results
    for (int i = 0; i < N; i++)
        std::cout << A[i] << ", " << B[i] << ", " << C[i] << std::endl;

    return 0;
}

void add( int * A, int * B, int * C )
{
    int index = 0;

    //go through each index of the arrays and make the operation
    while(index < N){
        C[index] = A[index] + B[index];
        index++;
```

```
    }
}
```

LISTING 1.1: *CPU Vector Addition*

We can notice if we set N to be a large number, the function *add* could take a large amount of time to execute. But the example only illustrates the used of the CPU as a single core, however nowadays CPUs commonly have around 4-8 cores. To be able to execute the previous code on all the cores available in the CPU, threads are needed to be implemented. But you would need reasonable amount of code and debugging to make that happen. Also is a complicated task to schedule all the threads in the CPU.

1.3.1.2 GPU Code

We can accomplish the same operation very similar in the GPU with CUDA. First create CPU and GPU memory, with there corresponded code. Send the CPU memory to the device, make calculations on the highly parallel GPU, finally return the results the CPU.

```
#include <iostream>
#define N 100

// CUDA KERNEL
__global__ void add( int *a, int *b, int *c );

int main()
{
    int a[N], b[N], c[N];
    int *dev_a, *dev_b, *dev_c;

    // allocate the memory on the GPU
    cudaMalloc( (void**)&dev_a, N * sizeof(int) ) );
    cudaMalloc( (void**)&dev_b, N * sizeof(int) ) );
    cudaMalloc( (void**)&dev_c, N * sizeof(int) ) );

    //allocate the memory on the CPU
    for(int i = 0; i < N; i++){
        A[i] = 1; B[i] = i;
    }

    //calculate the vector addition in the GPU
    add<<<N,1>>>( dev_a, dev_b, dev_c );

    //copy back the result from the GPU to the CPU
    cudaMemcpy( c, dev_c, N * sizeof(int), cudaMemcpyDeviceToHost ) );

    //Display the results
    for (int i = 0; i < N; i++)
        std::cout << A[i] << ", " << B[i] << ", " << C[i] << std::endl;

    cudaFree( dev_a );
```

```
    cudaFree( dev_b );
    cudaFree( dev_c );

    return 0;
}
```

Listing 1.2: *GPU Vector Addition*

The function *cudaMalloc* and *cudaFree* are very similar to the C functions *malloc* and *fee*, which allocating memory and deleting memory respectively.

CUDA automatically spams the threads to it correspondent block, so we only need to access the index of the block and pass it to the index arrays. To parallel code will stop in-till the block index reaches the number of elements of the arrays, N.

```
void add( int * A, int * B, int * C )
{
    // handle the data at this index if (tid < N)
    int index = blockIdx.x;
    if(index < N)
        c[index] = a[index] + b[index];
}
```

Listing 1.3: *GPU Vector Addition*

The biggest difference between the CPU code and the GPU code is how threads are managed within the process. The CPU code has only one thread, thrust one loop, however if we want to expand the CPU code to multiples threads, extra loops are required for each additional thread. Based on this idea, the GPU code is launched to every threads accessible by the device chip.

Finally, this chapter provided a overview of heterogeneous programming in a modern context. CUDA enhance the C language with parallel computing support. Which is possible to launch enormous amounts of parallel threads, oppose of few threads on the CPU. The number of GPU cores will continue to increase in proportion to increase in available transistors as silicon process improve. In addition, GPUs will continue to go through vigorous architectural evolution. Despite their demonstration high performance on data-parallel applications. [12]

Chapter 2

Heterogeneous Performance Analysis and Practices

When working with GPUs hardware challenges emerges. How can we make the best usage of the GPU hardware. In the conventional CPU model we have what is called linear or flat memory model. This appears to the programmer as a single contiguous address space. The CPU can directly address all the available memory, in other words there is almost no efficiency penalty in creating global data, local data, or even access data that is located on a opposite memory location, all of this can be access as a contiguous block. [5] Meanwhile on the GPU there are expectations, their exists different memory hierarchies which dramatically change the performance output. By allocation the optimal memory types, seed-up and increase throughput can be accomplished, but also analyzing. To ensure optimization, some analysis should be done, like comparing latency, memory hierarchies and data bandwidth between CUDA kernels, The study of the performance of the CUDA code can be done by using NVIDIA's Visual Profiler.

2.1 Practices

There are three rules based on NVIDIAs standers to follow for creating a high performance GPGPU (General-purpose on the GPU) program.[7]

1. Get the data on the GPU device and keep it there
2. Process all the data en the GPU, give it enough work to do.
3. Focus on data reuse within the GPU context, to avoid memory bandwidth limitations

GPUs are plugged into the PCI Express bus of the host computer. The PCIe bus has extremely slow bandwidth compared with the GPU. This is why is important to store the data on the GPU and keep it busy. And minimize the data transfer to the host and back to the device. We can see this in the following table 2.1. Because CUDA-enable GPUs can carry out petaFLOP performance, they are fast enough to compute large amount of data. So each Kernel launch needs to use all the available resources of the GPU and avoid wasting compute cycles. If a single Kernel doesn't use all of the available bandwidth, multiple kernels can be launched at the same time on a single GPU. For example a DP vectors require 8 bytes of storage per vector element this will double the bandwidth requirement. So is important to take advantage of the memory usage, take advantage of the memory types, use less memory copies between the GPU. [7]

	Bandwidth (GB/s)	Speedup over PCIe Bus
PCIe x16 v2.0 bus (one-way)	8	1
GPU global memory	160 to 200	20x to 28x

FIGURE 2.1: *PCIe bus and GPU bandwidth comparison*

Some practices should keep in mind to rapidly identify the portions of code where it would be beneficial for GPU acceleration.[17]

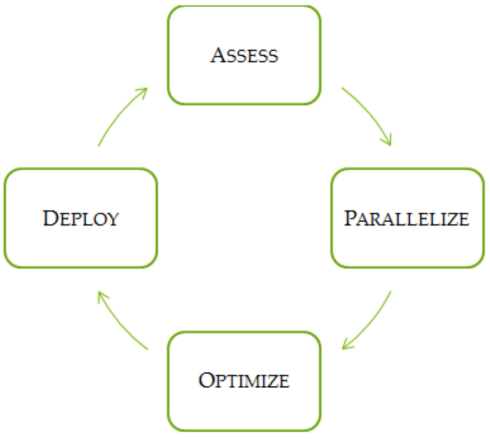

FIGURE 2.2: *Different memory type and penalties usage*

Asses

The first step is to locate the part of the code where the majority of the execution time occurs. The programmer can evaluate memory bottlenecks for GPU parallelization.

Parallelize

Increase parallelization from the original code, could be either adding GPU-optimized

libraries such as cuBLAS, cuFFT, or including more amount of parallelism exposure though the use of CUDA code.

Optimize

The developer can optimize the implementation performance through a number of considerations, overlapping kernel executing, kernel profiling, memory handling and fine-tuning floating-point operations.

Deploy

Compare the outcome with the original expectation. Determinate the potential speedup by accelerating a given section. First a partial parallelization should be implementation before carrying out a complete change.

2.2 Performance Metrics

Before trying to make your simulation run faster, you should understand how it currently performs and where the bottlenecks are. There are many possible approaches to profiling the code, but in all cases the objective is the same: to identify the function or functions in which the application is spending most of its execution time and increase the throughput by a giving kernel. Throughput is how many operations completed per cycle.

2.2.1 Timing

Timing a launched kernel can be done on either the GPU or the CPU. Is important to remember that the CPU and GPU are not synchronized. So its necessary to synchronize the CPU thread with the GPU kernels launches. CUDA provides the required functions to synchronize the CPU with the GPU calling immediately before starting the timer.[17]. CUDA also can handle timers within the GPU, and record times in a floating-point value in milliseconds. This is done with *cudaEventRecord*(), just by including *start* and *stop* in the function inputs. Note that the timing are measured on the GPU clock, so the timing is independent from the OS. [5].

2.2.2 Bandwidth

The bandwidth refers to the rate at which data can be transferred between host and device and vi-versa. The bandwidth is one of the most important factors for testing performance o the GPUs. Choosing the right type of memory could dramatically increase performance and bandwidth. There are two main memory to indicate performance,

theoretical bandwidth and effective bandwidth. The theoretical bandwidth is base on the hardware specifications that is available by NVIDIA. This is calculated using the following formula:

$$theoreticalbandwidth = (clockrate * (bit - wide - memory - interface/8) * 2)/10^9$$

For example the NVIDIA GeForce GTX 280 uses DDR RAM with a memory clock rate of 1,105 MhZ and a 512-bit-wide memory interface

$$(1107 * 10^6 * (512/8.0) * 2)/10^9 = 141.6Gb/sec$$

The GTX 280 has a theoretical bandwidth of $141.6Gb/sec$. The effective bandwidth is calculated by timing specific program activities and by knowing how data is accessed by the application. [17]

$$effective - bandwidth = ((Br - Bw)/109)/time$$

Where Br is the number of bytes read per kernel, Bw is the number of bytes written per kernel and t is the elapsed time given in seconds. [24]

In practice the difference between theoretical bandwidth and effective bandwidth indicated how much bandwidth is wasted on accessing memory and calculations. If the effective bandwidth is low compared to the theoretical bandwidth is one indication that there is not enough work being done in the GPUs. There a several solutions, analyze the code to make more parallelize instructions, execute more computational instructions on the GPUs, finally analyze the number of threads per block that are executing on execute kernels .

2.3 Memory Handling with CUDA

In this section four types of memory handling are going to be explained, shared memory, global memory (device memory) and finally host memory. As the figure 2.3 illustrates the position of the different types of memory inside the device chip. The global memory is faraway the registers and CUDA core locations, however is very large in comparison to the shared memory. [5].

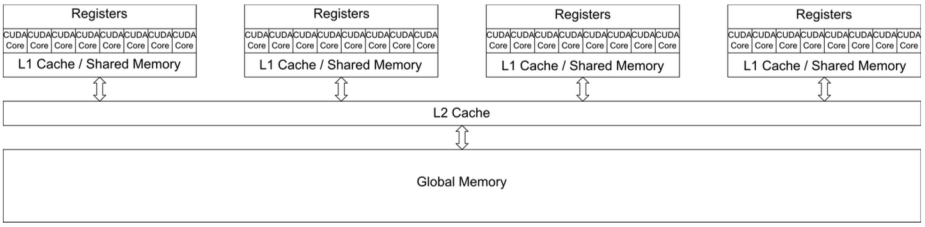

FIGURE 2.3: *The schematic cache hierarchy of a CUDA GPU with 4 Streaming Multiprocessors and 8 CUDA Cores each.*

In figure 2.4 each memory type has it's bandwidth penalty of used and latency in cycles. Each one can be used in different applications to maximize the memory used. The shared Memory is very limited so it cannot be handler for all the kernels, when performed wrong on the device there is a huge latency and bandwidth penalty, instead having a gain in performance

Storage Type	Registers	Shared Memory	Texture Memory	Constant Memory	Global Memory
Bandwidth	~8 TB/s	~1.5 TB/s	~200 MB/s	~200 MB/s	~200 MB/s
Latency	1 cycle	1 to 32 cycles	~400 to 600	~400 to 600	~400 to 600

FIGURE 2.4: *Different memory type and penalties usage*

2.3.1 Global Memory

Understanding how to efficiently use global memory is essential in CUDA memory management. Focusing on data reuse within the SM and caches avoids memory bandwidth limitations. Global memory on the GPU is designed to quickly stream memory blocks of data into the SM.

- Get the data on to the Device, keep it there.
- Give the GPU enough workload, this using all the resources available from the GPU.
- Focus on data reuse within the GPGPU to avoid memory bandwidth limitations.

In other words the global memory resides on the device, and it can be anything from 1 byte to 8GB, depending on the GPU. Also the memory is visible to all the threads of the grid. Any thread can read and write to any location of the global memory, The memory is always allocated with *cadaMalloc*. And only global memory can be passed to the kernels and are called with _global _. [7]

2.3.2 Shared Memory

CUDA C compiler treats variables differently than a typical variable, it creates a copy of the variable for each block that is launched on the GPU, now every thread in that block can access the memory, this is why is called shared memory. This memory reside physically on the GPU, because the memory is very close the cache, the latency is typical very low.[25]. One thing comes to mind, if the threads can communicate with others threads, so there should be way to synchronize all the threads. A simple case should be if thread A writes a value into the shared memory, and Thread B wants to access we need to synchronize, when thread A finish writing then Thread B can access it. This is typical case when shared memory with synchronize thread is needed. [5] Shared memory is magnitudes faster to access than global memory, essentially is like a local cache for each threads of a block. While the shared memory is limited to 48K a block, the global memory is the amount of DRAM on the device. The duration of the shared memory on the device is the lifetime of the thread block. Using _shared _in-front of the kernel call will invocate shared memory.

2.3.3 Constant Memory

Is an excellent way to store and broadcast read-only data to all the threads on the GPU. One thing to keep in mind is that the constant memory is limited to 64KB. [7]. A simple analogue is the *#define* or *const* attribute in the c++ programming language, the variable performed like a variable that cannot be modified. On CUDA is excitability the same, the value can only be read and not written, the value will not change over the course of a kernel execution and only the host can write the constant memory.[25]

2.3.4 Texture Memory

Like constant memory, texture memory is another variety of read-only memory that can improve performance and reduce memory traffic when reads have certain access patterns. . Traditionally Texture memory id used for computer graphics applications, but it can also be use for HPC. The main idea of this read-only memory is that threads are likely to read from address "near' the address they nearby threads.[25]

The texture Memory in a form works like the GPU graphics Texture, when you want to use the texture bind with some sort of data is necessary and when you finish using it unbind the texture from the data. The usage can be summarized in the following table:

- Allocate global memory in the Host.

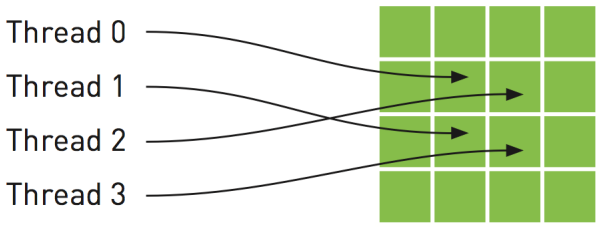

FIGURE 2.5: *Mapping of threads into a two dimensional array of texture memory*

- Create Texture reference and bind it to memory object.
- On the device obtain the reference from the texture.
- Use Texture memory operations on the device
- When the work is done on the Texture, unbind the texture reference on the host.

2.3.5 Thread Synchronization

This refers to synchronizing threads operations. For efficiency, a pipeline can be created by queuing a number of kernels to keep the GPGPU busy for as long as possible. Further, some form of synchronization is required so that the host can determine when the kernel or pipeline has completed. [7] Commonly used synchronization mechanisms are:

- Explicitly calling cudaThreadSynchronize(), which acts as a barrier causing the host to stop and wait for all queued kernels to complete.
- Performing a blocking data transfer with cudaMemcpy() as cudaThreadSynchronize() is called inside cudaMemcpy().

The basic unit of work on the GPU is a thread. It is important to understand from a software point of view that each thread is separate from every other thread. Every thread acts as if it has its own processor with separate registers and identity. Will wait for all threads to finish there job. [7]

2.4 Concurrent Kernels

As we seen kernels are executed in a sequential form with parallel instructions. With CUDA's streams is possible to launch several kernels in parallel, overlap kernel in the same launch sequence. As illustrated in Figure 5.3.

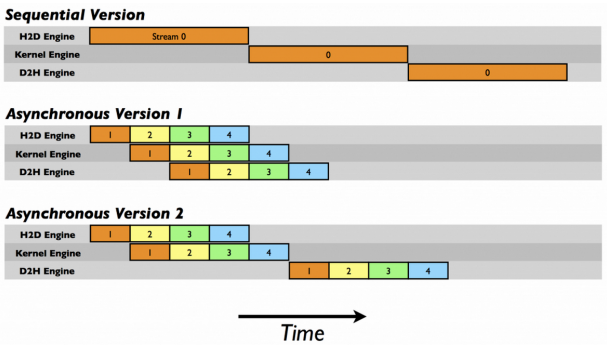

FIGURE 2.6: *Overlaping kernel execution using CUDA streams*

To overlap kernel execution and data transfers, in addition to pinned host memory, the data transfer and kernel must use different, non-default streams. Non-default streams are required for this overlap because memory copy, memory set functions, and kernel calls that use the default stream begin only after all preceding calls on the device (in any stream) have completed, and no operation on the device (in any stream) commences until they are finished. The following is an example of overlapping kernel execution and data transfer. As the 5.3 shows. [12]

By using two or more CUDA streams, we can allow the GPU to simultaneously execute a kernel while performing a copy between the host and the GPU. We need to careful about two things. First, the host memory involved needs to be allocated, since we will queue our memory copies, we need to asyncronize those copies. Second. we need to be aware that the order in which we add operations to our streams will affect out capacity to achieve overlapping of copies and kernel execution. The general guideline involves a breadth-first, or round robin, to assign work and queue work to the kernels. [25]

2.5 Kernel Analysis

As said before, kernels are the essential part of CUDA programming, threads are launched automatically throughout each thread blocks of the device. Furthermore it millions of threads execute the same code parallel, which is When execution the

Memory Bandwidth Bound

This refers when the code/application is limited by memory access. Most GPUs card have 1GB- 6GB of memory, this is used to process the data on the GPU, while the CPU has massively amount of memory available for use. A solution to

this is to reuse the data, change the type of memory used in the GPU. A multi-GPU approach, launching kernels in several GPUs at once. This will dramatically increase the amount of memory in the application.

Compute Bound

Refers to the computation time execution, in other works calculations done in the device, under the assumption that theres is enough memory for the calculations. what is actually the analysis time operations on the kernels. Theoretical bandwidth vs effective Bandwidth can measure performance for a compute-bound Kernel. Therefore its possible to increase the FLOPS per device.

Latency Bound

Is one whose predominate stall reason is due to memory fetches. This is actually the saturating the global memory, or any type, but still have to wait to get the data into the kernel. Physically can be the data being sent from one part of the Device to the other. Also depends the time required to perform an operation, and are counted in cycles of operations. A way to reduce the latency is to increase the number of parallel instructions (more calls per thread), in other words more work per thread and fewer threads.

The performance of relatively simple kernels, which perform computations across a large number of data elements, is more a function of the GPU's memory system performance than the processing performance. It can be beneficial for such memory-bound kernels to decrease the amount of memory access required by increasing the complexity of the computation. [5]

2.6 Hardware constraints

This refers to the limit how many threads per block a kernel launch can have. If exceed this values they kernel will never run. The threads per block really depends of the hardware capabilities. The compute capabilitiesThe compute capability of a device is represented by a version number, also sometimes called its "SM version". This version number identifies the features supported by the GPU hardware and is used by applications at runtime to determine which hardware features and/or instructions are available on the present GPU.[18] In a roughly summarized as:

- Each block cannot have more than 512/1024 threads in total. (Capability 1.x or 2.x-3.x)

- The Maximum dimensions of each block are limited to [512,512, 64]/[1024, 1024, 64](compute 1,1.2)
- Each block cannot consume more than to 8k, 16k, 32K registers total
- Each block cannot consume more than 16kb/48kb of shared memory

SM Resources, improve performance of an application by trading one resource usage for another. [17]

Another inefficiency that can cause low performance to the applications is the number transfers memory calls between the CPU and GPU. The GPU communicates with the CPU via a *PCIe* bus, in addition all of the massive FLOPS per second that can be achieve cannot actually be sent to CPU. The GPU should be filled with the enough workload at the beginning of the application and at the end only return the memory to the CPU.

2.6.1 Thread Division

The hardware has its limits, how much thread per block a kernel can handle. Launching a kernel with the hardware constrains for above can only ensure us that the kernel will actually be executed in the device, nonetheless not 100% optimal. Furthermore is necessary to launch kernels with the amount of threads per block base on the hardware contains and the problem. The block size that is chosen will determine how faster the code will run. By Benchmarking, is possible to find what configuration is the best for the problem. One thing to notice is that thread blocks should be a multiple number of SMs, with this idea is possible to obtain optimal thread block configuration.

2.7 Visual Profiler

Is a hard task to keep track of each individual thread. This becomes difficult for debugging highly parallel applications. The NVIDIA's Visual Profiler is a profiling tool that can be used to measure performance and find potential opportunities for optimization in order to archive maximum performance on the GPUs. The Profiler provides metrics in the form of plots and graphs, which describes opportunities to fully utilize the compute and data movements capabilities of the GPU, as well of each kernel launch in the application. See Figure 2.7.

NVIDIA's profiling tools comes in various flavors; a standalone profiler through the visual profiler compiler nvvp, integrated in a GUI Nsight Eclipse Edition as NSight

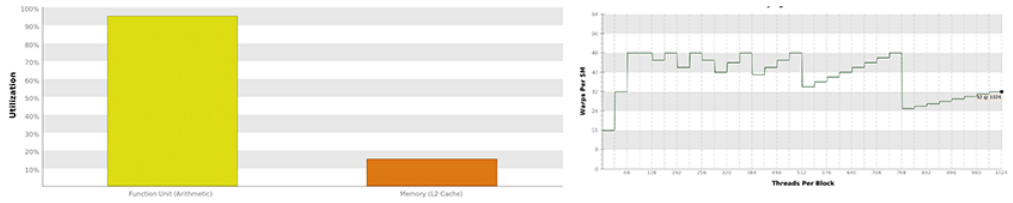

FIGURE 2.7: *Profiler provides optimization metrics*

command (Visual Profiler), and as a command-line profiler though nvprof command. Each one has its disadvantages and advantages. The command-line profiler is useful for remotely access, where a GUI is not available, while the NSight can show graphs, plots and timeline of the application. The Profiler support CUDA applications as well as openCL applications, however both have some exceptions.

The Visual Profiler, by default, will execute the entire application, nonetheless typically only some parts of application only need performance optimization. This enables to determine kernels, code where critical performances is needed. The common situations where profiling a region of the application is helpful.[18]

- Analyze data initialization and movement in the CPU and GPU, as well as evaluating CUDA calls.
- The application operates in phases, where a algorithm operates throughout each region. The application can be optimized independently from other phases of the code.
- The application contains algorithms that operate though a large number of iterations. In this case is possible to collect data from a portion of the iterations.

The Visual Profiler provides a step-by-step optimization guidance, where is possible to evaluate the GPU usage, examine individual kernels and analyze timeline of the application which the profiler shows memory movements and usage, CUDA calls, number of threads and performance. The figure 2.8 shows, each Kernel has its own percentage of execution time of the overall application.[17]

2.7.1 Profiler Kernel Report

The profiler will execute several times the application for it to collect data from each kernels. This enables to precisely optimize phases of the application[25]. The profiling tools can verify how long the application spends executing each kernel as well the

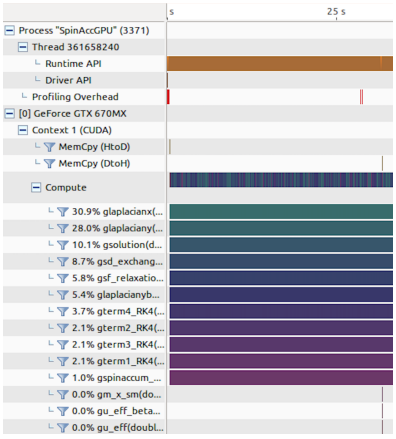

FIGURE 2.8: *Visual Profiler kernel execution*

number of used blocks and threads. Through this is possible to obtain various memory throughput measures, like global load throughput and global store throughput, indicate the global memory throughput requested by the kernel and therefore corresponding to the effective bandwidth mentioned in the last section.

As we know the profiler executes the application several time to collect data about each kernel. The information obtained by each kernel can be sum-up in-to a report that can be exported in a pdf file, which has the following information.

1. **Compute, Bandwidth, or Latency Bound**
   The performance determines if the kernel is bounded by computation, memory bandwidth, or instructions/memory latency. It shows how is limiting the performance respectively.

2. **Instructions and Memory Latency**
   Instruction and memory latency limit the performance of a kernel when the GPU does not have enough work to keep busy. The performance of latency-limited kernels can often be improved by increasing occupancy. Occupancy is a measure of how many warps the kernel has active on the GPU, relative to the maximum number of warps supported by the GPU.

3. **Compute Resources**
   GPU compute resources limit the performance of a kernel when those resources are insufficient or poorly utilized. Compute resources are used most efficiently when instructions do not overuse a function unit.

4. **Floating-Point Operation Counts**
   floating-point operations executed by the kernel, can be either single precision or double precision.

5. **Memory Bandwidth**
   Memory bandwidth limits the performance of a kernel when one or more memories in the GPU cannot provide data at the rate requested by the kernel.

2.7.2 Collect Data On Remote System

As mention before, is possible to collect data from a remote system where a GUI is not available, using the command-line nvprof. Remote profiling is the process of collecting profile data from a remote system that is different than the host system at which that profile data will be viewed and analyzed. Once the data is collected is possible to access the data using the Visual profiler, which enables a GUI and more compressive information about the application. There are two ways to perform remote profiling. To use nvvp remote profiling you must install the same version of the CUDA Toolkit on both the host and remote systems. It is not necessary for the host system to have an NVIDIA GPU. [18]

Finally, this chapter gives a overview of practices and performance studies for GPGPU. Also a better understanding of the hardware and memory management, as well as hardware limitation, which determinate the best usage of the GPUs. As we can see NVIDIA's profiling tools is useful to analyze different stages of our application, moreover to determined which parts of the CUDA code is better to optimize from others to gain more performance.

Chapter 3

Introduction to Domain Wall Dynamics

This chapter is a brief overview of the theory of spintronics and the study of Domain Wall Dynamics under Nonlocal Spin-Transfer Torque. This is a quantitatively test the effects of spin-diffusion, on real Domain Wall (DW) structures, by numerically implementing the Zhang-LI model into a NiFe soft nanostrip. The numerical method used for the solution is a the method known as Finite Differences in the Time Domain (FDTD) on a 3D cell grid with whose integration is done using a 4th order Runge-Kutta integration (RK4).

3.1 Spintronics

Spintronics is a new type of electronics that exploits the spin degree of freedom of an electron in addition to its charge. [32]. The interest is motivated by the quest to understand basic physical principles underlying the electron and nuclear spin interactions in materials and by possible technological applications. The field of spintronics has attracted massive interest since the discovery of giant magnectroresistence (GMR) effect in 1988 by Albert Fert and Peter Grünberg who were awarded the 2007 Nobel Prize in physics. The GMR effect has been widely used in hard disk drives (HDD) which have brought a huge impact on industries and consumer electronics.

Spintronics is a promising technology which will complement the present electronics with addition "spin" quantum freedom to charge freedom that is currently used in devices [10].

Spin polarized transport occurs naturally in any materials which have a spin imbalance between spin-up and spin-down at the fermi Level. It occurs and spin-down electrons is often nearly identical, but the states are shifted in energy with respect to each other. Fermi level is the term used to describe the top of the collection of electron energy levels at absolute zero temperature [28].

Amongst the rapidly growing variety of proposed and developed spin structures, nonlocal spin detection devices, where the measurement and current excitation paths are

Contrarily to charge, spin accumulate in metals, The associated diffusion current flows in all directions, giving rise to nonlocal effects. Beyond transport properties, conduction electrons spin resonance and spin pumping provide further testimonies for non-locality in spin transport.

Spin current which is a flow of spin angular momentum, is generated in addition to the charge current. The spin current normally appears in ferromagnets. However, it can also be generated also in non-magnets. The simplest method of generating a spin-polarized current in a metal is to pass the current throughout a ferromagnetic material. A common application is the GMR as mentioned before [28].

Spin-Transfer torque is an effect in which the orientation of the magnetic layer in a magnetic tunnel junction or spin value can be modified using s spin-polarized current.

The success of spintronics untimely depends on out ability to precisely control the polarization of electrons transported within the actual thin film structure [23].

These works all refer to samples consisting in piecewise uniform layers or blocks, magnetic or not. Of special significance to the present work in the non-collinear geometry where a spin current with polarization transverse to the magnetization exists, whose absorption in the vicinity of the surface of a magnetic layer creates a torque on the magnetization, known as spin transfer torque (SFF). [4]. This phenomenon is usually understood as a consequence of angular momentum conservation. the direction of the current polarization is therefore changed, or rotated by the free layer, which exerts a torque on the spin of the current.[10]. Spin-transfer torque is a torque that exerts on a magnetization by conduction electron spins, in other words the angular momentum transferred from spins to magnetic moment [33].

This has simulated research into domain wall (DW) dynamics, particularly those resulting from interactions with current passing through the DW via the phenomenon of spin momentum transfer (SMT) [28]

3.2 Domain Wall

An abrupt in magnetization at the boundary of two anti-aligned domains is not a favorable condition. Domain walls form between such domains as means of minimizing the energy of the two anti-aligned domains. Domains walls are transitions layers in which the magnetization changes gradually from on magnetization to another. In other words the boundaries between regions of uniform magnetization. The gradual change prevents the large increase in exchange energy that would accompany an abrupt change in the magnetization angle. Common domain wall geometric include Bloch walls, Néel walls and vortex walls. [8]. In this study only two DW are analyzed.

Vortex Wall (VW)

In the case of Vortex wall the magnetization rotates in the place perpendicular to the domain wall, but the local magnetization is wrapped around a single vortex point. See figure 3.1.

Asymmetric Transverse Wall (ATW)

The transverse wall has a reflection symmetry about a line perpendicular to the strip axis, and a lack of symmetry about the center line of the strip. However, asymmetric transverse wall, is the absence of such symmetry, figure 3.1.

FIGURE 3.1: *Vortex Wall (VW) and Asymmetric Transverse Wall (ATW)*

Domain walls are the basis for various spintronics devices that uses magnetic momentums, in other words spin of electronics. the used of the spin degree of freedom. With this it is expected that electronics technology and devices will be faster, compacter and more energy-saving. A interesting application using this idea is new design for a different type memory disk drive called racetrack memory by Parkin in 2008[20]. The racetrack memory stores bits along a single ferromagnetic wire. To write and read information, a current is applied along the wire that moves the bits to writing or reading unit. Advances in spintronics recognized by 2007 Nobel Prize in Physics have enable over the last decade advances in computer memory, in hard drives, this is a metal based structures which utilize magnetoresistive effects to save and read data from a magnetic disk. [28]

STT by zhang and li

It deals with the spin-transfer torque in the case of a continuously varying magnetization. In this case the spin-transfer torque acts on inhomogeneous magnetization patterns, such as domain walls or magnetic vortices. Thus, also the magnetic processes in a racetrack memory12 and gyrating magnetic vortices driven by spin-transfer torque15,16 can be described.

3.3 Zhang and Li Model

The inclusion of STT into micromagnetics has up to now been performed with locla termis that express the STT as a function of the local magnetization only. The magnetization dynamics is decrecibed by the classical Landau-Lifshitz-Gilbert (LLG) equation, argumented with a STT

$$\frac{\partial \vec{m}}{\partial t} = \gamma_0 \vec{H}_{eff} \times \vec{m} + \alpha \vec{m} \times \frac{\partial \vec{m}}{\partial t} - \vec{T} \tag{3.1}$$

with $\vec{m} = \vec{M}/M_s$

Within a nano-strip, on the other hand, a moving (DW), because it concentrates all of the magnetization non-uniformity, acts as a built-in detector of spin torques. application racetrack, , All in all, however, micromagnetics and spin-polarized transport need to be suitably admixed for a meaningful comparison between theoretical expectations and experiments.

Tss the SST as a function of the local magnetization only.

We Quantitatively test the effects of spin diffusion, on real Domain walls structures, this is done by numerically solve the Zhang-Li model [33] into micro-magnetics.

$$D_0 \bigtriangledown^2 \delta\vec{m} \frac{1}{\tau_{sd}} \delta\vec{m} \times \vec{M} + \frac{1}{\tau_{sf}} \delta\vec{m} = -\frac{\mu_B P}{e} (j_e \cdot \bigtriangledown)\vec{M} \tag{3.2}$$

The equation is physically realistic however computationally expensive.

3.4 Numerical solution

he numerical method used for the solution is a the method known as Finite Differences in the Time Domain (FDTD) whose integration is done using a 4th order Runge-Kutta integration.

$$\frac{\partial \delta\vec{m}}{\partial t} = D_0 \bigtriangledown^2 \delta\vec{m} - \frac{1}{\tau_{sd}}\delta\vec{m} \times \vec{M} - \frac{1}{\tau_{sf}}\delta\vec{m} + (\vec{\mu} \cdot \vec{\bigtriangledown})\vec{M} \tag{3.3}$$

Asymmetric Transverse Wall (ATW), maps of magnetization components of non equilibrium spin accumulation under a uniform current density with $D = 0, 1$ and $10nm^2/ps$. Figure 3.2.

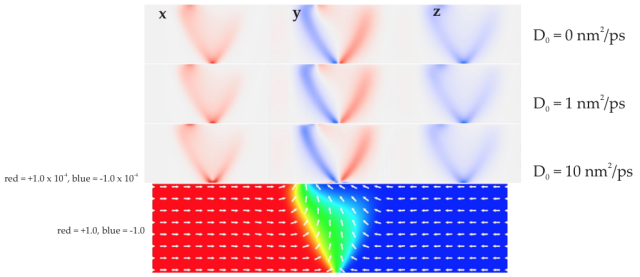

FIGURE 3.2: *Domain Wall - Vortex*

Vortex Wall (VW) same as for ATW, we point out the noticeable effect of the diffusion constant around the vortex core, which is the smallest feature of the wall. Figure 3.3.

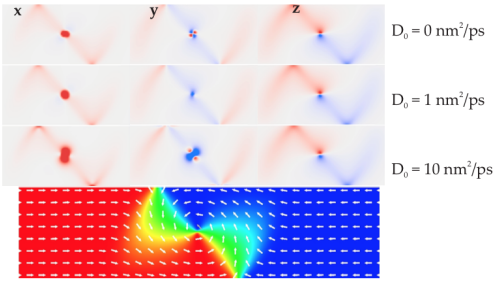

FIGURE 3.3: *Domain Wall - Vortex*

The sample that is considerate is a 300 nm wide and 5 nm tick NiFe soft nanostrip. This dimensions are widely used for experimental use.

Therefore, a simultaneous solution of the diffusive Zhang and Li model together with the magnetization dynamics equation has uncovered a qualitatively new feature of the spin-transfer torque effect in the presence of spin diffusion.

[13]

3.4.1 Finite differences in the time domain

The finite difference in the time domain (FDTD) method can solve complicated problems, but it is generally computationally expensive. Solutions may require a large

amount of memory and computation time. FDTD is a numerical analysis technique use for approximating solutions to the associates system of differential equations. The method belongs in the general class of grid-based differential numerical modeling methods [6].

The finite difference in the time domain method essentially uses a weighted summation of functions values at neighboring points to approximate the derivate at a particular point, in this case a point in a 3d grid. The result for each cell is based on the results from the cell and its neighbors at the previous time-frame, figure 3.4.

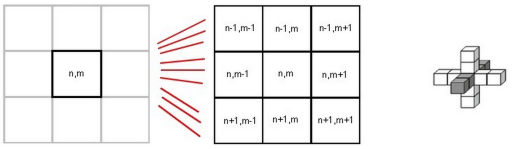

FIGURE 3.4: *The result for each cell is based on evaluating the derivate cell neighbors.*

The Second order Taylor expansion readily yields expressions for the first and seconds central derivates. First and second-order derivates of the magnetization components in order to define the divergence of the magnetization ($\nabla \cdot m$), and the components of the exchange field ($\nabla^2 m$), respectively. The magnetization components along boundaries also need to be evaluated in order to define surface charges ($m \cdot n$). Boundary conditions need to be incorporated in the evaluated of the effective field without loss of accuracy.

Consider a regular, differentiable one-dimension scalar function $f(x)$ sampled at regular intervals, a, see figure 3.5. Second order Taylor expansion readily tiles expressions for the first and seconds central derivates that are widely used in numerics, namely $\frac{df}{dx} = \frac{f_{i+1} - f_{i-1}}{2a}$ and $\frac{d^2 f}{dx^2} = \frac{f_{i+1} - 2f_i + f_{i-1}}{a^2}$.

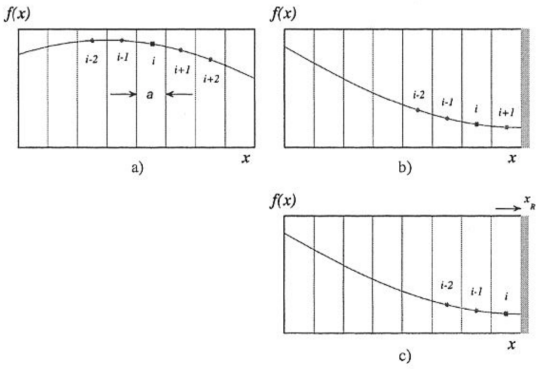

FIGURE 3.5: *Sampled at regular intervals a, (a) Function of inside the grid. (b) Mesh points second to closest to boundary. (c) Mesh points closet to boundary*

However, the numerical derivation of the structure of a simple Bloch wall using such expressions soon reveals that second order Taylor expansion ledes to restricted accuracy. Fourth order expansion as actually been found to prove much superior. [6]

Taylor expansion of the function $f(x)$ around $x = x_i$ yields where $f^{(k)}(x_i) = f(x)$ if $k = 0$

$$f(x) = \sum_{k=0}^{\infty} \frac{(x - x_i)^k}{k!} f^{(k)}(x_i) = \sum_{k=0}^{\infty} \frac{(x - x_i)^k}{k!} f^{(k)}$$

Applying the previous equation to nearest and next nearest neighbor to grid pint i and truncation the the 4th order yields a set of four equations

The set of linear equations provide numerical estimates for the first, second, third and fourth derivatives of f at any given point i. The general form of the first and second derivate based on second nearest neighbors expansion reads:

$$f_i^{(1)} = \frac{f_{i-2} - 8f_{i-1} + 8f_{i+1} - f_{i+2}}{12a} \tag{3.4}$$

$$f_i^{(2)} = \frac{f_{i-2} + 16f_{i-1} - 30f_i + 16f_{i+1} - f_{i+1}}{12a^2} \tag{3.5}$$

The equation 3.4 for the second derivate based on second nearest neighbors expansion solves for the laplacian operator in the Zhang -Li Model equation 3.3. However, points close to the edges need to be evaluated for great precession.

3.4.1.1 Boundary conditions implementation

Expressions above 3.4 crease to be valid when the grid point becomes closet or next-to-closet to the boundary of the magnetic box. Specific accuracy preserving, expansion need to be worked out. The general principal in the rpese approach is to replace equations that are missing because of the lack of grid points outside the magnetic volume by equations including explicit reference to boundary conditions. [6]

Consider first a point second to closet to bound, 3.5-b. Grid point $i + 1$ is missing for this particular geometry. However, defining x_R as the right boundary coordinate along the x axis. The $f^{(1)}(x_R)$ to be know along the boundary to be replace by the derivate of Taylor's expansion

$$f^{(1)}(x) = \sum_{k=0}^{\infty} \frac{(x - x_i)^{k-1}}{(k-1)!} f^{(k)}(x_i) \tag{3.6}$$

Using 3.5-b. $x_R - x_i = 3a/2$ becomes.

$$\begin{bmatrix} -2a & \frac{(-2a)^2}{2!} & \frac{-(2a)^3}{3!} & \frac{(-2a)^4}{4!} \\ -a & \frac{(-a)^2}{2!} & \frac{(-a)^3}{3!} & \frac{(-a)^4}{4!} \\ a & \frac{(a)^2}{2!} & \frac{(a)^3}{3!} & \frac{(a)^4}{4!} \\ 2a & \frac{(2a)^2}{2!} & \frac{(2a)^3}{3!} & \frac{(2a)^4}{4!} \end{bmatrix} \begin{bmatrix} f_i^{(1)} \\ f_i^{(2)} \\ f_i^{(3)} \\ f_i^{(4)} \end{bmatrix} = \begin{bmatrix} f_{i-2} - f_i \\ f_{i-1} - f_i \\ f_{i+1} - f_i \\ f^{(1)}(x_R) \end{bmatrix} \tag{3.7}$$

Similarly, for a point closet to boundary, reference 3.5-c, grid points i + 1 and i + 2 are missing. The two first equation of ... need now to be replaced by a single equation, whilst the two remaining equations need to be truncated to the third order. For the geometry illustrated in 3.5-c, the minimal set of equations now reads.

$$\begin{bmatrix} -2a & \frac{(-2a)^2}{2!} & \frac{-(2a)^3}{3!} \\ -a & \frac{(-a)^2}{2!} & \frac{(-a)^3}{3!} \\ 1 & \frac{(+a)}{2} & \frac{(+a/2)^3}{2!} \end{bmatrix} \begin{bmatrix} f_i^{(1)} \\ f_i^{(2)} \\ f_i^{(3)} \end{bmatrix} = \begin{bmatrix} f_{i-2} - f_i \\ f_{i-1} - f_i \\ f^{(1)}(x_R) \end{bmatrix} \tag{3.8}$$

In both cases, and second derivatives and fully determined provided $f^{(1)}(x_R)$ be known along the boundary. For further reference [6]. The implementation to solve the laplacian with boundaries conditions check chapter 4.

3.4.2 Fourth order Runge and Kutta method

Modern numerical algorithms for the solution of ordinary differential equations are based on the method of the Taylor series. Algorithm such as the Runge-Kutta method are constructed so they give an expression depending of the parameter (h), in other works the step as an approximate solution of the first terms of the Taylor series. [26] The method can accurately tackle a wide range of problems as well as can solve complicated problem, but it is generally computationally expensive. Solutions require large amount of memory and computational time.

There exist several computational numeric methods to solver such equations, methods like Euler, Midpoint Method and Runge-Kutta integrator method can solve this type of equations. The RK4 this method is used for the simulation because its numerically more accurate when compared to the others.

The RG4 method differs widely from the Euler method and the Midpoint method. The Euler method is the simplest, the derivative at the starting point of each interval is extrapolated to find the next function value, see figure 3.6. Euler method only has first order accuracy while the RK4 its fourth order integrator [22].

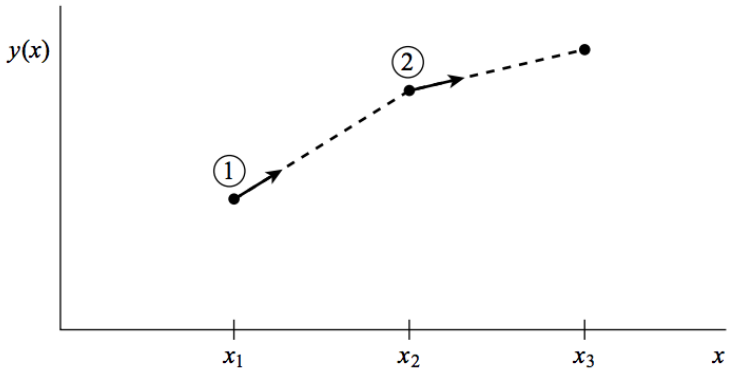

FIGURE 3.6: *Euler Method, Is the simplest approximate to solver differential equation or numerically solve equations.*

RK4 goes as follows:

$$y_{n+1} = y_n + 1/6K_1 + 1/3K_2 + 1/3K_3 + 1/6K_4 \tag{3.9}$$

where

$$\begin{aligned} K_1 &= h\dot{f}(x_n, y_n) \\ K_2 &= h\dot{f}(x_n + h/2, y_n + k_1/2) \\ K_3 &= h\dot{f}(x_n + h/2, y_n + k_2/2) \\ K_4 &= h\dot{f}(x_n + h, y_n + k_3) \end{aligned} \tag{3.10}$$

As the equations shows, each step, the derivative is evaluated four times, once at the initial point, twice at trial midpoints, and once at a trial endpoint. From these four values, the final value is calculated, just like the equation **??**.

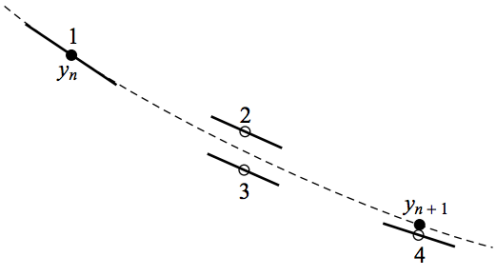

FIGURE 3.7: *Fourth-order Runge and Kutta method, Each step the derivative is evaluated four times.*

3.4.3 Effective Beta

We show that and effective non-adiabatic parameter β_{diff} dependent on the DW structure, provides

$$(\beta\upsilon)^* = \frac{\delta\vec{m}\cdot\partial_x\vec{m}}{\tau_{sd}\|\partial_x\vec{M}\|^2} \tag{3.11}$$

Therefore, a simultaneous solution of the diffusive Zhang and Li model together with the magnetization dynamics equation has uncovered a qualitatively new feature of the spin-transfer torque effect in the presence of spin diffusion, namely the dependence of the steady-state DW velocity on DW structure

3.4.4 Procedure

The procedure is (i) compute the non-equilibrium spin density $\delta\vec{m}$ with the DW at rest, solve equation 3.3 to convergence or directly its time-independent version. (ii) compute the β_{diff} distribution from equation 3.11 and finally compute β_{diff} by averaging with the $|\partial_x\vec{m}|^2$ weight function.

In summarize, We Quantitatively test the effects of spin diffusion, on real Domain walls structures, this is done by numerically solve the Zhang-Li model into micro-magnetics. The numerical methods used to solve such model as metioned is the

Ind addition, these results offers a starting point to study multilayer structures like spin-value nano strips, where the understanding of the observed increased efficecnctiy of SST to drive DW's still remains elusive.

Chapter 4

Implementation of DW Dynamics under Nonlocal Spin-Transfer Torque

This chapter is the study of the heterogenous implementation of Domain Wall Dynamics under Nonlocal Spin-Transfer Torque. We use the massively parallel capabilities of a single GPU to numerically solve a mathematical equation, known as the Zhang-Li model. The numerical method used for the solution is a the method known as Finite Differences in the Time Domain (FDTD) whose integration is done using the 4th order Runge - Kutta. The integration is done on a 3D grid space which outputs a single value, the effective beta.

4.1 Simulation

The simulation consist of the integration of the equation 3.3, know as the Zhang and Li model for $1ns$ in a grid of 57,600 cells. The sample considered is a 300nm wide in y direction and 5nm thick in z direction NiFe (nickeliron alloy) soft nanostrip, a material and size widely uses in experiments with this characteristics. Using this size the asymmetric transverse wall 3.2, and the vortex wall. have nearly equal energies. The numerical mesh size is 3 x 3 x 5 nm^3, and the calculation box has a length (x direction) of 1,200 or 3,172 nm. The table 4.1 illustrates mesh information and calculation box for the simulation [4].

The table 4.2 shows the constant values for the equation 3.3 such as μ, D_0, τ_{sd} and τ_{sf}.

Mesh size	value	calculation box	value
Cell NX	480	Box TX	1200.0
Cell NY	120	Box TY	300.0
Cell NZ	1	Box TZ	5.0

TABLE 4.1: *Mesh size and calculation box*

The simulation is divided into two calculations parts, the host code and the device code. As the figure 4.1 illustrates the data flow of the simulation. Each step of the simulation is going to explain in the following section with more detail. First the initial values are read from a data file. Then those values are used to calculate the initial matrices for the simulation. This values are only calculated once. Afterwards the simulation begins with a time step of 1.0 iterations. In addition each time step the fourth order Runge and Kutta(RK4) integration is calculated to solve 3.3. Each 50,000 iterations the Beta difference is evaluated, if the beta difference convergence to 1.0e-9 the simulation stops. As the figure 4.1 shows all the intense computation is done on the GPU side. While on the CPU only minor intense computation are done such as I/O data, memory allocation and final beta variation.

Diffusion parameters	Value	Runge - Kutta 4th	Value
μ	1	time step (dt)	$25.0e^{-6}$
D_0	$1.0e^{3}$ nm mm^2/ns	tmax	1.0
τ_{sd}	$1.0e^{-3}$ ns	beta difference	$1.0e^{-9}$
τ_{sf}	$25.0e^{-3}$ ns	Iterations	50,000

TABLE 4.2: *Diffusion parameters and Runge - Kutta 4th*

4.1.1 Data allocation and threads

The first section of the implementation starts by allocation data into several matrices for both host memory and device memory. The initial magnetization data can be either self generated by the application or by reading a file which contains information related to the magnetization. In both cases the data is divide into two blocks of data. Both blocks have 57600 (480 x 120) rows of information The first 57600 rows contains initial magnetization x, y coordinates. The next block of 57600 rows is the initial magnetization in x, y, and z. The data being read is stored on a three temporary 2D matrix, that corresponds to the x, y, and z coordinate. In addition the three matrices are flatten into three continuous memory blocks, as showed in figure 4.2. The device code 4.1 flattens the 2d index into a single linear 1D index.

```
int i = blockIdx.x * blockDim.x + threadIdx.x + 2;
int j = blockIdx.y * blockDim.y + threadIdx.y;
// map the two 2D indices to a single linear, 1D index
int index = j * grid_width + i;
```

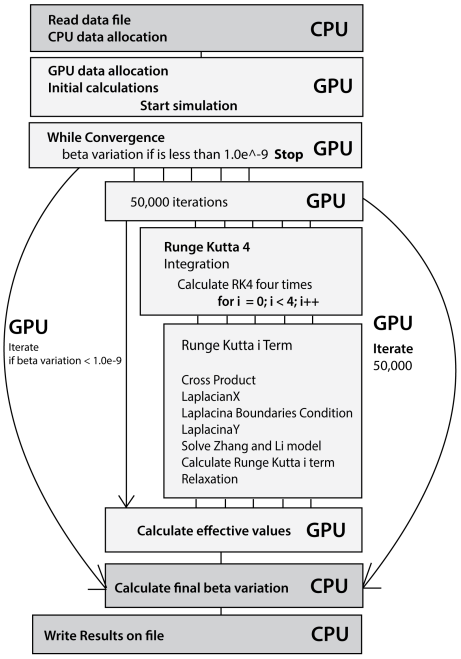

FIGURE 4.1: *Control flow of the simulation*

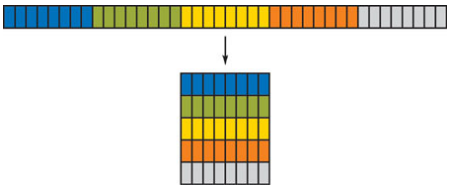

FIGURE 4.2: *Converting 2D array to a single continuous block of memmory*

LISTING 4.1: *Kernel Flatten*

To ensure optimal memory allocation on the GPU side is best to assign square matrices to the device. The calculation for this operation is done using the first two operations in 4.2.

Matrix size X	480	Device allocation X	512
Matrix size Y	120	Device allocation Y	128

TABLE 4.3: *Matrix allocation size*

The magnetization data is stored on matrices of x, y, and z, which has 56700 values, in other words 480 times 120. Base on this information we want to calculate the optimal number of grids that will ensure complete use of the hardware resources. The number of blocks per grid corresponds dividing the dimensions of the array by the number of threads. The last two operations in 4.2.

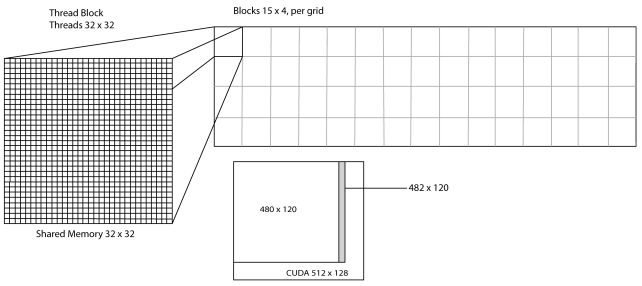

FIGURE 4.3: *Memory allocation in terms of the blocks per threads and grids*

```
NXCUDA = (int)powf(2,ceilf(logf(NX)/logf(2)));
NYCUDA = (int)powf(2,ceilf(logf(NY)/logf(2)));

//Setup optimum number of blocks
XBLOCKS_PERGRID = (int)ceil((float)NX/(float)XTHREADS_PERBLOCK);
YBLOCKS_PERGRID = (int)ceil((float)NY/(float)YTHREADS_PERBLOCK);
```

LISTING 4.2: *Device capacity calculation and number of block per grid*

Depending on the hardware properties, each GPU can allocate different number of threads per block and as well as different shared memory size. The Shared memory in this implementation relays on the number of threads per block. In addition the number of blocks depends on the input matrix and the number of threads. See figure 4.3.

	Fermin	Kepler
Threads per block X	16	32
Threads per block Y	16	32
Number of blocks X	30	15
Number of blocks Y	8	4
Shared memory	16 * 16	32 * 32

TABLE 4.4: *Threads, blocks size*

4.1.2 Initial Calculations

The initial calculation is only a minor part of the whole simulation. However only once at the begining of the simulation the calculations are performed, 4.3.

```
    gsource << <blocks, threads >> >(...); //Compute x, y and z component of source term
    gsource << <blocks, threads >> >(...);
    gsource << <blocks, threads >> >(...);

    //Project source term on magnetization components by computing
    //a cross product twicse
```

```
gm_x_source << <blocks, threads >> >(...);
gm_x_source << <blocks, threads >> >(...);
```

LISTING 4.3: *Initial calculations*

In **??** the kernel *gsource* evaluates once the matrix *sm*, which is used to compute the Zhang-Li model in the RK4 integration.

///shift error // in implementation

As mention before the matrices for CUDA are square matrices 512 x 128, however the data set is 480 x 120. Because of the matrices size difference we need to limit the number of threads execution of the CUDA kernels. To limit such threads branching with a simple if within the kernels solves this issue **??**. Due to the boundaries condition in the implementing of the FDTD a small shift in the x direction is necessary.

```
if (i > 1 && i < NX + 2 && j >= 0 && j < NY)
{
//calculations
}
```

LISTING 4.4: *Laplacian X using global memory*

4.1.3 Numerical Methods

micromagnetic simulation and demonstrate how to advance the configuration of the system through time. we do not know for how long we need to integrate the system until it stops in a local energy minimum configuration.

This step is where all the computational intense operations are performed. The figure **??** demonstrates the operations

Data: deltam
Result: how to write algorithm with LaTeX2e
initialization;
while $b_{eff} < 1.0e^{-9}$ **do**
    Runge and Kutta 4th;
    for $i = 1; i <= 4; i+ = 1$ **do**
        sdex ← crossProduct(deltam, mag); calculate cross product
        FDTD with boundary condition
        laplacian ← laplacianXYBoundary(deltam);
        evaluate Zhang-Li model
        solveZhangLi ← solveZhang(sfrelax, sdex, laplacian, sm);
        RK4 evaluation
        rkterm(i) ← rktime(i, solveZhangLi, dt);
        if $i == 4$ **then**
            deltam ← rk4(solveZhangLi, temp, dt, rkterm(1), rkterm(2), rkterm(3), rkterm(4))
        else
            deltam ← rk4(solveZhanLi, temp, dt)
        end
        evaluate RK4 term
        deltam ← rk4(solveZhanLi, temp, dt)
        sfrelax ← relaxation(deltam, tau)
        if $i == 4$ **then**
            temp ← copy(rkterm(4));
        end
    end
end

Algorithm 1: Runge and Kutta 4th integration implementation

4.1.3.1 Finite differences in the time domain

The finite differences method requires the domain of interest to be broken down into small regions. Such a subdivision of space is known as a mesh or grid, cell division is explained in the table 4.1, whose implementation in CUDA threads and blocks are done with 4.3 and 4.4. Based on the equations from chapter three 3.4. The first and second derivate are based on seconds nearest neighbors expands are calculated. The base idea is showed on the figure . The equation 3.4 is evaluated for three coordinates x, y and z.

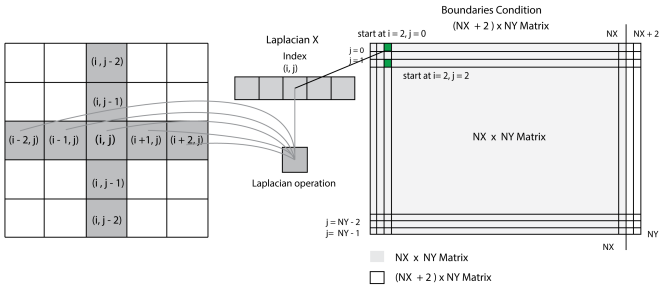

FIGURE 4.4: *Laplacian XY block calculation and boundaries condition*

As the Figure 4.4 demonstrate the calculation the nearest neighbors expansion by evaluation a neighborhood of $[-2, 2]$ values in the x direction. In addition the index begins at $i = 2$ and finishes at $NX + 2$. The same occurs for the laplacian in the Y direction, however it begins at $j = 2$ and finish at $NY - 2$. The implementation 4.5 uses the equation from chapter 3 3.4 as previous mention. The calculation 4.5 is done for each three x, y and z coordinates.

```
int i = blockIdx.x * blockDim.x + threadIdx.x + 2;
int j = blockIdx.y * blockDim.y + threadIdx.y;
// map the two 2D indices to a single linear, 1D index
int idx = j * grid_width + i;

lapy[idx] = - deltam[idx + 2] / 12.0 + 4.0 * deltam[idx + 1] / 3.0
            - 5.0 * deltam[idx] / 2.0
            - deltam[idx - 2] / 12.0 + 4.0 * deltam[idx - 1] / 3.0;
```

LISTING 4.5: *Laplacian X using global memory*

However the calculation of the nearest neighbors only work for values points inside inside a grid of [-2, 2] in x, y, and z. In addition we need to calculate the boundaries values for those values that are in the edge of the grid, such as the beginning points and the end points. To solve the boundaries issue we use two square matrices matrices from chapter three, The equation 3.8 for boundaries at $j = 0$ and $j = NY - 1$ for all values in the i cell, and the equation 3.7 for the condition $j = 1$ and $j = NY - 2$ for all i values. The code 4.6 demonstrate how the implementation was done, to achieve the correct values first the laplacian in the y direction is calculated, then the boundary condition, and finally the in the x direction.

```
__global__ void glaplaciany(...){} //Compute laplacian in Y direction

__global__ void glaplacianBoundaries(...){
    if (i > 1 && i < NX + 2 && j == 0){
        // Update Laplacian Boundaries Equation 3.10
    }
    else if (i > 1 && i < NX + 2 && j == 1){
        // Update Laplacian Boundaries Equation 3.9
    }
```

```
    else if (i > 1 && i < NX + 2 && j == NY - 2){
        // Update Laplacian Boundaries Equation 3.9
    }
    else if (i > 1 && i < NX + 2 && j == NY - 1){
        // Update Laplacian Boundaries Equation 3.10
    }
}
__global__ void glaplacianx(...){} //Compute laplacian in X direction
```

LISTING 4.6: *Evaluation of Laplacian X, Y with boundary condition*

The three CUDA kernels *glaplaciany*, *glaplacianx* and *glaplaciany* are evaluated for each x, y and z coordinate. In addition the three coordinate sum up to 172,800 cell points to be calculated.

4.1.3.2 Zhang and Li Model

The equation of Zhang - Li Model 3.3 is solved using the following following code 4.8. This function is used for the 3.9 integration equation. The first term of the equation *sfrelax* is calculated in the in the relaxation process at the end of the RK4 integration process **??**. The term *sdex* is evaluated once at the beginning the RK term integration, in the Cross Product. The matrix *sm* is only calculated once at the initial calculations process, in the kernel *gsource*. Finally the lapl matrix is evaluated in the Laplacian X, Y and boundary condition. In addition this process is the most computational expensive operation.

```
        sfrelax[idx] = -deltam[idx] / tau_sf;
        sdex[idx] = -(deltam[idx] * m[index] - deltam[idx] * m[idx]) / tau_sd;

        //Evaluate Zhang - Li Method
        solveZhangLi[idx] = sfrelax[idx] + sdex[idx] + lapl[idx] - sm[idx];
```

LISTING 4.7: *Runge and Kutta 4th Terms*

The output *solveZhangLi* of the Zhang - Li Model evaluation 4.7 (last term), past to the calculation of the i term of the Runge Kutta Integration.

4.1.3.3 Runge and Kutta

Intuitively the equation 3.9 implementation code is done by using 4 CUDA kernels, each kernel calculates the step of the integration. The first part of 4.8 computes the Runge and Kutta's 1st, 2nd, and 3rd term 3.10. The final fourth term, is the sum of the previous 3 terms, the last two lines of code in 4.8 show the calculation.

```
    rk1[idx] = dt * deltam[idx];  // Terms k1, k2, k3
    deltam[idx] = temp[idx] + 0.5 * rk1[idx];

    rk4[idx] = dt * deltam[idx]; //final k4
    deltam[idx] = temp[idx] + (rk1[idx] + 2.0 * (rk2[idx] + rk3[idx])
                                + rk4[idx]) / 6.0;
```

LISTING 4.8: *Runge and Kutta 4th Terms*

4.1.3.4 Final evaluation

The integration can be sum up as two for cycles. The first *for* calculating the RK4 and the second one each x, y, and z coordinate 4.9.

```
for(int term = 0; term < 4; term++)
    for(int coord = 0; coord < 3; coord++)
        gsd_exchange<<<blocks, threads>>>(term, coord);
        glaplacianx<<<blocks, threads>>>(term, coord);
        glaplacianyboundaries<<<blocks, threads>>>(term, coord);
        glaplaciany<<<blocks, threads>>>(term, coord);
        gsolution<<<blocks, threads >>>(term, coord);
        gterm_RK4<<<blocks, threads >>>(term, coord);
}
```

LISTING 4.9: *Summarize of Runge and Kutta Integration*

4.1.4 Calculate effective beta

The final calculation of the simulation, which calculates the effective beta. The following kernels are launched only when the RK4 integration is done, for this implementations is 50,000 iterations of RK4. 4.1

```
    gm_x_sm << <blocks, threads >> >(...); //Calculate
    gu_eff << <blocks, threads >> >(...);  //Calculate
    gu_eff_beta_eff << <blocks, threads >> >(...);  //Calculate
    gbeta_eff << <blocks, threads >> >(..);     //Calculate
    gbeta_diff << <blocks, threads >> >(...);  //Calculate
```

LISTING 4.10: *Calculate effective beta*

The final step of the simulation is calculating on the host the single value beta variation.

Note that the execution time can generally be reduced significantly by decreasing the amount of converges of the effective bete. However, this can result in wrong data.

4.2 Validation

Once obtain the results from the simulation, the results are written into two separated data files; .eff and .spin. depending of the configuration of the application is possible to obtain the uVW or the ATWpm. Because CUDA framework is highly parallel system is fairly easy to obtain erroneous data from the calculations, even setting up the threads per block incorrectly is possible to get data set that is wrong, or results that don't diverge. When making changes to the code, its is necessary to validate the results, to continue to make changes.

The validation is done by checking the output of the simulation with a valid data set, the output of the validation application tells us the error factor of the current data with the valid set. So for each data set there is a threshold value, that can tell if the that is close enough to the results. A example of the validation performed. According to our results, new code shouldn't produce errors in the $*$-spin.dat data greater than 7.0e-17, in other words valid code don't lead to differences greater than the precision expected from computations with double precision 1.0e-16 in the case of eff data the errors are in the order of 1.0e-11 and no greater than 6e-11. For the diffuse beta variation the precision expected to be within the double precision range of 1e-16.

For example the validation test are done with the following output values.

Data set	Simulation time	Diffuse beta
upVW magnetization	377590.3ms	4.848728452719814e-02
ATWpm magnetization	377409.2ms	4.054674178687585e-02

TABLE 4.5: *Calculation results*

To conclude, the simulating at its core uses the RK4 for integration which uses as function the equation of Zhang-li 3.3. In addition to solve such differential equations the FDTD method is used. As we can expected the simulation is computational expensive, because the RK4 evaluates fourth times the Zhang-Li equation. Moreoever,

Chapter 5

Optimization Results

This chapter is the results of the CUDA code implementation launched on several different GPUs nodes. The test are performed on various GPUs architectures, which, has different hardware characteristics. Each GPU node is analyzed using the NVIDIA's Visual Profiler, in addition the CUDA kernels are evaluated in performance; throughput, bandwidth, executing and parallel time. Furthermore the results, are analyzed and optimized using the schemes from chapter 3. Lastly the code is executed remotely on the supercomputer "Piritakua" at the Department of Multidisciplinary Studies Yuriria, University of Guanajuato

5.1 Supercomputer "Piritakua"

The experiments are carried out using the supercomputer Piritakua. The massive GPU cluster was design and built by Dr. Claudio from the University of Guanajuato Multidisciplinary Studies Yuriria. The GPU cluster is located at a small town of Mexico, Yuriria. The supercomputer at the Front-end has a eight core Intel Xeon at 2.4 Ghz, at the back-end several GPU are connected, one NVIDIA Tesla K20, two Tesla M2070 and a GTX 580.

A GNU LINUX distribution installed on the system, the CentOS 64 bits version 6.4. CentOS stands for Community Enterprise Operating System which is free operating system and one of the most popular GNU Linux distribution for web servers and as well is supported by RHEL (Red Hat Enterprise Linux). [2]

The specifications of the front-end cluster.

The CUDA Code was launched on only two CPUs, a laptop with a eight core intel i7-3630QM and a high-end CPU Xeon Phi 7120p from the cluster. In addition the Xeon

Processor	Number	Cores	RAM
Server Dell Intel Xeon E5620 2.4 GHz	1	8	12 GB
Server HP Proliant SL 350s Gen3 Intel Xeon X5650 2.67 GHz	2	24	32 GB
Server HP Proliant SL 250s Gen8 Intel Xeon E5-2670 2.60 GHz	3	48	104 GB
CPU Xeon Phi 5110p	1	8	8 GB
CPU Xeon Phi 7120p	1	8	16 GB

TABLE 5.1: *CPU specifications*

Phi was used for all the experiments for the Cluster's GPUs. The Xeon Phi 720p is capable of achieving f 1.2 teraflops of double precision floating point instructions with 352 GB/sec memory bandwidth at 300 W.

When accessing "Piritakua" remotely is possible to use all the GPUs available on the cluster. The specifications of the GPU connected to the back-end are as follow, CC stands for compute capability.

Model	Core	RAM	DP GF	SP GF	Bandwidth	GHz	CC	Power
Tesla K20m	2496	5GB	1,170	3,520	208GB/s	0.73	3.5	225W
Tesla M2070	448	6GB	515	1,030	150GB/s	1.15	2.0	225W
Tesla C2050	448	2.5GB	512	1,030	144GB/s	1.15	2.0	238W
GeForce 580	512	1.5GB	520	1,154	192.2GB/s	1.5	2.0	244W
GeForce 670MX	960	3GB	520	1,154	67.2GB/s	0.6	3.0	-

TABLE 5.2: *GPU technical specifications*

The code was launched on all Piritakua's GPUs and on external GeForce GTX 670m, located on a laptop. The "m" stands for the mobil graphic card version. In addition the 670m card is design for less power usage, but with high graphics power, it even has more cores than some Tesla models, however this types of cards has way more less Bandwidth than standard versions.

5.1.1 Architecture Differences

Architecture dependent technical differences of NVIDIA GPUs. During CUDA development a lot of internal features have been improved, but most paradigms for the programmer stayed the same. For example a streaming processor can now handle 2048 threads at a time, but the maximum block size stayed at 1024. This results in a 100% theoretical occupancy for block sizes of 1024 compared to 66% of Fermi. Another example is the use of Shared Memory. Maxwell has 64KB dedicated Shared Memory. The maximum amount of Shared Memory per Block is 48KB for all three architectures. [9]

There are two GPU architectures that code was launched, the Fermi and the Kepler. The Tesla K20m is base on "Kepler" GPU architecture and the Tesla M2070, M2050 and GeForce GTX 580 on the Fermi architecture. The Kepler is a newer architecture than the Fermi. The big difference between the is the number of CUDA cores per SM. Roughly summarized as:

Name	Fermi		Kepler		Maxwell
Compute Capability	2.0	2.1	3.0	3.5	5.0
Single Precision Operation per Clock/SM	32	48	192		128
Double Precision Operation per Clock/SM	4/16[1]	4	8	8/64[2]	1[3]
Max Number of Threads per SM / SM	16		32		
Max Number of Registers per Thread/SM	1536		2048		
Max Number of Threads per Block	1024				
Active Thread Blocks per SM / SM	8		16		32
Max Warps per Multiprocessor/ SM	48		64		
Registers / SM	32K		64K		
Level 1 Cache	16/48 KB		16/32/48 KB		64 KB
Shared Memory / SM	16/48 KB		16/32/48 KB		64 KB
Warp Size	32				

TABLE 5.3: *GPU Architecture Specifications*

5.1.2 Experiment metrics

The initial implementation was launched on several GPU nodes as well as several times on the same node. The implementation was launched 10 times on each node, For example the following table are the results of the initial implementation launched on the NVIDIA Tesla K20m.

number	time
1	64846.0
2	59010.4
3	67332.4
4	68171.8
5	61818.0
6	65111.3
7	67346.4
8	65666.6
9	67343.3
10	65681.8

As we can see each time the code is executed, different time results. The order in which operations are evaluated can significantly affect the final value of a floating point

computation; t It's possible that the first issued block might be issued to different multiprocessor each time, and if there are an uneven number of blocks across multiprocessors, then the execution order could vary slightly between runs [5].

As we know there is no guaranty that threads will execute at the same order. To accomplish such task thread synchronization is needed.

5.2 Results

The CUDA code was launched on each GPU of the "Piritakua" supercomputer. As we know the supercomputer has different GPU, as well as several architectures and different number of CUDA cores.

mention CUDA versions. as well as the compiler used for the test.

Node	initial Avg time	1st optimization	2nd optimization
Tesla K20m	64846.0	55	33
Tesla M2070	64846.0	55	33
GeForce GTX 580	64846.0	55	33
GeForce 670m	64846.0	55	33

5.2.1 Initial Test

The initial implementation was launched on several GPU nodes, as previous mentioned. As we know. Se figure.5.1.

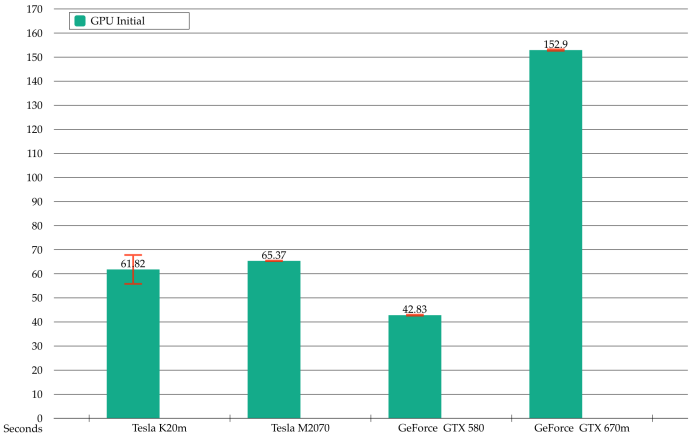

FIGURE 5.1: *Initial results of the implementation running on several different GPU nodes*

5.2.1.1 Visual profiler

The visual profiler.

The visual profiler was used on Laptop with GeForce GTX 670m with the intel eight core i7-3630QM.

the

command

nvprof o nvprof.log ./command

5.2.2 Branching

CUDA follows the Single Instruction Multiple Thread architecture. This means that there are running several threads executing the same code. Each thread can operate on its own data and has its own address counter. They are free to use each data dependent path. But also each thread is executing the same operation at the same time. When a thread within a warp branches differently the other threads get deactivated. This can be described by the following listing and illustrated by [9].

5.2

```
__global__ void kernel(int* out){

idx = threadIdx.x;
int result;

if(idx == 0){
    result = foo();
} else {
    result = bar();
    out[idx] = result;
}
```

Listing 5.1: *CPU Vector Addition*

This problem ocurr when analysing the boundary condition for the matrices, only a single kernel was checking boundaring. Which a bottleneck ocurr. Bec

This implementation gets the job done, however a minor part of the threads are working, which is a waste of computation.

```
//Compute laplacian in Y direction
__global__ void glaplaciany(...);
```

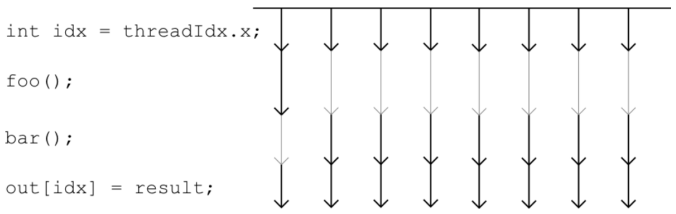

FIGURE 5.2: *The execution flow of a branching code, with warp size 8. Black arrows are active threads, and the grey ones are disabled.*

```
//Compute laplacian in X direction
__global__ void glaplacianx(...);

__global__ void glaplacianyboundaries(...){
    if (i > 1 && i < NX + 2 && j == 0)
    {
        // Update Laplacian Boundaries
    }
    else if (i > 1 && i < NX + 2 && j == 1)
    {
        // Update Laplacian Boundaries
    }
    else if (i > 1 && i < NX + 2 && j == NY - 2)
    {
        // Update Laplacian Boundaries
    }
    else if (i > 1 && i < NX + 2 && j == NY - 1)
    {
        // Update Laplacian Boundaries
    }
}
```

LISTING 5.2: *Evaluation of x, y, z coordinates of the Zhang and Li model in a single kernel*

Solving the issue is including more work on the laplacian boundaries calculation.

```
__global__ void glaplacianyboundaries(...){
    if (i > 1 && i < NX + 2 && j == 0)
    {
        // Update Laplacian Boundaries
    }
    else if (i > 1 && i < NX + 2 && j == 1)
    {
        // Update Laplacian Boundaries
    }
    else if (i > 1 && i < NX + 2 && j == NY - 2)
    {
        // Update Laplacian Boundaries
    }
    else if (i > 1 && i < NX + 2 && j == NY - 1)
    {
```

```
        // Update Laplacian Boundaries
    }

    //Compute laplacian in Y direction
    glaplaciany(...);

    //Compute laplacian in X direction
    glaplacianx(...);

}
```

LISTING 5.3: *Evaluation of x, y, z coordinates of the Zhang and Li model in a single kernel*

The optimization

5.2.3 Occupancy

Increase the used of constant memory in the device with values that only change during run-time for example the code int

```
gsource << <blocks, threads >> >(u_val, dev_sm_z, dev_mz, NXCUDA);

sfrelax_y[index] = -deltam_y[index] / tau_sf;

DELTAX = (double)TX / (double)NX;
```

LISTING 5.4: *Evaluation of x, y, z coordinates of the Zhang and Li model in a single kernel*

profiler

5.2.4 Concurrent Kernels

Initially each kernel was launched in the default steam 0, the figure 5.3 illustrates such result in the Visual Profiler. Each kernel that is being launched cannot run simultaneously because the next kernel launches needs to compute data, in other words the kernels are not independent from each other.

FIGURE 5.3: *Kernels running in the default 0 Stream.*

The gsolution kernel computes the Zhang an Li model for x, y, z coordinates using extensively the global memory from the device. The kernel which is launched in the

default stream cannot run in parallel with others kernels. To manage concurrency the kernel is divided into three kernels which computes individual each coordinate.

```
__global__ void gsolution(double *sfrelax_x, double *sfrelax_y, double *sfrelax_z,
                          double *sm_x, double *sm_y, double *sm_z,
                          double *sdex_x, double *sdex_y, double *sdex_z,
                          double *lapl_x, double *lapl_y, double *lapl_z,
                          double *deltam_x, double *deltam_y, double *deltam_z,
                          int grid_width)
{
    int i = blockIdx.x * blockDim.x + threadIdx.x + 2;
    int j = blockIdx.y * blockDim.y + threadIdx.y;

    int index = j * grid_width + i;

    if (i > 1 && i < NX + 2 && j >= 0 && j < NY)
    {
        deltam_x[index] = sfrelax_x[index] + sdex_x[index] + lapl_x[index]
                          - sm_x[index];
        deltam_y[index] = sfrelax_y[index] + sdex_y[index] + lapl_y[index]
                          - sm_y[index];
        deltam_z[index] = sfrelax_z[index] + sdex_z[index] + lapl_z[index]
                          - sm_z[index];
  }
}
```

LISTING 5.5: *Evaluation of x, y, z coordinates of the Zhang and Li model in a single kernel*

To achieve concurrent kernels the streams need to access memory blocks that are pinned to a stream. So each memory block corresponding x, y, z are mapped to 3 streams, furthermore all the matrices corresponding for example x are mapped to stream 1.

```
__global__ void gsolution(double *deltam,
                          double *sfrelax, double *sm, double *sdex, double *lapl)
{
    int i = blockIdx.x * blockDim.x + threadIdx.x + 2;
    int j = blockIdx.y * blockDim.y + threadIdx.y;

    int index = j * NXCUDA_CONST + i;

    if (i > 1 && i < NX + 2 && j >= 0 && j < NY)
    {
        deltam[index] = sfrelax[index] + sdex[index] + lapl[index] - sm[index];
    }
}
```

LISTING 5.6: *Evaluation of individual coordinates of the Zhang and Li model*

This same method is applied to every kernel that can be separated into three kernels calls. Some kernels cannot be separate such as the cross product, because the product uses pinned memory block from the other streams. Instead of running one big kernel,

three individual kernels are launched simultaneous. The figure 5.4 shows the results of concurrent kernels in the Tesla K20.

```
for (int i  = 0; i < 3; i++)
{
gsolution<<<blocks, threads, 0, stream[i]>>>(spinAccXYZ[i]->getDev_deltam(),
                                             spinAccXYZ[i]->getDev_sfrelax(),
                                             spinAccXYZ[i]->getDev_sm(),
                                             spinAccXYZ[i]->getDev_sdex(),
                                             spinAccXYZ[i]->getDev_lapl());
}
```

LISTING 5.7: *Evaluation of individual coordinates of the Zhang and Li model*

FIGURE 5.4: *Concurrent kernels in the Tesla K20*

5.2.4.1 Results

graphic.

k20 6.0 speed up.

However

5.2.5 Shared Memory

As we know shared memory is faster than global memory, however shared memory is very limited.

To increase occupancy

LISTING 5.8: *Evaluation of individual coordinates of the Zhang and Li model*

http://www.bu.edu/pasi/files/2011/07/Lecture31.pdf

5.2.5.1 Results

5.2.6 Structure of Arrays, SAO

AoS and SoA refer to "Array of Structures" and "Structure of Arrays" respectively. These two terms refer to two different ways of laying out your data in memory. This

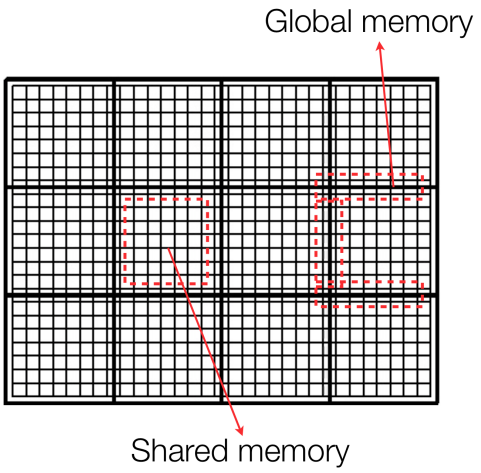

FIGURE 5.5: *Shared Memory Strategy*

is illustrated in figure 5.6 and 5.7 respectively. AOS, grouping properties of an object together and making an array of those objects in memory, whereas a structure of arrays would be a single structure in which you make an array for each property. The structure of arrays can allow for better cache utilization, easier to access continues data, making better use of each read you make from memory, providing a more effective route to memory.

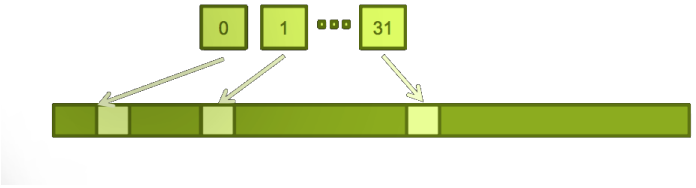

FIGURE 5.6: *AOS memory layout*

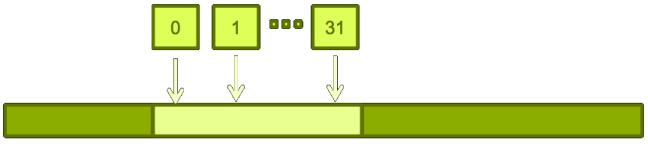

FIGURE 5.7: *SAO memory layout*

The initial implementation the x, y, z data was allocated in separated blocks. Furthermore when accessing blocks of the the same coordinates, the register access the data as the figure5.6.

```
deltam_x = (double **)calloc(NYCUDA, sizeof(double));
deltam_y = (double **)calloc(NXCUDA, sizeof(double *));
deltam_z = (double **)calloc(NXCUDA, sizeof(double *));
```

Listing 5.9: *AOS implementation*

To solve this issue, first a custom class named GPUMatrix was programmed. Moreover it allocated the data for each coordinate and free the memory automatically when the simulation is over. The allocation of the memory is related to the operations that are being done by the kernels for faster memory access.

```
GPUMatrix<T> *dev_deltam;
GPUMatrix<T> *dev_sdex; //Exchange term
GPUMatrix<T> *dev_sfrelax;
GPUMatrix<T> *dev_m;
```

Listing 5.10: *SOA implementation*

5.3 Optimization Results

Summarize the data

GPU	Original	Constant	Streams	Shared	SAO	Shared 2
Tesla K20m	0	0	0	0	0	0
Tesla M2070	110912.3	0	130754.1	97343.4	73938.1	0
Tesla C2050	109635.1	0	128516.6	96762.0	72964.5	0
GeForce GTX 580	70002.7	0	76481.9	70567.1	51603.7	0
GeForce 650m	441933.8	0	492718.3	0	0	0

Table 5.4: *GPU Optimization time*

GPU	Original	Constant	Streams	Shared	SAO	Shared 2
Tesla K20m	0	0	0	0	0	0
Tesla M2070	3.403x	0	2.888x	3.879x	5.107x	0
Tesla C2050	3.442x	0	2.938x	3.902x	5.175x	0
GeForce GTX 580	5.391x	0	4.937x	5.351x	7.317x	0
GeForce 650m	1.113x	0	-1.040x	0	0	0

Table 5.5: *Speedup performance*

The graphs

We could expected the newest card Tesla k20m would obtain the most speedup and lest time of all the GPU cards, it because it has more CUDA cores, the highest compute capabilities. However if falls behind the GeForce 580 with about 1.5x speedup, furthermore it out performer the other Teslas card, but with no outstanding performance. The GeForce 5.2 compared with the others GPUs specifications has most Processor clock (GHz).

Finally,

Chapter 6

Conclusions and future work

GPUs definitely have a place in the world of computational physics, their use allows to do the same work with less energy and more science with less resources. They make HPC computing clusters affordable for small research groups. The true limit test of this new technology will be if it is actually used to advance new science. In the field of computational physics studies that do push the barrier of what is computationally feasible, from speedups of 1.5x to 20x using GPUs[16].

Acceptance has been slow due to many factors, GPUs are sometimes seen as a fad or a niche, the specialized skill set and effort required for GPU programming along with the risk of spending money to setup a GPU cluster, does raise a concern for productivity and viability of this technology. Adopting this technology requires abandoning legacy codes and smart optimizations that have been developed over the years. A wrong choice may result in wasted time and effort.

What is certain is at the moment, is the overall direction of the industry towards higher parallelism, as single threaded performance has reached a local limit, all types of processors are seeking more performance out of parallelism. This means that a large portion of the work needed to parallelize a code for a certain parallel architecture will most probably be applicable to another parallel architecture as well. From the literature and my experiences, one can observe that in order to achieve good results in programming with GPUs it is necessary to take a Heterogeneous approach to coding. That is adopting multi-threaded CPUs and concurrent GPU type algorithms.

Spintronics. In particular we are involved in designing new magnetic materials for spin-devices and modeling and understanding of spin-transport at molecular and atomic scale. By computer simulation is possible to predict their output. Furthermore prove the theoretical experiments.

In the simu

The current thread is to push the hardware capabilities and performance along with Mooers' Law, despite these issues there are some trends in the hardware industry that will make working with GPU easier and more widespread within a HPC context:

3D Memory

Stacks DRAM chips into dense modules with wide interfaces, and brings them inside the same package as the GPU. This lets GPUs get data from memory more quickly boosting throughput and efficiency allowing us to build more compact GPUs that put more power into smaller devices. The result: several times greater bandwidth, more than twice the memory capacity and quadrupled energy efficiency.

NVLink

Todays computers are constrained by the speed at which data can move between the CPU and GPU. NVLink puts a fatter pipe between the CPU and GPU, allowing data to flow at more than 80GB per second, compared to the 16GB per second available now.

Pascal Module

NVIDIA has designed a module to house Pascal GPUs with NVLink. At one-third the size of the standard boards used today, theyll put the power of GPUs into more compact form factors than ever before.

Mobile and embedded Devices

Kepler Erista Maxwell GPU

Cloud Computing

To conclude, I offer my personal perspective on GPU computing. I think the importance of using accelerator hardware is an economic and environmental issue. The environmental aspect of doing computing is often overlooked, but an ever increasing important one. As heavy computer users we will have to take responsibility for our electricity use. The benefit of less energy use is clear.

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