

# 16.317: Microprocessor Systems Design I

Fall 2015

## Homework 2

Due **2:00 PM, Friday, 9/25/15**

### Notes:

- While typed solutions are preferred, handwritten solutions are acceptable.
- All solutions must be legible and contained in one file. Archive files are not acceptable.
- Electronic submissions should be e-mailed to Dr. Geiger at [Michael\\_Geiger@uml.edu](mailto:Michael_Geiger@uml.edu).
- This assignment is worth 100 points.

1. (60 points) Assume the state of an x86 processor's registers and memory are:

	Address
EAX: 00000010H	20100H
EBX: 00000020H	20104H
ECX: 00000030H	20108H
EDX: 00000040H	2010CH
CF: 1	20110H
ESI: 00020100H	20114H
EDI: 00020100H	20118H
	2011CH
	20120H

10	00	08	00
10	10	FF	FF
08	00	19	91
20	40	60	80
02	00	AB	0F
30	00	11	55
40	00	7C	EE
FF	00	42	D2
30	00	30	90

What is the result produced in the destination operand by each of the instructions listed below?  
Assume that the instructions execute in sequence.

```
ADD AX, 00FFh
ADC CX, AX
INC BYTE PTR [20100h]
SUB DL, BL
SBB DL, [20114h]
DEC BYTE PTR [EDI+EBX]
NEG BYTE PTR [EDI+0018h]
MUL DX
IMUL BYTE PTR [ESI+0006h]
DIV BYTE PTR [ESI+0008h]
IDIV BYTE PTR[ESI+0010h]
```

2. (40 points) Assume the state of an x86 processor's registers and memory are:

EAX: 00005555H	<b>Address</b>				
EBX: 00045010H	45100H	0F	F0	00	FF
ECX: 00000010H		...			
EDX: 0000AAAAH	45200H	30	00	19	91
ESI: 000000F2H		...			
EDI: 00000200H	45210H	AA	AA	AB	0F
		...			
	45220H	55	55	7C	EE
		...			
	45300H	AA	55	30	90

What is the result produced in the destination operand by each of the instructions listed below?  
Assume that the instructions execute in sequence.

AND BYTE PTR [45300H], 0FH  
SAR DX, 8  
OR [EBX+EDI], AX  
SHL AX, 2  
XOR AX, [ESI+EBX]  
NOT BYTE PTR [45300H]  
SHR AX, 4