

16.317: Microprocessor Systems Design I

Spring 2014

Homework 3

Due **Wednesday, 3/5/14**

Notes:

- While typed solutions are preferred, handwritten solutions are acceptable.
- Electronic submissions should be e-mailed to Dr. Geiger at Michael_Geiger@uml.edu.
- All electronic submissions must be contained in a single file (Word document or PDF). Archived submissions (e.g., zipped folders sent as a .zip file) are not acceptable.
- This assignment is worth 50 points.

1. (20 points) Assume the state of an x86 processor's registers and memory are:

EAX: 00005555H	Address				
EBX: 00000010H	45100H				
ECX: 00000010H	<table><tr><td>0F</td><td>F0</td><td>00</td><td>FF</td></tr></table>	0F	F0	00	FF
0F	F0	00	FF		
EDX: 0000AAAAH	...				
ESI: 000000F2H	45200H				
EDI: 00000200H	<table><tr><td>30</td><td>00</td><td>19</td><td>91</td></tr></table>	30	00	19	91
30	00	19	91		
DS: 4500H	...				
	45210H				
	<table><tr><td>AA</td><td>AA</td><td>AB</td><td>0F</td></tr></table>	AA	AA	AB	0F
AA	AA	AB	0F		
	...				
	45220H				
	<table><tr><td>55</td><td>55</td><td>7C</td><td>EE</td></tr></table>	55	55	7C	EE
55	55	7C	EE		
	...				
	45300H				
	<table><tr><td>AA</td><td>55</td><td>30</td><td>90</td></tr></table>	AA	55	30	90
AA	55	30	90		

What is the result produced in the destination operand by each of the instructions listed below?
Assume that the instructions execute in sequence.

```
AND BYTE PTR [0300H], 0FH
SAR DX, 8
OR [BX+DI], AX
ROL AX, 2
XOR AX, [SI+BX]
NOT BYTE PTR [0300H]
RCR AX, 4
```

2. (10 points) Assume the state of an x86 processor's registers and memory are:

EAX: 00005555H	Address
EBX: 00000010H	ABD00H
ECX: 00000010H	...
EDX: 0000AAAAH	45200H
ESI: 000000F2H	...
EDI: 00000200H	45210H
DS: ABC0H	...
	45220H
	...
	45300H

Also, assume all flags (ZF, CF, SF, PF, OF) are initialized to 0.

For the instruction sequence shown below, list all changed registers and/or memory locations and their new values, as well as all changed flags from the list above. Note that the registers and memory have the same starting values at the beginning of each sequence, but a value changed by one instruction in a sequence can affect the results of all other instructions in the same sequence.

```
BT      AX, 4
SETC    [100H]
BTS     AX, 5
SETC    [101H]
BTR     AX, 6
SETC    [102H]
BTC     AX, 7
SETC    [103H]
```

3. (20 points) As noted in class, the SETcc instruction can be used to combine multiple conditions together to create a compound conditional test. For example, the code below tests the condition $((A < B) \ \&\& \ (C < D))$, storing the result in DL:

```
MOV    AX, A
CMP    AX, B
SETL   DL
MOV    AX, C
CMP    AX, D
SETL   DH
AND    DL, DH
```

For each part of this problem, assume A, B, C, D, E, and F refer to signed integers stored in memory.

What compound condition is tested by each of the code sequences below?

a.

```
MOV    AX, A
CMP    AX, B
SETLE  BL
CMP    AX, E
SETGE  BH
OR     BL, BH
```

b.

```
MOV    AX, C
CMP    AX, A
SETE   BL
MOV    AX, B
CMP    AX, A
SETNE  BH
AND    BL, BH
CMP    AX, C
SETL   BH
AND    BL, BH
CMP    AX, A
SETZ   BH
OR     BL, BH
```

c.

```
MOV    AX, A
SUB    AX, B
CMP    AX, C
SETGE  BL
MOV    AX, D
ADD    AX, E
SUB    AX, F
SETNZ  BH
OR     BL, BH
```