16.317: Microprocessor Systems Design I

Summer 2012

Homework 2

Due **Monday, 7/30/12**

<u>NOTE:</u> No late assignments will be accepted, as the solution will be posted after Monday's class to allow you time to study it before the second exam.

1. *(20 points)* Assume the state of the 80386DX's registers and memory are:

EAX: 00000010H
EBX: 00000020H
ECX: 00000030H
EDX: 00000040H
CF: 1
ESI: 00000100H
EDI: 00000100H
DS: 2000H

Address				
20100H	10	00	08	00
20104H	10	10	FF	FF
20108H	08	00	19	91
2010CH	20	40	60	80
20110H	02	00	AB	0F
20114H	30	00	11	55
20118H	40	00	7C	EE
2011CH	FF	00	42	D2
20120H	30	00	30	90

What is the result produced in the destination operand by each of the instructions listed below? Assume that the instructions execute in sequence—for example, your answer to part (b) will depend on your answer to part (a).

a. ADD AX, 00FFH
b. ADC SI, AX
c. INC BYTE PTR [0100H]
d. SUB DL, BL
e. SBB DL, [0114H]
f. DEC BYTE PTR [DI+BX]
g. NEG BYTE PTR [DI+0018H]
h. MUL DX
i. IMUL BYTE PTR [SI+FEF7H]
j. DIV BYTE PTR [SI+FEF9H]
k. IDIV BYTE PTR[SI+FF01H]

2. *(20 points)* Assume the state of the 80386DX's registers and memory are:

EAX: 00005555H
EBX: 00000010H
ECX: 00000010H
EDX: 0000AAAAH
ESI: 000000F2H
EDI: 00000200H
DS: 4500H

Address				
45100H	0F	F0	00	FF
	…			
45200H	30	00	19	91
	…			
45210H	AA	AA	AB	0F
	…			
45220H	55	55	7C	EE
	…			
45300H	AA	55	30	90

What is the result produced in the destination operand by each of the instructions listed below? Assume that the instructions execute in sequence—for example, your answer to part (b) may depend on your answer to part (a).

a. AND BYTE PTR [0300H], 0FH
b. SAR DX, 8
c. OR [BX+DI], AX
d. ROL AX, 2
e. XOR AX, [SI+BX]
f. NOT BYTE PTR [0300H]
g. RCR AX, 4

3. *(30 points)* Assume the state of the 80386DX's registers and memory are:

EAX: 00005555H
EBX: 00000010H
ECX: 00000010H
EDX: 0000AAAAH
ESI: 000000F2H
EDI: 00000200H
DS: ABC0H

Address				
ABD00H	0F	F0	00	FF
	…			
45200H	30	00	19	91
	…			
45210H	AA	AA	AB	0F
	…			
45220H	55	55	7C	EE
	…			
45300H	AA	55	30	90

Also, assume all flags (ZF, CF, SF, PF, OF) are initialized to 0.

For each instruction sequence shown below, list <u>all</u> changed registers and/or memory locations and their new values, as well as all changed flags from the list above. Note that the registers and memory have the same starting values at the beginning of each sequence, but a value changed by one instruction in a sequence can affect the results of all other instructions in the same sequence.

a.
```
BT      AX, 4
SETC    [100H]
BTS     AX, 5
SETC    [101H]
BTR     AX, 6
SETC    [102H]
BTC     AX, 7
SETC    [103H]
```

b.
```
    CMP  AL, 56H
    JL   L1
    JG   L2
    MOV  AH, BL
    JMP  E
L1: MOV  AH, CH
    JMP  E
L2: MOV  AH, DL
E:  SETL [DI]
```

4. *(30 points)* As noted in class, the SETcc instruction can be used to combine multiple conditions together to create a compound conditional test. For example, the code below tests the condition `((A < B) && (C < D))`, storing the result in DL:

```
MOV     AX, A
CMP     AX, B
SETL    DL
MOV     AX, C
CMP     AX, D
SETL    DH
AND     DL, DH
```

For each part of this problem, assume A, B, C, D, E, and F refer to signed integers stored in memory.

What compound condition is tested by each of the code sequences below?

a.
```
MOV     AX, A
CMP     AX, B
SETLE   BL
CMP     AX, E
SETGE   BH
OR      BL, BH
```

b.
```
MOV     AX, C
CMP     AX, A
SETE    BL
MOV     AX, B
CMP     AX, A
SETNE   BH
AND     BL, BH
CMP     AX, C
SETL    BH
AND     BL, BH
CMP     AX, A
SETZ    BH
OR      BL, BH
```

c.
```
MOV     AX, A
SUB     AX, B
CMP     AX, C
SETGE   BL
MOV     AX, D
ADD     AX, E
SUB     AX, F
SETNZ   BH
OR      BL, BH
```