16.317: Microprocessor Systems Design I

Summer 2013

Lecture 4: Key Questions
July 18, 2013

1. **Example:** Given AL = 43H, CL = 04H, and CF = 0, show the state of AL after each instruction in the sequence below:

   ```
   ROR AL, 2
   ROL AL, CL
   RCR AL, 3
   RCL AL, 4
   ```

2. Explain the operation of the bit test instructions (BT, BTR, BTS, BTC)

3. Explain the operation of the bit scan instructions (BSF, BSR).

4. **Example:** Given the following initial state, list all changed registers and/or memory locations and their new values. Where appropriate, you should also list the state of the carry flag (CF).

Initial state:

EAX: 00000000H
EBX: 0000000AH
ECX: 00000000H
EDX: 00000000H
CF: 0
ESI: 00000008H
EDI: FFFF0000H
EBP: 00000400H
ESP: 00002000H
DS: 2110H
SS: 1000H

Address	Lo			Hi
21100H	04	00	10	10
21104H	89	01	20	40
21108H	02	00	00	16
2110CH	17	03	FF	00
21110H	1E	00	06	00
21114H	08	00	0A	00

Instructions:

```
BT    WORD PTR [02H], 4
BTC   WORD PTR [10H], 1
BTS   WORD PTR [04H], 1
BSF   CX, WORD PTR [0EH]
BSR   DX, WORD PTR [09H]
```

5. Describe the operation of the compare instruction.

6. Complete the following table that describes the different x86 condition codes.

Mnemonic (cc)	Condition tested	Status flag setting for true condition
O		
NO		
B, NAE, C		
NB, AE, NC		
S		
NS		
P, PE		
NP, PO		
E, Z		
NE, NZ		
BE, NA		
NBE, A		
L, NGE		
NL, GE		
LE, NG		
NLE, G		

7. Describe the operation of the conditional move instruction.

8. Describe the operation of the SETcc instruction. How can this instruction be used?

9. **Example:** Show the results of the following instructions, assuming that DS:100H = 0001H, DS:102H = 0003H, DS:104H = 1011H, DS:106H = 1011H, DS:108H = ABCDH, DS:10AH = DCBAH

   What complex condition does this sequence test?

```
MOV     AX, [100H]
CMP     AX, [102H]
SETLE   BL
MOV     AX, [104H]
CMP     AX, [106H]
SETE    BH
AND     BL, BH
MOV     AX, [108H]
CMP     AX, [10AH]
SETNE   BH
OR      BL, BH
```