1 10-layers PCB Regular

Thickness: **1.6MM** Finished Outer Copper: **1OZ**
Inner Copper: **1OZ** Inner layer Residual copper ratio: **70%**

Layer	Material	Thickness (mm)	Thickness after lamination(mm)
L1-CU	Outer Base Copper 0.5OZ	0.0175	0.0175 (Plating to 1OZ)
PP	3313 RC58% DK:4.45	0.1030	0.0925
L2-CU	Inner Copper 1OZ	0.0350	0.2 (Core with Cu)
CORE	Core DK:4.6	0.1300	
L3-CU	Inner Copper 1OZ	0.0350	
PP	7628 RC46% DK:4.74	0.1960	0.1750
L4-CU	Inner Copper 1OZ	0.0350	0.2 (Core with Cu)
CORE	Core DK:4.6	0.1300	
L5-CU	Inner Copper 1OZ	0.0350	
PP	7628 RC46% DK:4.74	0.1960	0.1750
L6-CU	Inner Copper 1OZ	0.0350	0.2 (Core with Cu)
CORE	Core DK:4.6	0.1300	
L7-CU	Inner Copper 1OZ	0.0350	
PP	7628 RC46% DK:4.74	0.1960	0.1750
L8-CU	Inner Copper 1OZ	0.0350	0.2 (Core with Cu)
CORE	Core DK:4.6	0.1300	
L9-CU	Inner Copper 1OZ	0.0350	
PP	3313 RC58% DK:4.45	0.1030	0.0925
L10-CU	Outer Base Copper 0.5OZ	0.0175	0.0175 (Plating to 1OZ)

* Thickness after lamination: 1.55mm, tolerance: ±10%
* Finished PCB Thickness: 1.65mm, tolerance: ±10%
* Inner layer Residual copper ratio > 60%, it is suitable to choose a lamination structure with 70% inner layer Residual copper ratio.

Microcontroller

File: microcontroller.kicad_sch

Ethernet PHY

File: ethernet_phy.kicad_sch

RF Chain

File: rf_chain.kicad_sch

3V3 Power

File: power.kicad_sch

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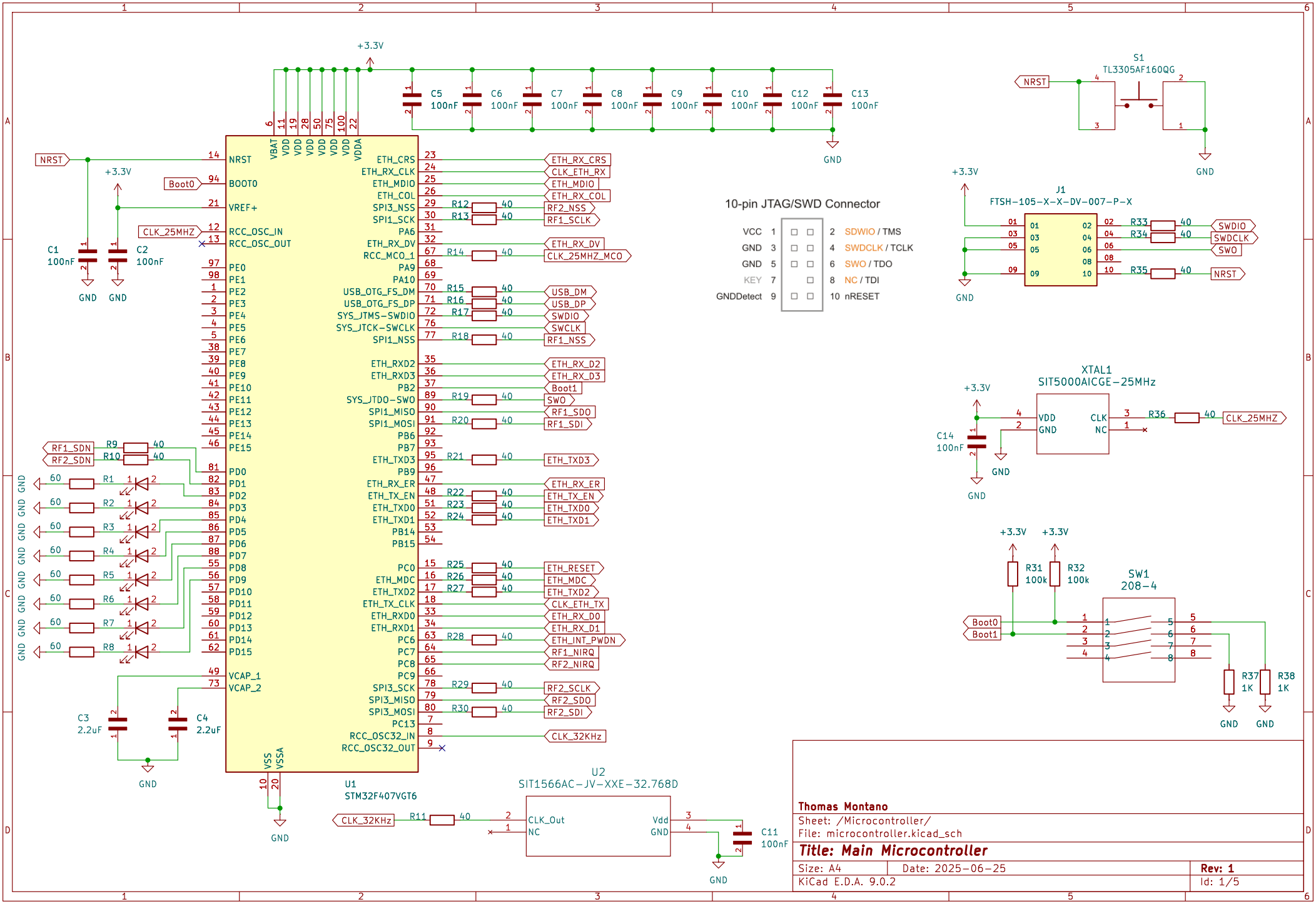
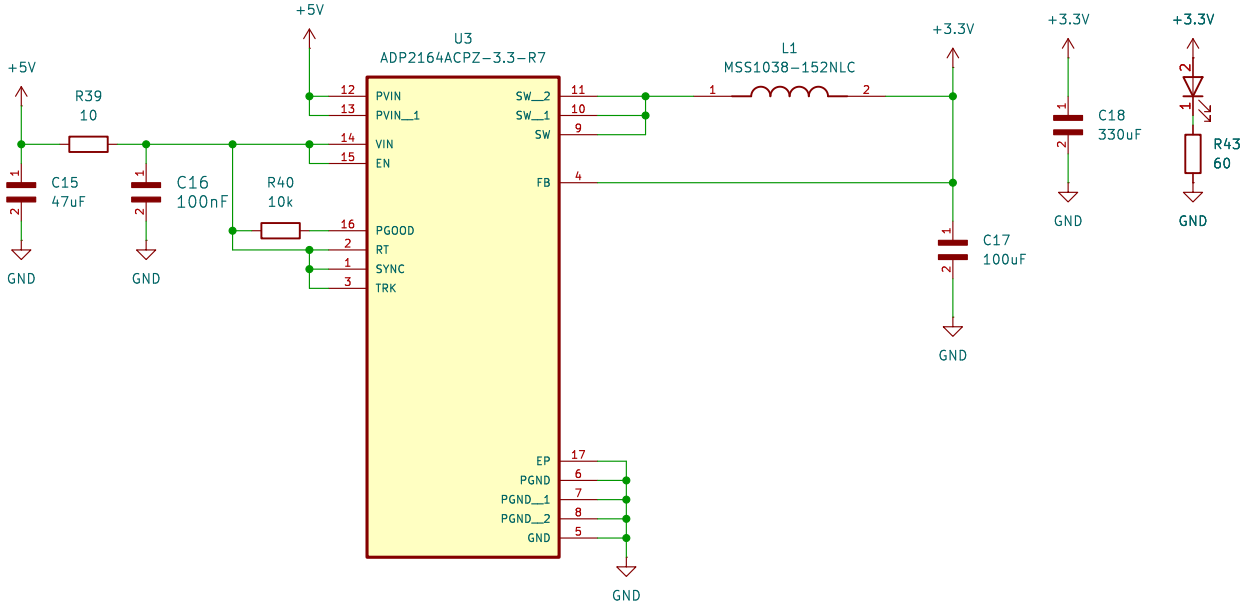
Sheet: /
File: Radio Project.kicad_sch

Title: RF Puck

Size: A4	Date: 2025-06-22	**Rev: 1**
KiCad E.D.A. 9.0.2		Id: 1/5


+3.3V
C5 100nF
C6 100nF
C7 100nF
C8 100nF
C9 100nF
C10 100nF
C12 100nF
C13 100nF
GND
S1
TL3305AF160QG
NRST
J1
FTSH-105-X-X-DV-007-P-X
SWDIO
SWDCLK
SWO
NRST
10-pin JTAG/SWD Connector
VCC 1
GND 3
GND 5
KEY 7
GNDDetect 9
2 SDWIO / TMS
4 SWDCLK / TCLK
6 SWO / TDO
8 NC / TDI
10 nRESET
XTAL1
SIT5000AICGE-25MHz
CLK_25MHZ
C14 100nF
R36 40
R31 100k
R32 100k
SW1
208-4
R37 1K
R38 1K
Boot0
Boot1
U1
STM32F407VGT6
U2
SIT1566AC-JV-XXE-32.768D
CLK_32KHz
R11 40
C11 100nF
C1 100nF
C2 100nF
C3 2.2uF
C4 2.2uF
Boot0 94
CLK_25MHZ 12
RF1_SDN R9 40
RF2_SDN R10 40
R1 60
R2 60
R3 60
R4 60
R5 60
R6 60
R7 60
R8 60
ETH_CRS
ETH_RX_CLK
ETH_MDIO
ETH_COL
SPI3_NSS R12 40 RF2_NSS
SPI1_SCK R13 40 RF1_SCLK
PA6
ETH_RX_DV
RCC_MCO_1 R14 40 CLK_25MHZ_MCO
PA9
PA10
USB_OTG_FS_DM R15 40 USB_DM
USB_OTG_FS_DP R16 40 USB_DP
SYS_JTMS-SWDIO R17 40 SWDIO
SYS_JTCK-SWCLK SWCLK
SPI1_NSS R18 40 RF1_NSS
ETH_RXD2 ETH_RX_D2
ETH_RXD3 ETH_RX_D3
PB2 Boot1
SYS_JTDO-SWO R19 40 SWO
SPI1_MISO RF1_SDO
SPI1_MOSI R20 40 RF1_SDI
PB6
PB7
ETH_TXD3 R21 40 ETH_TXD3
PB9
ETH_RX_ER
ETH_TX_EN R22 40 ETH_TX_EN
ETH_TXD0 R23 40 ETH_TXD0
ETH_TXD1 R24 40 ETH_TXD1
PB14
PB15
PC0 R25 40 ETH_RESET
ETH_MDC R26 40 ETH_MDC
ETH_TXD2 R27 40 ETH_TXD2
ETH_TX_CLK CLK_ETH_TX
ETH_RXD0 ETH_RX_D0
ETH_RXD1 ETH_RX_D1
PC6 R28 40 ETH_INT_PWDN
PC7 RF1_NIRQ
PC8 RF2_NIRQ
PC9
SPI3_SCK R29 40 RF2_SCLK
SPI3_MISO RF2_SDO
SPI3_MOSI R30 40 RF2_SDI
PC13
RCC_OSC32_IN CLK_32KHz
RCC_OSC32_OUT
NRST
BOOT0
VREF+
RCC_OSC_IN
RCC_OSC_OUT
PE0
PE1
PE2
PE3
PE4
PE5
PE6
PE7
PE8
PE9
PE10
PE11
PE12
PE13
PE14
PE15
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
PD8
PD9
PD10
PD11
PD12
PD13
PD14
PD15
VCAP_1
VCAP_2
VBAT
VDD
VDDA
VSS
VSSA
Thomas Montano
Sheet: /Microcontroller/
File: microcontroller.kicad_sch
Title: Main Microcontroller
Size: A4
Date: 2025-06-25
Rev: 1
KiCad E.D.A. 9.0.2
Id: 1/5



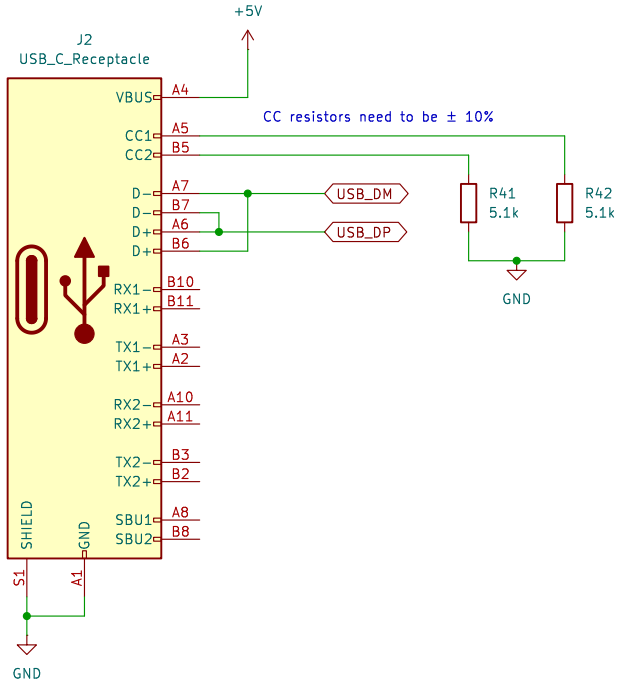
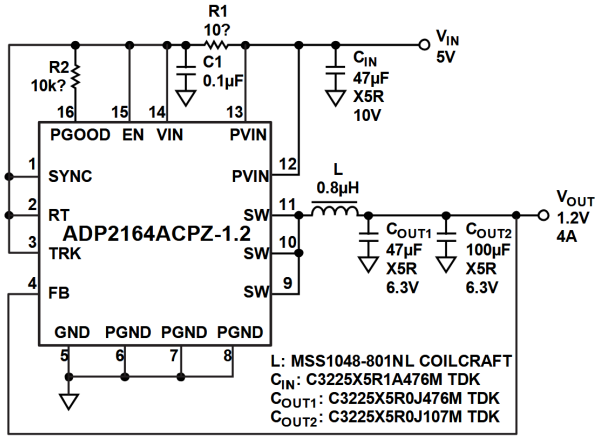


Table 6. Recommended L and C_{OUT} Values at f_S = 600 kHz

V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)
3.3	1.0	1	100 + 100
3.3	1.2	1	100 + 100
3.3	1.5	1	100 + 47
3.3	1.8	1	100 + 47
3.3	2.5	1	100
5	1.0	1	100 + 100
5	1.2	1.5	100 + 100
5	1.5	1.5	100 + 47
5	1.8	1.5	100 + 47
5	2.5	1.5	100
5	3.3	1.5	100



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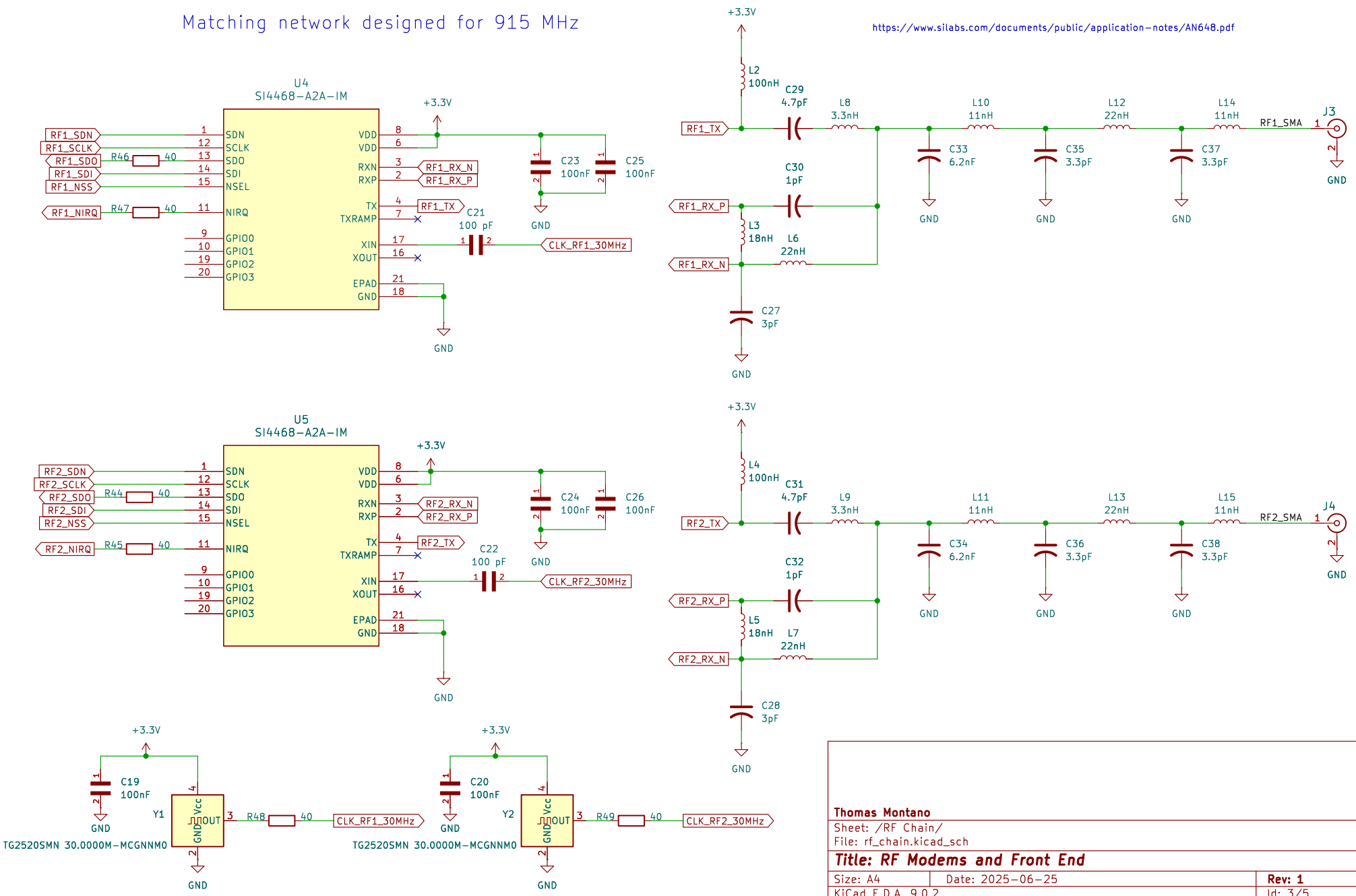
Sheet: /3V3 Power/

File: power.kicad_sch

Title: 3.3V Power Block

Size: A4	Date: 2025-06-22	Rev: 1
KiCad E.D.A. 9.0.2		Id: 2/5


Matching network designed for 915 MHz
https://www.silabs.com/documents/public/application-notes/AN648.pdf
U4
SI4468-A2A-IM
U5
SI4468-A2A-IM
RF1_SDN
RF1_SCLK
RF1_SDO
RF1_SDI
RF1_NSS
RF1_NIRQ
RF2_SDN
RF2_SCLK
RF2_SDO
RF2_SDI
RF2_NSS
RF2_NIRQ
SDN
SCLK
SDO
SDI
NSEL
NIRQ
GPIO0
GPIO1
GPIO2
GPIO3
VDD
RXN
RXP
TX
TXRAMP
XIN
XOUT
EPAD
GND
RF1_RX_N
RF1_RX_P
RF1_TX
RF2_RX_N
RF2_RX_P
RF2_TX
CLK_RF1_30MHz
CLK_RF2_30MHz
R46
R47
R44
R45
C21
C22
C23
C24
C25
C26
100 pF
100nF
+3.3V
GND
RF1_TX
RF1_RX_P
RF1_RX_N
RF2_TX
RF2_RX_P
RF2_RX_N
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11
L12
L13
L14
L15
100nH
18nH
22nH
3.3nH
11nH
C27
C28
C29
C30
C31
C32
C33
C34
C35
C36
C37
C38
3pF
4.7pF
1pF
6.2nF
3.3pF
RF1_SMA
RF2_SMA
J3
J4
C19
C20
Y1
Y2
TG2520SMN 30.0000M-MCGNNM0
R48
R49
Vcc
OUT
Thomas Montano
Sheet: /RF Chain/
File: rf_chain.kicad_sch
Title: RF Modems and Front End
Size: A4
Date: 2025-06-25
Rev: 1
KiCad E.D.A. 9.0.2
Id: 3/5

Bias Resistor Connection: A 4.87−kΩ ±1% resistor must be connected from RBIAS to GND.

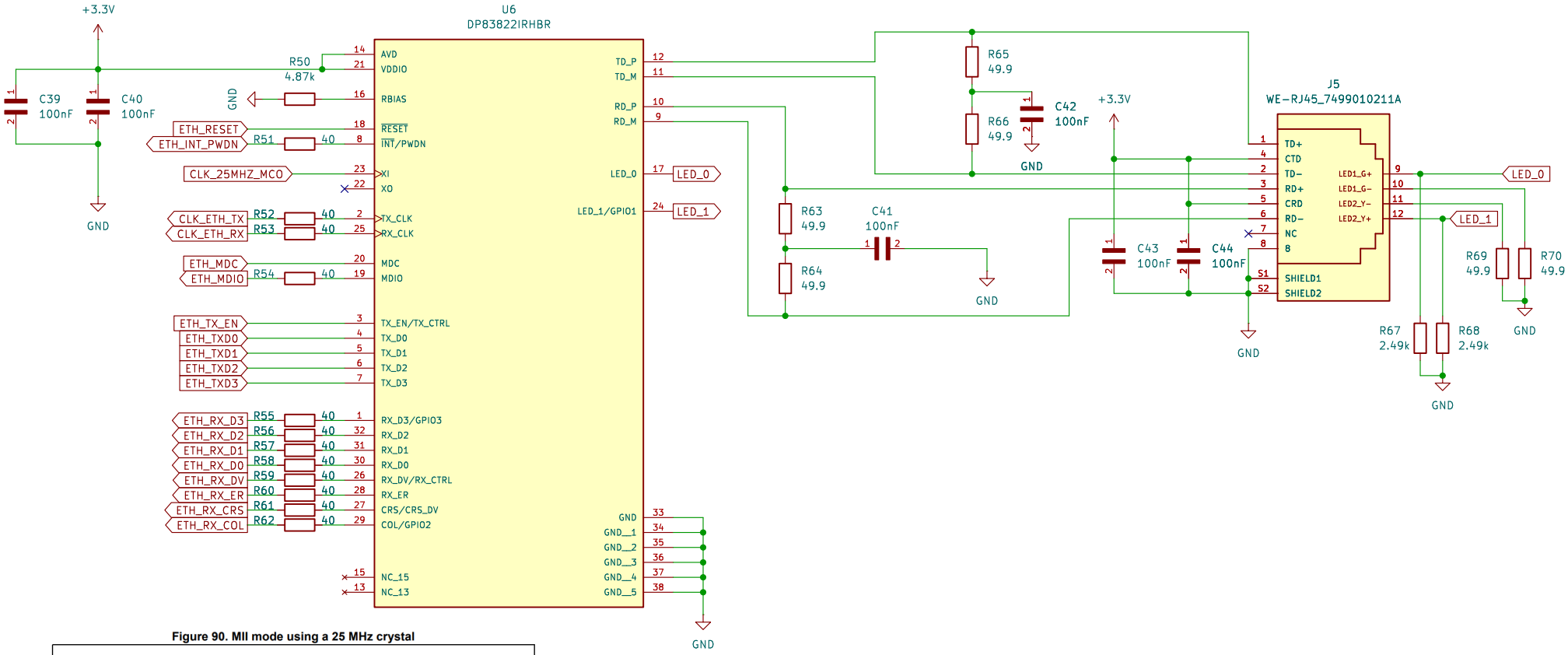
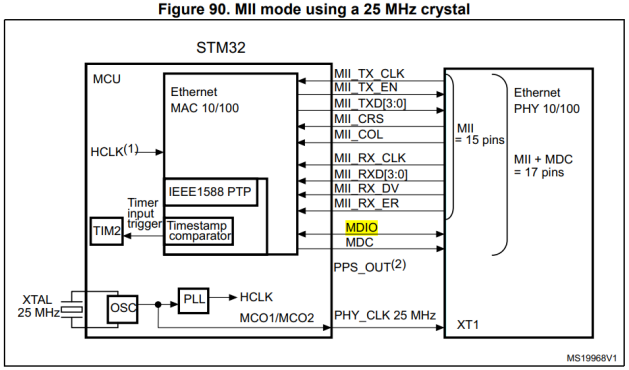


Figure 90. MII mode using a 25 MHz crystal



1. f_{HCLK} must be greater than 25 MHz.
2. Pulse per second when using IEEE1588 PTP optional signal.

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Sheet: /Ethernet PHY/
File: ethernet_phy.kicad_sch

Title: Ethernet PHY Interface

Size: A4	Date: 2025−06−25	**Rev: 1**
KiCad E.D.A. 9.0.2		Id: 4/5