Ερώτημα 1

Κώδικας:

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

entity latch is port (
D : in bit;
EN : in bit;
Q : out bit);
end latch;

ARCHITECTURE dataflow OF latch IS
BEGIN
  process (d, en) begin
     if (en = '1') then
          q <= d;
     end if;
  end process;
END dataflow;
```

Wave

Κώδικας TestBench:

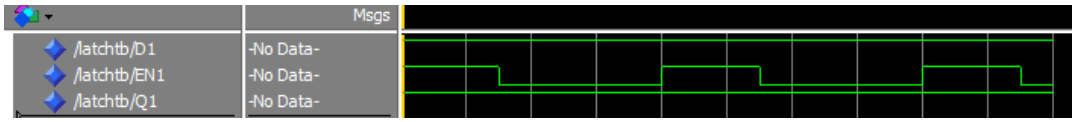
```
entity latchtb is
end latchtb;

architecture tb of latchtb is
signal D1, EN1, Q1: bit;
component latch port (D, EN: in bit; Q: out bit);
end component;
begin
M1: latch PORT MAP (D=>D1, EN=>EN1, Q=>Q1);
process
 begin
 EN1 <= '1'; wait for 130 ns;
 EN1 <= '0'; wait for 270 ns;
 EN1 <= '1'; wait for 130 ns;
 EN1 <= '0'; wait for 270 ns;
 EN1 <= '1'; wait for 130 ns;
 EN1 <= '0'; wait for 270 ns;
 end process;

process
 begin
 D1 <= '1'; wait for 270 ns;
 D1 <= '1'; wait for 310 ns;
 D1 <= '1'; wait for 230 ns;
 D1 <= '1'; wait for 170 ns;
 D1 <= '1'; wait for 90 ns;
 D1 <= '1'; wait for 120 ns;
end process;

end tb;
```

Wave



Ερώτημα 2

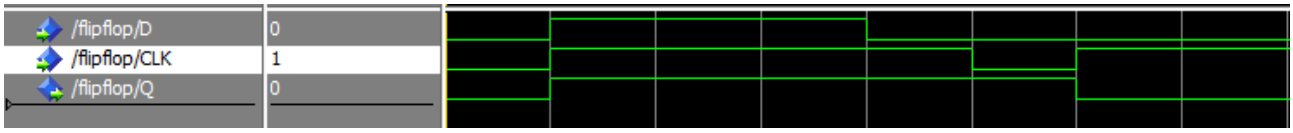
Κώδικας:

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

entity flipflop is port (
D : in bit;
CLK : in bit;
Q : out bit);
end flipflop;

ARCHITECTURE dataflow OF flipflop IS
BEGIN
  process(d, clk) begin
     if (clk 'event and clk = '1') then
       q <= d;
     end if;
  end process;
end dataflow;
```

Wave



Ερώτημα 3

Κώδικας:

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

entity flipflop is port (
D : in bit;
CLK : in bit;
Rstn: in bit;
Q : out bit);
end flipflop;

ARCHITECTURE dataflow OF flipflop IS
BEGIN
  process(cld, rstn) begin
      if (rstn = '0') then
        q <= '0';
      elsif (clk 'event and clk = '1') then
        q <= d;
      end if;
  end process;
end dataflow;
```

Wave