Πανεπιστήμιο Δυτικής Αττικής
Σχολή Μηχανικών
Τμήμα Μηχανικών Πληροφορικής και Υπολογιστών

Εργαστήριο
Σχεδίασης Ψηφιακών Συστημάτων

ΝΙΚΟΛΑΟΣ ΘΩΜΑΣ
ΑΜ: 21390068
ΤΜΗΜΑ: Τμήμα 2 Τρίτη 10.00-12.00

ΑΘΗΝΑ
Παρασκευή, 5 Μαΐου 2023

Ερώτημα 1

Κώδικας:

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY mux2to1 IS PORT (
  a, b, s: IN bit;
  c: OUT bit);
END mux2to1 ;

ARCHITECTURE dataflow OF mux2to1 IS
BEGIN
        c <= a WHEN s='1' ELSE b;
END dataflow;
```

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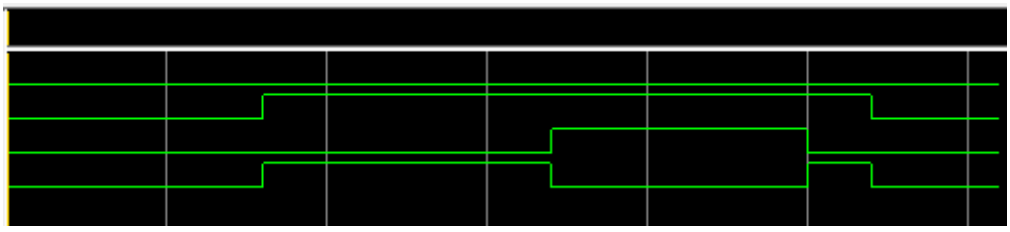

Ερώτημα 2

Κώδικας:

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY mux2to1 IS PORT (
  a, b, s: IN bit;
  c: OUT bit);
END mux2to1 ;

ARCHITECTURE dataflow OF mux2to1 IS
BEGIN
        c <= a WHEN s='1' ELSE b;
END dataflow;
```

Κώδικας TestBench:

```
entity test_mux is
end test_mux;

architecture test_b of test_mux is
signal A1, B1, S1, C1: bit;
component mux2to1 port (a, b, s: in bit; c: out bit);
end component;

begin
 M1: mux2to1 PORT MAP (a=>A1, b=>B1, s=>s1, c=>c1);
process
 begin
   A1 <= '1'; B1 <= '0'; S1 <= '1'; wait for 20 ps;
   A1 <= '1'; B1 <= '0'; S1 <= '0'; wait for 20 ps;
 end process;
end test_b;
```

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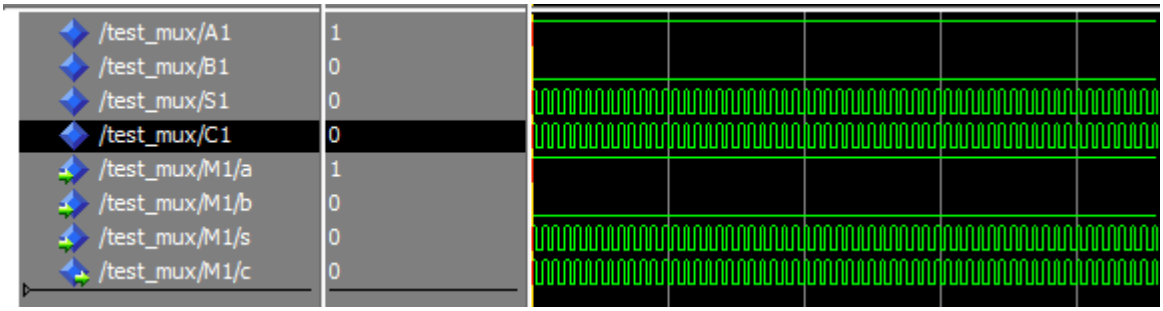

Ερώτημα 3

Κώδικας:

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY mux2to1 IS PORT (
 a, b: in std_logic_vector(2 downto 0);
 s: in std_logic;
 d: out std_logic_vector(2 downto 0));
END mux2to1 ;

ARCHITECTURE dataflow OF mux2to1 IS
BEGIN
d <= a WHEN s='1' ELSE b;
END dataflow;
```

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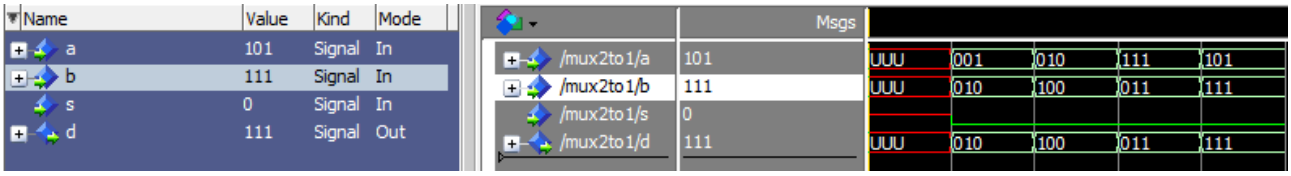

Πίνακας:

s	a	b	d
0	001	010	001
0	010	100	010
0	111	011	111
0	101	111	101
1	010	001	001
1	000	101	101
1	101	010	010
1	111	101	101

Ερώτημα 4

Κώδικας:

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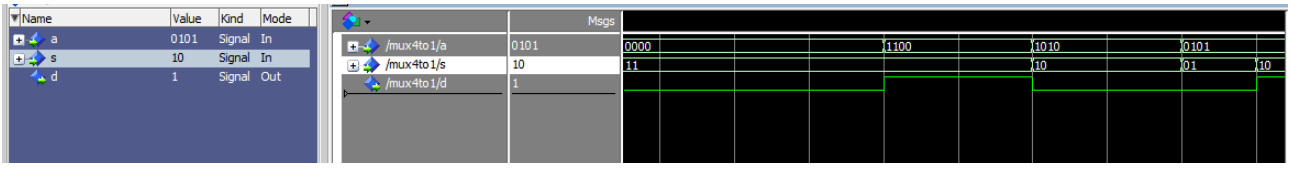
```
entity mux_4to1 is port (
 a: in std_logic_vector(4 downto 1);
 s: in std_logic_vector(2 downto 1);
 d: out std_logic);
end mux_4to1;
```



Πίνακας:

a	s	d
0000	00	0
0101	01	0
1010	10	0
1100	11	0

Ερώτημα 5

Κώδικας:

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

entity dec2to4 is
port (
a: in std_logic_vector(2 downto 1);
d: out std_logic_vector(4 downto 1));
end dec2to4;

ARCHITECTURE dataflow OF dec2to4 IS
BEGIN
    d(1) <= not a(1) and not a(2);
    d(2) <= not a(1) and a(2);
    d(3) <= a(1) and not a(2);
    d(4) <= a(1) and a(2);
END dataflow;
```

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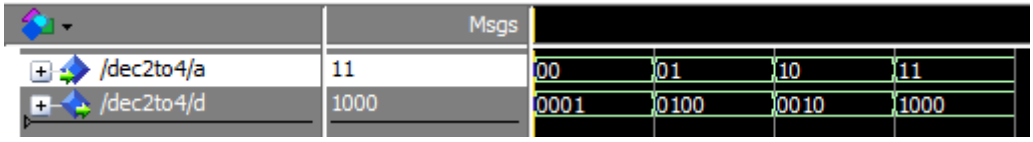

Πίνακας:

a	d
00	0001
01	0100
10	0010
11	1000

Ερώτημα 6

Κώδικας:

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

entity dec_2to4 is
port (
a: in std_logic_vector(2 downto 1);
en: in std_logic;
d: out std_logic_vector(4 downto 1) );
end dec_2to4;

ARCHITECTURE dataflow OF dec_2to4 IS
BEGIN
    d(1) <= not a(1) and not a(2) and en;
    d(2) <= not a(1) and a(2) and en;
    d(3) <= a(1) and not a(2) and en;
    d(4) <= a(1) and a(2) and en;
END dataflow;
```

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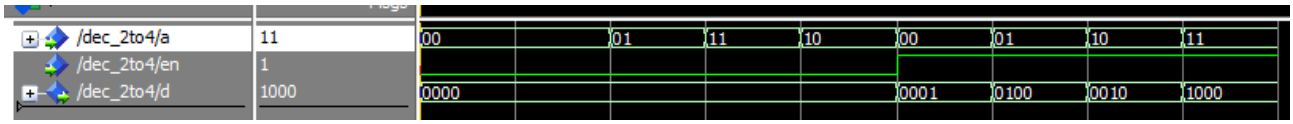


Πίνακας:

a	en	d
00	0	0
01	0	0
10	0	0
11	0	0
00	1	0001
01	1	0100
10	1	0010
11	1	1000

Ερώτημα 7

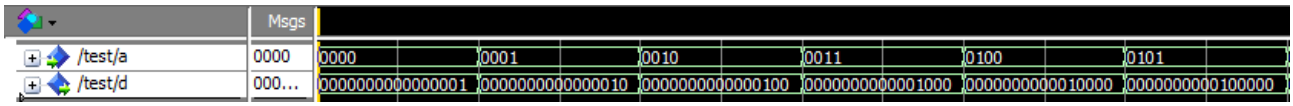
Κώδικας:

```
library ieee;
use ieee.std_logic_1164.all;

entity dec_4to16 is port (
a: in std_logic_vector( 4 downto 1);
d: out std_logic_vector(16 downto 1));
end dec_4to16;

ARCHITECTURE dataflow OF dec4tol6 IS
BEGIN
    d(1)  <= not a(4) and not a(3) and not a(2) and not a(1);
    d(2)  <= not a(4) and not a(3) and not a(2) and     a(1);
    d(3)  <= not a(4) and not a(3) and     a(2) and not a(1);
    d(4)  <= not a(4) and not a(3) and     a(2) and     a(1);
    d(5)  <= not a(4) and     a(3) and not a(2) and not a(1);
    d(6)  <= not a(4) and     a(3) and not a(2) and     a(1);
    d(7)  <= not a(4) and     a(3) and     a(2) and not a(1);
    d(8)  <= not a(4) and     a(3) and     a(2) and     a(1);
    d(9)  <=     a(4) and not a(3) and not a(2) and not a(1);
    d(10) <=     a(4) and not a(3) and not a(2) and     a(1);
    d(11) <=     a(4) and not a(3) and     a(2) and not a(1);
    d(12) <=     a(4) and not a(3) and     a(2) and     a(1);
    d(13) <=     a(4) and     a(3) and not a(2) and not a(1);
    d(14) <=     a(4) and     a(3) and not a(2) and     a(1);
    d(15) <=     a(4) and     a(3) and     a(2) and not a(1);
    d(16) <=     a(4) and     a(3) and     a(2) and     a(1);
END dataflow;
```

Wave



Πίνακας:

a	d
0000	0000000000000001
0001	0000000000000010
0010	0000000000000100
0011	0000000000001000
0100	0000000000010000
0101	0000000000100000
0110	0000000001000000
0111	0000000010000000
1000	0000000100000000
1001	0000001000000000
1010	0000010000000000
1011	0000100000000000
1100	0001000000000000
1101	0010000000000000
1110	0100000000000000
1111	1000000000000000

Ερώτημα 8

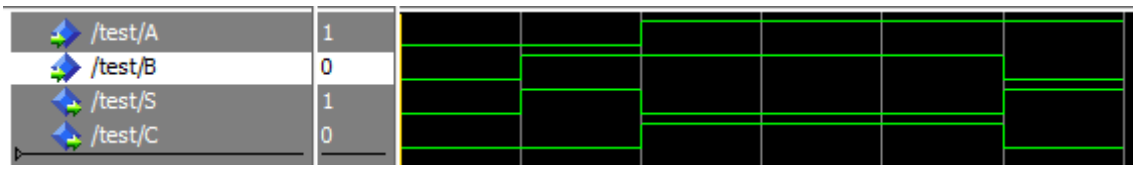
Κώδικας:

```
library ieee;
use ieee.std_logic_1164.all;

entity ha is port (
   A, B  : in  bit;
   S,C   : out bit);
end ha;

ARCHITECTURE dataflow OF ha IS
BEGIN
      s <= a xor b;
      c <= a and b;
END dataflow;
```

Wave



Πίνακας:

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Ερώτημα 9

Κώδικας:

```
library ieee;
use ieee.std_logic_1164.all;

entity fa is port (
  A, B, Cin : in  bit;
  S, Cout   : out bit);
end fa;

ARCHITECTURE dataflow OF fa IS
BEGIN
    S <= a xor b xor Cin;
    Cout <= (a and b) or (cin and (a xor b));
END dataflow;
```

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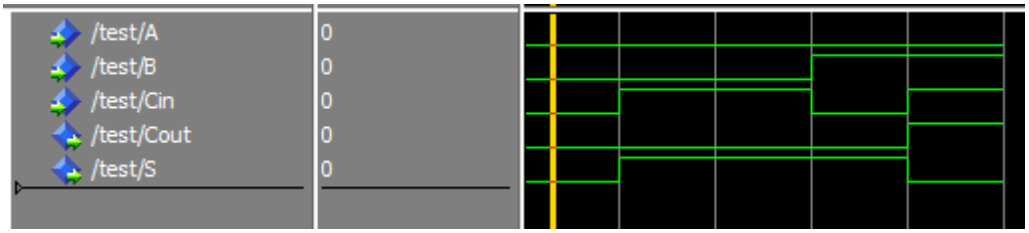

Πίνακας:

A	B	Cin	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Ερώτημα 10

Κώδικας:

```
library ieee;
use ieee.std_logic_1164.all;

ENTITY adder4 IS PORT (
 Cin  : IN  STD_LOGIC;
 X, Y : IN  STD_LOGIC_VECTOR(3 DOWNTO 0);
 S    : OUT STD_LOGIC_VECTOR(3 DOWNTO 0);
 Cout : OUT STD_LOGIC);
END adder4;
```

Wave

Πίνακας:

A	B	Cin	Cout	S
0000	0000	0	0	0000
1111	1111	0	1	1110
1111	1111	1	1	1111