

EE 209 Lab 5 - Enter the Code

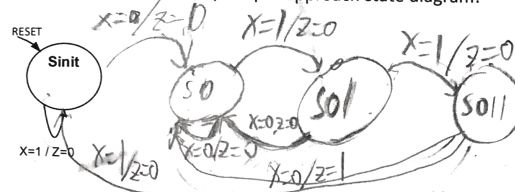
**6 Review / Lab Report**Name: Zhiyuan Ning

Score: \_\_\_\_\_

Due: \_\_\_\_\_

(Detach and turn this sheet along with any other requested work or printouts)

1. Reprint your Mealy-output approach state diagram:



2. Show your state code assignment for the states above.

Sinit	00
S0	01

S01	10
S011	11

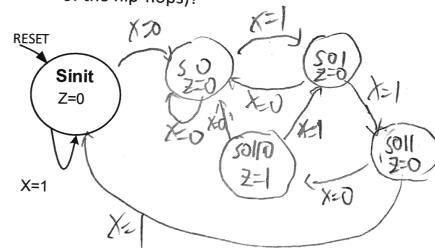
$$D_0 = \overline{X} + \overline{X}Q_0$$

$$Z = Q_0 \overline{X}$$

$$D_1 = \overline{Q_0} \overline{X} + Q_0 \overline{X}$$

3. How many states did your Mealy-style approach require?
- 4

4. Go back and consider a Moore-style output approach for Z. Draw the required state diagram (you don't actually have to design the logic for this approach, just the state diagram). How many flip-flops would this design require? What size K-map (3-var, 4-var, 5-var, etc.) would be required to find the logic for the D-inputs of the flip-flops?

How many flip-flops will this Moore-Design require? 3What size K-Maps (3, 4, 5-var, etc.) would your D-inputs require? 4

Turn in the following items:

- Completed seqdet.v and seqdet\_tb.v on our website
- The answers to the questions above on this page