Thomas Pickell

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in thomaspickell ○ ThomasPickle7

An Electrical and Computer Engineering student specializing in FPGA-based signal processing, high-frequency RF systems, and THz RADAR. Passionate about ensuring the mission-critical reliability and success of human spaceflight systems through rigorous testing, validation, and robust engineering. Seeking to apply advanced skills in system characterization and validation to a Fall 2025 internship focused on launch reliability at SpaceX.

Education

Rice University	Houston, TX	*August 2022 - Expected*
BS in Electrical and Computer Engineering (GPA: 3.6/4.0)		*May 2026*

- **Coursework:** Intro to Computer Vision, Optimization Concepts, Signals, Systems, and Transforms, Learning from Sensor Data, 2D-Materials and Devices, Imaging Optics, Physical Electronics

Academic and Research Experience

Research Intern, Notre Dame Wireless Institute	*May 2025 – Present*	*Notre Dame, IN*

- Architecting a robust FPGA-based data acquisition system on a PolarFire FPGA Fabric using Libero SoC, Verilog, C, and Shell scripting for the Radiohound RF sensor network.
- Increased the spectrum mapping sampling rate from 48MHz to 200MHz in initial testing (a 4x improvement), with a target of over 600MHz for high-fidelity data acquisition.

Research Assistant, Terahertz RADAR Lab	*March 2025 – Present*	*Houston, TX*

- Characterizing and repairing a 3.4THz RADAR system with the goal of designing an extremely high-resolution, reliable imaging system.
- Using a terahertz bolometer and an interferometry setup to perform precision alignment of the system's 12 Quantum Cascade Lasers (QCLs).
- Successfully documented and aligned 2 of the 12 QCLs, proving the viability and repeatability of the repair and alignment procedure.

Research Assistant, Rice Networks Group	*May 2024 – December 2024*	*Houston, TX*

- Engineered a robust localization algorithm for terahertz (THz) devices, achieving 2mm accuracy for precise receiver positioning—a critical requirement for identifiable low-fidelity terahertz signals.
- Wrote experiment automation scripts in Python, reducing data collection time by up to 75%.
- Presented the positioning algorithm design to engineers from the Army Research Lab and CISCO.

Personal Engineering Projects

16-bit FPGA CPU Implementation	*2023*

- Architected, implemented, and validated a 16-bit instruction set CPU, including a custom ALU, program counter, and register file, on an AMD Xilinx FPGA.
- Tested the CPU's internal function via rigorous timing analysis and verified operational reliability by successfully executing a recursive Fibonacci sequence calculation.

Technologies

Languages: Python, C, C++, Verilog, Java, Shell Scripting, TCL, HTML/CSS

Hardware & RF: THz Systems, RF Electronics/RADAR, FPGA, PolarFire SoC, Laser Alignment, Terahertz Bolometer, Interferometry, Oscilloscope, Network Analyzer, PID Controls

EDA & Simulation: Libero SoC, Xilinx Vivado, Altium, KiCAD, LTSpice, Solidworks, Onshape

Software & Tools: Git, Linux, JSON, Microsoft Office