CoreAXI4DMAController User Guide

Introduction (Ask a Question)

CoreAXI4DMAController is an AXI4 Direct Memory Access (DMA) controller designed to perform memory to memory style DMA transfers in an AXI system. The core provides in-built flow control techniques to ensure that the bandwidth of the AXI interface is optimally utilized. In addition, the core provides a bridge to AXI4 memory-mapped targets for AXI4-Stream initiators. CoreAXI4DMAController allows efficient data transfer between memory and AXI4-Stream target peripherals, which helps to improve the system performance. This core offers a range of adjustable parameters, including data width, burst size, transfer mode, address alignment, and buffer size, to ensure compatibility and optimal performance within the specific demands of the intended application and system architecture.

CoreAXI4DMAController Summary

Core Version	This document applies to CoreAXI4DMAController v2.2
Supported Device Families	• PolarFire® SoC • PolarFire • RT PolarFire® • RTG4™ • IGLOO® 2 • SmartFusion® 2 **Note:** For additional information, visit the CoreAXI4DMAController product page.
Supported Tool Flow	Requires Libero® SoC v8.6 or later releases.
Supported Interfaces	• **AXI4 Stream**: Dedicated for the core to receive stream data from an external AXI4-Stream initiator interface • **AXI4 Lite**: Dedicated to access configuration of control and status registers inside the core
Licensing	No license is required for the use of this core. Complete RTL source code is provided for the core and testbenches.
Installation Instructions	CoreAXI4DMAController must be installed to the **IP Catalog** of Libero SoC automatically through the IP Catalog update function. Alternatively, CoreAXI4DMAController could be manually downloaded from the catalog. Once the IP core is installed, it is configured, generated, and instantiated within SmartDesign for inclusion in the project.
Device Utilization and Performance	A summary of utilization and performance information for CoreAXI4DMAController is listed in 8. Device Utilization and Performance.

CoreAXI4DMAController Change Log Information

This section provides a comprehensive overview of the newly incorporated features, beginning with the most recent release. For more information about the problems resolved, see the 7. Resolved Issues section.

CoreAXI4DMAController v2.2	What's New	• Resolved the AXI interconnect issue when crossbar set for 64-bit accessing CoreAXI4DMAController
CoreAXI4DMAController v2.1	What's New	• Combinational loops when stream support is enabled

Table of Contents

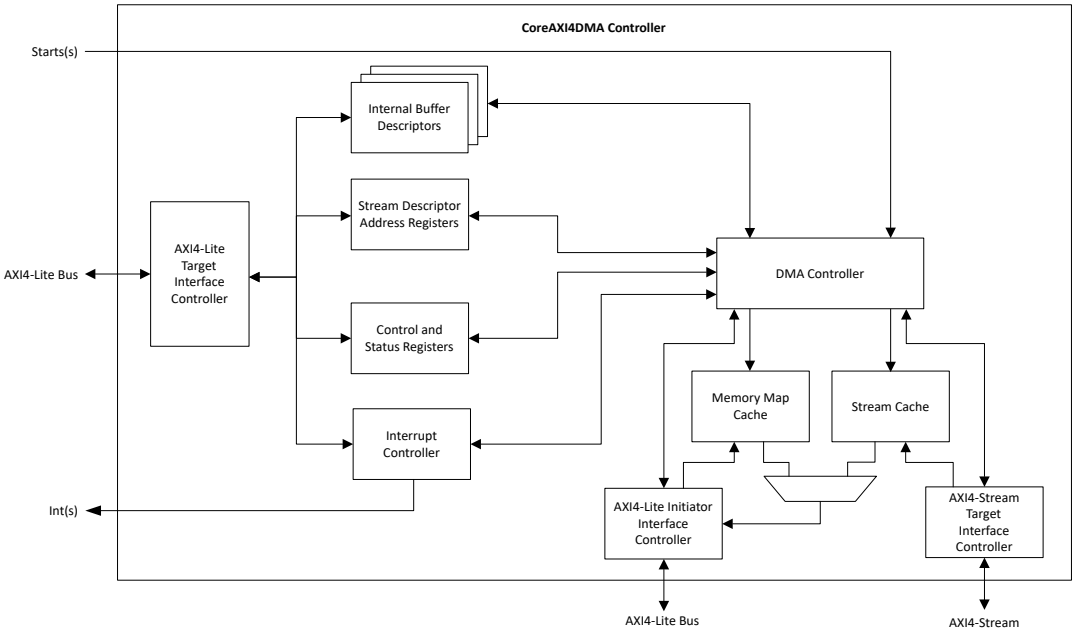
1. Functional Description (Ask a Question)

This section discusses the functional description of CoreAXI4DMAController.

1.1 Architecture (Ask a Question)

The following figure shows a high-level view of the internal architecture of the CoreAXI4DMAController.

Figure 1-1. CoreAXI4DMAController Internal Architecture



1.1.1 AXI4-Lite Target Interface Controller (Ask a Question)

The AXI4-Lite target interface controller is responsible for translating AXI4-Lite write and read transactions into the internal register interface protocol. This provides access to the internal registers (including buffer descriptors) from an AXI4-Lite initiator, allowing AXI4-Lite initiators to initiate and configure DMA transfers.

1.1.2 Control and Status Registers (Ask a Question)

The Control and Status Registers block contains the Version register to relay the major, minor, and the build number of the core to the controlling initiators along with providing a register for initiating DMA operations.

1.1.3 Buffer Descriptors (Ask a Question)

The internal buffer descriptors contain the information required to configure a DMA operation, including the start and destination addresses, the type of DMA operation and the number of bytes to be transferred. The number of internal descriptors instantiated is configurable through the parameter, in the range 4–32. Internal descriptors are stored in LSRAM and can be chained together to perform scatter-gather or circular buffer DMA operations. In addition, internal descriptors are used to point to external descriptors.

1.1.4 DMA Controller (Ask a Question)

CoreAXI4DMAController provides a dedicated external start bit for each internal buffer descriptor (maximum of 32 Bits) which allows DMA operations already configured in the core's internal buffer

descriptors to be kicked off from a simple fabric controller. Alternatively, DMA operations are kicked off by writing to the corresponding bit in the Start Operation register.

Start bits are queued and processed using a round-robin arbiter kicking off one operation per clock cycle. This loads the DMA requests into the DMA controller with the DMA operation commencing once control is granted to that operation on the AXI4 initiator interface. This setup allows multiple operations to be kicked off in a single control initiator write preventing conflicts arising from multiple internal and external start bits being asserted in the same cycle.

The arbiter decides the DMA operation that gets serviced on the AXI4 interface. Buffer descriptors are assigned a fixed priority upfront. As the largest permitted DMA operation is 8 MB, DMA operations are divided into multiple transactions with the maximum DMA transaction size determined by the priority of the buffer descriptor to which it is associated and the maximum number of beats permitted for this priority level, configured through a parameter. As AXI4 transactions must run to completion once initiated, this mechanism allows transactions with higher priorities to have more bandwidth whilst forcing transactions with lower priorities to enter back into the arbitration sequence more frequently to check for higher priority DMA operations in the queue. Round-robin arbitration is performed to service requests with the same priority level. No bandwidth is allocated to the descriptors with a lower priority level if a higher priority descriptor is being processed. The maximum transaction size for the highest level of priority is 4 KB to prevent AXI transactions from crossing 4 KB address boundaries.

When enabled, AXI4-Stream operations shares the highest priority level, priority level 0. It is possible to associate no internal buffer descriptors with priority level 0 at configuration time to allocate the entire bandwidth of the AXI4 DMA interface to AXI4-Stream operations when they exist. Otherwise, AXI4-Stream to memory map forwarding operations are interleaved with operations of internal descriptors at the highest priority level.

1.1.5 Memory Map Cache (Ask a Question)

CoreAXI4DMAController contains two 4 KB SRAM caches to allow the core to complete the forward part of an AXI4-memory map store and forward operation whilst performing the store element of the next store and forward operation. The DMA Controller block is responsible for switching between the internal caches autonomously in a round-robin fashion.

1.1.6 Stream Cache (Ask a Question)

If the AXI4-Stream configuration is selected, the core contains two additional 4 KB store caches allowing stream data received through the AXI4-Stream interface to be buffered before initiating multi-beat AXI4 forward transactions on the AXI4 interface. This allows stream operations to be received asynchronously to other DMA operations as the AXI4-Stream transfer is initiated by the AXI4-Stream initiator. The DMA Controller block is responsible for switching between the internal stream caches autonomously in a round-robin fashion.

1.1.7 Interrupt Controller (Ask a Question)

CoreAXI4DMAController allows users to enable multiple interrupt outputs and to associate each interrupt output with one or more internal buffer descriptors. The Interrupt Controller block is responsible for routing the events of each descriptor to the associated interrupt output. A configurable depth queue for each interrupt output is contained within this block to allow DMA operations to take place whilst waiting on the Control initiator to handle and clear previous interrupt events. If an interrupt queue backs up all operations of descriptors associated with this interrupt are suspended until space is freed in the interrupt queue by the Control initiator. DMA operations of other descriptors not associated with this interrupt queue will still be processed. This setup facilitates multiple processors to use the DMA controller concurrently.

Important: The interrupt association for an external descriptor is inherited from the previous internal descriptor in the chain. Interrupt events of Stream descriptors are always associated with Interrupt 0.

1.1.8 AXI4 Initiator Interface Controller (Ask a Question)

The AXI4 initiator interface controller is responsible for performing the DMA operation outlined by the DMA Controller block using AXI4 write and read transactions. This block returns a flag to the DMA controller when the requested store and forward operation is completed. If an AXI4 error is returned by a downstream target during the read/store operation before the write/forward operation for that operation has commenced, the AXI4 Initiator Interface Controller continues the read/store to completion and reports the error to the control initiator without performing the write.

1.1.9 AXI4-Stream Target Interface Controller (Ask a Question)

The AXI4-Stream target interface controller provides a unidirectional bridge to the AXI4 memory map for AXI4 stream initiators. The AXI4-Stream target interface controller notifies the DMA Controller that a stream operation has commenced and of the position of the external descriptor in AXI4 memory describing the AXI4-Stream operation. Caching of the stream data in one of the internal 4 KB stream caches is performed in parallel to the fetching of the stream descriptor over the AXI4 DMA interface and completion of the previous memory mapped or stream DMA operation.

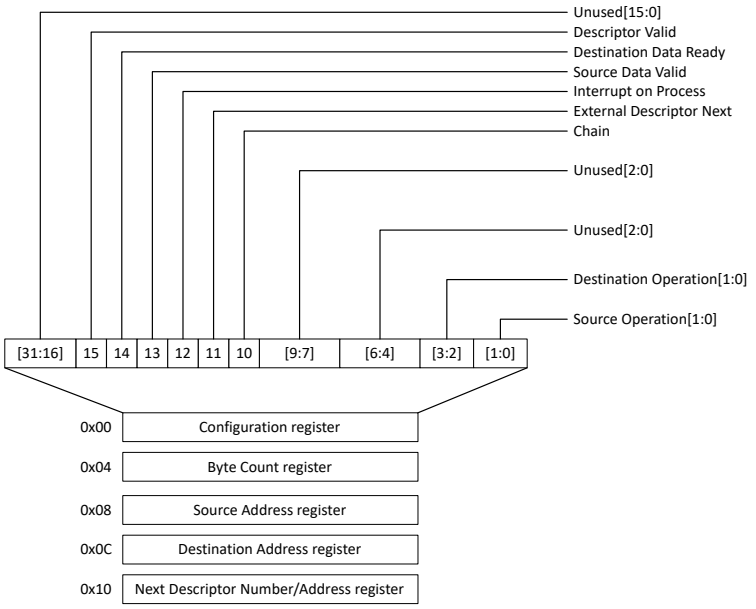
1.2 Buffer Descriptors (Ask a Question)

This section discusses the types of buffer descriptors of the CoreAXI4DMAController.

1.2.1 Internal Descriptor Support (Ask a Question)

Internal descriptors are implemented using LSRAM with the number of internal descriptors configurable through the parameter in the range 4–32. Each internal descriptor has the ability to operate as a competing DMA channel. The format of an internal descriptor is as shown in the following figure.

Figure 1-2. Internal Descriptor Format



Chaining of internal descriptors is supported to perform scatter-gather DMA operations where data is collected from one or more contiguous or non-contiguous locations and forwarded to one

or more contiguous or non-contiguous locations. Each descriptor or chain of descriptors can be configured to perform repetitive cyclic operations. For information on performing such operations, see Scatter-Gather section and Cyclic Operations section. Fetching of internal descriptors is performed in parallel to DMA data transferring and has no impact on DMA throughput performance provided that the operation described by the current descriptor being operated on is sufficiently large.

At the time of instantiation, the priority level and interrupt output associated with operations of any internal descriptor must be configured through parameter.

Important: Each internal descriptor can operate as a competing DMA channel provided that it's not chained with other internal descriptors.

1.2.2 External Descriptor Support (Ask a Question)

External descriptors are defined in the AXI4 address space and fetched over the AXI4 DMA interface. The structure of an external descriptor takes the same format as an internal descriptor.

External descriptors are pointed to using an internal descriptor with the Chain and External Descriptor bits set in the internal descriptor's Configuration register by passing the base address of the external descriptor to the Next Descriptor Number or Address register. Fetching of external descriptors over the DMA interface has a minor impact on overall DMA throughput performance provided that DMA operations are sizeable.

Chaining of external descriptors is supported through this mechanism. An external descriptor is chained back to an internal descriptor by setting the Chain bit with the External Descriptor bit cleared in the external descriptor's Configuration register and passing the internal descriptor number to the Next Descriptor Number or Address register. Cyclic operations of external descriptors are achieved linking the last external descriptor in the chain back to the first internal descriptor.

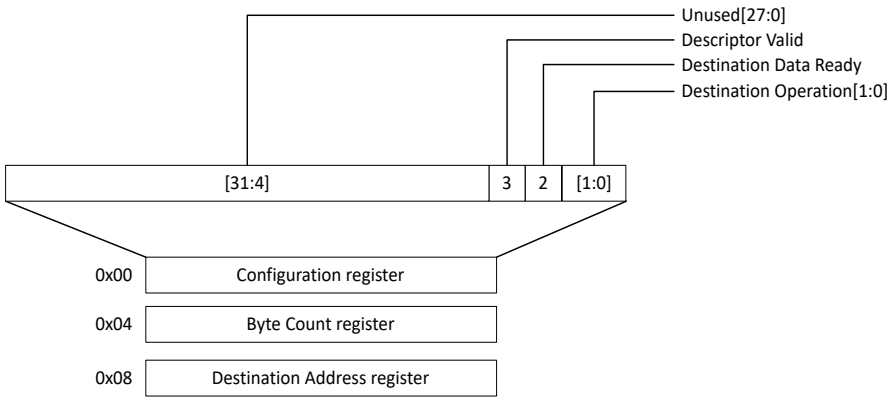
The priority level and interrupt association of an external descriptor is inherited from the previous internal descriptor in the chain.

Important: The address of the Configuration register of an external descriptor must be aligned to the bus width of the AXI4 DMA interface configured through the AXI_DMA_DWIDTH parameter.

1.2.3 Stream Descriptor Support (Ask a Question)

Stream descriptors describe the AXI4-Stream transaction that is received from the AXI4-Stream initiator over the AXI4-Stream target interface. The TDEST signal of the stream interface is used to select the CoreAXI4DMAController Stream Descriptor Address register that points to the stream descriptor describing the AXI4-Stream transaction that is in progress. The address of the stream descriptor must be written to the appropriate Stream Descriptor Address register prior to the AXI4-Stream transaction being initiated, along with the prior existence of the valid stream descriptor in the AXI4 DMA address space. The format of stream descriptors is as shown in the following figure.

Figure 1-3. Stream Descriptor Support



The Destination Data Ready bit is used by control initiators to denote when a buffer has been allocated for the reception of the stream data in the AXI4 memory-map address space. The first 4 KB of the stream transaction is cached whilst the descriptor is being fetched. No further transfers in the AXI4-Stream transaction are acknowledged until the Destination Data Ready bit is asserted, allowing the forwarding operation to the AXI4 memory map to commence when allocated bandwidth by the DMA arbiter.

If the Descriptor Valid bit of the stream descriptor that the AXI4-Stream transaction relates to is not set when the stream transaction is initiated and the descriptor is fetched, an invalid descriptor interrupt event is triggered.

Stream descriptors are fetched over the AXI4 DMA interface when TVALID is asserted for the first transfer in the AXI4-Stream transaction once the current AXI4 or AXI4-Stream transaction completes. The maximum transfer size of a single stream transaction is 8 MB.

Important: The address of the Configuration register of a stream descriptor must be aligned to the bus width of the AXI4 DMA interface configured through the AXI_DMA_DWIDTH parameter. The bus width of the AXI4 DMA and stream interfaces are synonymous.

1.2.4 Descriptor Management (Ask a Question)

As external start inputs exist for each internal descriptor and descriptors are chained together, it is impossible for firmware to determine if a descriptor is currently involved in a DMA operation as it is initiated by a separate or external process. For this reason, it is advised to keep hardware-initiated DMA operations in separate descriptors to dynamically configured, firmware initiated operations. Once a descriptor is initialized by firmware during initial configuration, the Descriptor Valid bit must be set in the descriptor's Configuration register.

Important: If you use a UIC script to initialize internal descriptors in LSRAM, the Descriptor Valid bit needs to be set through firmware due to the order in which the UIC script writes the data into LSRAM (writes the Configuration register first, followed by the Byte Count register, hence the Descriptor Valid bit is cleared automatically by the DMA Controller).

If the start input associated with a descriptor is tied off, then it is permitted for the firmware to modify the descriptor contents on the fly, provided that no firmware initiated operations are being processed on the particular descriptor or which include the descriptor in a chain or cyclic buffer. Once any field in the descriptor is written to, the Descriptor Valid bit is automatically cleared by

the CoreAXI4DMAController. It is the responsibility of the firmware to set this bit only when the descriptor has been reconfigured.

If a DMA operation is initiated through an external start input assertion or a write to the Start Operation register on an uninitialized descriptor, an interrupt is generated reporting an invalid descriptor error.

1.3 Flow Control/Throttling (Ask a Question)

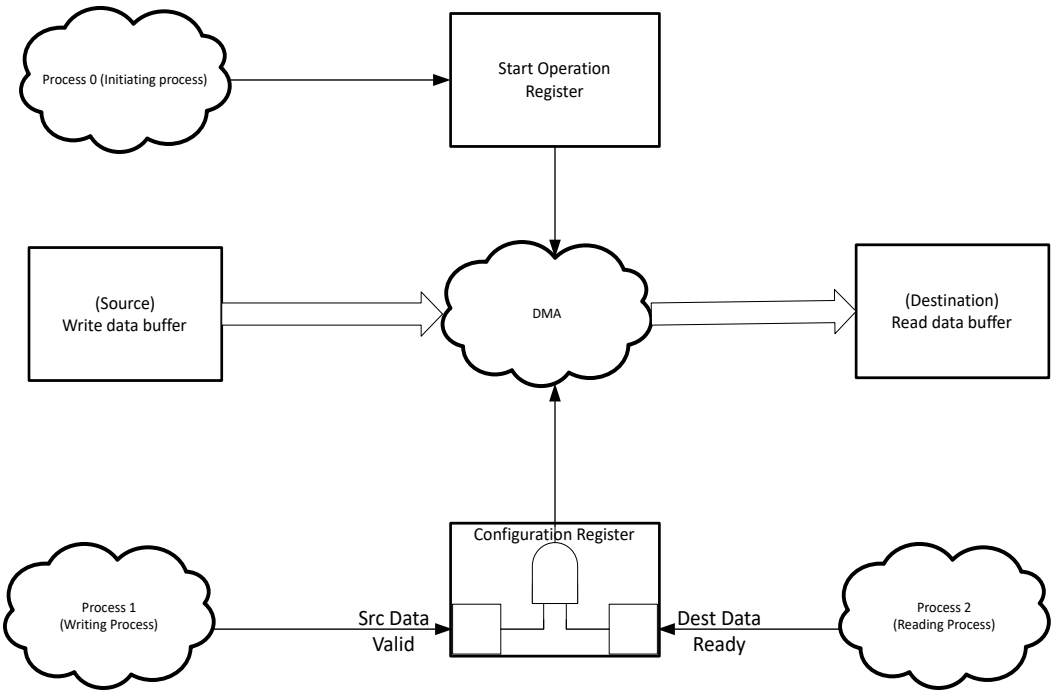
Once an AXI transaction is initiated by an initiator sending the write/read address, it must run to completion. A target forces the initiator to wait before sending additional write data or receiving read data using the valid-ready flow control signals built into the AXI4 protocol. However, initiators cannot determine up-front that a target is unable to handle more data and thereby may hog the bus.

To prevent the CoreAXI4DMAController relying on AXI targets always having data in place and room for write data, CoreAXI4DMAController implements separate Source Data Ready and Destination Data Valid bits in both internal and external descriptors to support firmware flow control management. In order for a descriptor to be operated on, firmware must set both flow control bits whether or not the descriptor is part of a descriptor chain.

Important: Both the Source Data Valid and Destination Data Ready flow control bits must be set again every time that a descriptor is processed as part of a cyclic chain.

To support the separation of the application into multiple processes, a descriptor is kicked off in the Start Operation register before either or both flow control bits are set, but no bandwidth is granted to this descriptor until both bits are subsequently set either together or separately in the same process or in a separate processes altogether. The conceptual flow control management of CoreAXI4DMAController is as shown in the following figure.

Figure 1-4. Multi Process Flow Control Management



The CoreAXI4DMAController automatically clears the Source Data Valid and Destination Data Ready flow control bits for both internal and external descriptors each time a descriptor completes the operation.

If either the Source Data Valid or Destination Data Ready flow control bits are low when an external descriptor is fetched, the external descriptor's Configuration register is fetched again over the AXI4 interface until both bits are detected high every time that this DMA channel is apportioned a time slot by the DMA arbiter. The allotted bandwidth is passed-over, if either bit remains low when fetched. No DMA transfer is performed whilst arbitration is re-entered immediately.

Stream descriptors support a Destination Data Ready bit for flow control purposes. As with internal and external descriptors, the Destination Data Ready bit is cleared by the DMA controller when the AXI4-Stream transaction data described in the stream descriptor has been forwarded to the AXI4 memory-map address space. The Destination Data Ready flow control bit is fetched every time that the stream descriptor is allocated bandwidth by the DMA arbiter in the manner described for the preceding external descriptors.

1.4 DMA Operations (Ask a Question)

This section discusses the DMA operations.

1.4.1 Chain Operations (Scatter-Gather) (Ask a Question)

Chain operations are typically used to implement scatter-gather DMA operations where data is collected from multiple non-concurrent memory blocks and spread to a number of concurrent or non-concurrent locations. A chain can be formed using a single internal descriptor and multiple external descriptors, multiple internal descriptors or using a mix of internal and external descriptors. The starting point for a descriptor chain must be an internal descriptor.

To configure a chain operation, create a number of buffer descriptors with the Chain bit set in each buffer descriptor except the last. The Next Descriptor field in all buffer descriptors other than the last must point to the next descriptor in the chain. This field is ignored for the last descriptor in the chain (denoted by a descriptor without the Chain bit set). The External Descriptor Next bit is used to denote the type of the next descriptor in the chain. Chain operations can be initiated by writing to the internal start bit or by triggering the start input signal associated with the first descriptor in the chain.

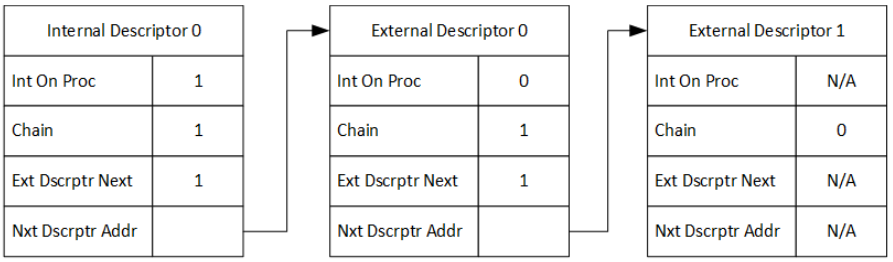
If a chain operation is configured with all descriptors having the Interrupt on Process bit cleared, an interrupt is only generated on error or when the operation described by the last descriptor in the chain has completed.

Alternatively, if the Interrupt on Process bit is set for one or more descriptors in a chain, an interrupt is generated when the operation described in each descriptor with its Interrupt on Process bit set is completed, however, this will not stall the next descriptor in the chain from being processed by the DMA controller, unless the associated interrupt queue has backed-up.

Important: Descriptor chaining must only be performed with buffer descriptors of the same priority level.

The following figure shows the format of one possible descriptor chain. Notice that the Chain bit is set for every descriptor other than the last. In this case, the Interrupt on Process bit is set for the first internal descriptor in the chain, Internal BD0 and External BD1. This generates an interrupt when each of these descriptors are processed. No interrupt is generated for the processing of External BD0. An interrupt is always generated when the last descriptor in a chain is processed, regardless of the Interrupt on Process configuration.

Figure 1-5. Example Descriptor Chain

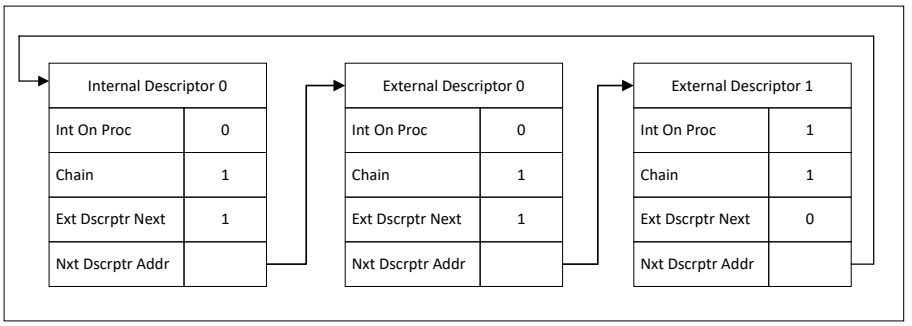


CoreAXI4DMAController supports a source address and destination no-op feature to allow an internal descriptor to point at an external descriptor without the internal descriptor performing a DMA data transfer. Refer to the Source and Destination Operation fields of the descriptor's Configuration register.

1.4.2 Cyclic Operations (Ask a Question)

Cyclic operations can be set up by creating a number of buffer descriptors with the Chain bit set in each buffer descriptor. The Next Descriptor field for each descriptor must be assigned the number corresponding to the next descriptor in the chain. Unlike standard chain operations, the last descriptor must have the Chain bit set and must point back to the first descriptor in order to make the operation cyclic. The cyclic operation is initiated by writing to the associated start bit for the first buffer descriptor in the cyclic chain. Every time a descriptor has been processed, the flow control bits must be reset, provided that there is valid data at the source and room for data at the destination. If a descriptor is reached without one or both flow control bits set, the DMA operation is passed over in the DMA arbiter, allowing other DMA operations to proceed while waiting on buffer allocation.

Figure 1-6. Example Cyclic Descriptor Chain



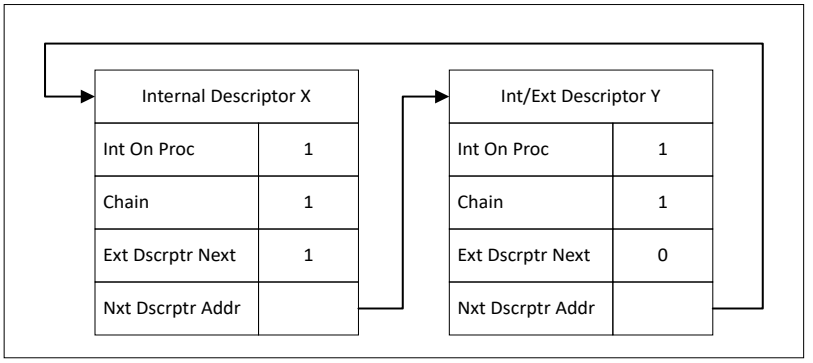
Cyclic operations are terminated by clearing the Chain bit in the descriptor to stop at when next reached. When this descriptor is reached and the DMA operation within the descriptor has been carried out, an interrupt is asserted signifying the completion of the DMA cyclic operation. If external buffer descriptors are included in a descriptor chain, the cycle is stopped on an internal descriptor from the Control interface of CoreAXI4DMAController. The chain terminates on an external descriptor if the control initiator clears the Chain bit in the external descriptor's Configuration register in the AXI4 memory map address space.

Ensure that the Interrupt on Process bit is asserted for at least the last or tail descriptor in a descriptor chain. This provides notice to the firmware application that the chain is being processed. Also set the Source Data Valid and Destination Data Ready flow control bit for each descriptor in the chain before another complete cycle of the chain takes place. The DMA arbiter allows the DMA transfer to continue on each descriptor in the chain provided that both flow control bits are set and that the descriptor is valid. The status of the next descriptor's flow control bits will not impact the current descriptors service.

1.4.2.1 Ping-Pong (Ask a Question)

Support for ping-pong cyclic DMA operations where data is read from one location and written to two or more memory buffers with an interrupt generated every time that a buffer is filled is provided through use of descriptor chaining and the Interrupt on Process bit within buffer descriptors. The Interrupt on Process bit causes an interrupt to be raised every time that a descriptor is processed. This feature is supported for both internal and external buffer descriptors. The resetting of the data valid bit signifies that the buffer can be re-written to by the DMA controller.

Figure 1-7. Ping-Pong Cyclic Descriptor Chain

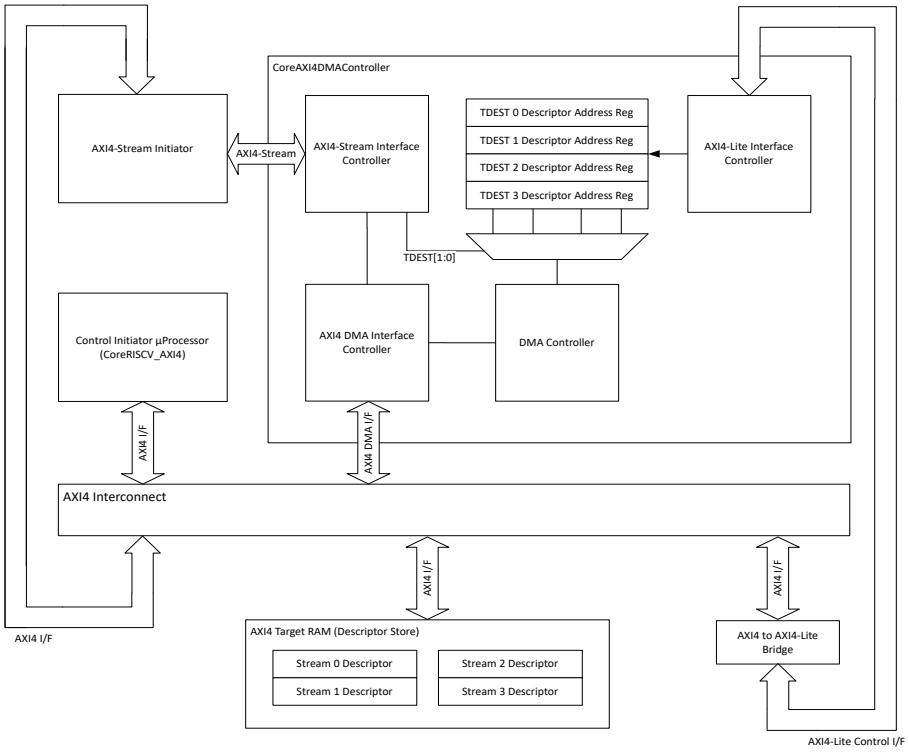


1.5 AXI4-Stream Bridge (Ask a Question)

In addition to AXI4 memory-map to memory-map DMA operations, the CoreAXI4DMAController provides a bridge to the AXI4 memory-map address space for AXI4-Stream initiators. Before a stream initiator initiates a stream transaction, the Control initiator must first write a description of the imminent AXI4-Stream transaction to the AXI4 memory map in the stream descriptor format.

Next, the address of the Configuration register of this stream descriptor needs to be written to the Stream Descriptor Address register within CoreAXI4DMAController associated with the TDEST signal value of the AXI4-Stream transaction. The TDEST signal provides destination routing information, used to multiplex between the four Stream Descriptor Address registers inside CoreAXI4DMAController, as shown in the following figure.

Figure 1-8. AXI4-Stream to AXI4 Memory Map Bridging



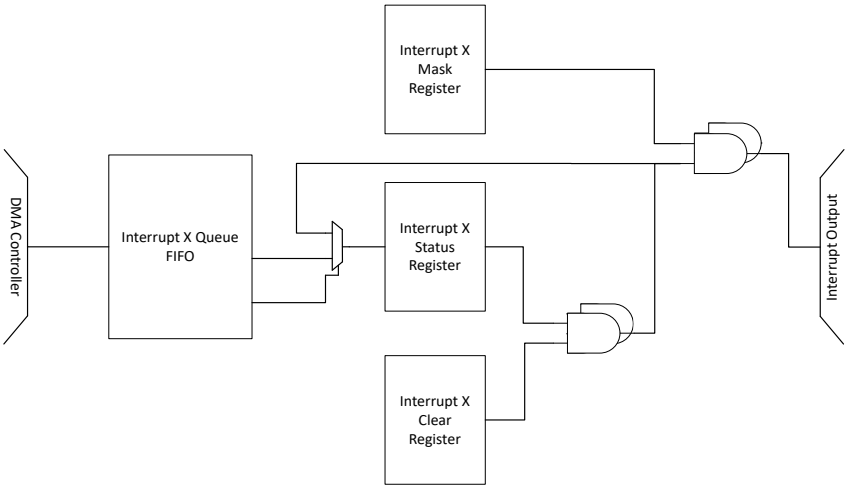
Once the first transfer of the AXI4-Stream transaction is received, the TDEST signal is used to select the Stream Descriptor Address register that contains the address of the stream descriptor describing the AXI4-Stream transaction. The stream descriptor is then fetched over the AXI4 DMA interface once the current AXI4 DMA transaction completes, while the stream data is cached in parallel. If the stream descriptor is valid, then it is loaded into the DMA Arbiter where it competes for bandwidth with other priority 0 requests. Otherwise, an invalid descriptor interrupt event is generated. Once the bandwidth is allocated to the stream request, if the Destination Data Ready flow control bit is set when the descriptor is fetched, the AXI4 memory map forward operation commences on the AXI4 DMA interface. If the flow control bit is not set, then the flow control bit is re-fetched from the stream descriptor over the AXI4 DMA interface until it is detected as begin set, at which point the AXI4 memory map forward commences.

Once the AXI4 memory-map forward related to the AXI4-Stream read is completed, an interrupt is generated on the Interrupt 0 output.

1.6 Interrupts (Ask a Question)

CoreAXI4DMAController provides a configurable number of interrupt outputs, each with independent status, mask and clear registers along with independent configurable depth queues. Descriptors must be associated with interrupt outputs at instantiation time. Multiple descriptors are associated with a single interrupt output. The following figure shows the logic implemented for each enabled interrupt output.

Figure 1-9. Interrupt Queue Logic



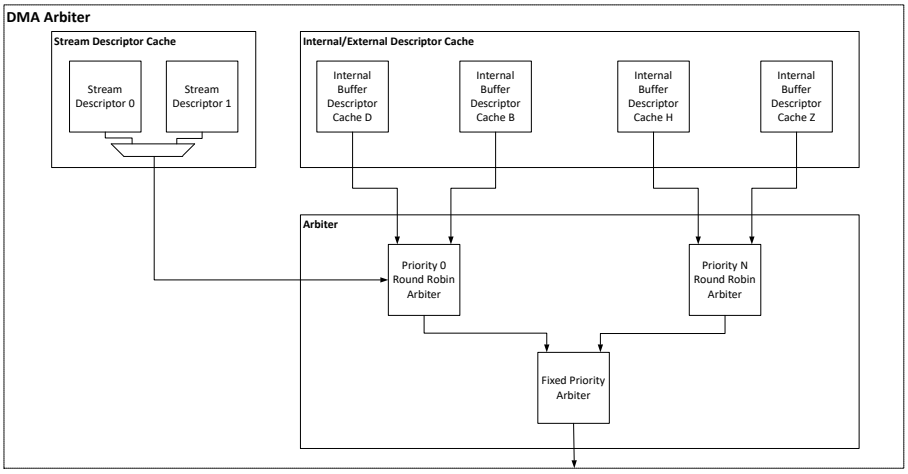
Interrupts are generated on error or completion. When configuring a descriptor, the Interrupt on Process field provides the user with a means to generate an interrupt every time that a particular descriptor is processed in a chain or circular buffer configuration, provided that this descriptor is not the last descriptor in the chain. DMA operations are not halted for interrupts of this type and proceeds in the background provided that the associated interrupt queue has not backed-up.

The current interrupt status remains valid in the Interrupt X Status register associated with the interrupt output until all unmasked bits (masked-off using the Interrupt Mask register) in the Interrupt Status register is cleared through the Interrupt Clear register.

1.7 Arbitration (Ask a Question)

CoreAXI4DMAController supports fixed priority arbitration between multiple priority levels. If multiple requests exist of the same priority level, round-robin arbitration is performed between these requests. Higher priority requests are allowed to perform larger AXI4 burst transfers. This forces faster re-entrance into the arbitration logic by lower priority requests to ensure that higher priority requests are detected sooner.

Figure 1-10. Descriptor Arbitration



Important: No bandwidth is allotted to lower priority descriptor requests when a request from a higher priority descriptor with both its flow control bits set exists.

As, a total transfer size of 8 MB is permitted for an operation of a single descriptor, DMA operations are divided into multiple AXI4 transactions, with a maximum permitted transaction size of 4 KB to provide AXI4 boundary protection. Access is re-evaluated every time that an AXI4 transaction completes. If multiple large descriptor requests of the same priority level exist, then AXI4 transactions of each descriptor are interleaved in a round-robin fashion.

Important: CoreAXI4DMAController does not support interleaving of transfers within AXI4 transactions (xID signal unused). Only 1 descriptor is serviced per AXI4 transaction.

When enabled, the AXI4-Stream requests are interleaved with operations of the highest priority level, priority 0. If the performance of the AXI4-Stream initiator is paramount, no internal descriptors must be assigned priority 0. Priority association can be done at instantiation time to allocate the entire bandwidth of the AXI4 memory map interface to the AXI4-Stream operation. Unlike standard AXI4 DMA operations which enter back into the arbitration algorithm every time that an AXI4 transaction is performed provided that the destination transaction does not span a 4 KB boundary, which is not aligned to the source address (in which case, the core performs multiple AXI writes to empty the read cache that was filled by a single AXI read transaction before entering back into arbitration), whether or not the AXI4 transaction completely services the descriptor request, AXI4-Stream operations do not enter back into arbitration until the entire stream request has been serviced, even if this requires multiple AXI4 write transactions to prevent crossing a 4 KB boundary in a sequential transaction and to empty the stream read cache.

Priority level assignment must be performed in a descending, contiguous fashion. If a priority level is enabled with no descriptors allocated to it (apart from priority 0 when Stream support is enabled), the underlying logic related to this priority level is removed from the core. For this reason, no priority level must be enabled without descriptors allocated to it when lower priority levels are enabled with descriptors allocated to them.

To reduce the setup overhead on DMA transfers, the core allows multiple descriptors to be kicked off in a single write to the Start Operation register. It is difficult to determine the order in which DMA operations take place in as the core has the facility for multiple start bits to get kicked off in the same cycle, each with shared or separate priority levels. All start bits are maintained in an internal register and loaded into the descriptor cache using a non-weighted round-robin arbiter, with only one start bit loaded in any given cycle. The weighted round-robin DMA arbiter then reads out of the descriptor cache and fills a two-stage pipeline to ensure that DMA transfers happen in a back-to-back fashion on the DMA interface and to ensure that read-ahead is performed for the next DMA operation as there are two internal caches. To ensure that DMA operations happen in order, either wait for an interrupt to be received on the first operation before kicking off the next operation, else form a chain with the descriptors of interest.

1.8 AXI Transactions (Ask a Question)

The source and destination addresses of all DMA operations must be aligned to AXI bus width instantiated.

Important: CoreAXI4DMAController does not perform unaligned AXI transactions and data realignment.

The size of the AXI transaction generated is dependent upon the width of the AXI DMA interface instantiated. CoreAXI4DMAController generates transactions with the AxSIZE field set at the maximum for the instantiated bus width exclusively.

The length of the AXI transaction is dependent upon the priority level of the descriptor which the AXI transaction is related to, the maximum permitted burst size at this priority level and the

source address, destination address, and the number of bytes in the DMA operation. If the store DMA operation spans a 4 KB boundary, CoreAXI4DMAController generates multiple shorter read transactions to prevent crossing the 4 KB boundary in a sequential transfer and vice versa for the forward transactions if the forward DMA operation spans a 4 KB boundary. Arbitration is performed on completion of each read transaction to determine if a higher priority requests exists or if there are other requests at this priority level that need to be serviced. The last transfer of the last transaction of a DMA operation is narrowed by the way of the AXI write strobes to provide N-byte DMA transfer support.

A single AXI read transaction results in multiple AXI write transactions, if the source operation is confined within a 4 KB slot and the destination operations spans a 4 KB boundary.

The core supports DMA read ahead to read in the next data to the internal cache whilst the previous write operation is completing. This increases the throughput of the AXI interface significantly for queued AXI DMA operations in busy AXI systems. AXI outstanding address transactions are not generated by CoreAXI4DMAController.

1.9 AXI4-Stream Transactions (Ask a Question)

CoreAXI4DMAController supports AXI4-Stream transactions where each bit of TSTRB mirrors TKEEP, indicating either data or null bytes. Position bytes occur when a TKEEP bit is asserted and the corresponding TSTRB bit is de-asserted. Position bytes are not supported by CoreAXI4DMAController.

The core expects all AXI4-Stream transactions to start from an address aligned to bus width, set through the AXI_DMA_DWIDTH parameter. The first transfer in the transaction cannot be unaligned by using the TKEEP and TSTRB.

In addition, the core permits the last transfer in an AXI4-Stream transaction to be narrow by keeping the TKEEP and TSTRB bits low for the associated byte lanes, making N-byte AXI4-Stream to AXI4 memory map bridging possible. An example of this would be where TKEEP and TSTRB are both 0x7F for the last transfer in the transaction and 0xFF for all other transfers in the transaction on a 64-bit bus.

It is expected that all TSTRB and TKEEP bits are asserted for every transfer other than the last transfer in an AXI4-Stream transaction. Sparse strobe assertion is not supported where TSTRB and TKEEP are both 0x55 for instance.

Important: AXI4 Stream Transactions must be performed whenever there is no pending request for memory map to memory map data transfer and vice-versa.

1.10 Cache Coherence (Ask a Question)

Data integrity issues arise where a DMA read is performed on a shared, cacheable memory where the cached memory contents has been updated but not yet written back to memory. To cover such an event, the application must ensure that the contents of the cache is written back to memory before kicking of a DMA read operation in a cacheable region. Processor operations to this memory space must be suspended until the DMA read has completed.

Similarly, where a DMA write is performed on cacheable memory, the application needs to ensure that the contents of the cache is flushed and refilled to prevent the processor from operating on out-of-date data once the memory has been written via the DMA operation. Processor operations to this memory space must be suspended until the DMA write has completed.

Important: Cache coherence is not handled by CoreAXI4DMAController and remains the responsibility of the Firmware application.

2. CoreAXI4DMAController Parameters and Interface Signals (Ask a Question)

This section discusses the parameters in the CoreAXI4DMAController Configurator settings and I/O signals.

2.1 Configuration of GUI Parameters (Ask a Question)

There are a number of configurable options, which are applied to CoreAXI4DMAController (as shown in the following table). If a configuration other than the default is required, then the configuration dialog box in SmartDesign must be used to select appropriate values for the configurable options.

Important: The Parameter Name column in the following table shows the actual parameter names used in RTL. The Description column starts with the parameter names as they appear in the CoreAXI4DMAController Configurator.

Table 2-1. CoreAXI4DMAController Configuration Options

Parameter Name	Valid Range	Default	Description
ECC	0 or 1	0	**Notes:** This feature is only valid for RTG4™, PolarFire®, and PolarFire SoC device families. For more information on ECC Flags (SB_CORRECT and DB_DETECT), see Interrupt Status Register description. Error Correcting Code: • 0: ECC is disabled for uSRAM or LSRAM RAM • 1: ECC is enabled for LSRAM RAM
AXI4_STREAM_IF	0 or 1	0	AXI Stream target interface. Provides bridge for AXI4-Stream initiators to access the AXI4 memory map.
AXI_DMA_DWIDTH	32, 64,128, 256, 512	32	Data width of the AXI DMA and optional AXI4-Stream interfaces.
ID_DWIDTH	1–8	1	ID width for AXI DMA transactions. ID is always be driven out as zeros (unused – no transaction interleaving support).
NUM_PRI_LVLS	1–8	1	Number of fixed priority levels supported
PRI_0_NUM_OF_BEATS	1, 4, 8, 16, 32, 64, 128, 256	256	Maximum number of transfers in an AXI transaction of this priority level
PRI_1_NUM_OF_BEATS	1, 4, 8, 16, 32, 64, 128, 256	128	Maximum number of transfers in an AXI transaction of this priority level. Must be ≤ PRI_0_NUM_OF_BEATS
PRI_2_NUM_OF_BEATS	1, 4, 8, 16, 32, 64, 128, 256	64	Maximum number of transfers in an AXI transaction of this priority level. Must be ≤ PRI_1_NUM_OF_BEATS
PRI_3_NUM_OF_BEATS	1, 4, 8, 16, 32, 64, 128, 256	32	Maximum number of transfers in an AXI transaction of this priority level. Must be ≤ PRI_2_NUM_OF_BEATS
PRI_4_NUM_OF_BEATS	1, 4, 8, 16, 32, 64, 128, 256	16	Maximum number of transfers in an AXI transaction of this priority level. Must be ≤ PRI_3_NUM_OF_BEATS
PRI_5_NUM_OF_BEATS	1, 4, 8, 16, 32, 64, 128, 256	8	Maximum number of transfers in an AXI transaction of this priority level. Must be ≤ PRI_4_NUM_OF_BEATS
PRI_6_NUM_OF_BEATS	1, 4, 8, 16, 32, 64, 128, 256	4	Maximum number of transfers in an AXI transaction of this priority level. Must be ≤ PRI_5_NUM_OF_BEATS

.....continued

Parameter Name	Valid Range	Default	Description
PRI_7_NUM_OF_BEATS	1, 4, 8, 16, 32, 64, 128, 256	1	Maximum number of transfers in an AXI transaction of this priority level. Must be ≤ PRI_6_NUM_OF_BEATS
NUM_OF_INTS	1–4	1	Number of interrupt outputs enabled
INT_0_QUEUE_DEPTH	1–8	1	Number of interrupt events that are queued for the interrupt 0 output
INT_1_QUEUE_DEPTH	1–8	1	Number of interrupt events that are queued for the interrupt 1 output
INT_2_QUEUE_DEPTH	1–8	1	Number of interrupt events that are queued for the interrupt 2 output
INT_3_QUEUE_DEPTH	1–8	1	Number of interrupt events that are queued for the interrupt 3 output
NUM_INT_BDS	4, 8, 16, 32	4	Number of internal buffer descriptors supported
DSCRPTR_0_PRI_LVL	0–7	0	Buffer Descriptor 0 priority level. Fixed priority level associated with operations of this descriptor.
DSCRPTR_0_INT_ASSOC	0–3	0	Buffer Descriptor 0 interrupt association. Associate interrupt events of this buffer descriptor with an interrupt output.
DSCRPTR_31_PRI_LVL	0–7	0	Buffer Descriptor 31 priority level. Fixed priority level associated with operations of this descriptor.
DSCRPTR_31_INT_ASSOC	0–3	0	Buffer Descriptor 31 interrupt association. Associate interrupt events of this buffer descriptor with an interrupt output.

Important: When ECC is enabled, the core generates all the memories into LSRAM.

2.2 Inputs and Outputs Signals (Ask a Question)

Signal descriptions for CoreAXI4DMAController are defined in the following table.

Table 2-2. CoreAXI4DMAController Input and Output Signals

Name	Width	Direction	Description
General Ports			
CLOCK	1	Input	Clock signal to all sequential elements within the core
RESETN	1	Input	Active-Low reset signal to all sequential elements within the core. Reset de-assertion must be synchronous to CLOCK rising edge as per AXI4 specification. This reset must be synchronized in the CLOCK clock domain externally.
AXI4-Lite Control Interface Ports			
CTRL_AWVALID	1	Input	Write address valid Indicates that the control initiator is presenting valid write address information.
CTRL_AWREADY	1	Output	Write address ready Indicates that the CoreAXI4DMAController is ready to receive write address information
CTRL_AWADDR[10:0]	11	Input	AXI4-Lite write address bus
CTRL_WVALID	1	Input	Write data valid Indicates that the control initiator is presenting write data

.....continued

Name	Width	Direction	Description
CTRL_WLAST	1	Input	Indicates that the current transfer is the last transfer in the write transaction
CTRL_WREADY	1	Output	Indicates that the CoreAXI4DMAController is ready to receive write data
CTRL_WSTRB[3:0]	4	Input	Write strobes Indicates the byte lanes of the WDATA bus, which contain valid write data.
CTRL_WDATA[31:0]	32	Input	AXI4-Lite write data bus
CTRL_BVALID	1	Output	Write response valid Indicates that the CoreAXI4DMAController is presenting valid write response information. Only occurs at the end of a write transaction.
CTRL_BREADY	1	Input	Indicates that the control initiator is ready to receive write response information
CTRL_BRESP[1:0]	2	Output	Write response Indicates the status of a write transaction "Okay" and "SLVERR" responses are returned by the core. The core returns "SLVERR" when an invalid address is latched on AXI4-Lite write address bus.
CTRL_ARVALID	1	Input	Read address valid Indicates that the control initiator is presenting valid address information
CTRL_ARREADY	1	Output	Read address ready Indicates that the CoreAXI4DMAController is ready to receive address information
CTRL_ARADDR[10:0]	11	Input	AXI4-Lite read address bus
CTRL_RVALID	1	Output	Read data valid Indicates that the CoreAXI4DMAController is presenting valid read data
CTRL_RREADY	1	Input	Indicates that the control initiator is ready to receive read data
CTRL_RDATA[31:0]	32	Output	AXI4-Lite read data bus
CTRL_RLAST	1	Output	Indicates that the current transfer is the last transfer in the read transaction
CTRL_RRESP[1:0]	2	Output	Read response valid Indicates that the CoreAXI4DMAController is presenting valid read response information. Valid for every transfer in a transaction. "Okay" and "SLVERR" responses are returned by the core. The core returns SLVERR when an invalid address is latched on the AXI4-Lite read address bus.
AXI4 DMA Interface Ports			
DMA_AWVALID	1	Output	Write address valid Indicates that the CoreAXI4DMAController is presenting valid address information
DMA_AWREADY	1	Input	Write address ready Indicates that the AXI4 target is ready to receive address information
DMA_AWADDR[31:0]	32	Output	DMA write address bus

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Name	Width	Direction	Description
DMA_AWID[ID_WIDTH-1:0]	ID_WIDTH	Output	Write address ID Identification tag for write address group of signals. Driven out as zeros as ID support not implemented by CoreAXI4DMAController. All transactions are processed in order.
DMA_AWLEN[7:0]	8	Output	Indicates the number of transfers in the AXI write transaction Allows 1–256 transfers per transaction
DMA_AWSIZE[2:0]	3	Output	Indicates the size of transfers in the AXI write transaction. CoreAXI4DMAController generates transactions of the data bus width size exclusively. $DMA\_AWSIZE = \log_2\left(\frac{AXI\_DMA\_DWIDTH}{8}\right)$
DMA_AWBURST[1:0]	2	Output	Write burst address type Only fixed and incrementing DMA transfers are generated by the CoreAXI4DMAController
DMA_WVALID	1	Output	Write data valid Indicates that the is presenting valid write data
DMA_WLAST	1	Output	Indicates that the current transfer is the last transfer in the write transaction
DMA_WREADY	1	Input	Indicates that the AXI4 target is ready to receive write data
DMA_WSTRB[(AXI_DMA_DWIDTH/8)-1:0]	AXI_DMA_DWIDTH/8	Output	Write strobes Indicates the byte lanes of the WDATA bus which contain valid write data
DMA_WDATA[AXI_DMA_DWIDTH-1:0]	AXI_DMA_DWIDTH	Output	DMA write data bus
DMA_BVALID	1	Input	Write response valid Indicates that the AXI4 target is presenting valid write response information. Only occurs at the end of a transaction.
DMA_BREADY	1	Output	Indicates that the CoreAXI4DMAController is ready to receive write response information
DMA_BID[ID_WIDTH:0]	ID_WIDTH	Input	Write response ID Identification tag for write response group of signals
DMA_BRESP[1:0]	2	Input	Write response Indicates the status of a write transaction
DMA_ARVALID	1	Output	Read address valid Indicates that the CoreAXI4DMAController is presenting valid address information
DMA_ARREADY	1	Input	Read address ready Indicates that the control initiator is ready to receive address information
DMA_ARADDR[31:0]	32	Output	DMA read address bus
DMA_ARID[ID_WIDTH-1:0]	ID_WIDTH	Output	Read ID Identification tag for read address group of signals. Driven out as zeros as ID support not implemented by CoreAXI4DMAController. All transactions are processed in order.
DMA_ARLEN[7:0]	8	Output	Indicates the number of transfers in the AXI read transaction Allows 1–256 transfers per transaction

.....continued

Name	Width	Direction	Description
DMA_ARSIZE[2:0]	3	Output	Indicates the size of transfers in the AXI read transaction CoreAXI4DMAController generates transactions of the data bus width size exclusively. $DMA\_ARSIZE = \log_2\left(\frac{AXI\_DMA\_DWIDTH}{8}\right)$
DMA_ARBURST[1:0]	2	Output	Read burst address type CoreAXI4DMAController generates only fixed and incrementing DMA transfers.
DMA_RVALID	1	Input	Read data valid Indicates that the AXI4 target is presenting read data
DMA_RREADY	1	Output	Indicates that the CoreAXI4DMAController is ready to receive read data
DMA_RDATA[AXI_DMA_DWIDTH-1:0]	AXI_DMA_DWIDTH	Input	DMA read data bus
DMA_RLAST	1	Input	Indicates that the current transfer is the last transfer in the read transaction
DMA_RRESP[1:0]	2	Input	Read response data Read response data returned by the AXI4 target. Valid for every transfer in a transaction.
DMA_RID[ID_WIDTH-1:0]	ID_WIDTH	Input	Read ID Identification tag for read group of signals
AXI4-Stream Interface			
TVALID	1	Input	AXI4-Stream initiator is driving a valid transfer
TREADY	1	Output	CoreAXI4DMAController is ready to receive stream data
TDATA[AXI_DMA_DWIDTH-1:0]	AXI_DMA_DWIDTH	Input	Stream data bus
TSTRB[(AXI_DMA_DWIDTH/8)-1:0]	AXI_DMA_DWIDTH/8	Input	Indicates whether the associated byte lane within TDATA must be treated as a data byte or a position byte TSTRB[0] is associated with TDATA[7:0], and so on.
TKEEP[(AXI_DMA_DWIDTH)-1:0]	AXI_DMA_DWIDTH/8	Input	Indicates the byte lanes of the TDATA bus which are processed as part of the stream Byte lanes that have the associated TKEEP bit de-asserted contain null bytes. TKEEP[0] is associated with TDATA[7:0], and so on.
TLAST	1	Input	Indicates the boundary of a packet
TID[ID_WIDTH-1:0]	ID_WIDTH	Input	Data stream identifier
TDEST[1:0]	2	Input	Provides routing information for the data stream
Interrupt Interface Ports			
Interrupt 0	1	Output	Interrupt 0 output. Remains asserted until all unmasked bits in the Interrupt 0 Status register are cleared through the Interrupt 0 Clear register. Interrupt events of buffer descriptors associated with this Interrupt output are queued.
Interrupt 3	1	Output	Interrupt 3 output, enabled at instantiation time when NUM_OF_INTS = 3. Remains asserted until all unmasked bits in the Interrupt 3 Status register are cleared through the Interrupt 3 Clear register. Interrupt events of buffer descriptors associated with this Interrupt output are queued.

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Name	Width	Direction	Description
Start Interface Ports			
STRTDMAOP [NUM_INT_BDS-1:0]	NUM_INT_BDS	Input	Input to allow the DMA operation described in an internal buffer descriptor, to be initiated by a fabric controller. The DMA operation is kicked off when this bit is asserted for one clock cycle. This signal must be synchronized in the CLOCK clock domain externally.

3. Implementation of CoreAXI4DMAController in Libero SoC (Ask a Question)

This section describes implementation of the CoreAXI4DMAController in Libero SoC.

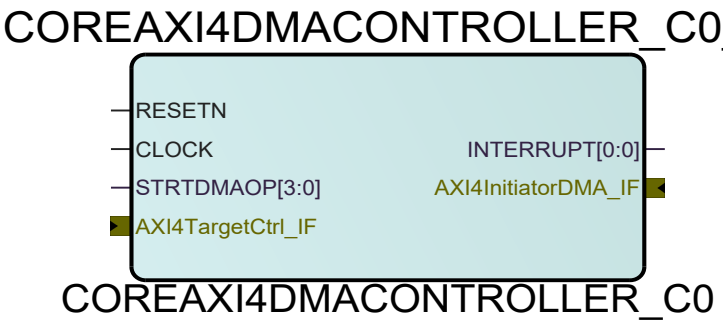
3.1 SmartDesign (Ask a Question)

CoreAXI4DMAController is preinstalled in the SmartDesign IP deployment design environment. An example instantiated view is shown in the following figure. The core is configured using the configuration GUI within SmartDesign, as shown in the following figure. To know how to create a SmartDesign project using the IP cores, see Libero SoC online help and use the latest SmartDesign user guide.

After configuring and generating the core instance, basic functionality is simulated using the testbench supplied with CoreAXI4DMAController. The testbench parameters automatically adjust to the CoreAXI4DMAController configuration.

Important: Certain RTL within CoreAXI4DMAController is automatically created when the core instance is generated in SmartDesign based upon the Priority and Interrupt associations of descriptors. For this reason, top-level parameters must only be modified in the CoreAXI4DMAController configurator in SmartDesign to ensure that the underlying RTL reflects the parameter modifications for both simulation and synthesis flows.

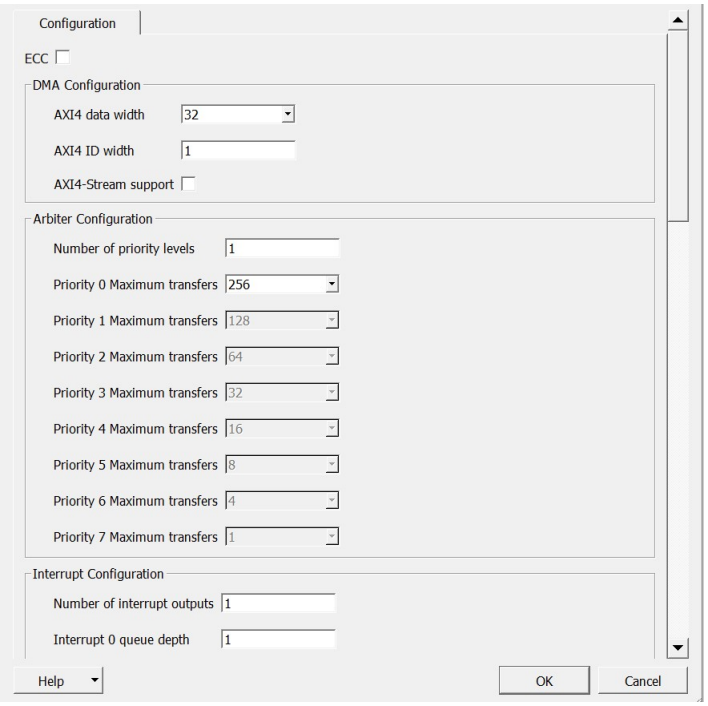
Figure 3-1. SmartDesign CoreAXI4DMAController Instance View



3.1.1 Configuring the CoreAXI4DMAController (Ask a Question)

The core is configured using the configuration GUI within SmartDesign, as shown in the following figure.

Figure 3-2. SmartDesign CoreAXI4DMAController Configuration Dialog Box



3.1.2 Simulation Flow (Ask a Question)

The user testbench for CoreAXI4DMAController is included in all releases.

To run simulation, perform the following steps:

1. Select the user testbench flow within SmartDesign.
2. Click **Save and Generate** in the Generate pane. The user testbench is selected through the Core Testbench Configuration GUI.
3. When SmartDesign generates the Libero SoC project, it installs the user testbench files.

To run the user testbench, perform the following steps:

1. Set the design root to the CoreAXI4DMAController instantiation in the Libero SoC **Design Hierarchy** pane.
2. Click **Simulation** in the Libero SoC Design Flow window. This invokes Modelsim and automatically runs the simulation.

3.1.3 Synthesis in Libero SoC (Ask a Question)

To run synthesis on the CoreAXI4DMAController, set the design root to the IP component instance and run the synthesis tool from the Libero SoC design flow pane.

3.1.4 Place-and-Route in Libero SoC (Ask a Question)

After the design is synthesized, run the compilation and then place-and-route the tools.

CoreAXI4DMAController requires no special place-and-route settings.

3.2 Verification (Ask a Question)

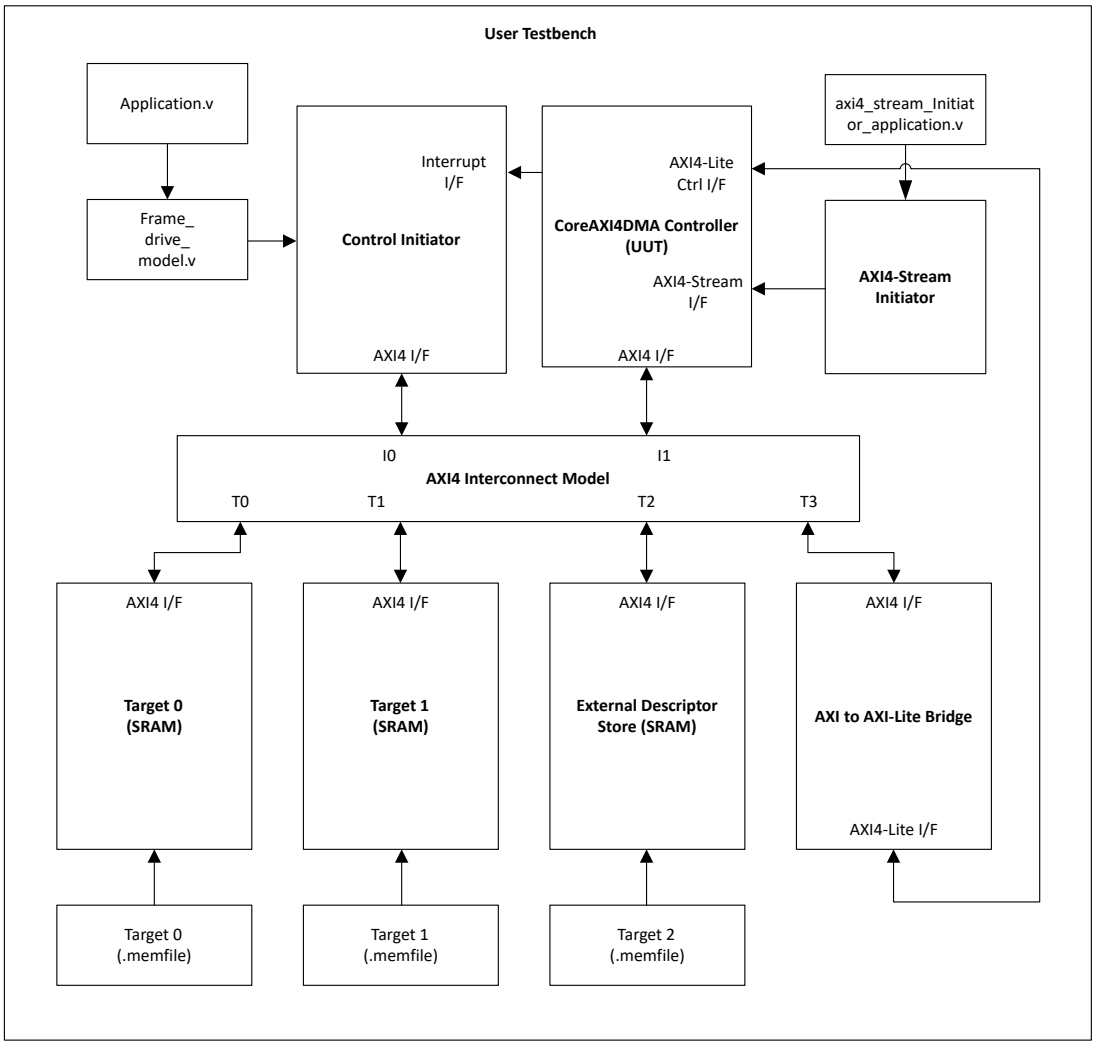
This section describes verification of the CoreAXI4DMAController.

3.2.1 Testbench (Ask a Question)

A unified testbench is used to verify and test CoreAXI4DMAController called as user testbench.

The testbench packaged along with CoreAXI4DMAController includes an instantiation of CoreAXI4DMAController, connected up to an AXI4 subsystem, as shown in the following figure.

Figure 3-3. User Testbench



The CoreAXI4DMAController testbench environment consists of the following components:

- Control Initiator: The Control Initiator component emulates the operation of an AXI4 bus initiator. The operations carried out by the Control initiator are issued from the `application.v` file, which calls the functions implemented in the `firmware_driver_model.v` file to model the intended operation of CoreAXI4DMAController from a firmware driver and application perspective. Users can modify the `application.v` script in order to simulate custom cases.
- CoreAXI4DMAController: An instance of CoreAXI4DMAController, the Unit Under Test (UUT). In the user testbench, the DMA interface of the core is connected to a initiator slot on the AXI4 interconnect model. External fetches are fetched from the External Descriptor store over the AXI4 DMA interface. The interrupt output of the core is connected to the Control Initiator to inform

the initiator when a DMA operation has completed or failed. The test cases provided in the `application.v` file perform data transfers between the Target0 and Target1 AXI4 target RAM blocks.

- AXI4 Interconnect Model: A lightweight AXI4 interconnect simulation model facilitating the connection of two initiators to four targets. Round-robin arbitration is performed to share control between the two initiators. The interconnect implements separate channels for the write address, read address, write data, read data, and write response AXI4 channels.
- Target 0 (SRAM): AXI4 RAM wrapper simulation model. Configurable address width supported to allow larger RAM blocks to be implemented. The contents of the RAM is initialized by `target0.mem`.
- Target1 (SRAM): AXI4 RAM wrapper simulation model. Configurable address width supported to allow larger RAM blocks to be implemented. The contents of the RAM is initialized by `target1.mem`.
- External Descriptor Store (SRAM): The purpose of this AXI4 RAM wrapper simulation model is to store external descriptors describing DMA operations. When pointed to via an internal descriptor, CoreAXI4DMAController fetches the descriptor from the External Descriptor Store through the AXI4 DMA interface and executes the operation described in the descriptor, before clearing the source data valid and destination data ready bits for each executed descriptor in the External descriptor store on completion of the DMA operation. The Control Initiator must then determine if the target memory related to the external descriptor DMA operation is ready before re-setting the source data valid and destination data ready bits for that descriptor in the External Descriptor Store. The contents of the External Descriptor Store is initialized by `DscrptrStore.mem`.
- AXI4 to AXI4-Lite Bridge: An AXI4 to AXI4-Lite protocol bridge simulation model to facilitate an AXI4 initiator connecting to the AXI4-Lite control interface of CoreAXI4DMAController. Buffering is performed within the simulation model to break sequential burst transactions into non-sequential, single beat transactions on the AXI4-Lite side.
- AXI4-Stream Initiator: An AXI-Stream initiator model is included in the user testbench when the AXI4_STREAM_IF parameter is set to 1 when CoreAXI4DMAController is instantiated. This generates the AXI4-Stream transactions defined in the `axi4_stream_initiator_application.v` file.

Important:

- The CoreAXI4DMAController testbench only executes for the default configuration of CoreAXI4DMAController, as the RTL is generated based on user configuration parameters when the SmartDesign sheet containing this instance of CoreAXI4DMAController is generated. In addition, no data width translation logic is included in the testbench between the interconnect target port 3 and the AXI4-Lite bridge to the AXI4-Lite Control interface of CoreAXI4DMAController (fixed data width of 32-bit on the Control interface).
- Ignore the warnings during simulation of user testbench, if any.

4. Register Map and Descriptions (Ask a Question)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	VERSION_REG	7:0	BUILD_NUM[7:0]							
		15:8	MINOR_NUM[7:0]							
		23:16	MAJOR_NUM[7:0]							
		31:24	RESERVED[7:0]							
0x04	START_OPERATION_REG	7:0	START_BIT_7	START_BIT_6	START_BIT_5	START_BIT_4	START_BIT_3	START_BIT_2	START_BIT_1	START_BIT_0
		15:8	START_BIT_15	START_BIT_14	START_BIT_13	START_BIT_12	START_BIT_11	START_BIT_10	START_BIT_9	START_BIT_8
		23:16	START_BIT_23	START_BIT_22	START_BIT_21	START_BIT_20	START_BIT_19	START_BIT_18	START_BIT_17	START_BIT_16
		31:24	START_BIT_31	START_BIT_30	START_BIT_29	START_BIT_28	START_BIT_27	START_BIT_26	START_BIT_25	START_BIT_24
0x08 ... 0x0F	Reserved									
0x10	INTR_0_STAT_REG	7:0	DESC_RNUM[3:0]				INVLD_BUFF_DESC	DMA_RD_TRAN_ERR	DMA_WR_TRAN_ERR	OPS_COMPL
		15:8							DESC_RNUM[5:4]	
		23:16								
		31:24								
0x14	INTR_0_MASK_REG	7:0					INVLD_BUFF_DESC	DMA_RD_TRAN_ERR	DMA_WR_TRAN_ERR	OPS_COMPL
		15:8								
		23:16								
		31:24								
0x18	INTR_0_CLEAR_REG	7:0					INVLD_BUFF_DESC	DMA_RD_TRAN	DMA_WR_TRAN	OPS_COMPL
		15:8								
		23:16								
		31:24								
0x1C	INTR_0_EXT_ADDR_REG	7:0	DES_ADDR[7:0]							
		15:8	DES_ADDR[15:8]							
		23:16	DES_ADDR[23:16]							
		31:24	DES_ADDR[31:24]							
0x20	INTR_1_STAT_REG	7:0	DESC_RNUM[3:0]				INVLD_BUFF_DESC	DMA_RD_TRAN_ERR	DMA_WR_TRAN_ERR	OPS_COMPL
		15:8							DESC_RNUM[5:4]	
		23:16								
		31:24								
0x24	INTR_1_MASK_REG	7:0					INVLD_BUFF_DESC	DMA_RD_TRAN_ERR	DMA_WR_TRAN_ERR	OPS_COMPL
		15:8								
		23:16								
		31:24								
0x28	INTR_1_CLEAR_REG	7:0					INVLD_BUFF_DESC	DMA_RD_TRAN	DMA_WR_TRAN	OPS_COMPL
		15:8								
		23:16								
		31:24								
0x2C	INTR_1_EXT_ADDR_REG	7:0	DES_ADDR[7:0]							
		15:8	DES_ADDR[15:8]							
		23:16	DES_ADDR[23:16]							
		31:24	DES_ADDR[31:24]							
0x30	INTR_2_STAT_REG	7:0	DESC_RNUM[3:0]				INVLD_BUFF_DESC	DMA_RD_TRAN_ERR	DMA_WR_TRAN_ERR	OPS_COMPL
		15:8							DESC_RNUM[5:4]	
		23:16								
		31:24								

.....continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x34	INTR_2_MASK_REG	7:0					INVLD_BUFF_DESC	DMA_RD_TRAN_ERR	DMA_WR_TRAN_ERR	OPS_COMPL
		15:8								
		23:16								
		31:24								
0x38	INTR_2_CLEAR_REG	7:0					INVLD_BUFF_DESC	DMA_RD_TRAN	DMA_WR_TRAN	OPS_COMPL
		15:8								
		23:16								
		31:24								
0x3C	INTR_2_EXT_ADDR_REG	7:0	DES_ADDR[7:0]							
		15:8	DES_ADDR[15:8]							
		23:16	DES_ADDR[23:16]							
		31:24	DES_ADDR[31:24]							
0x40	INTR_3_STAT_REG	7:0	DESC_RNUM[3:0]				INVLD_BUFF_DESC	DMA_RD_TRAN_ERR	DMA_WR_TRAN_ERR	OPS_COMPL
		15:8							DESC_RNUM[5:4]	
		23:16								
		31:24								
0x44	INTR_3_MASK_REG	7:0					INVLD_BUFF_DESC	DMA_RD_TRAN_ERR	DMA_WR_TRAN_ERR	OPS_COMPL
		15:8								
		23:16								
		31:24								
0x48	INTR_3_CLEAR_REG	7:0					INVLD_BUFF_DESC	DMA_RD_TRAN	DMA_WR_TRAN	OPS_COMPL
		15:8								
		23:16								
		31:24								
0x4C	INTR_3_EXT_ADDR_REG	7:0	DES_ADDR[7:0]							
		15:8	DES_ADDR[15:8]							
		23:16	DES_ADDR[23:16]							
		31:24	DES_ADDR[31:24]							
0x50 ... 0x5F	Reserved									
0x60	DESC_0_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x64	DESC_0_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x68	DESC_0_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x6C	DESC_0_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x70	DESC_0_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x74 ... 0x7F	Reserved									

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x80	DESC_1_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x84	DESC_1_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x88	DESC_1_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x8C	DESC_1_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x90	DESC_1_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x94 ... 0x9F	Reserved									
0xA0	DESC_2_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0xA4	DESC_2_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0xA8	DESC_2_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0xAC	DESC_2_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0xB0	DESC_2_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0xB4 ... 0xBF	Reserved									
0xC0	DESC_3_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0xC4	DESC_3_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0xC8	DESC_3_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xCC	DESC_3_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0xD0	DESC_3_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0xD4 ... 0xDF	Reserved									
0xE0	DESC_4_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0xE4	DESC_4_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0xE8	DESC_4_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0xEC	DESC_4_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0xF0	DESC_4_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0xF4 ... 0xFF	Reserved									
0x0100	DESC_5_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0104	DESC_5_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0108	DESC_5_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x010C	DESC_5_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0110	DESC_5_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0114 ... 0x011F	Reserved									

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0120	DESC_6_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0124	DESC_6_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0128	DESC_6_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x012C	DESC_6_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0130	DESC_6_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0134 ... 0x013F	Reserved									
0x0140	DESC_7_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0144	DESC_7_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0148	DESC_7_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x014C	DESC_7_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0150	DESC_7_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0154 ... 0x015F	Reserved									
0x0160	DESC_8_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0164	DESC_8_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0168	DESC_8_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x016C	DESC_8_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0170	DESC_8_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0174 ... 0x017F	Reserved									
0x0180	DESC_9_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0184	DESC_9_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0188	DESC_9_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x018C	DESC_9_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0190	DESC_9_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0194 ... 0x019F	Reserved									
0x01A0	DESC_10_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x01A4	DESC_10_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x01A8	DESC_10_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x01AC	DESC_10_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x01B0	DESC_10_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x01B4 ... 0x01BF	Reserved									

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x01C0	DESC_11_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x01C4	DESC_11_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x01C8	DESC_11_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x01CC	DESC_11_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x01D0	DESC_11_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x01D4 ... 0x01DF	Reserved									
0x01E0	DESC_12_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x01E4	DESC_12_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x01E8	DESC_12_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x01EC	DESC_12_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x01F0	DESC_12_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x01F4 ... 0x01FF	Reserved									
0x0200	DESC_13_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0204	DESC_13_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0208	DESC_13_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x020C	DESC_13_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0210	DESC_13_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0214 ... 0x021F	Reserved									
0x0220	DESC_14_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0224	DESC_14_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0228	DESC_14_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x022C	DESC_14_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0230	DESC_14_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0234 ... 0x023F	Reserved									
0x0240	DESC_15_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0244	DESC_15_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0248	DESC_15_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x024C	DESC_15_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0250	DESC_15_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0254 ... 0x025F	Reserved									

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0260	DESC_16_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0264	DESC_16_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0268	DESC_16_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x026C	DESC_16_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0270	DESC_16_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0274 ... 0x027F	Reserved									
0x0280	DESC_17_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0284	DESC_17_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0288	DESC_17_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x028C	DESC_17_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0290	DESC_17_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0294 ... 0x029F	Reserved									
0x02A0	DESC_18_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x02A4	DESC_18_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x02A8	DESC_18_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x02AC	DESC_18_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x02B0	DESC_18_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x02B4 ... 0x02BF	Reserved									
0x02C0	DESC_19_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x02C4	DESC_19_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x02C8	DESC_19_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x02CC	DESC_19_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x02D0	DESC_19_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x02D4 ... 0x02DF	Reserved									
0x02E0	DESC_20_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x02E4	DESC_20_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x02E8	DESC_20_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x02EC	DESC_20_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x02F0	DESC_20_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x02F4 ... 0x02FF	Reserved									

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0300	DESC_21_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0304	DESC_21_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0308	DESC_21_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x030C	DESC_21_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0310	DESC_21_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0314 ... 0x031F	Reserved									
0x0320	DESC_22_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0324	DESC_22_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0328	DESC_22_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x032C	DESC_22_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0330	DESC_22_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0334 ... 0x033F	Reserved									
0x0340	DESC_23_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0344	DESC_23_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0348	DESC_23_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x034C	DESC_23_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0350	DESC_23_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0354 ... 0x035F	Reserved									
0x0360	DESC_24_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0364	DESC_24_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0368	DESC_24_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x036C	DESC_24_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0370	DESC_24_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0374 ... 0x037F	Reserved									
0x0380	DESC_25_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0384	DESC_25_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0388	DESC_25_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x038C	DESC_25_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0390	DESC_25_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0394 ... 0x039F	Reserved									

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x03A0	DESC_26_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x03A4	DESC_26_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x03A8	DESC_26_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x03AC	DESC_26_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x03B0	DESC_26_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x03B4 ... 0x03BF	Reserved									
0x03C0	DESC_27_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x03C4	DESC_27_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x03C8	DESC_27_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x03CC	DESC_27_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x03D0	DESC_27_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x03D4 ... 0x03DF	Reserved									
0x03E0	DESC_28_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x03E4	DESC_28_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x03E8	DESC_28_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x03EC	DESC_28_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x03F0	DESC_28_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x03F4 ... 0x03FF	Reserved									
0x0400	DESC_29_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0404	DESC_29_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0408	DESC_29_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x040C	DESC_29_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0410	DESC_29_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0414 ... 0x041F	Reserved									
0x0420	DESC_30_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0424	DESC_30_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0428	DESC_30_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x042C	DESC_30_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0430	DESC_30_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0434 ... 0x043F	Reserved									

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Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0440	DESC_31_CONFIG_REG	7:0					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
		15:8	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
		23:16								
		31:24								
0x0444	DESC_31_BYTE_COUNT_REG	7:0	NUMBER_OF_BYTES[7:0]							
		15:8	NUMBER_OF_BYTES[15:8]							
		23:16		NUMBER_OF_BYTES[22:16]						
		31:24								
0x0448	DESC_31_SOURCE_ADDR_REG	7:0	SOURCE_ADDR[7:0]							
		15:8	SOURCE_ADDR[15:8]							
		23:16	SOURCE_ADDR[23:16]							
		31:24	SOURCE_ADDR[31:24]							
0x044C	DESC_31_DEST_ADDR_REG	7:0	DEST_ADDR[7:0]							
		15:8	DEST_ADDR[15:8]							
		23:16	DEST_ADDR[23:16]							
		31:24	DEST_ADDR[31:24]							
0x0450	DESC_31_NEXT_DESC_ADDR_REG	7:0	DESC_NUM_ADDR[7:0]							
		15:8	DESC_NUM_ADDR[15:8]							
		23:16	DESC_NUM_ADDR[23:16]							
		31:24	DESC_NUM_ADDR[31:24]							
0x0454 ... 0x045F	Reserved									
0x0460	STREAM_0_ADDR_REG	7:0	STREAM_DESC_ADDR[7:0]							
		15:8	STREAM_DESC_ADDR[15:8]							
		23:16	STREAM_DESC_ADDR[23:16]							
		31:24	STREAM_DESC_ADDR[31:24]							
0x0464	STREAM_1_ADDR_REG	7:0	STREAM_DESC_ADDR[7:0]							
		15:8	STREAM_DESC_ADDR[15:8]							
		23:16	STREAM_DESC_ADDR[23:16]							
		31:24	STREAM_DESC_ADDR[31:24]							
0x0468	STREAM_2_ADDR_REG	7:0	STREAM_DESC_ADDR[7:0]							
		15:8	STREAM_DESC_ADDR[15:8]							
		23:16	STREAM_DESC_ADDR[23:16]							
		31:24	STREAM_DESC_ADDR[31:24]							
0x046C	STREAM_3_ADDR_REG	7:0	STREAM_DESC_ADDR[7:0]							
		15:8	STREAM_DESC_ADDR[15:8]							
		23:16	STREAM_DESC_ADDR[23:16]							
		31:24	STREAM_DESC_ADDR[31:24]							

4.1 VERSION_REG (Ask a Question)

Name: VERSION_REG
Offset: 0x000
Reset: 0x0
Property: Read-only

Register holding the major, minor, and build number of the core.

Bit	31	30	29	28	27	26	25	24
	RESERVED[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	MAJOR_NUM[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	MINOR_NUM[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BUILD_NUM[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:24 – RESERVED[7:0] Reserved - Returns all zeros if read.

Bits 23:16 – MAJOR_NUM[7:0] Major version number of the CPZ.

Bits 15:8 – MINOR_NUM[7:0] Minor version number of the CPZ.

Bits 7:0 – BUILD_NUM[7:0] Build number of the CPZ.

4.2 STREAM_3_ADDR_REG (Ask a Question)

Name: STREAM_3_ADDR_REG
Offset: 0x46C
Reset: 0x0
Property: Read/Write

External stream descriptor address associated with AXI4-Stream transactions of with TDEST = 0b00.

Bit	31	30	29	28	27	26	25	24
	STREAM_DESC_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	STREAM_DESC_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	STREAM_DESC_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STREAM_DESC_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – STREAM_DESC_ADDR[31:0] Address of the Configuration register of the stream descriptor in the AXI4 memory-map address space.

4.3 STREAM_2_ADDR_REG (Ask a Question)

Name: STREAM_2_ADDR_REG
Offset: 0x468
Reset: 0x0
Property: Read/Write

External stream descriptor address associated with AXI4-Stream transactions of with TDEST = 0b10.

Bit	31	30	29	28	27	26	25	24
	STREAM_DESC_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	STREAM_DESC_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	STREAM_DESC_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STREAM_DESC_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – STREAM_DESC_ADDR[31:0] Address of the Configuration register of the stream descriptor in the AXI4 memory-map address space.

4.4 STREAM_1_ADDR_REG (Ask a Question)

Name: STREAM_1_ADDR_REG
Offset: 0x464
Reset: 0x0
Property: Read/Write

External stream descriptor address associated with AXI4-Stream transactions of with TDEST = 0b01.

Bit	31	30	29	28	27	26	25	24
	STREAM_DESC_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	STREAM_DESC_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	STREAM_DESC_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STREAM_DESC_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – STREAM_DESC_ADDR[31:0] Address of the Configuration register of the stream descriptor in the AXI4 memory-map address space.

4.5 STREAM_0_ADDR_REG (Ask a Question)

Name: STREAM_0_ADDR_REG
Offset: 0x460
Reset: 0x0
Property: Read/Write

External stream descriptor address associated with AXI4-Stream transactions of with TDEST = 0b00.

Bit	31	30	29	28	27	26	25	24
	STREAM_DESC_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	STREAM_DESC_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	STREAM_DESC_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	STREAM_DESC_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – STREAM_DESC_ADDR[31:0] Address of the Configuration register of the stream descriptor in the AXI4 memory-map address space.

4.6 START_OPERATION_REG (Ask a Question)

Name: START_OPERATION_REG
Offset: 0x004
Reset: 0x0
Property: Write-only

Start bits to kick off DMA operations.

Bit	31	30	29	28	27	26	25	24
	START_BIT_31	START_BIT_30	START_BIT_29	START_BIT_28	START_BIT_27	START_BIT_26	START_BIT_25	START_BIT_24
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	START_BIT_23	START_BIT_22	START_BIT_21	START_BIT_20	START_BIT_19	START_BIT_18	START_BIT_17	START_BIT_16
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	START_BIT_15	START_BIT_14	START_BIT_13	START_BIT_12	START_BIT_11	START_BIT_10	START_BIT_9	START_BIT_8
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	START_BIT_7	START_BIT_6	START_BIT_5	START_BIT_4	START_BIT_3	START_BIT_2	START_BIT_1	START_BIT_0
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit 31 – START_BIT_31 Kicks off the DMA operation described in Internal Descriptor 31

Bit 30 – START_BIT_30 Kicks off the DMA operation described in Internal Descriptor 30

Bit 29 – START_BIT_29 Kicks off the DMA operation described in Internal Descriptor 29

Bit 28 – START_BIT_28 Kicks off the DMA operation described in Internal Descriptor 28

Bit 27 – START_BIT_27 Kicks off the DMA operation described in Internal Descriptor 27

Bit 26 – START_BIT_26 Kicks off the DMA operation described in Internal Descriptor 26

Bit 25 – START_BIT_25 Kicks off the DMA operation described in Internal Descriptor 25

Bit 24 – START_BIT_24 Kicks off the DMA operation described in Internal Descriptor 24

Bit 23 – START_BIT_23 Kicks off the DMA operation described in Internal Descriptor 23

Bit 22 – START_BIT_22 Kicks off the DMA operation described in Internal Descriptor 22

Bit 21 – START_BIT_21 Kicks off the DMA operation described in Internal Descriptor 21

Bit 20 – START_BIT_20 Kicks off the DMA operation described in Internal Descriptor 20

Bit 19 – START_BIT_19 Kicks off the DMA operation described in Internal Descriptor 19

Bit 18 – START_BIT_18 Kicks off the DMA operation described in Internal Descriptor 18

Bit 17 – START_BIT_17 Kicks off the DMA operation described in Internal Descriptor 17

Bit 16 – START_BIT_16 Kicks off the DMA operation described in Internal Descriptor 16

Bit 15 – START_BIT_15 Kicks off the DMA operation described in Internal Descriptor 15

Bit 14 – START_BIT_14 Kicks off the DMA operation described in Internal Descriptor 14

Bit 13 – START_BIT_13 Kicks off the DMA operation described in Internal Descriptor 13

Bit 12 – START_BIT_12 Kicks off the DMA operation described in Internal Descriptor 12

Bit 11 – START_BIT_11 Kicks off the DMA operation described in Internal Descriptor 11

Bit 10 – START_BIT_10 Kicks off the DMA operation described in Internal Descriptor 10

Bit 9 – START_BIT_9 Kicks off the DMA operation described in Internal Descriptor 9

Bit 8 – START_BIT_8 Kicks off the DMA operation described in Internal Descriptor 8

Bit 7 – START_BIT_7 Kicks off the DMA operation described in Internal Descriptor 7

Bit 6 – START_BIT_6 Kicks off the DMA operation described in Internal Descriptor 6

Bit 5 – START_BIT_5 Kicks off the DMA operation described in Internal Descriptor 5

Bit 4 – START_BIT_4 Kicks off the DMA operation described in Internal Descriptor 4

Bit 3 – START_BIT_3 Kicks off the DMA operation described in Internal Descriptor 3

Bit 2 – START_BIT_2 Kicks off the DMA operation described in Internal Descriptor 2

Bit 1 – START_BIT_1 Kicks off the DMA operation described in Internal Descriptor 1

Bit 0 – START_BIT_0 Kicks off the DMA operation described in Internal Descriptor 0

4.7 INTR_3_STAT_REG (Ask a Question)

Name: INTR_3_STAT_REG
Offset: 0x040
Reset: 0x0
Property: Read-only

Status register containing status information for Interrupt 3 events. Returns the status information for the event at the head of the Interrupt 3 Queue.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							DESC_RNUM[5:4]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	DESC_RNUM[3:0]				INVLD_BUFF_DESC	DMA_RD_TRAN_ERR	DMA_WR_TRAN_ERR	OPS_COMPL
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:4 – DESC_RNUM[5:0]

Value	Description
0-31	Internal descriptor number that the status information is related to.
32	Refer to the External Descriptor Address register to determine the address of the external buffer descriptor to which the status information is associated.
33	Stream operation complete. Refer to the External Descriptor Address register to determine the address of the stream descriptor to which the status information is associated.

Bit 3 – INVLD_BUFF_DESC An attempt was made to initiate a DMA operation on an invalid descriptor.

Bit 2 – DMA_RD_TRAN_ERR An AXI error was returned by the Target during an AXI read transaction.

Bit 1 – DMA_WR_TRAN_ERR An AXI error was returned by the Target during an AXI write transaction.

Bit 0 – OPS_COMPL Kicks off the DMA operation described in Internal Descriptor 3.

4.8 INTR_3_MASK_REG (Ask a Question)

Name: INTR_3_MASK_REG
Offset: 0x044
Reset: 0x0
Property: Read/Write

Configure flags in the Interrupt 3 Status register that can generate an interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					INVLD_BUFF_DESC	DMA_RD_TRAN_ERR	DMA_WR_TRAN_ERR	OPS_COMPL
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – INVLD_BUFF_DESC

Value	Description
0	No interrupt generated when the corresponding bit in the Interrupt 3 status register is asserted.
1	Assert an interrupt when an invalid descriptor is processed.

Bit 2 – DMA_RD_TRAN_ERR

Value	Description
0	No interrupt generated when the corresponding bit in the Interrupt 3 status register is asserted.
1	Assert an interrupt when an AXI read error is detected.

Bit 1 – DMA_WR_TRAN_ERR

Value	Description
0	No interrupt generated when the corresponding bit in the Interrupt 3 status register is asserted.
1	Assert an interrupt when an AXI write error is detected.

Bit 0 – OPS_COMPL

Value	Description
0	No interrupt generated when the corresponding bit in the Interrupt 3 status register is asserted.
1	Assert an interrupt when a DMA operation completes.

4.9 INTR_3_EXT_ADDR_REG (Ask a Question)

Name: INTR_3_EXT_ADDR_REG
Offset: 0x04C
Reset: 0x0
Property: Read-only

Address of the external buffer descriptor with which the contents of the Interrupt Status register is associated.

Bit	31	30	29	28	27	26	25	24
	DES_ADDR[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DES_ADDR[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DES_ADDR[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DES_ADDR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DES_ADDR[31:0] Address of the external or stream descriptor to which the contents of the Interrupt Status register is related. The contents of this register should be ignored and will return all zeros if the contents of the Descriptor Number field in the Interrupt Status register is something other than 32 or 33.

4.10 INTR_3_CLEAR_REG (Ask a Question)

Name: INTR_3_CLEAR_REG
Offset: 0x048
Reset: 0x0
Property: Write-only

Clear flags asserted in the Interrupt 3 Status register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					INVLD_BUFF_DESC	DMA_RD_TRAN	DMA_WR_TRAN	OPS_COMPL
Access					W	W	W	W
Reset					0	0	0	0

Bit 3 – INVLD_BUFF_DESC Writing a 1 to this bit clears the corresponding bit in the Interrupt 3 Status register.

Bit 2 – DMA_RD_TRAN Writing a 1 to this bit clears the corresponding bit in the Interrupt 3 Status register.

Bit 1 – DMA_WR_TRAN Writing a 1 to this bit clears the corresponding bit in the Interrupt 3 Status register.

Bit 0 – OPS_COMPL Writing a 1 to this bit clears the corresponding bit in the Interrupt 3 Status register.

4.11 INTR_2_STAT_REG (Ask a Question)

Name: INTR_2_STAT_REG
Offset: 0x030
Reset: 0x0
Property: Read-only

Status register containing status information for Interrupt 2 events. Returns the status information for the event at the head of the Interrupt 2 Queue.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							DESC_RNUM[5:4]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	DESC_RNUM[3:0]				INVLD_BUFF_DESC	DMA_RD_TRAN_ERR	DMA_WR_TRAN_ERR	OPS_COMPL
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:4 – DESC_RNUM[5:0]

Value	Description
0-31	Internal descriptor number that the status information is related to.
32	Refer to the External Descriptor Address register to determine the address of the external buffer descriptor to which the status information is associated.
33	Stream operation complete. Refer to the External Descriptor Address register to determine the address of the stream descriptor to which the status information is associated.

Bit 3 – INVLD_BUFF_DESC An attempt was made to initiate a DMA operation on an invalid descriptor.

Bit 2 – DMA_RD_TRAN_ERR An AXI error was returned by the Target during an AXI read transaction.

Bit 1 – DMA_WR_TRAN_ERR An AXI error was returned by the Target during an AXI write transaction.

Bit 0 – OPS_COMPL Kicks off the DMA operation described in Internal Descriptor 2.

4.12 INTR_2_MASK_REG (Ask a Question)

Name: INTR_2_MASK_REG
Offset: 0x034
Reset: 0x0
Property: Read/Write

Configure flags in the Interrupt 2 Status register that can generate an interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					INVLD_BUFF_DESC	DMA_RD_TRAN_ERR	DMA_WR_TRAN_ERR	OPS_COMPL
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – INVLD_BUFF_DESC

Value	Description
0	No interrupt generated when the corresponding bit in the Interrupt 2 status register is asserted.
1	Assert an interrupt when an invalid descriptor is processed.

Bit 2 – DMA_RD_TRAN_ERR

Value	Description
0	No interrupt generated when the corresponding bit in the Interrupt 2 status register is asserted.
1	Assert an interrupt when an AXI read error is detected.

Bit 1 – DMA_WR_TRAN_ERR

Value	Description
0	No interrupt generated when the corresponding bit in the Interrupt 2 status register is asserted.
1	Assert an interrupt when an AXI write error is detected.

Bit 0 – OPS_COMPL

Value	Description
0	No interrupt generated when the corresponding bit in the Interrupt 2 status register is asserted.
1	Assert an interrupt when a DMA operation completes.

4.13 INTR_2_EXT_ADDR_REG (Ask a Question)

Name: INTR_2_EXT_ADDR_REG
Offset: 0x03C
Reset: 0x0
Property: Read-only

Address of the external buffer descriptor with which the contents of the Interrupt Status register is associated.

Bit	31	30	29	28	27	26	25	24
	DES_ADDR[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DES_ADDR[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DES_ADDR[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DES_ADDR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DES_ADDR[31:0] Address of the external or stream descriptor to which the contents of the Interrupt Status register is related. The contents of this register should be ignored and will return all zeros if the contents of the Descriptor Number field in the Interrupt Status register is something other than 32 or 33.

4.14 INTR_2_CLEAR_REG (Ask a Question)

Name: INTR_2_CLEAR_REG
Offset: 0x038
Reset: 0x0
Property: Write-only

Clear flags asserted in the Interrupt 2 Status register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					INVLD_BUFF_DESC	DMA_RD_TRAN	DMA_WR_TRAN	OPS_COMPL
Access					W	W	W	W
Reset					0	0	0	0

Bit 3 – INVLD_BUFF_DESC Writing a 1 to this bit clears the corresponding bit in the Interrupt 2 Status register.

Bit 2 – DMA_RD_TRAN Writing a 1 to this bit clears the corresponding bit in the Interrupt 2 Status register.

Bit 1 – DMA_WR_TRAN Writing a 1 to this bit clears the corresponding bit in the Interrupt 2 Status register.

Bit 0 – OPS_COMPL Writing a 1 to this bit clears the corresponding bit in the Interrupt 2 Status register.

4.15 INTR_1_STAT_REG (Ask a Question)

Name: INTR_1_STAT_REG
Offset: 0x020
Reset: 0x0
Property: Read-only

Status register containing status information for Interrupt 1 events. Returns the status information for the event at the head of the Interrupt 1 Queue.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							DESC_RNUM[5:4]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	DESC_RNUM[3:0]				INVLD_BUFF_DESC	DMA_RD_TRAN_ERR	DMA_WR_TRAN_ERR	OPS_COMPL
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:4 – DESC_RNUM[5:0]

Value	Description
0-31	Internal descriptor number that the status information is related to.
32	Refer to the External Descriptor Address register to determine the address of the external buffer descriptor to which the status information is associated.
33	Stream operation complete. Refer to the External Descriptor Address register to determine the address of the stream descriptor to which the status information is associated.

Bit 3 – INVLD_BUFF_DESC An attempt was made to initiate a DMA operation on an invalid descriptor.

Bit 2 – DMA_RD_TRAN_ERR An AXI error was returned by the Target during an AXI read transaction.

Bit 1 – DMA_WR_TRAN_ERR An AXI error was returned by the Target during an AXI write transaction.

Bit 0 – OPS_COMPL Kicks off the DMA operation described in Internal Descriptor 0.

4.16 INTR_1_MASK_REG (Ask a Question)

Name: INTR_1_MASK_REG
Offset: 0x024
Reset: 0x0
Property: Read/Write

Configure flags in the Interrupt 1 Status register that can generate an interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					INVLD_BUFF_DESC	DMA_RD_TRAN_ERR	DMA_WR_TRAN_ERR	OPS_COMPL
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – INVLD_BUFF_DESC

Value	Description
0	No interrupt generated when the corresponding bit in the Interrupt 1 status register is asserted.
1	Assert an interrupt when an invalid descriptor is processed.

Bit 2 – DMA_RD_TRAN_ERR

Value	Description
0	No interrupt generated when the corresponding bit in the Interrupt 1 status register is asserted.
1	Assert an interrupt when an AXI read error is detected.

Bit 1 – DMA_WR_TRAN_ERR

Value	Description
0	No interrupt generated when the corresponding bit in the Interrupt 1 status register is asserted.
1	Assert an interrupt when an AXI write error is detected.

Bit 0 – OPS_COMPL

Value	Description
0	No interrupt generated when the corresponding bit in the Interrupt 1 status register is asserted.
1	Assert an interrupt when a DMA operation completes.

4.17 INTR_1_EXT_ADDR_REG (Ask a Question)

Name: INTR_1_EXT_ADDR_REG
Offset: 0x02C
Reset: 0x0
Property: Read-only

Address of the external buffer descriptor with which the contents of the Interrupt Status register is associated.

Bit	31	30	29	28	27	26	25	24
	DES_ADDR[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DES_ADDR[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DES_ADDR[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DES_ADDR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DES_ADDR[31:0] Address of the external or stream descriptor to which the contents of the Interrupt Status register is related. The contents of this register should be ignored and will return all zeros if the contents of the Descriptor Number field in the Interrupt Status register is something other than 32 or 33.

4.18 INTR_1_CLEAR_REG (Ask a Question)

Name: INTR_1_CLEAR_REG
Offset: 0x028
Reset: 0x0
Property: Write-only

Clear flags asserted in the Interrupt 1 Status register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					INVLD_BUFF_DESC	DMA_RD_TRAN	DMA_WR_TRAN	OPS_COMPL
Access					W	W	W	W
Reset					0	0	0	0

Bit 3 – INVLD_BUFF_DESC Writing a 1 to this bit clears the corresponding bit in the Interrupt 1 Status register.

Bit 2 – DMA_RD_TRAN Writing a 1 to this bit clears the corresponding bit in the Interrupt 1 Status register.

Bit 1 – DMA_WR_TRAN Writing a 1 to this bit clears the corresponding bit in the Interrupt 1 Status register.

Bit 0 – OPS_COMPL Writing a 1 to this bit clears the corresponding bit in the Interrupt 1 Status register.

4.19 INTR_0_STAT_REG (Ask a Question)

Name: INTR_0_STAT_REG
Offset: 0x010
Reset: 0x0
Property: Read-only

Status register containing status information for Interrupt 0 events. Returns the status information for the event at the head of the Interrupt 0 Queue.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							DESC_RNUM[5:4]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	DESC_RNUM[3:0]				INVLD_BUFF_DESC	DMA_RD_TRAN_ERR	DMA_WR_TRAN_ERR	OPS_COMPL
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:4 – DESC_RNUM[5:0]

Value	Description
0-31	Internal descriptor number that the status information is related to.
32	Refer to the External Descriptor Address register to determine the address of the external buffer descriptor to which the status information is associated.
33	Stream operation complete. Refer to the External Descriptor Address register to determine the address of the stream descriptor to which the status information is associated.

Bit 3 – INVLD_BUFF_DESC An attempt was made to initiate a DMA operation on an invalid descriptor.

Bit 2 – DMA_RD_TRAN_ERR An AXI error was returned by the Target during an AXI read transaction.

Bit 1 – DMA_WR_TRAN_ERR An AXI error was returned by the Target during an AXI write transaction.

Bit 0 – OPS_COMPL Kicks off the DMA operation described in Internal Descriptor 0.

4.20 INTR_0_MASK_REG (Ask a Question)

Name: INTR_0_MASK_REG
Offset: 0x014
Reset: 0x0
Property: Read/Write

Configure flags in the Interrupt 0 Status register that can generate an interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					INVLD_BUFF_DESC	DMA_RD_TRAN_ERR	DMA_WR_TRAN_ERR	OPS_COMPL
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – INVLD_BUFF_DESC

Value	Description
0	No interrupt generated when the corresponding bit in the Interrupt 0 status register is asserted.
1	Assert an interrupt when an invalid descriptor is processed.

Bit 2 – DMA_RD_TRAN_ERR

Value	Description
0	No interrupt generated when the corresponding bit in the Interrupt 0 status register is asserted.
1	Assert an interrupt when an AXI read error is detected.

Bit 1 – DMA_WR_TRAN_ERR

Value	Description
0	No interrupt generated when the corresponding bit in the Interrupt 0 status register is asserted.
1	Assert an interrupt when an AXI write error is detected.

Bit 0 – OPS_COMPL

Value	Description
0	No interrupt generated when the corresponding bit in the Interrupt 0 status register is asserted.
1	Assert an interrupt when a DMA operation completes.

4.21 INTR_0_EXT_ADDR_REG (Ask a Question)

Name: INTR_0_EXT_ADDR_REG
Offset: 0x01C
Reset: 0x0
Property: Read-only

Address of the external buffer descriptor with which the contents of the Interrupt Status register is associated.

Bit	31	30	29	28	27	26	25	24
	DES_ADDR[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DES_ADDR[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DES_ADDR[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DES_ADDR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DES_ADDR[31:0] Address of the external or stream descriptor to which the contents of the Interrupt Status register is related. The contents of this register should be ignored and will return all zeros if the contents of the Descriptor Number field in the Interrupt Status register is something other than 32 or 33.

4.22 INTR_0_CLEAR_REG (Ask a Question)

Name: INTR_0_CLEAR_REG
Offset: 0x018
Reset: 0x0
Property: Write-only

Clear flags asserted in the Interrupt 0 Status register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					INVLD_BUFF_DESC	DMA_RD_TRAN	DMA_WR_TRAN	OPS_COMPL
Access					W	W	W	W
Reset					0	0	0	0

Bit 3 – INVLD_BUFF_DESC Writing a 1 to this bit clears the corresponding bit in the Interrupt 0 Status register.

Bit 2 – DMA_RD_TRAN Writing a 1 to this bit clears the corresponding bit in the Interrupt 0 Status register.

Bit 1 – DMA_WR_TRAN Writing a 1 to this bit clears the corresponding bit in the Interrupt 0 Status register.

Bit 0 – OPS_COMPL Writing a 1 to this bit clears the corresponding bit in the Interrupt 0 Status register.

4.23 DESC_9_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_9_SOURCE_ADDR_REG
Offset: 0x188
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.24 DESC_9_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_9_NEXT_DESC_ADDR_REG
Offset: 0x190
Reset: 0x0
Property: Read/Write

Descriptor number or address of the next internal or external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the chain bit is not set in the Configuration register of this descriptor. The value specified in this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.25 DESC_9_DEST_ADDR_REG (Ask a Question)

Name: DESC_9_DEST_ADDR_REG
Offset: 0x18C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.26 DESC_9_CONFIG_REG (Ask a Question)

Name: DESC_9_CONFIG_REG
Offset: 0x180
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation - Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation - Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.27 DESC_9_BYTE_COUNT_REG (Ask a Question)

Name: DESC_9_BYTE_COUNT_REG
Offset: 0x184
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.28 DESC_8_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_8_SOURCE_ADDR_REG
Offset: 0x168
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.29 DESC_8_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_8_NEXT_DESC_ADDR_REG
Offset: 0x170
Reset: 0x0
Property: Read/Write

Descriptor number or address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.30 DESC_8_DEST_ADDR_REG (Ask a Question)

Name: DESC_8_DEST_ADDR_REG
Offset: 0x16C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.31 DESC_8_CONFIG_REG (Ask a Question)

Name: DESC_8_CONFIG_REG
Offset: 0x160
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.32 DESC_8_BYTE_COUNT_REG (Ask a Question)

Name: DESC_8_BYTE_COUNT_REG
Offset: 0x164
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.33 DESC_7_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_7_SOURCE_ADDR_REG
Offset: 0x148
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.34 DESC_7_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_7_NEXT_DESC_ADDR_REG
Offset: 0x150
Reset: 0x0
Property: Read/Write

Descriptor number or address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.35 DESC_7_DEST_ADDR_REG (Ask a Question)

Name: DESC_7_DEST_ADDR_REG
Offset: 0x14C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.36 DESC_7_CONFIG_REG (Ask a Question)

Name: DESC_7_CONFIG_REG
Offset: 0x140
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.37 DESC_7_BYTE_COUNT_REG (Ask a Question)

Name: DESC_7_BYTE_COUNT_REG
Offset: 0x144
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.38 DESC_6_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_6_SOURCE_ADDR_REG
Offset: 0x128
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.39 DESC_6_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_6_NEXT_DESC_ADDR_REG
Offset: 0x130
Reset: 0x0
Property: Read/Write

Descriptor number or address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.40 DESC_6_DEST_ADDR_REG (Ask a Question)

Name: DESC_6_DEST_ADDR_REG
Offset: 0x12C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.41 DESC_6_CONFIG_REG (Ask a Question)

Name: DESC_6_CONFIG_REG
Offset: 0x120
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.42 DESC_6_BYTE_COUNT_REG (Ask a Question)

Name: DESC_6_BYTE_COUNT_REG
Offset: 0x124
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.43 DESC_5_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_5_SOURCE_ADDR_REG
Offset: 0x108
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.44 DESC_5_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_5_NEXT_DESC_ADDR_REG
Offset: 0x110
Reset: 0x0
Property: Read/Write

Descriptor number or address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.45 DESC_5_DEST_ADDR_REG (Ask a Question)

Name: DESC_5_DEST_ADDR_REG
Offset: 0x10C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.46 DESC_5_CONFIG_REG (Ask a Question)

Name: DESC_5_CONFIG_REG
Offset: 0x100
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.47 DESC_5_BYTE_COUNT_REG (Ask a Question)

Name: DESC_5_BYTE_COUNT_REG
Offset: 0x104
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.48 DESC_4_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_4_SOURCE_ADDR_REG
Offset: 0x0E8
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.49 DESC_4_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_4_NEXT_DESC_ADDR_REG
Offset: 0x0F0
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.50 DESC_4_DEST_ADDR_REG (Ask a Question)

Name: DESC_4_DEST_ADDR_REG
Offset: 0x0EC
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.51 DESC_4_CONFIG_REG. (Ask a Question)

Name: DESC_4_CONFIG_REG
Offset: 0x0E0
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.52 DESC_4_BYTE_COUNT_REG (Ask a Question)

Name: DESC_4_BYTE_COUNT_REG
Offset: 0x0E4
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.53 DESC_3_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_3_SOURCE_ADDR_REG
Offset: 0x0C8
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.54 DESC_3_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_3_NEXT_DESC_ADDR_REG
Offset: 0x0D0
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.55 DESC_3_DEST_ADDR_REG (Ask a Question)

Name: DESC_3_DEST_ADDR_REG
Offset: 0x0CC
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.56 DESC_3_CONFIG_REG (Ask a Question)

Name: DESC_3_CONFIG_REG
Offset: 0x0C0
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.57 DESC_3_BYTE_COUNT_REG (Ask a Question)

Name: DESC_3_BYTE_COUNT_REG
Offset: 0x0C4
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.58 DESC_31_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_31_SOURCE_ADDR_REG
Offset: 0x448
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.59 DESC_31_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_31_NEXT_DESC_ADDR_REG
Offset: 0x450
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.60 DESC_31_DEST_ADDR_REG (Ask a Question)

Name: DESC_31_DEST_ADDR_REG
Offset: 0x44C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.61 DESC_31_CONFIG_REG (Ask a Question)

Name: DESC_31_CONFIG_REG
Offset: 0x440
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.62 DESC_31_BYTE_COUNT_REG (Ask a Question)

Name: DESC_31_BYTE_COUNT_REG
Offset: 0x444
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.63 DESC_30_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_30_SOURCE_ADDR_REG
Offset: 0x428
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.64 DESC_30_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_30_NEXT_DESC_ADDR_REG
Offset: 0x430
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.65 DESC_30_DEST_ADDR_REG (Ask a Question)

Name: DESC_30_DEST_ADDR_REG
Offset: 0x42C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.66 DESC_30_CONFIG_REG (Ask a Question)

Name: DESC_30_CONFIG_REG
Offset: 0x420
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.67 DESC_30_BYTE_COUNT_REG (Ask a Question)

Name: DESC_30_BYTE_COUNT_REG
Offset: 0x424
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.68 DESC_2_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_2_SOURCE_ADDR_REG
Offset: 0x0A8
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.69 DESC_2_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_2_NEXT_DESC_ADDR_REG
Offset: 0x0B0
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.70 DESC_2_DEST_ADDR_REG (Ask a Question)

Name: DESC_2_DEST_ADDR_REG
Offset: 0x0AC
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.71 DESC_2_CONFIG_REG (Ask a Question)

Name: DESC_2_CONFIG_REG
Offset: 0x0A0
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.72 DESC_29_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_29_SOURCE_ADDR_REG
Offset: 0x408
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.73 DESC_2_BYTE_COUNT_REG (Ask a Question)

Name: DESC_2_BYTE_COUNT_REG
Offset: 0x0A4
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.74 DESC_29_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_29_NEXT_DESC_ADDR_REG
Offset: 0x410
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.75 DESC_29_DEST_ADDR_REG (Ask a Question)

Name: DESC_29_DEST_ADDR_REG
Offset: 0x40C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.76 DESC_29_CONFIG_REG (Ask a Question)

Name: DESC_29_CONFIG_REG
Offset: 0x400
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor
1	External buffer descriptor

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.77 DESC_29_BYTE_COUNT_REG (Ask a Question)

Name: DESC_29_BYTE_COUNT_REG
Offset: 0x404
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.78 DESC_28_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_28_SOURCE_ADDR_REG
Offset: 0x3E8
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.79 DESC_28_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_28_NEXT_DESC_ADDR_REG
Offset: 0x3F0
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.80 DESC_28_DEST_ADDR_REG (Ask a Question)

Name: DESC_28_DEST_ADDR_REG
Offset: 0x3EC
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.81 DESC_28_CONFIG_REG (Ask a Question)

Name: DESC_28_CONFIG_REG
Offset: 0x3E0
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.82 DESC_28_BYTE_COUNT_REG (Ask a Question)

Name: DESC_28_BYTE_COUNT_REG
Offset: 0x3E4
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.83 DESC_27_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_27_SOURCE_ADDR_REG
Offset: 0x3C8
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.84 DESC_27_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_27_NEXT_DESC_ADDR_REG
Offset: 0x3D0
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.85 DESC_27_DEST_ADDR_REG (Ask a Question)

Name: DESC_27_DEST_ADDR_REG
Offset: 0x3CC
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.86 DESC_27_CONFIG_REG (Ask a Question)

Name: DESC_27_CONFIG_REG
Offset: 0x3C0
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.87 DESC_27_BYTE_COUNT_REG (Ask a Question)

Name: DESC_27_BYTE_COUNT_REG
Offset: 0x3C4
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.88 DESC_26_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_26_SOURCE_ADDR_REG
Offset: 0x3A8
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.89 DESC_26_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_26_NEXT_DESC_ADDR_REG
Offset: 0x3B0
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.90 DESC_26_DEST_ADDR_REG (Ask a Question)

Name: DESC_26_DEST_ADDR_REG
Offset: 0x3AC
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.91 DESC_26_CONFIG_REG (Ask a Question)

Name: DESC_26_CONFIG_REG
Offset: 0x3A0
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.92 DESC_26_BYTE_COUNT_REG (Ask a Question)

Name: DESC_26_BYTE_COUNT_REG
Offset: 0x3A4
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.93 DESC_25_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_25_SOURCE_ADDR_REG
Offset: 0x388
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.94 DESC_25_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_25_NEXT_DESC_ADDR_REG
Offset: 0x390
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.95 DESC_25_DEST_ADDR_REG (Ask a Question)

Name: DESC_25_DEST_ADDR_REG
Offset: 0x38C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.96 DESC_25_CONFIG_REG (Ask a Question)

Name: DESC_25_CONFIG_REG
Offset: 0x380
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.97 DESC_25_BYTE_COUNT_REG (Ask a Question)

Name: DESC_25_BYTE_COUNT_REG
Offset: 0x384
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.98 DESC_24_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_24_SOURCE_ADDR_REG
Offset: 0x368
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.99 DESC_24_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_24_NEXT_DESC_ADDR_REG
Offset: 0x370
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal or external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.100 DESC_24_DEST_ADDR_REG (Ask a Question)

Name: DESC_24_DEST_ADDR_REG
Offset: 0x36C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.101 DESC_24_CONFIG_REG (Ask a Question)

Name: DESC_24_CONFIG_REG
Offset: 0x360
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.102 DESC_24_BYTE_COUNT_REG (Ask a Question)

Name: DESC_24_BYTE_COUNT_REG
Offset: 0x364
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.103 DESC_23_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_23_SOURCE_ADDR_REG
Offset: 0x348
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.104 DESC_23_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_23_NEXT_DESC_ADDR_REG
Offset: 0x350
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.105 DESC_23_DEST_ADDR_REG (Ask a Question)

Name: DESC_23_DEST_ADDR_REG
Offset: 0x34C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.106 DESC_23_CONFIG_REG (Ask a Question)

Name: DESC_23_CONFIG_REG
Offset: 0x340
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.107 DESC_23_BYTE_COUNT_REG (Ask a Question)

Name: DESC_23_BYTE_COUNT_REG
Offset: 0x344
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.108 DESC_22_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_22_SOURCE_ADDR_REG
Offset: 0x328
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.109 DESC_22_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_22_NEXT_DESC_ADDR_REG
Offset: 0x330
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.110 DESC_22_DEST_ADDR_REG (Ask a Question)

Name: DESC_22_DEST_ADDR_REG
Offset: 0x32C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.111 DESC_22_CONFIG_REG (Ask a Question)

Name: DESC_22_CONFIG_REG
Offset: 0x320
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.112 DESC_22_BYTE_COUNT_REG (Ask a Question)

Name: DESC_22_BYTE_COUNT_REG
Offset: 0x324
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.113 DESC_21_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_21_SOURCE_ADDR_REG
Offset: 0x308
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.114 DESC_21_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_21_NEXT_DESC_ADDR_REG
Offset: 0x310
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.115 DESC_21_DEST_ADDR_REG (Ask a Question)

Name: DESC_21_DEST_ADDR_REG
Offset: 0x30C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.116 DESC_21_CONFIG_REG (Ask a Question)

Name: DESC_21_CONFIG_REG
Offset: 0x300
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.117 DESC_21_BYTE_COUNT_REG (Ask a Question)

Name: DESC_21_BYTE_COUNT_REG
Offset: 0x304
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.118 DESC_20_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_20_SOURCE_ADDR_REG
Offset: 0x2E8
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.119 DESC_20_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_20_NEXT_DESC_ADDR_REG
Offset: 0x2F0
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.120 DESC_20_DEST_ADDR_REG (Ask a Question)

Name: DESC_20_DEST_ADDR_REG
Offset: 0x2EC
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.121 DESC_20_CONFIG_REG (Ask a Question)

Name: DESC_20_CONFIG_REG
Offset: 0x2E0
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.122 DESC_20_BYTE_COUNT_REG (Ask a Question)

Name: DESC_20_BYTE_COUNT_REG
Offset: 0x2E4
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.123 DESC_1_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_1_SOURCE_ADDR_REG
Offset: 0x088
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.124 DESC_1_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_1_NEXT_DESC_ADDR_REG
Offset: 0x090
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.125 DESC_1_DEST_ADDR_REG (Ask a Question)

Name: DESC_1_DEST_ADDR_REG
Offset: 0x08C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.126 DESC_1_CONFIG_REG (Ask a Question)

Name: DESC_1_CONFIG_REG
Offset: 0x080
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.127 DESC_1_BYTE_COUNT_REG (Ask a Question)

Name: DESC_1_BYTE_COUNT_REG
Offset: 0x084
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.128 DESC_19_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_19_SOURCE_ADDR_REG
Offset: 0x2C8
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.129 DESC_19_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_19_NEXT_DESC_ADDR_REG
Offset: 0x2D0
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.130 DESC_19_DEST_ADDR_REG (Ask a Question)

Name: DESC_19_DEST_ADDR_REG
Offset: 0x2CC
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.131 DESC_19_CONFIG_REG (Ask a Question)

Name: DESC_19_CONFIG_REG
Offset: 0x2C0
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.132 DESC_19_BYTE_COUNT_REG (Ask a Question)

Name: DESC_19_BYTE_COUNT_REG
Offset: 0x2C4
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.133 DESC_18_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_18_SOURCE_ADDR_REG
Offset: 0x2A8
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.134 DESC_18_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_18_NEXT_DESC_ADDR_REG
Offset: 0x2B0
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.135 DESC_18_DEST_ADDR_REG (Ask a Question)

Name: DESC_18_DEST_ADDR_REG
Offset: 0x2AC
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.136 DESC_18_CONFIG_REG (Ask a Question)

Name: DESC_18_CONFIG_REG
Offset: 0x2A0
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.137 DESC_18_BYTE_COUNT_REG (Ask a Question)

Name: DESC_18_BYTE_COUNT_REG
Offset: 0x2A4
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.138 DESC_17_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_17_SOURCE_ADDR_REG
Offset: 0x288
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.139 DESC_17_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_17_NEXT_DESC_ADDR_REG
Offset: 0x290
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.140 DESC_17_DEST_ADDR_REG (Ask a Question)

Name: DESC_17_DEST_ADDR_REG
Offset: 0x28C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.141 DESC_17_BYTE_COUNT_REG (Ask a Question)

Name: DESC_17_BYTE_COUNT_REG
Offset: 0x284
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.142 DESC_17_CONFIG_REG (Ask a Question)

Name: DESC_17_CONFIG_REG
Offset: 0x280
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.143 DESC_16_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_16_SOURCE_ADDR_REG
Offset: 0x268
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.144 DESC_16_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_16_NEXT_DESC_ADDR_REG
Offset: 0x270
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.145 DESC_16_DEST_ADDR_REG (Ask a Question)

Name: DESC_16_DEST_ADDR_REG
Offset: 0x26C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.146 DESC_16_CONFIG_REG (Ask a Question)

Name: DESC_16_CONFIG_REG
Offset: 0x260
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.147 DESC_16_BYTE_COUNT_REG (Ask a Question)

Name: DESC_16_BYTE_COUNT_REG
Offset: 0x264
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.148 DESC_15_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_15_SOURCE_ADDR_REG
Offset: 0x248
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.149 DESC_15_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_15_NEXT_DESC_ADDR_REG
Offset: 0x250
Reset: 0x0
Property: Read/Write

Descriptor number or address of the next internal or external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.150 DESC_15_DEST_ADDR_REG (Ask a Question)

Name: DESC_15_DEST_ADDR_REG
Offset: 0x24C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.151 DESC_15_CONFIG_REG (Ask a Question)

Name: DESC_15_CONFIG_REG
Offset: 0x240
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.152 DESC_15_BYTE_COUNT_REG (Ask a Question)

Name: DESC_15_BYTE_COUNT_REG
Offset: 0x244
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.153 DESC_14_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_14_SOURCE_ADDR_REG
Offset: 0x228
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.154 DESC_14_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_14_NEXT_DESC_ADDR_REG
Offset: 0x230
Reset: 0x0
Property: Read/Write

Descriptor number/address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.155 DESC_14_DEST_ADDR_REG (Ask a Question)

Name: DESC_14_DEST_ADDR_REG
Offset: 0x22C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.156 DESC_14_CONFIG_REG (Ask a Question)

Name: DESC_14_CONFIG_REG
Offset: 0x220
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.157 DESC_14_BYTE_COUNT_REG (Ask a Question)

Name: DESC_14_BYTE_COUNT_REG
Offset: 0x224
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.158 DESC_13_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_13_SOURCE_ADDR_REG
Offset: 0x208
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.159 DESC_13_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_13_NEXT_DESC_ADDR_REG
Offset: 0x210
Reset: 0x0
Property: Read/Write

Descriptor number or address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.160 DESC_13_DEST_ADDR_REG (Ask a Question)

Name: DESC_13_DEST_ADDR_REG
Offset: 0x20C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.161 DESC_13_CONFIG_REG (Ask a Question)

Name: DESC_13_CONFIG_REG
Offset: 0x200
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN __TABLE__ 0 Â¤ Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain. Â¢ 1 Â¤ Descriptor is part of a chain __ENDTABLE__

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type: __TABLE__ 0b00 Â¤ No operation â€“ Suits pointing at external descriptors Â¢ 0b01 Â¤ Incrementing address Â¢ 0b10 Â¤ Fixed address Â¢ 0b11 Â¤ Unused __ENDTABLE__

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type: __TABLE__ 0b00 Â¤ No operation â€“ Suits pointing at external descriptors Â¢ 0b01 Â¤ Incrementing address Â¢ 0b10 Â¤ Fixed address Â¢ 0b11 Â¤ Unused __ENDTABLE__

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.162 DESC_13_BYTE_COUNT_REG (Ask a Question)

Name: DESC_13_BYTE_COUNT_REG
Offset: 0x204
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.163 DESC_12_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_12_SOURCE_ADDR_REG
Offset: 0x1E8
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.164 DESC_12_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_12_NEXT_DESC_ADDR_REG
Offset: 0x1F0
Reset: 0x0
Property: Read/Write

Descriptor number or address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.165 DESC_12_DEST_ADDR_REG (Ask a Question)

Name: DESC_12_DEST_ADDR_REG
Offset: 0x1EC
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.166 DESC_12_CONFIG_REG (Ask a Question)

Name: DESC_12_CONFIG_REG
Offset: 0x1E0
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.167 DESC_12_BYTE_COUNT_REG (Ask a Question)

Name: DESC_12_BYTE_COUNT_REG
Offset: 0x1E4
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.168 DESC_11_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_11_SOURCE_ADDR_REG
Offset: 0x1C8
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.169 DESC_11_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_11_NEXT_DESC_ADDR_REG
Offset: 0x1D0
Reset: 0x0
Property: Read/Write

Descriptor number or address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.170 DESC_11_DEST_ADDR_REG (Ask a Question)

Name: DESC_11_DEST_ADDR_REG
Offset: 0x1CC
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.171 DESC_11_CONFIG_REG (Ask a Question)

Name: DESC_11_CONFIG_REG
Offset: 0x1C0
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.172 DESC_11_BYTE_COUNT_REG (Ask a Question)

Name: DESC_11_BYTE_COUNT_REG
Offset: 0x1C4
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.173 DESC_10_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_10_NEXT_DESC_ADDR_REG
Offset: 0x1B0
Reset: 0x0
Property: Read/Write

Descriptor number or address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.174 DESC_10_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_10_SOURCE_ADDR_REG
Offset: 0x1A8
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.175 DESC_10_DEST_ADDR_REG (Ask a Question)

Name: DESC_10_DEST_ADDR_REG
Offset: 0x1AC
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.176 DESC_10_CONFIG_REG (Ask a Question)

Name: DESC_10_CONFIG_REG
Offset: 0x1A0
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

4.177 DESC_10_BYTE_COUNT_REG (Ask a Question)

Name: DESC_10_BYTE_COUNT_REG
Offset: 0x1A4
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.178 DESC_0_SOURCE_ADDR_REG (Ask a Question)

Name: DESC_0_SOURCE_ADDR_REG
Offset: 0x068
Reset: 0x0
Property: Read/Write

Start address to source data from for the DMA store operation.

Bit	31	30	29	28	27	26	25	24
	SOURCE_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SOURCE_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SOURCE_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SOURCE_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SOURCE_ADDR[31:0] Address to start the AXI read operation from during a store and forward operation.

4.179 DESC_0_NEXT_DESC_ADDR_REG (Ask a Question)

Name: DESC_0_NEXT_DESC_ADDR_REG
Offset: 0x070
Reset: 0x0
Property: Read/Write

Descriptor number or address of the next internal/external descriptor in the chain.

Bit	31	30	29	28	27	26	25	24
	DESC_NUM_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DESC_NUM_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DESC_NUM_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DESC_NUM_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESC_NUM_ADDR[31:0] Address or number of the next descriptor in the chain. This register is ignored if the Chain bit is not set in the Configuration register of this descriptor. The value specified to this register depends on the External Descriptor bit in the Configuration register.

Value	Description
0	Specify the internal descriptor number.
1	Specify the address of the external descriptor.

4.180 DESC_0_DEST_ADDR_REG (Ask a Question)

Name: DESC_0_DEST_ADDR_REG
Offset: 0x06C
Reset: 0x0
Property: Read/Write

Start address to forward data to for the DMA forward operation.

Bit	31	30	29	28	27	26	25	24
	DEST_ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DEST_ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DEST_ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEST_ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DEST_ADDR[31:0] Address to start the AXI write operation to during a store and forward operation.

4.181 DESC_0_BYTE_COUNT_REG (Ask a Question)

Name: DESC_0_BYTE_COUNT_REG
Offset: 0x064
Reset: 0x0
Property: Read/Write

Number of bytes to be transferred in the DMA operation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		NUMBER_OF_BYTES[22:16]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NUMBER_OF_BYTES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NUMBER_OF_BYTES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – NUMBER_OF_BYTES[22:0] Number of bytes to be transferred as part of the DMA operation. Maximum permitted is ~ 8 MB (8,388,608 bytes).

4.182 DESC_0_CONFIG_REG (Ask a Question)

Name: DESC_0_CONFIG_REG
Offset: 0x060
Reset: 0x0
Property: Read/Write

Register for configuring the DMA operation performed from by descriptor.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DESCRIPTOR_VALID	DEST_DATA_READY	SOURCE_DATA_VALID	INTR_ON_PROCESS	EXT_DESC	CHAIN		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					DESTINATION_OPR[1:0]		SOURCE_OPR[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 15 – DESCRIPTOR_VALID Indicates that this is a valid descriptor. Provides firmware with a mechanism to safely de-allocate buffer descriptors and prevents lock ups from external start inputs being triggered at start-up before firmware has defined a valid descriptor. This bit is automatically cleared when any field of this Configuration register is written. The bit should be subsequently reset by firmware when the descriptor is valid. This field needs to be set from a UIC script if a UIC script is used to predefine descriptors in memory. It is not recommended to modify descriptors that are kicked off using an external start input. Once a DMA operation has been initiated this bit is no longer referenced. Therefore an invalid descriptor interrupt will not be generated if a descriptor in operation is modified.

Bit 14 – DEST_DATA_READY Indicates that there is room for data at the destination. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for a buffer to be allocated at the destination. The operation defined in this descriptor will not be performed until this bit is set. The Destination Data Ready bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 13 – SOURCE_DATA_VALID Indicates that data is valid at the source. Useful for chain and cyclic operations to prevent the DMA controller from hogging the AXI DMA bus waiting for valid data at the source. The operation defined in this descriptor will not be performed until this bit is set. The Source Data Valid bit is cleared by the DMA controller every time that the operation defined in this descriptor has been completed. The control Initiator (firmware) must set this bit again for cyclic operations.

Bit 12 – INTR_ON_PROCESS Generates an interrupt when this descriptor has been processed as part of a chain. Setting this bit for the last descriptor in a non-cyclic chain has no effect. DMA operations are not halted on this channel when an interrupt is generated via this bit. DMA operations will only be paused as a result of this bit being set if the Interrupt Status bit associated with this descriptor is not clear in the Interrupt Clear

register after an interrupt has been fired resulting in the interrupt queue associated with this descriptor (and possibly other channels) becoming full.

Bit 11 – EXT_DESC The content of this field is irrelevant if the chain bit is not set.

Value	Description
0	Internal buffer descriptor.
1	External buffer descriptor.

Bit 10 – CHAIN

Value	Description
0	Buffer descriptor describes a single DMA operation or the last descriptor in a non-cyclic chain.
1	Descriptor is part of a chain.

Bits 3:2 – DESTINATION_OPR[1:0] Forward operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

Bits 1:0 – SOURCE_OPR[1:0] Store operation type.

Value	Description
0b00	No operation. Suits pointing at external descriptors.
0b01	Incrementing address.
0b10	Fixed address.
0b11	Unused.

5. Additional References (Ask a Question)

This section provides a list for additional information.

For updates and additional information about the software, devices, and hardware, visit the **Intellectual Property** pages on the Microchip FPGA Intellectual Property Cores.

5.1 Known Issues and Workarounds (Ask a Question)

There are no known limitations and workarounds in the CoreAXI4DMAController v2.2.

5.2 Discontinued Features and Devices (Ask a Question)

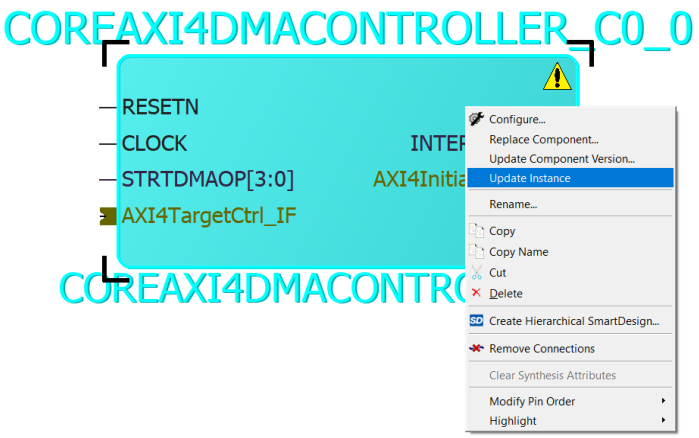
There were no discontinued features and devices in the CoreAXI4DMAController v2.2 release.

5.3 Migration (Ask a Question)

When migrating to CoreAXI4DMAController v2.2 from earlier versions, the users must expect to see changes in the SmartDesign and Logs window.

The following figure shows the updated SmartDesign view.

Figure 5-1. Updated SmartDesign to CoreAXI4DMAController v2.2 using Update Component Version Option



The log messages window while migrating to CoreAXI4DMAController v2.2 is shown in the following figure.

Figure 5-2. Log Messages Window

Message	Message ID	Source Location	Log Location
Design Entry			
SmartDesign Check (5 Error(s))			
You must create at least one port for a valid design	-	No Top Level Ports	-
Component definition is not consistent for instance COREAXI4DMACONTROLLER_C0_0	-	Out-of-date Instar	-
Unconnected input pin COREAXI4DMACONTROLLER_C0_0:RESETN	-	Undriven Pin	-
Unconnected input pin COREAXI4DMACONTROLLER_C0_0:CLOCK	-	Undriven Pin	-
Unconnected input pin COREAXI4DMACONTROLLER_C0_0:STRTDMAOP[3:0]	-	Undriven Pin	-
HDL Check			

Important: User must safely ignore such errors reported in the log window.

6. Glossary (Ask a Question)

The following are the list of terms and definitions used in the document.

Table 6-1. Terms and Definitions

Term	Definition
AXI	Advanced eXtensible Interface
BD	Buffer Descriptor
DMA	Direct Memory Access
FIFO	First In First Out
UIC	User Initialization Commands
UUT	User Under Test

7. Resolved Issues (Ask a Question)

The following table lists the issues that were resolved in the releases.

Table 7-1. Resolved Issues

Release	Description
2.2	The following is the list of all resolved issues in the v2.2 release: • Addressed the issue with interrupt width observed while performing the simulation • Addressed the register access issue when all bits of the write strobe (AXI4-Lite interface) are zero
2.1	The following is the list of all resolved issues in the v2.1 release: • CoreAXI4DMAController hang issue when accessing register addresses in between the descriptor set • CoreAXI4DMAController is shown in catalog for RTG4™ • PRIO_0_NUM_OF_BEATS min limit issue • TSTRB must be “AXI_DMA_DWIDTH/8” • Combinational loops when stream support is enabled CoreAXI4DMAController query on “STRTDMAOP” behavior • Multiple chain DMA issue • Not getting TREADY in STREAM transaction • Not getting “invalid desc” bit set in the interrupt status
2.0	First Release

8. Device Utilization and Performance (Ask a Question)

Utilization and performance data are listed in the following tables for their respective device families. The data listed in the following tables are indicative only. The overall device utilization and performance of the core is system dependent.

Table 8-1. CoreAXI4DMAController Device Utilization and Performance for PolarFire SoC Family (AXI4-Stream Disabled)

Family	Logic Elements			Performance (MHz)
	Sequential	Combinatorial	Total	
PolarFire® SoC (32-bit)	2743	4047	6790	203.25
PolarFire SoC (64-bit)	2975	4213	7188	202.76
PolarFire SoC (128-bit)	3434	4614	8048	198.26
PolarFire SoC (256-bit)	4308	6088	10396	194.33
PolarFire SoC (512-bit)	6088	7080	13168	197.43

Important: The data in the preceding table is achieved using Verilog RTL, with the following synthesis and layout settings (Timing-driven mode, high-effort) on a –1 speed grade part.

Table 8-2. CoreAXI4DMAController Device Utilization and Performance for PolarFire SoC Family (AXI4-Stream Enabled)

Family	Logic Elements			Performance (MHz)
	Sequential	Combinatorial	Total	
PolarFire® SoC (32-bit)	3503	5642	9145	197.01
PolarFire SoC (64-bit)	3891	5992	9883	183.35
PolarFire SoC (128-bit)	4588	6788	11376	184.95
PolarFire SoC (256-bit)	5941	8210	14151	177.49
PolarFire SoC (512-bit)	8735	11212	19947	192.6

Important: The data in the preceding table is achieved using Verilog RTL, with the following synthesis and layout settings (Timing-driven mode, high-effort) on a –1 speed grade part.

Table 8-3. CoreAXI4DMAController Device Utilization and Performance for PolarFire Family (AXI4-Stream Disabled)

Family	Logic Elements			Performance (MHz)
	Sequential	Combinatorial	Total	
PolarFire® (32-bit)	2743	4047	6790	203.25
PolarFire (64-bit)	2975	4213	7188	202.76
PolarFire (128-bit)	3434	4614	8048	198.26
PolarFire (256-bit)	4308	6088	10396	194.33
PolarFire (512-bit)	6088	7080	13168	197.43

Important: The data in the preceding table is achieved using Verilog RTL, with the following synthesis and layout settings (Timing-driven mode, high-effort) on a –1 speed grade part.

Table 8-4. CoreAXI4DMAController Device Utilization and Performance for PolarFire Family (AXI4-Stream Enabled)

Family	Logic Elements			Performance (MHz)
	Sequential	Combinatorial	Total	
PolarFire® (32-bit)	3503	5642	9145	197.01
PolarFire (64-bit)	3891	5992	9883	183.35
PolarFire (128-bit)	4588	6788	11376	184.95
PolarFire (256-bit)	5941	8210	14151	177.49
PolarFire (512-bit)	8735	11212	19947	192.6

Important: The data in the preceding table is achieved using Verilog RTL, with the following synthesis and layout settings (Timing-driven mode, high-effort) on a –1 speed grade part.

Table 8-5. CoreAXI4DMAController Device Utilization and Performance for RTG4 Family (AXI4-Stream Disabled)

Family	Logic Elements			Performance (MHz)
	Sequential	Combinatorial	Total	
RTG4™ (32-bit)	2974	4198	7172	196.309
RTG4 (64-bit)	3212	4465	7677	190.512
RTG4 (128-bit)	3689	4953	8462	185.322
RTG4 (256-bit)	4628	5754	10382	181.422
RTG4 (512-bit)	6449	7343	13792	185.357

Important: The data in the preceding table is achieved using Verilog RTL, with the following synthesis and layout settings (Timing-driven mode, high-effort) on a –1 speed grade part.

Table 8-6. CoreAXI4DMAController Device Utilization and Performance for RTG4 Family (AXI4-Stream Enabled)

Family	Logic Elements			Performance (MHz)
	Sequential	Combinatorial	Total	
RTG4™ (32-bit)	3748	5672	9420	181.061
RTG4 (64-bit)	4119	6101	10220	173.883
RTG4 (128-bit)	5251	7181	12432	164.76
RTG4 (256-bit)	6384	8261	14645	155.642
RTG4 (512-bit)	9249	11053	20302	165.207

Important: The data in the preceding table is achieved using Verilog RTL, with the following synthesis and layout settings (Timing-driven mode, high-effort) on a –1 speed grade part.

Table 8-7. CoreAXI4DMAController Device Utilization and Performance for SmartFusion 2 Family (AXI4-Stream Disabled)

Family	Logic Elements			Performance (MHz)
	Sequential	Combinatorial	Total	
SmartFusion® 2 (32-bit)	2964	4187	7151	236.967
SmartFusion 2 (64-bit)	3211	4431	7642	243.072
SmartFusion 2 (128-bit)	3693	4963	8656	229.621
SmartFusion 2 (256-bit)	4634	5777	10411	233.318

.....continued

Family	Logic Elements			Performance (MHz)
	Sequential	Combinatorial	Total	
SmartFusion 2 (512-bit)	6455	7345	13800	226.193

Important: The data in the preceding table is achieved using Verilog RTL, with the following synthesis and layout settings (Timing-driven mode, high-effort) on a –1 speed grade part.

Table 8-8. CoreAXI4DMAController Device Utilization and Performance for SmartFusion 2 Family (AXI4-Stream Enabled)

Family	Logic Elements			Performance (MHz)
	Sequential	Combinatorial	Total	
SmartFusion® 2 (32-bit)	3736	5634	9370	239.808
SmartFusion 2 (64-bit)	4125	6061	10186	234.797
SmartFusion 2 (128-bit)	5257	7172	12429	228.333
SmartFusion 2 (256-bit)	6389	8283	14672	221.877
SmartFusion 2 (512-bit)	9255	11014	20269	211.416

Important: The data in the preceding table is achieved using Verilog RTL, with the following synthesis and layout settings (Timing-driven mode, high-effort) on a –1 speed grade part.

Table 8-9. CoreAXI4DMAController Device Utilization and Performance for IGLOO 2 Family (AXI4-Stream Disabled)

Family	Logic Elements			Performance (MHz)
	Sequential	Combinatorial	Total	
IGLOO ®2 (32-bit)	2964	4187	7151	236.967
IGLOO 2 (64-bit)	3211	4431	7642	243.072
IGLOO 2 (128-bit)	3693	4963	8656	229.621
IGLOO 2 (256-bit)	4634	5777	10411	233.318
IGLOO 2 (512-bit)	6455	7345	13800	226.193

Important: The data in the preceding table is achieved using Verilog RTL, with the following synthesis and layout settings (Timing-driven mode, high-effort) on a –1 speed grade part.

Table 8-10. CoreAXI4DMAController Device Utilization and Performance for IGLOO 2 Family (AXI4-Stream Enabled)

Family	Logic Elements			Performance (MHz)
	Sequential	Combinatorial	Total	
IGLOO® 2 (32-bit)	3736	5634	9370	239.808
IGLOO 2 (64-bit)	4125	6061	10186	234.797
IGLOO 2 (128-bit)	5257	7172	12429	228.333
IGLOO 2 (256-bit)	6389	8283	14672	221.877
IGLOO 2 (512-bit)	9255	11014	20269	211.416

Important: The data in the preceding table is achieved using Verilog RTL, with the following synthesis and layout settings (Timing-driven mode, high-effort) on a –1 speed grade part.

9. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 9-1. Revision History

Revision	Date	Description
A	06/2024	The following is a summary of the changes in revision A of this document: • The document was migrated to the Microchip template • The document number was updated from HB0739 to DS50003714 • Updated the document for CoreAXI4DMAController v2.2. • Updated Figure 1-1 in 1.1. Architecture section • Updated Figure 3-1 in 3.1. SmartDesign section • Updated Figure 3-3 in 3.2.1. Testbench section • Added 7. Resolved Issues section
2.0	—	The following is a summary of the changes in revision 2.0 of this document: • Updated the document for CoreAXI4DMAController v2.1 • Updated Supported Families section • Updated 8. Device Utilization and Performance section • Updated the following tables: – 2.2. Inputs and Outputs Signals – 2.1. Configuration of GUI Parameters – Interrupt X Status Register Bit Definitions • Added Notes in Register Map Descriptions, Interrupt X Status Register Bit Definitions, Interrupt X Mask Register Bit Definitions, and Descriptor X Configuration Register Bit Definitions. • Removed Obfuscation section • Added RTL section • Updated SmartDesign section • Replaced SmartDesign CoreAXI4DMAController Instance View and SmartDesign CoreAXI4DMAController Configuration Dialog Box figures
1.0	—	The first publication of this document. Created for CoreAXI4DMAController v2.0.

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