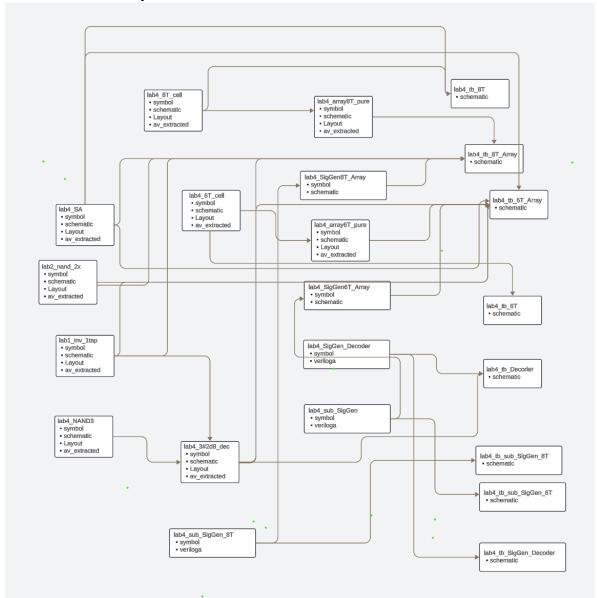
Overall hierarchy



Submitted files.

- Readme.
- Video.
- ece4740.zip.

To use files

- 1. Unzip ece4740.zip in the Cadence directory.
- 2. Ensure that the above files are present in the hierarchy.
- 3. Use the following steps to obtain desired results.

lab4_6T_cell testing

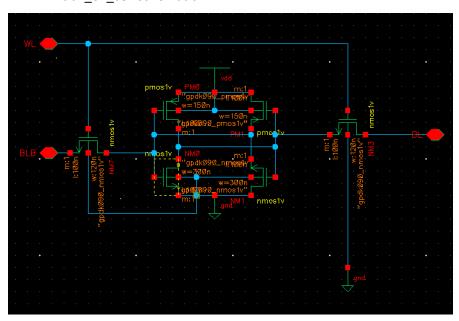
DRC/LVS on lab4_6T_cell

- 1. Open lab4_6T_cell layout
- 2. Run DRC check.
- 3. Run LVS check.

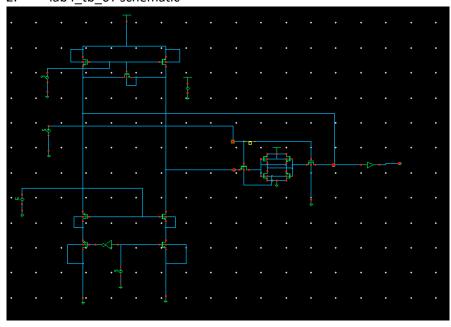
Lab4_tb_6T

Run the testbench.

1. Lab4_6T_cell schematic



2. lab4_tb_6T schematic

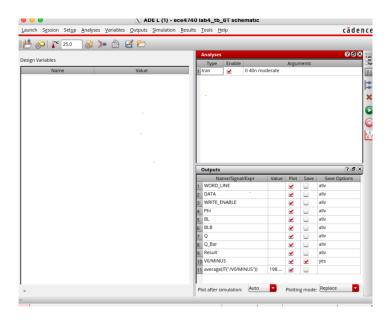


WL:01000000100010000000100

Phi_BAR: 1111000011111111100001111

Write_Enable: 11110000000111100000000

Data: 000000000001111111111111



lab4_8T_cell testing

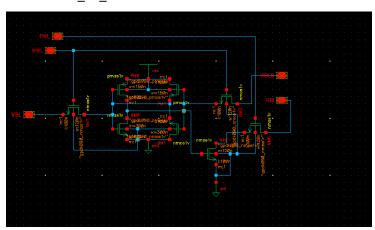
DRC/LVS on lab4_8T_cell

- 1. open lab4_8T_cell layout
- 2.Run DRC check.
- 3. Run LVS check.

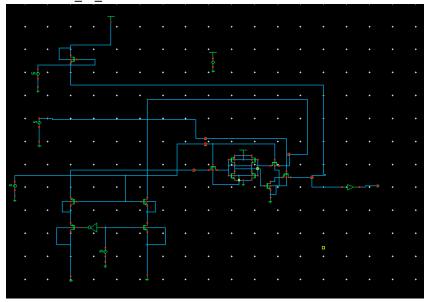
Lab4_tb_8T

Run the testbench.

1. Lab4_8T_cell schematic



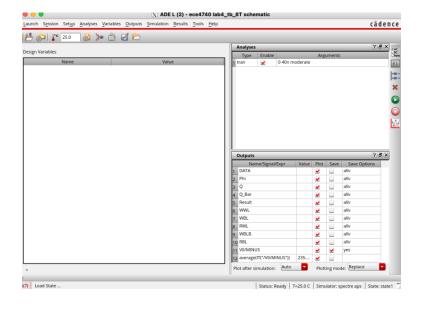
2 lab4_tb_8T schematic



Testing Vector for 8T CELL

RWL: 0000000010000000000100

Phi: 111100001111111100001111



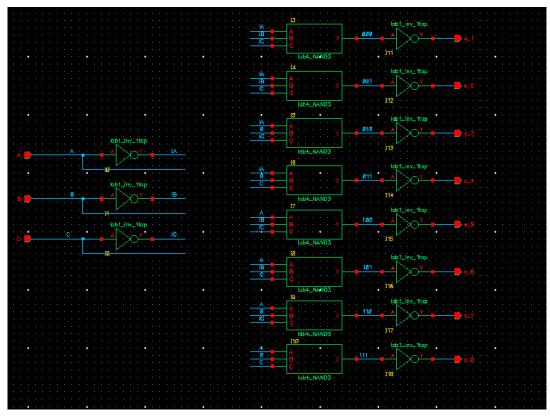
Decoder Testing

DRC/LVS on lab4 3-8 Dec layout

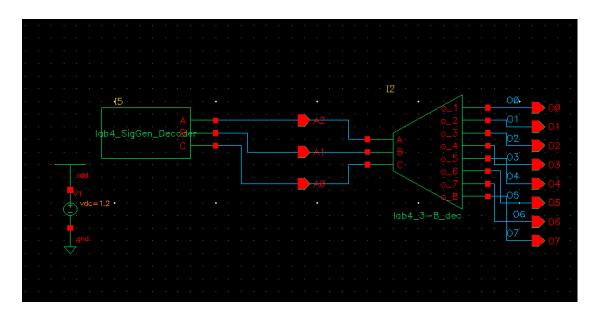
- 1.open lab4 3-8 dec layout
- 2.Run DRC check.
- 3. Run LVS check.

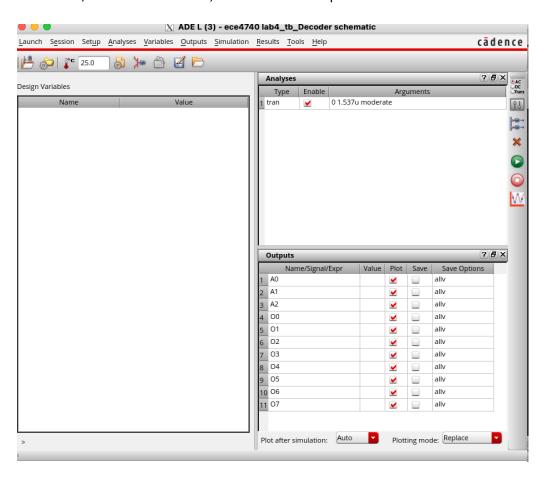
Run the testbench.

1. Lab4 3-8 dec schematic



2. lab4_tb_decoder schematic



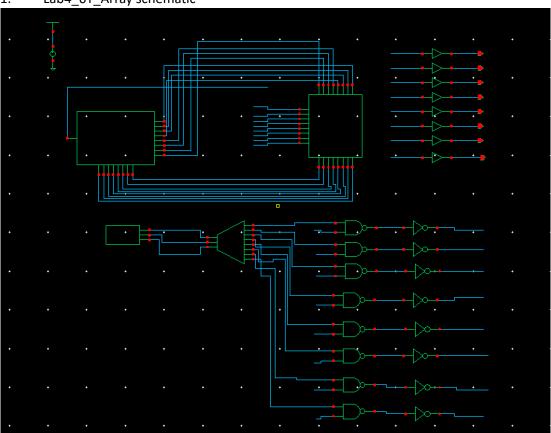


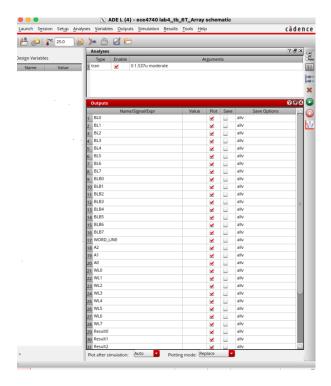
lab4_6T_Array testing

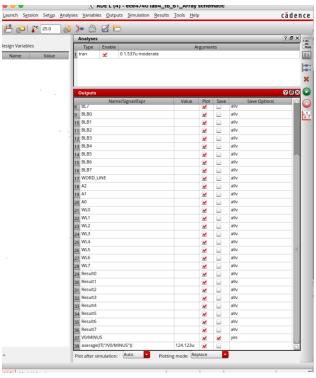
Lab4_tb_6T

Run the testbench.

1. Lab4_6T_Array schematic







lab4_8T_Array testing

Lab4_tb_8T

Run the testbench.

1. Lab4_8T_Array schematic

