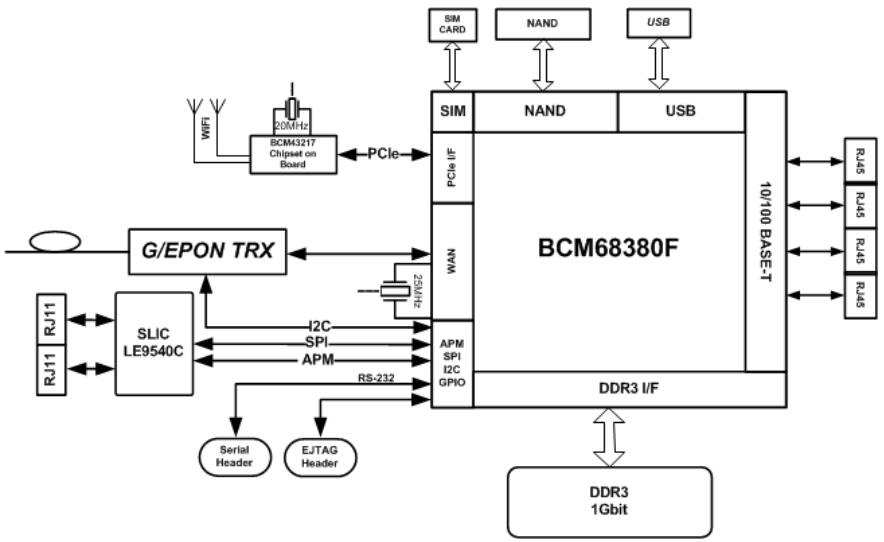
BCM968380FHGU

BCM968380FHGU - TOC

Reference Design - Block Diagram



Revision History

See last page for detailed changes list

REVISION	ECO	DATE	REWORK	REASON
X100			N/A	Preliminary
P103		Feb 28, 2013	N/A	Release to fabrication
P104		Mar 08, 2013	N/A	Correct HVG_IN and HVG_FB resistor values
P201		Mar 13, 2013	N/A	Layout change to correct BCM68380F symbol
P301		Apr 18, 2013	N/A	Connect Jtag RST to SYS_RESET_B
P302		Apr 29, 2013	N/A	Various minor changes
P401		July 28, 2013	N/A	Updated HVG circuit

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Title: BCM968380FHGU - Block Diagram

Size: A3 | Document Number: 824-125279-0040 (P401) | Rev: 01

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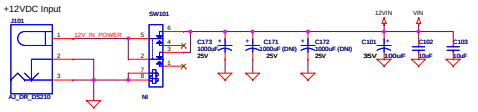
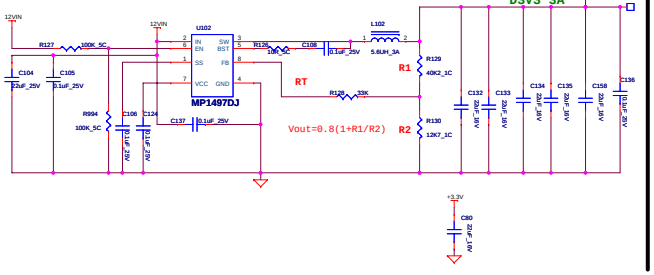
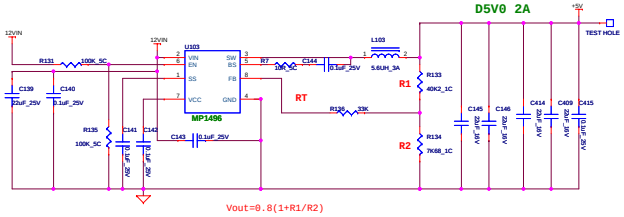
Power in

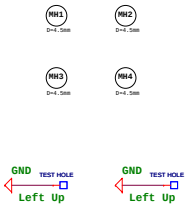


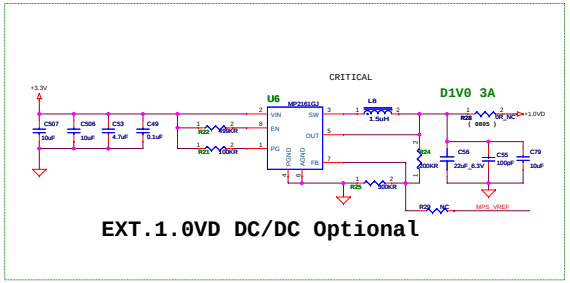
3.3V 3A DC/DC
Single power supply

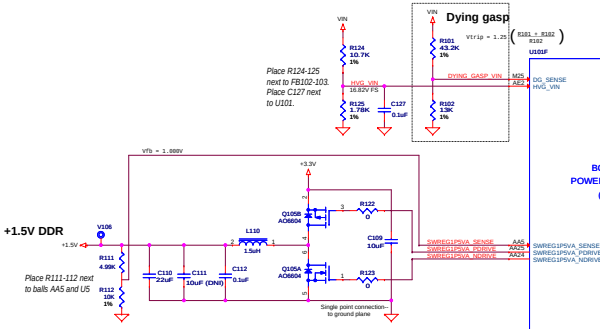


5V 2A DC/DC
FOR USB (If Populate)









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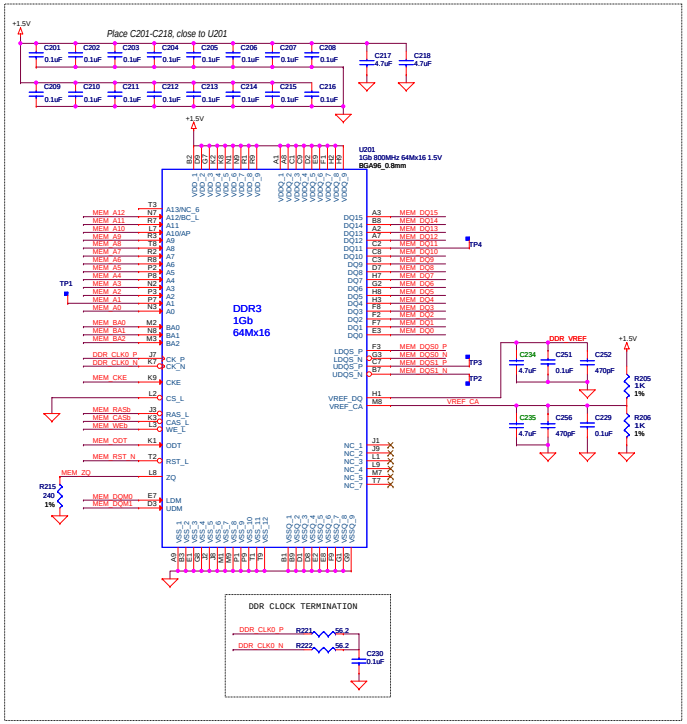
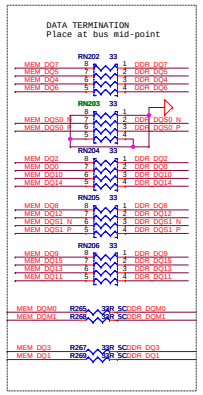
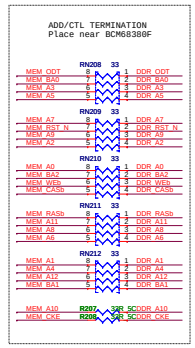
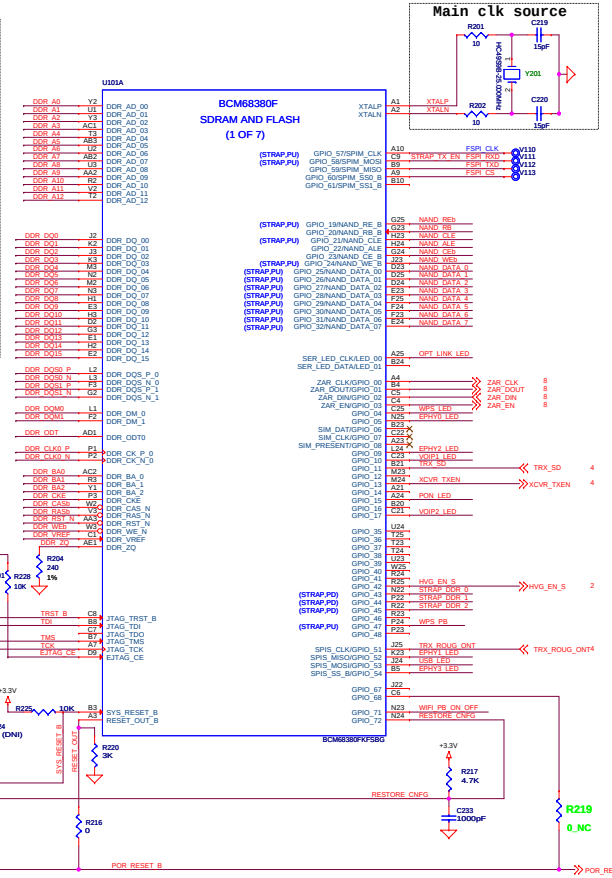
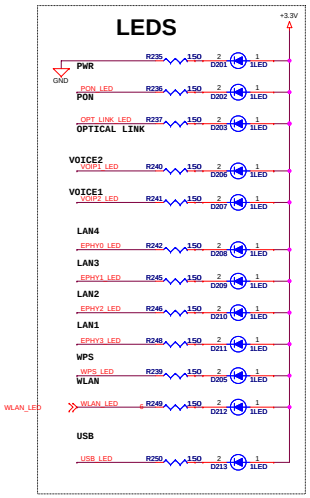
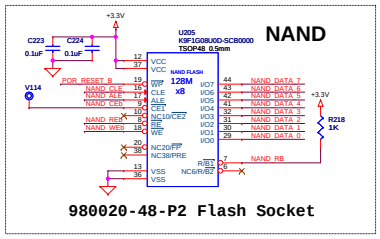












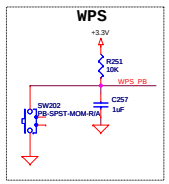
Strap Bit	Description				Default	
RESERVED	GPIO47				1	Don't put pull-down
RESERVED	GPIO31				1	Don't put pull-down
RESERVED	GPIO57				1	Don't put pull-down
RESERVED	GPIO28 GPIO29 GPOI30				1 1 1	Don't put pull-down Don't put pull-down Don't put pull-down
	BOOT_CFG[2:0]	STRAP_NAND_[1:0]	STRAP_NAND_[2:3]	Boot source	ECC	
boot_cfg_2\ GPIO21	100 101			SPI, 3 byte addressing SPI, 4 byte addressing		
boot_cfg_1\ GPIO22	111 111	1X 10	XX 00	NAND, Pre-Defined / ONFI / JEDEC Flash ID NAND, Pre-Defined / ONFI / JEDEC Flash ID	No ECC (debug / development) 1 bit ECC / 16 spare bytes	
boot_cfg_0\ GPOI32	111 111 111 111 110 000 001 010 011	10 10 10 10	01 10 11	NAND, Pre-Defined / ONFI / JEDEC Flash ID NAND, Pre-Defined / ONFI / JEDEC Flash ID NAND, Pre-Defined / ONFI / JEDEC Flash ID NAND NAND NAND NAND NAND	4 bit ECC / 16 spare bytes 8 bit ECC / 27 spare bytes 12 bit ECC / 27 spare bytes No ECC (debug / development) 1 bit ECC / 16 spare bytes 4 bit ECC / 16 spare bytes 8 bit ECC / 27 spare bytes 12 bit ECC / 27 spare bytes	
STRAP_NAND_0\ GPIO24 STRAP_NAND_1\ GPIO25	NAND page size: 00: 512 bytes 01: 2KB 10: 4KB 11: 8KB *** Relevant only in non-auto detect mode.**				1 1	Relevant only if NAND interface is used.
STRAP_NAND_2\ GPIO26 STRAP_NAND_3\ GPIO27	NAND row address size: 00: 1 byte 01: 2 bytes 10: 3 bytes 11: 4 bytes *** Relevant only in non-auto detect mode.**				1 1	Relevant only if NAND interface is used.
STRAP_NAND_BLK0_WP\ GPIO19	0: Write protect block 0 1: Do not write protect block 0				1	Relevant only if NAND interface is used.
STRAP_GPON_TX_EN\ GPIO58	0: Differential LVPECL 1: CMOS single ended				1	

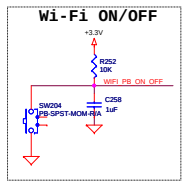
The DDR3 interface on the 2L board based on the 68380F chip must use the following straps in order to accommodate the correct frq. In order to achieve the supported freq (333MHz DDR3 clk rate) you need to use the following strap

DDR Strap	GPIO#	Value
STRAP_DDR_2	GPIO_45	0
STRAP_DDR_1	GPIO_44	1
STRAP_DDR_0	GPIO_43	0

PIN NAME	GPIO	STRAP NAME		+3.3V	STRAP pin has
STRAP_DDR_2	GPIO_45	DDR_CFG_2	R262	4.7K (DNI)	internal pull-down
STRAP_DDR_1	GPIO_44	DDR_CFG_1	R263	4.7K	internal pull-down
STRAP_DDR_0	GPIO_43	DDR_CFG_0	R264	4.7K (DNI)	internal pull-down

1	STRAP_TX_EN	GPIO_58	GPON_TX_EN	R253	4.7K (DNI) internal pull-up
1	NAND_CLE	GPIO_21	BOOT_CFG_0	R254	4.7K (DNI) internal pull-up
1	NAND_ALE	GPIO_22	BOOT_CFG_1	R255	4.7K (DNI) internal pull-up
1	NAND_DATA_7	GPIO_32	BOOT_CFG_2	R256	4.7K (DNI) internal pull-up
1	NAND_REb	GPIO_19	NAND_BLK0_WP	R257	4.7K (DNI) internal pull-up
0	NAND_WEb	GPIO_24	NAND_PAGE_SIZE_1	R258	4.7K internal pull-up
0	NAND_DATA_0	GPIO_25	NAND_PAGE_SIZE_0	R259	4.7K internal pull-up
0	NAND_DATA_1	GPIO_26	NAND_ADDR_SIZE_1	R260	4.7K internal pull-up
1	NAND_DATA_2	GPIO_27	NAND_ADDR_SIZE_0	R261	4.7K (DNI) internal pull-up





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Title: DDR3 AND FLASH MEMORY
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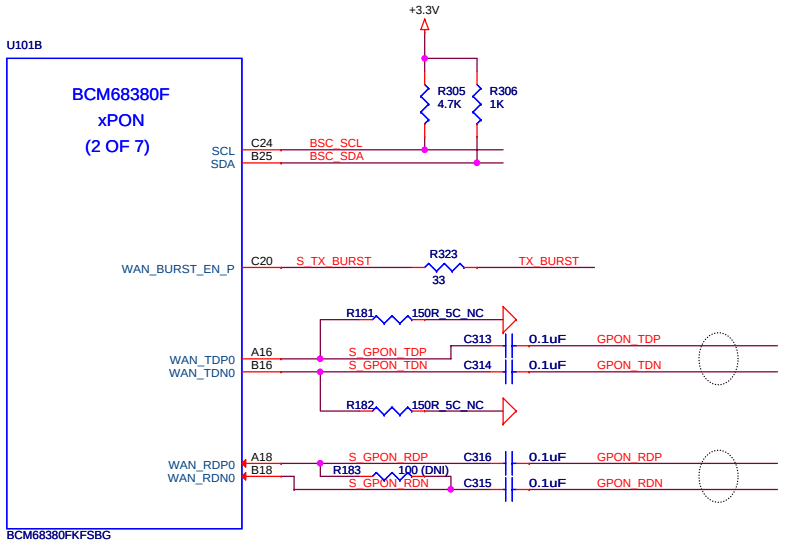
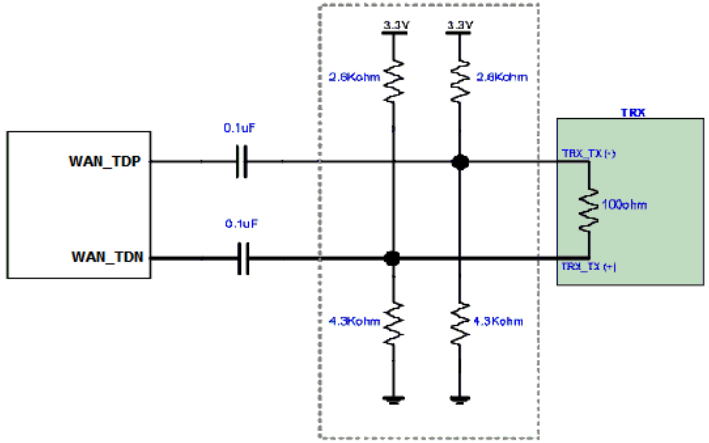
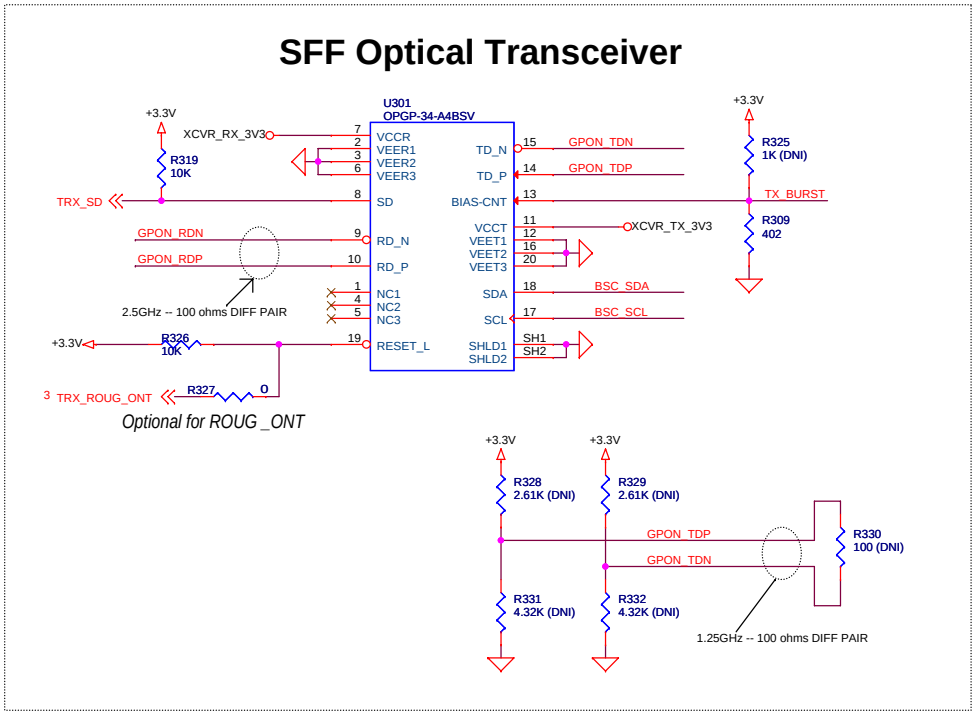
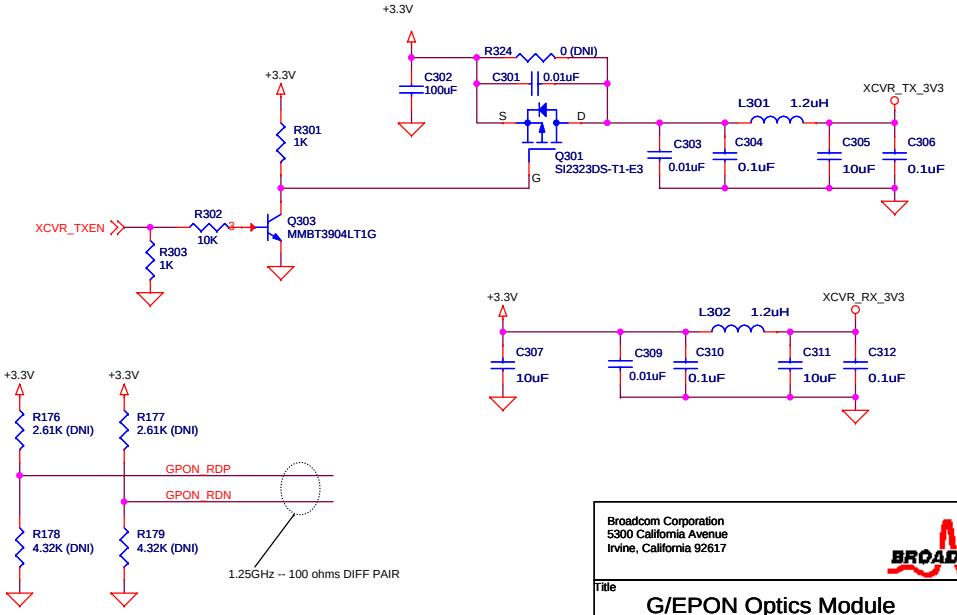




Note: Same connectivity for EPON and GPON Optical Transceivers





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Title	G/EPON Optics Module	
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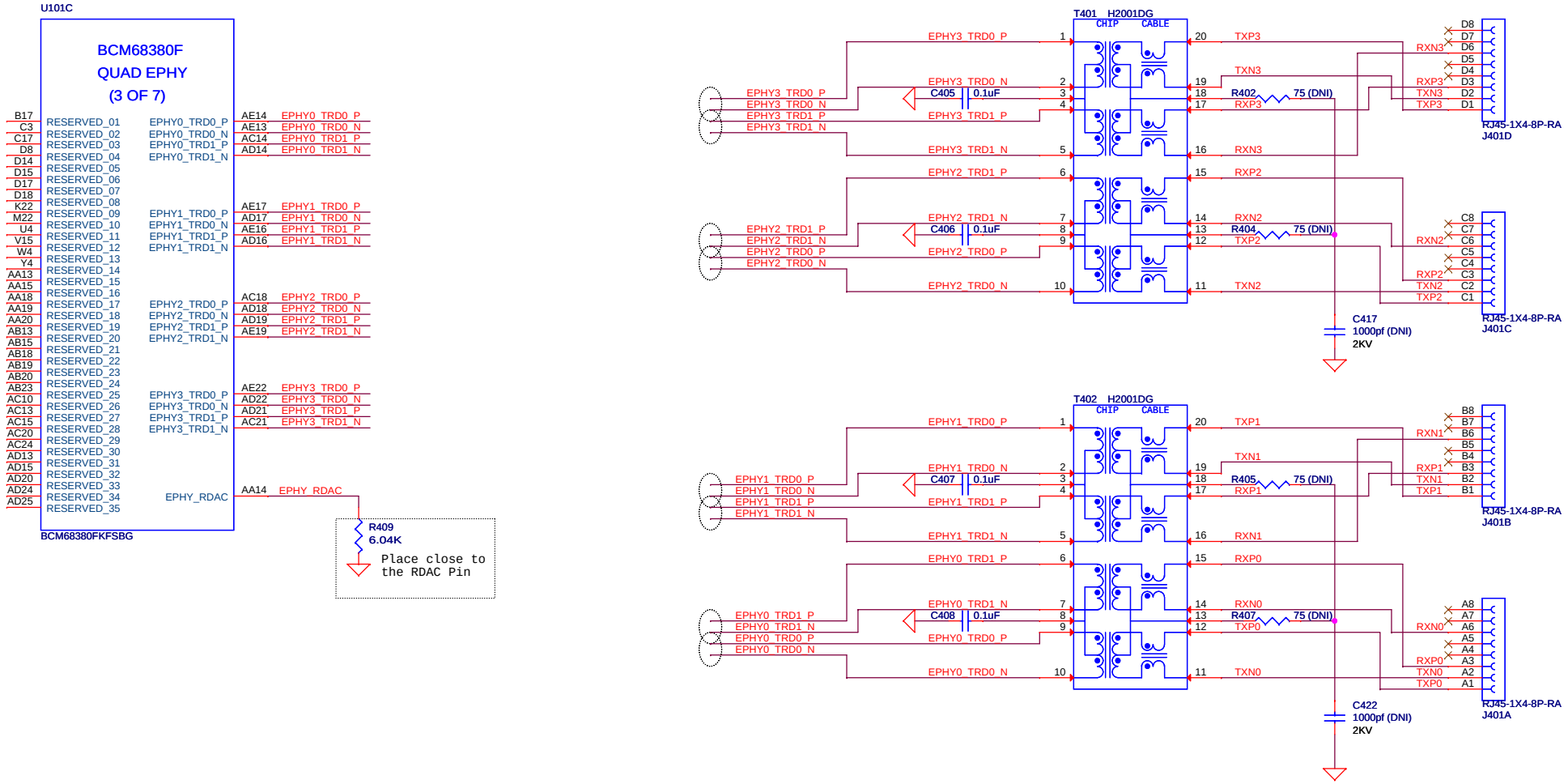
Route RD+/- and TD+/- pairs with
100-ohms differential trace immpedance



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Title: Quad EPHY

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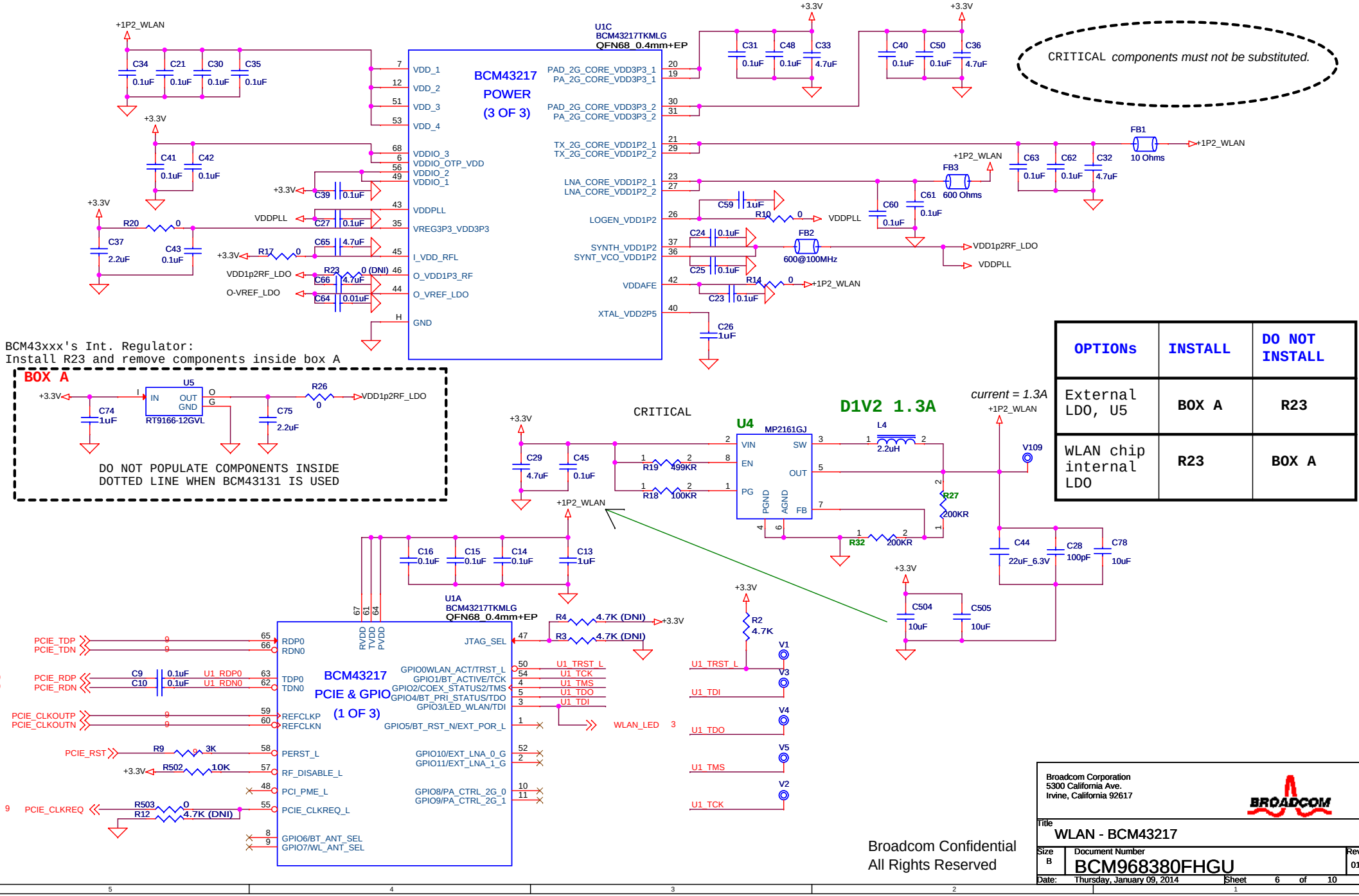

OPTIONs	INSTALL	DO NOT INSTALL
External LDO, U5	BOX A	R23
WLAN chip internal LDO	R23	BOX A

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Title: WLAN - BCM43217

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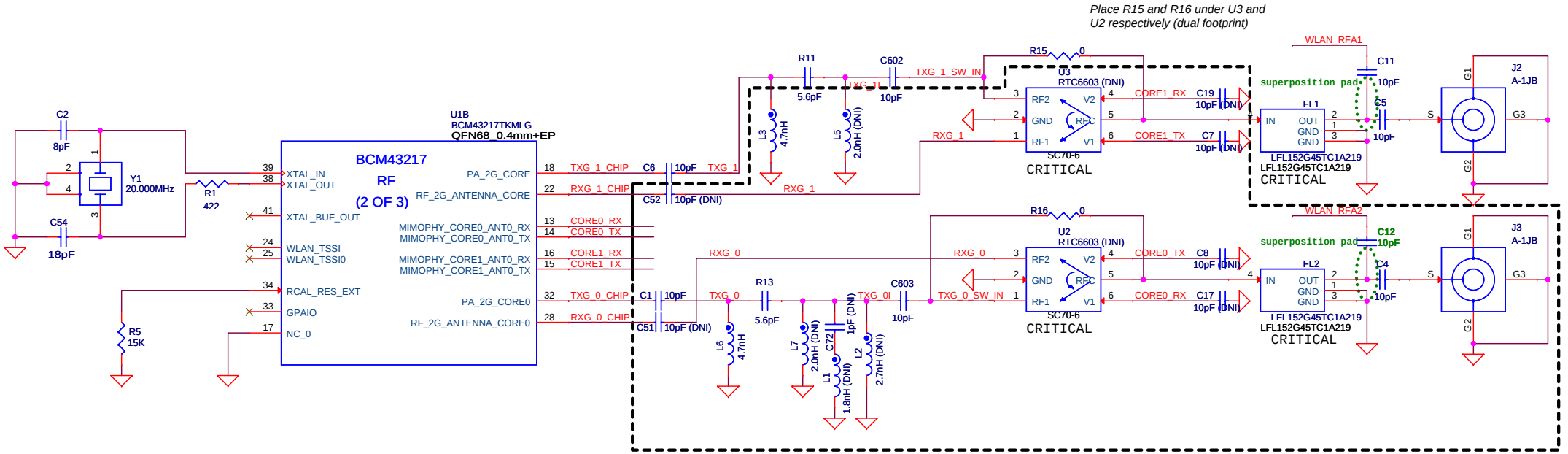
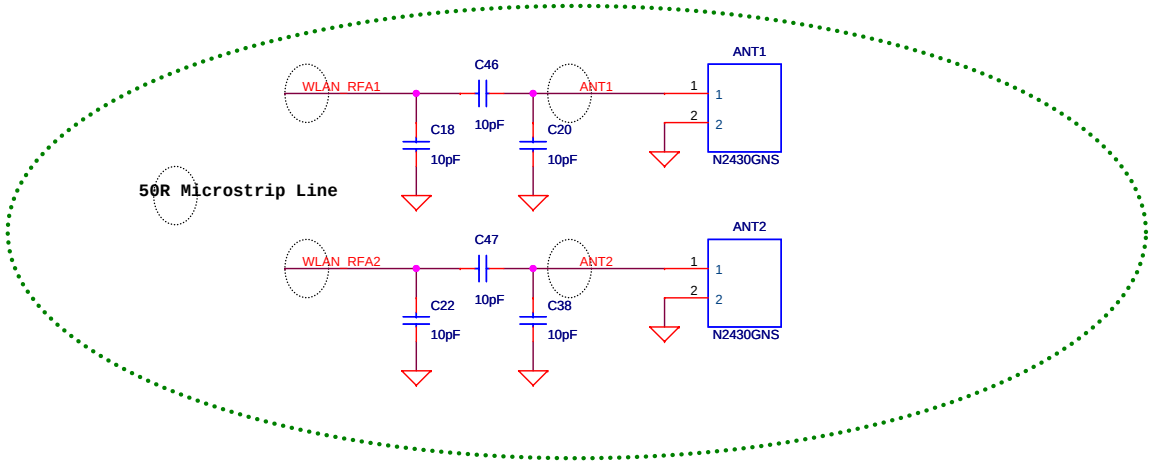
CRITICAL

components must not be substituted.



43217 with iTR (Internal T/R Switch):
Install R15 and R16 . DEPOP U3 and U2

43217 with eTR (External T/R Switch):
Install U3 and U2 . DEPOP R15 and R16



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Title	WLAN RF	
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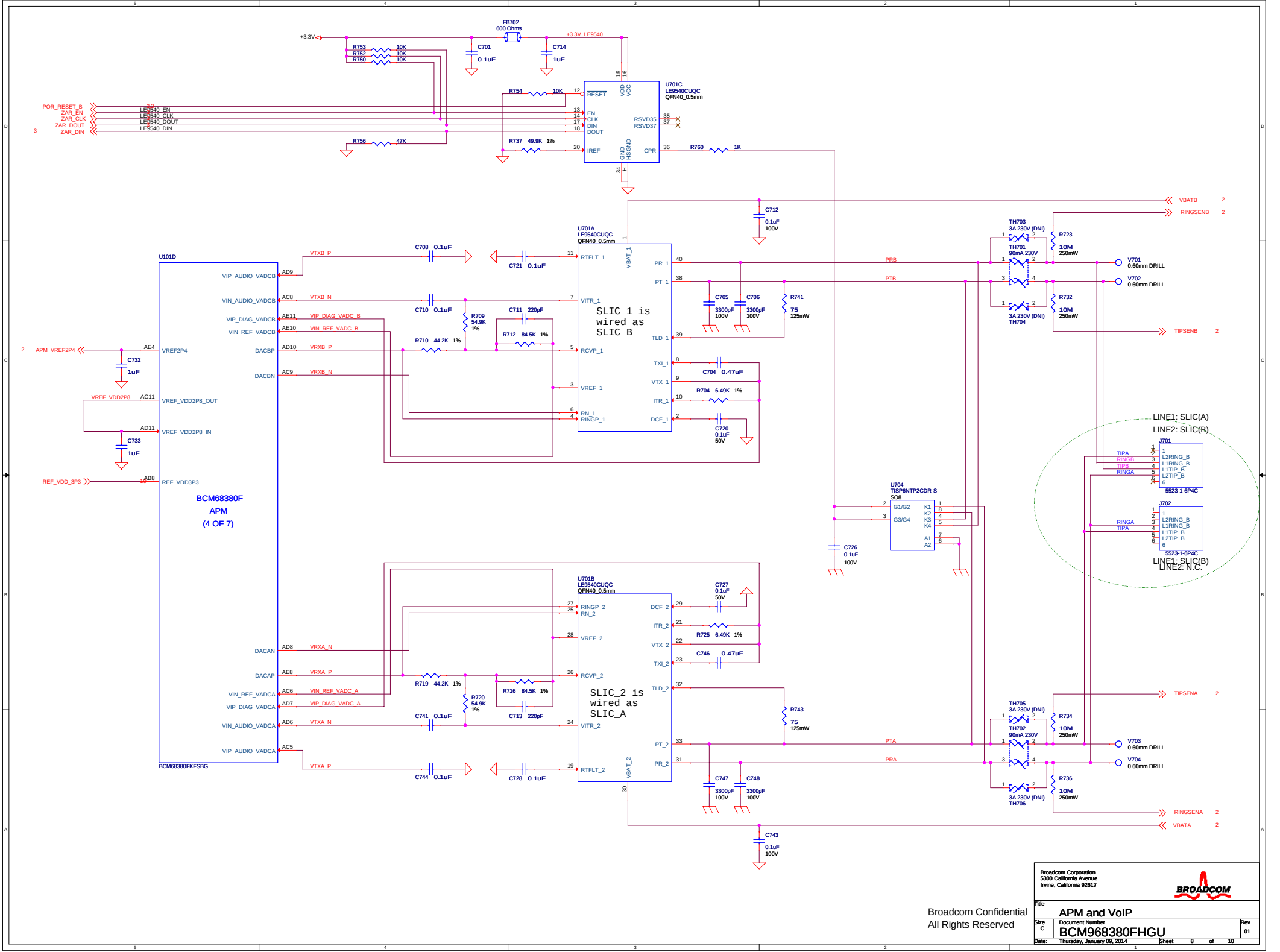
U101D
BCM68380F
APM
(4 OF 7)
BCM68380FKFSBG
U701A
LE9540CUQC
QFN40_0.5mm
SLIC_1 is wired as SLIC_B
U701B
LE9540CUQC
QFN40_0.5mm
SLIC_2 is wired as SLIC_A
U701C
LE9540CUQC
QFN40_0.5mm
FB702
600 Ohms
+3.3V
+3.3V_LE9540
POR_RESET_B
ZAR_EN
ZAR_CLK
ZAR_DOUT
ZAR_DIN
LE9540_EN
LE9540_CLK
LE9540_DOUT
LE9540_DIN
APM_VREF2P4
VREF_VDD2P8
REF_VDD_3P3
VTXB_P
VTXB_N
VIP_DIAG_VADC_B
VIN_REF_VADC_B
VRXB_P
VRXB_N
VRXA_N
VRXA_P
VIN_REF_VADC_A
VIP_DIAG_VADC_A
VTXA_N
VTXA_P
PRB
PTB
PTA
PRA
VBATB
RINGSENB
TIPSENB
TIPSENA
RINGSENA
VBATA
TH703
3A 230V (DNI)
TH701
90mA 230V
TH704
TH705
TH702
TH706
V701
V702
V703
V704
0.60mm DRILL
U704
TISP6NTP2CDR-S
SO8
J701
J702
5523-1-6P4C
LINE1: SLIC(A)
LINE2: SLIC(B)
LINE1: SLIC(B)
LINE2: N.C.
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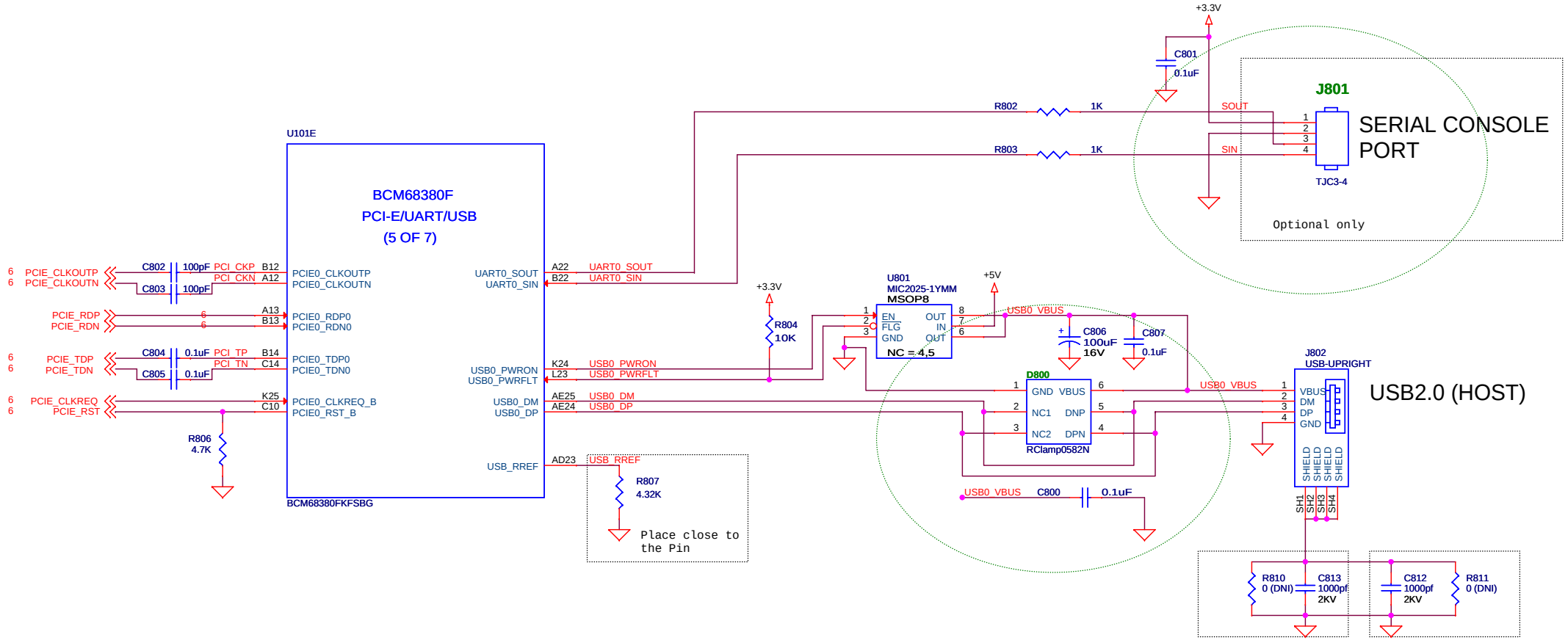

USB2.0 - Layout Guidelines & Notes

1. The Dp and Dn traces are length matched, with max differential skew, within 20mils
2. Differential trace length must be less than 5 inches
3. No more than 2 vias per trace, prefer zero.
4. Never split the ground plane under differential pair routing
5. Route differential pairs above the GND plane.
6. Differential impedance is 90 ohms for USB.
7. Adjacent differential pairs should be separated by at least 3 times the trace width. (e.g. 7.5 mil trace, leave >22.5mils between adjacent diff pairs)
8. Stitch gnd vias around each differential pair, but NOT between a given pair.

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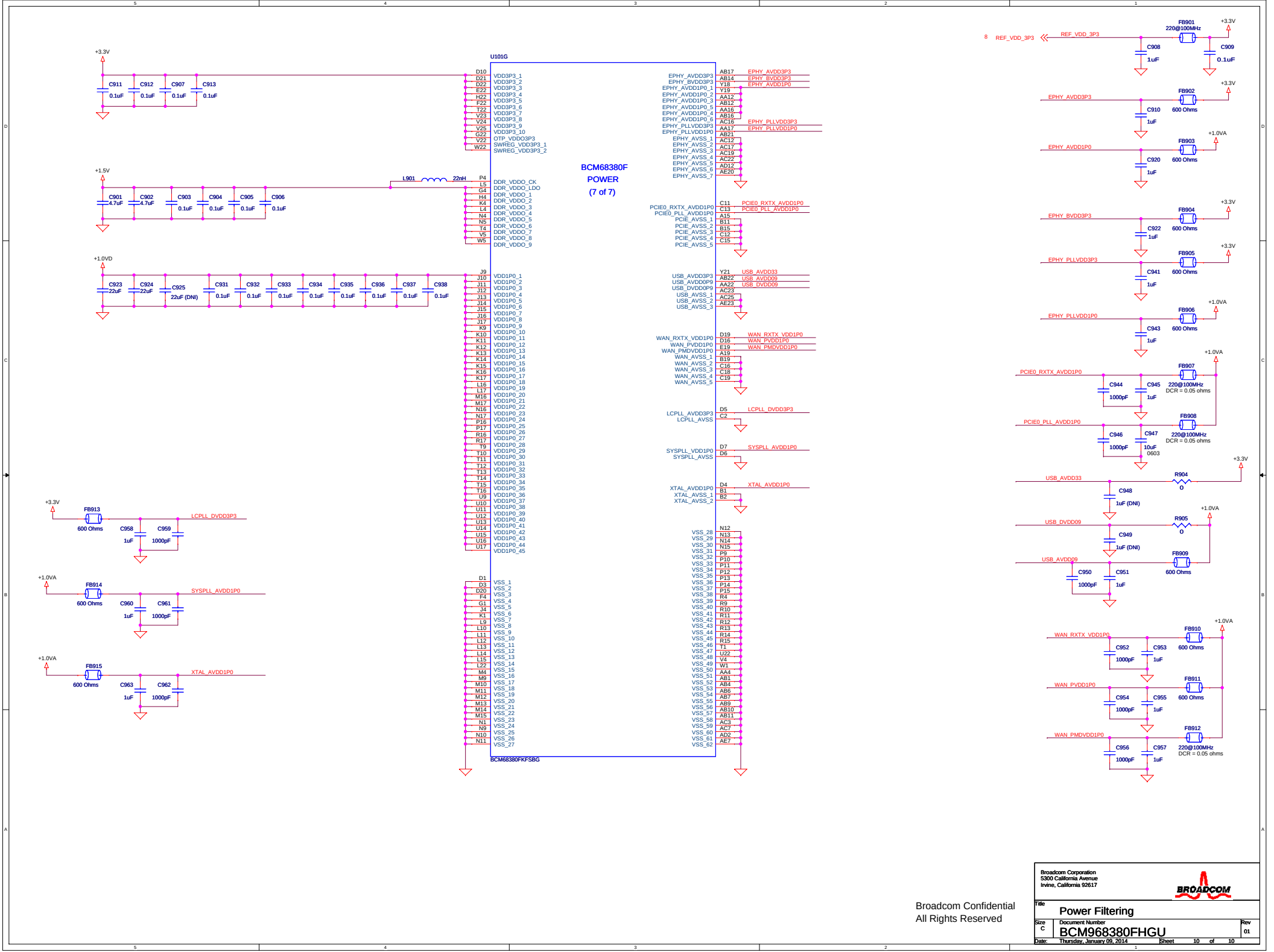

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Title: Power Filtering

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