FE1.1s

USB 2.0 High Speed 4-Port Hub Controller

Data Sheet

Introduction

The FE1.1s is a highly integrated, high quality, high performance, low power consumption, yet low cost solution for USB 2.0 High Speed 4-Port Hub.

It adopts *Single Transaction Translator* (STT) architecture to be more cost effective. Six, instead of two, non-periodic transaction buffers are used to minimize potential traffic jamming. The whole design is based on state-machine-control to reduce the response delay time; no micro controller is used in this chip.

To guarantee high quality, the whole chip is covered by *Test Scan Chain* – even on the high speed (480MHz) modules, so that all the logic components could be fully tested before shipping. Special *Build-In-Self-Test* mode is designed to exercise all high, full, and low speed Analog Front End (AFE) components on the packaging and testing stages as well.

Low power consumption is achieved by using 0.18 μm technology and comprehensive power/clock control mechanism. Most part of the chip will not be clocked unless needed.

Features

- Fully compliant with Universal Serial Bus Specification Revision 2.0 (USB 2.0);
  - Upstream facing port supports High-Speed (480MHz) and Full-Speed (12MHz) modes;
  - 4 downstream facing ports support High-Speed (480MHz), Full-Speed (12MHz), and Low-Speed (1.5MHz) modes;
- Integrated USB 2.0 Transceivers;
- Integrated upstream 1.5KΩ pull-up, downstream 15KΩ pull-down, and serial resisters;
- Integrated 5V to 3.3V and 1.8V regulator.
- Integrated Power-On-Reset circuit;
- Integrated 12MHz Oscillator with feedback resister, and crystal load capacitance;
- Integrated 12MHz-to-480MHz Phase Lock Loop (PLL);
- *Single Transaction Translator* (STT) –
  - One TT for all downstream ports;
  - The TT could handle 64 periodic Start-Split transactions, 32 periodic Complete-Split transactions, and 6 none-periodic transactions;
- Automatic self-power status monitoring;
  - Automatic re-enumeration when Self-

Powered switching to Bus-Powered;

- *Ganged Power Control* and *Global Over-Current Detection* support;
- EEPROM configured options –
  - *Vendor ID*, *Product ID*, & *Device Release Number*; and
  - *Number of Downstream Ports*;
- Comprehensive Port Indicators support:
  - *Downstream Port Enabled* indicator LED (x4, Green);
  - *Hub Active/Suspend* indicator LED.

BLOCK DIAGRAM

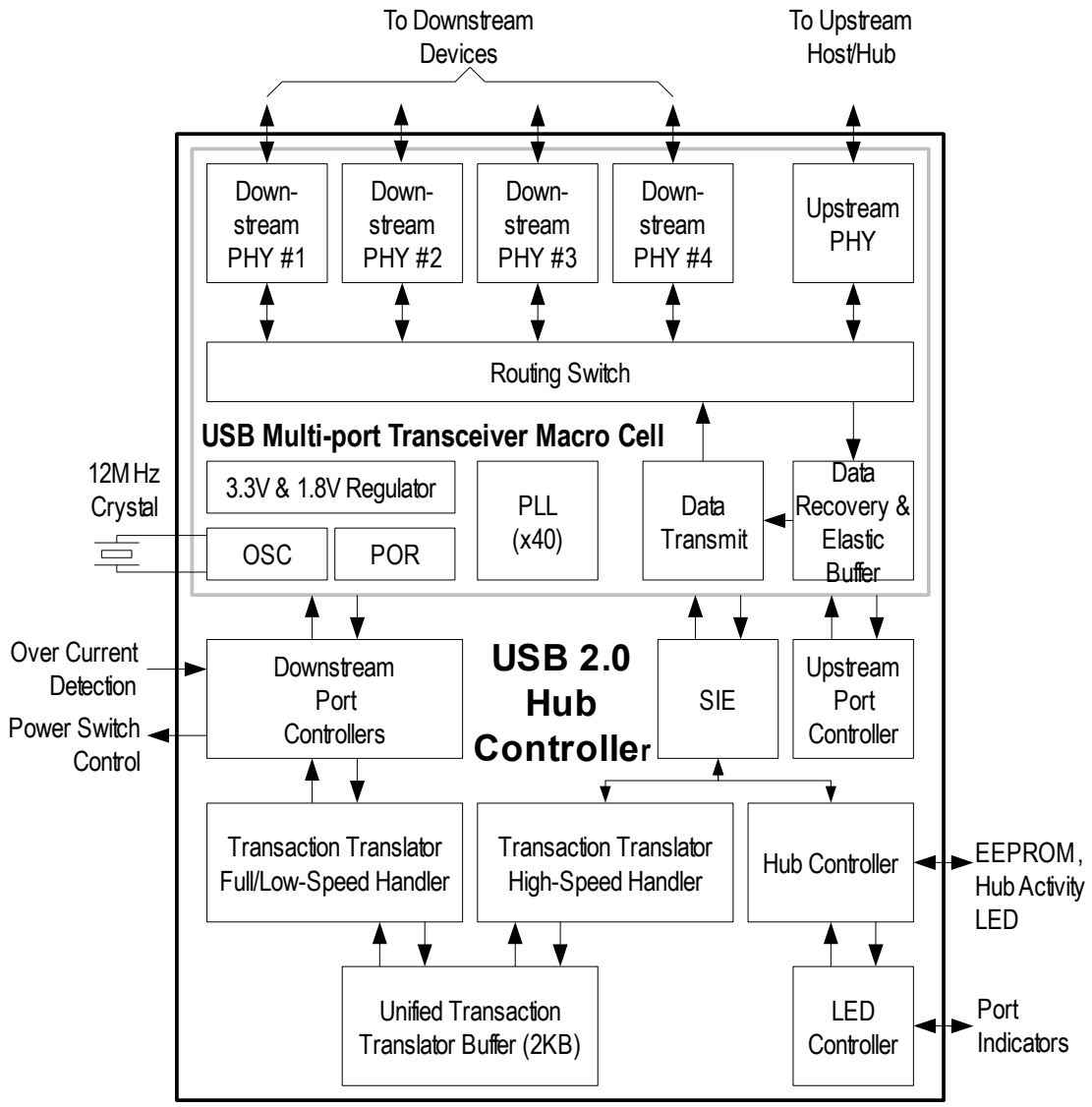


Fig. 1: Block Diagram

Package

28-pin SSOP
(Body Size: 10x4 mm, Pitch: 0.64 mm)

Pin Assignment

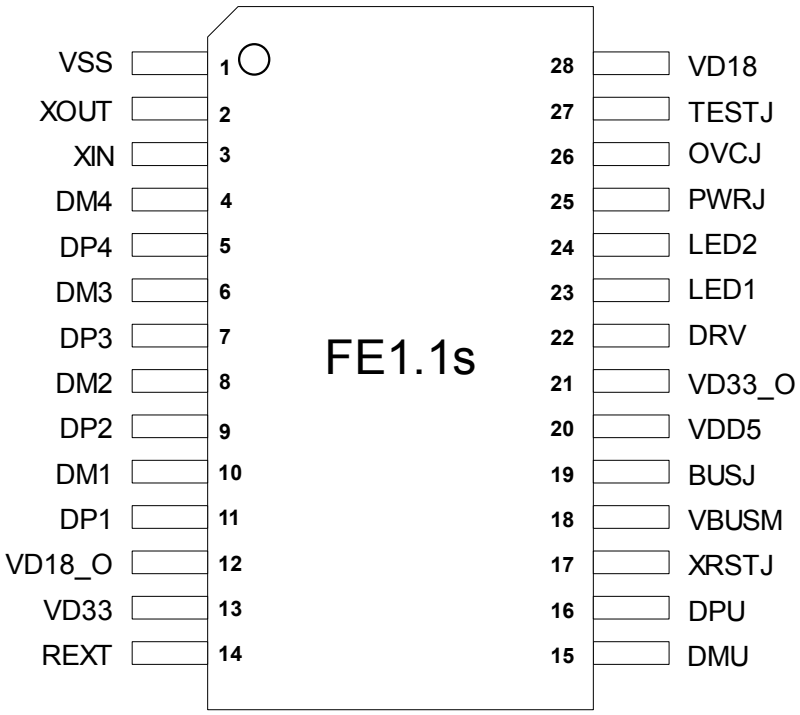


Fig. 2: SSOP-28 Pin Assignment

Pin Description Table

Pin Name	LQFP Pin No.	SSOP Pin No.	Type	Function	Note
VSS	10	1	P	Ground.	
XOUT	11	2	OSC	12 MHz Crystal Oscillator output	
XIN	12	3	OSC	12 MHz Crystal Oscillator input.	
DM4	14	4	UT	The D- pin of the 4th Downstream Facing Port.	
DP4	15	5	UT	The D+ pin of the 4th Downstream Facing Port.	
DM3	17	6	UT	The D- pin of the 3rd Downstream Facing Port.	
DP3	18	7	UT	The D+ pin of the 3rd Downstream Facing Port.	
DM2	20	8	UT	The D- pin of the 2nd Downstream Facing Port.	
DP2	21	9	UT	The D+ pin of the 2nd Downstream Facing Port.	
DM1	23	10	UT	The D- pin of the 1st Downstream Facing Port.	
DP1	24	11	UT	The D+ pin of the 1st Downstream Facing Port.	
VD18_O	26	12	P	1.8V power output from 3.3V→1.8V integrated regulator – a 10μF decoupling capacitor is required.	
VD33	27	13	P	3.3V power input for 3.3V→1.8V integrated regulator.	
REXT	28	14		A 2.7KΩ (± 1%) resister should be connected to VSS to provide internal bias reference.	
DMU	30	25	UT	The D- pin of the Upstream Facing Port.	
DPU	31	16	UT	The D+ pin of the Upstream Facing Port.	
XRSTJ	34	17	I	External Reset, active low, is an optional source of chip reset signal, beside the build-in Power-On-Reset. The minimum low pulse width is 10 μs.	
VBUSM	35	18	I	The V_{BUS} Monitor of upstream facing port.	
BUSJ	36	19	I	Bus power indicator: 0 – Bus Powered; 1 – Self Powered.	
VDD5	38	20	P	5V power input for integrated 5V→3.3V regulator.	
VD33_O	39	21	P	3.3V power output from 5V→3.3V integrated regulator – a 10μF decoupling capacitor is required.	
TEST	40	——	I	Test Mode Enable – should be tied to ground for normal operation.	
DRV	42	22	I/O	LED Drive Control	1

LED1/ EESCL	43	23	I/O	Port 1 and Port 3 Enabled Indicator (LED) Control, and external Serial EEPROM Clock.	1
LED2	44	24	I/O	Port 2 and Port 4 Enabled Indicator (LED) Control	1
PWRJ	47	25	O	Downstream Device Power Enable, active low, for *Ganged Power Switching*.	
OVCJ	48	26	I	Over Current Indicator, active low, for *Global Over-Current Protection.*	
TESTJ/ EESDA	2	27	I/O	Test Mode Enable, active low with internal pull-up, and external Serial EEPROM Data/Address.	1
VD18	9	28	P	1.8V power input.	

Type Abbreviation –

I : Input; O : Output; I/O : Input/Output; P : Power/Ground; UT: USB Transceiver.

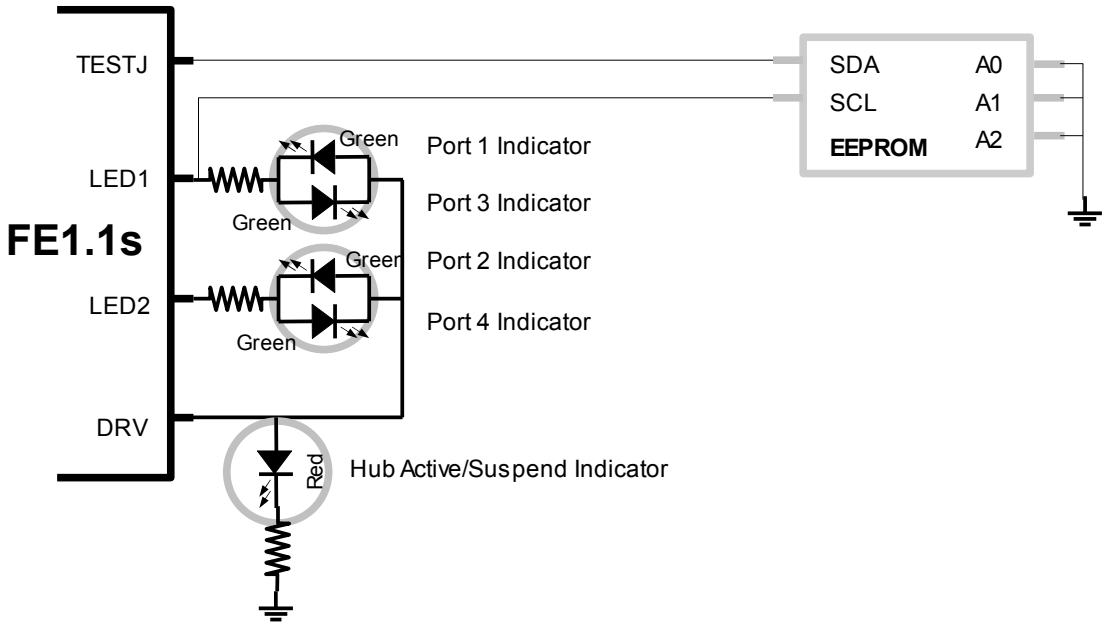


Fig. 3: LED and EEPROM Connections

Note 1 – LED Status Indicators and External Serial EEPROM Interface

The *FE1.1s* supports up to 5 LED for status indication with DRV, LED1, and LED2 pins, as shown by Fig. 4. For each Downstream Facing Port, one LED (Green) is provided to indicate that the attached device of the corresponding port is enabled or not. The fifth LED (Red) shows the Active (On) or Suspend (Off) status of the Hub itself. The *FE1.1s* can be configured by an external serial EEPROM via LED1 and TESTJ pins. The EEPROM is checked and loaded each time after chip reset.

EEPROM Contents

Address	Contents	Note
0x00	0x40	Constant, low byte of check code
0x01	0x1A	Constant, high byte of check code
0x02	Vendor ID (Low)	Low byte of Vendor ID, idVendor field of *Standard Device Descriptor*
0x03	Vendor ID (High)	High byte of Vendor ID
0x04	Product ID (Low)	Low byte of Product ID, idProduct field of *Standard Device Descriptor*
0x05	Product ID (High)	High Byte of Product ID
0x06	Device Release (Low)	Low byte of Device Release Number, must be Binary Coded Decimal, bcdDevice field of *Standard Device Descriptor*
0x07	Device Release (High)	High byte of Device Release Number, must be Binary Coded Decimal
0x08 ~ 0x19	Filling	All 0x00
0x1A	Port Number	Number of Downstream Ports, bNbrPorts field of *Hub Descriptor.*
0x1B ~ 0x1E	Filling	All 0x00
0x1F	Check Sum	The 8-bit sum of all value from 0x00 to 0x1E.

The first two bytes are the check code from the existence of EEPROM, their value must be 0x1A40. Any other value would cause the EEPROM loading mechanism of *FE1.1s* to conclude that the contents of this EEPROM is unusable, and use the default value instead.

The last byte, 0x1F, is a checksum made up of the sum of all value from 0x00 to 0x1E. The number must match to render the content of the EEPROM usable. Otherwise, the loading mechanism of *FE1.1s* would discard the value from EEPROM and use default value instead.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	TS	-55	+150	℃
Power Supply Voltage	VDD5 VD33 VD18	-0.5 -0.5 -0.5	+6.0 +4.0 +2.5	V
ESD Human Body Mode		-2000	2000	V
ESD Machine Mode		-200	200	V
Latch Up		-200	200	mA

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	TA	0		70	℃
Operating voltage	VDD5 VD33 VD18	4.5 3.0 1.62	5.0 3.3 1.8	5.5 3.6 1.98	V
LOW level voltage of digital input	VIL	-0.3		0.8	V
HIGH level voltage of digital input	VIH	2.0		5.5	V
Threshold voltage of digital input	VTH	1.45	1.58	1.74	V
Low-to-High level of schmitt-trigger input	VT+	1.44	1.5	1.56	V
High-to-Low level of schmitt-trigger input	VT-	0.89	0.94	0.99	V
LOW level voltage of digital output@4mA	VOL			0.4	V
HIGH level voltage of digital output@4mA	VOH	2.4			V

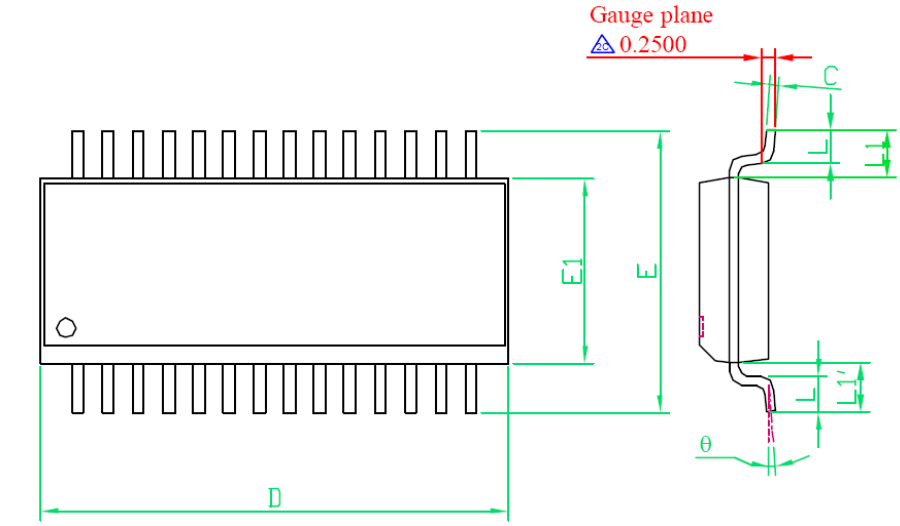
Power Consumption

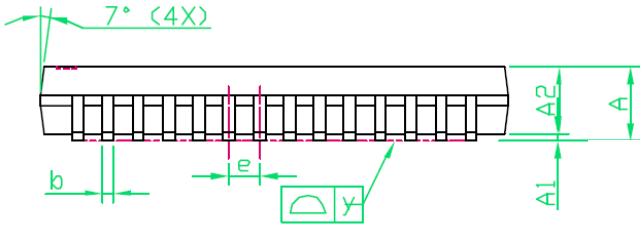
DC Supply Current

Symbol	Condition			Typ.	Unit
	Active ports	Host	Device		
I_suspend	Suspend			500	uA
Icc	4	Full-Speed	4x Full-Speed	25	mA
		High-Speed	4x High-Speed	100	mA
		High-Speed	4x Full-Speed	42	mA
	3	Full-Speed	3x Full-Speed	25	mA
		High-Speed	3x High-Speed	86	mA
		High-Speed	3x Full-Speed	42	mA
	2	Full-Speed	2x Full-Speed	25	mA
		High-Speed	2x High-Speed	71	mA
		High-Speed	2x Full-Speed	42	mA
	1	Full-Speed	1x Full-Speed	25	mA
		High-Speed	1x High-Speed	57	mA
		High-Speed	1x Full-Speed	42	mA
	No active	Full-Speed		25	mA
		High-Speed		42	mA

PACKAGE

28-pin SSOP (Body Size: 10x4 mm, Pitch: 0.64mm)





SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.60	1.75	0.053	0.064	0.069
A1	0.10	---	0.25	0.004	---	0.010
A2	---	1.45	---	---	0.057	---
b	0.20	0.25	0.30	0.008	0.010	0.012
C	0.19	---	0.25	0.007	---	0.010
D	9.80	---	10.00	0.386	---	0.394
E	5.80	6.0	6.20	0.228	0.236	0.244
E1	3.80	3.9	4.00	0.150	0.153	0.157
e	---	0.64	---	---	0.025	---
L	0.40	---	1.27	0.016	---	0.050
y	---	---	0.10	---	---	0.004
θ	0°	---	8°	0°	---	8°
L1-L1'	---	---	0.12	---	---	0.005
L1	1.04REF			0.041REF		

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