

CSc 137
Computer Organization
Spring 2017

Instructor: Nikrouz Faroughi
Office: RVR 3022
Office Hours: M W 4:20:5:20
Email address: faroughi@csus.edu

Catalog Description

Introduction to computer organization and architecture. Topics include combinational devices, sequential and synchronized circuits, memory organization, CPU architecture and organization, bus structures, input/output, interrupts, DMA, memory hierarchy, introduction to instruction level parallelism, multithreading, and multiprocessing; exposure to hardware security issues. Prerequisite: CSC 28, CSC 35, and CSC 130; 3 units.

Texts:

Textbook: Digital Logic Design and Computer Organization-with computer architecture for security, Nikrouz Faroughi, McGraw Hill.

Tools:

Verilog hardware description language, available remotely on Titan

Grading Policy:

Quiz/Homework/Projects	30%	Subject to change. Also see the Notes below
Midterm	35%	
Final	35%	Comprehensive

Notes 1:

1. No make-up exams
2. You are responsible for all the materials presented and announcements made in class.
4. To pass the class you must do satisfactory work in assignments, projects, and exams.
5. Drops after the 6th week will be permitted only with serious and compelling reasons.
6. You are required to submit an independent solution for all assignments and projects unless teamwork is explicitly specified in the assignment. Similar solutions may be viewed to be in violation of Academic Integrity. For Academic Honesty, Policy & Procedures refer to:
<http://www.ecs.csus.edu/wcm/csc/academic/academicintegrity.html>.

Note 2:

The assignments will be posted on my web site. You should check the web site periodically for new items.

Tentative schedule:

Topics	Readings (Selected Sections)	Tentative
Introduction	Chapter 1	1 week
Combinational logic: Small circuits	Chapter 2	1 1/2 weeks
Hardware description language and circuit simulations	Chapter 2	1 week
Combinational logic: Large circuits	Chapter 3	1 week
Sequential circuits: Core modules	Chapter 4	1/2 week
Sequential circuits: Small designs	Chapter 5	1 1/2 week
Sequential circuits: Large designs	Chapter 6	1 1/2 weeks
Memory organization, technology, and access	Chapter 7	1 week
Instruction set architecture (ISA)	Chapter 8	2 weeks
System interconnection	Chapter 9	1 week
Memory hierarchy	Chapter 10	1 week
Exposure to hardware security issues	Chapter 11	1 week
Exams		1 week