How to run Verilog simulator on Titan:

1. Logon to Titan. From off campus use *tital.ecs.csus.edu*. You can install a VNC Viewer such as Ultra VNC if you wish. If you use a VNC Viewer, use port 50 or 52 (enter machine name as *titan:50* from on campus or *titan.ecs.csus.edu:50* from off campus.) For secure off campus connection run VPN before you run VNC.

2. Enter `vcs +v2k filename.v` at the Unix prompt to compile your verilog code on Titan. The compiled file is saved as `simv` and to simulate the design enter simv at the Unix/Linux prompt. Use `` `include `` to include the lower level .v files in each of the higher level .v files; note the tick (`) before `include`. Save the simulation output into a file as `simv > outfile` if you wish.