1. Decoder 8 inputs and 0-250 outputs
2. D\_latch
3. D\_flipflops
4. 8-bit register
5. 251 bytes register bank
6. 16 bytes register bank A
7. 16 bytes register bank B
8. 16 bytes register bank C
9. Counter 8-bit \*\*
10. Add/Sub logic unit\*\*
11. Multiplication logic unit\*\*
12. Division logic unit\*\*
13. Modulus logic unit\*\*
14. Greater logic unit \*\*
15. Lesser logic unit \*\*
16. Equal logic unit \*\*
17. Not equal logic unit\*\*