Design the memory map and memory decoder for a 16 bits microprocessor system using the following memory requirements:

- **256KB EEPROM ending at FFFFFH, using 64K x 16 bits memories**
- **128KB DRAM, using 32K x 8 bits memories**

STEP 1

$$EEPROM\ \#\ circuits\ =\ \frac{256\ KB}{64\ K\ *\ 16\ bits} = 2$$

$$DRAM\ \#\ circuits\ =\ \frac{128\ KB}{32\ K\ *\ 8\ bits} = 4$$

STEP 2

$$EEPROM\ \#\frac{circuits}{block} = \frac{16}{16} = 1$$

$$EEPROM\ \#\ blocks = \frac{2}{1} = 2 \rightarrow B1, B2$$

$$DRAM\ \#\frac{circuits}{block} = \frac{16}{8} = 2$$

$$DRAM\ \#\ blocks = \frac{4}{2} = 2 \rightarrow B3, B4$$

STEP 3

BLOCK	*BLOCK SIZE*	*ADDRESS LINES*	*ADDRESS RANGE*	
B1	128 KB	17	0x0_0000	0x1_FFFF
B2	128 KB	17	0x0_0000	0x1_FFFF
B3	64 KB	16	0x0000	0xFFFF
B4	64 KB	16	0x0000	0xFFFF

STEP 4

TYPE	*BLOCK*	*MEMORY MAP*
DRAM	B3	0x0_0000
		0x0_FFFF
	B4	0x1_0000
		0x1_FFFF
. . .		
EEPROM	B1	0xC_0000
		0xD_FFFF
	B2	0xE_0000
		0xF_FFFF

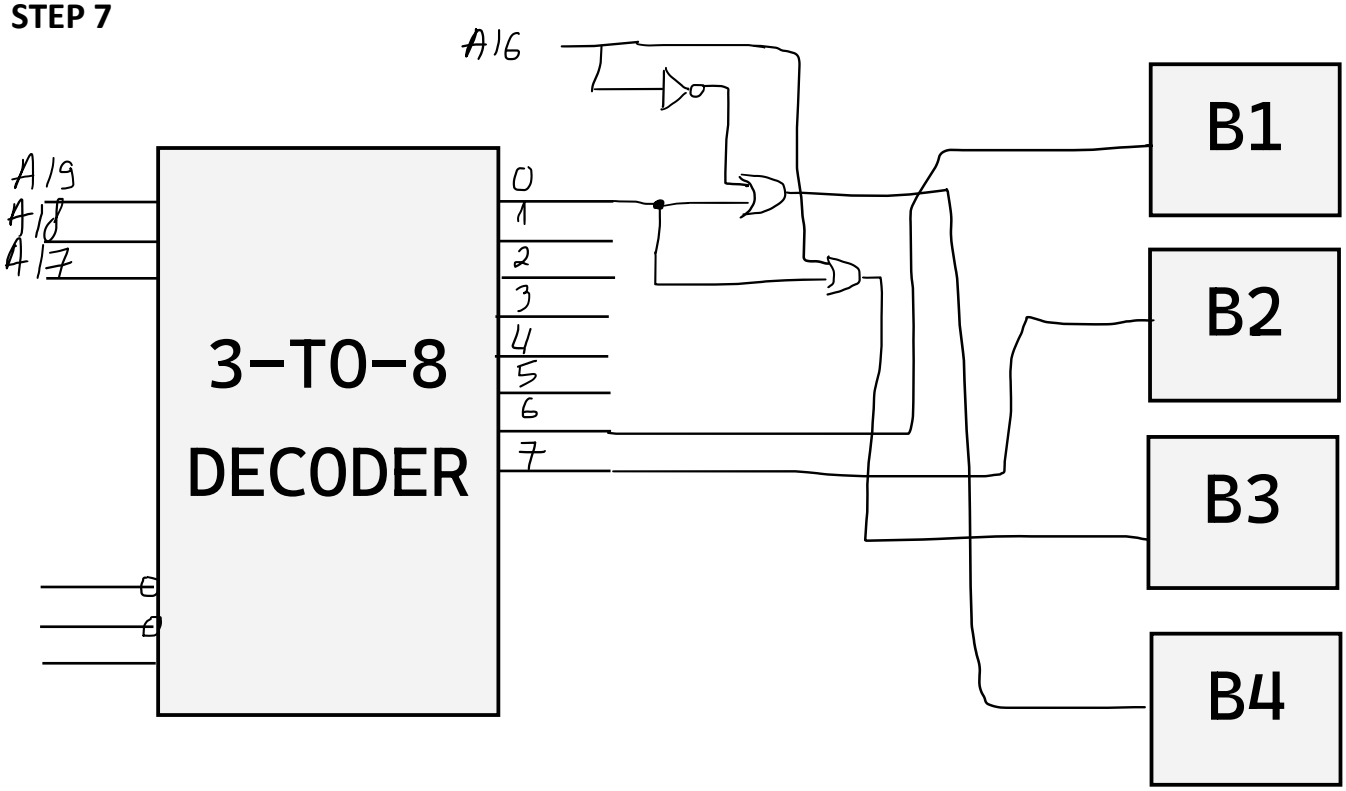
STEP 5

A19	A18	A17	A16	A15	A14	...	A1	A0	
1	1	0	0	0	0		0	0	B1
1	1	0	1	1	1		1	1	
1	1	1	0	0	0		0	0	B2
1	1	1	1	1	1		1	1	
0	0	0	0	0	0	...	0	0	B3
0	0	0	0	1	1		1	1	
0	0	0	1	0	0		0	0	B4
0	0	0	1	1	1		1	1	

STEP 6

$$\overline{C_{S1}} = \overline{A_{19} \cdot A_{18} \cdot \overline{A_{17}}}$$
$$\overline{C_{S2}} = \overline{A_{19} \cdot A_{18} \cdot A_{17}}$$
$$\overline{C_{S3}} = \overline{\overline{A_{19}} \cdot \overline{A_{18}} \cdot \overline{A_{17}} \cdot \overline{A_{16}}}$$
$$\overline{C_{S4}} = \overline{\overline{A_{19}} \cdot \overline{A_{18}} \cdot \overline{A_{17}} \cdot A_{16}}$$

STEP 7



Design the memory map and memory decoder for a 16 bits microprocessor system using the following memory requirements:

- **256KB EEPROM starting at 40000H, using 64K x 8 bits memories**
- **256KB DRAM, using 64K x 1 bit memories**

STEP 1

$$EEPROM\ \#\ circuits\ =\ \frac{256\ KB}{64\ K\ *\ 8\ bits} = 4$$

$$DRAM\ \#\ circuits\ =\ \frac{256\ KB}{64\ K\ *\ 1\ bits} = 32$$

STEP 2

$$EEPROM\ \#\frac{circuits}{block} = \frac{16}{1} = 16$$

$$EEPROM\ \#\ blocks = \frac{32}{16} = 2 \rightarrow B1, B2$$

$$DRAM\ \#\frac{circuits}{block} = \frac{16}{8} = 2$$

$$DRAM\ \#\ blocks = \frac{4}{2} = 2 \rightarrow B3, B4$$

STEP 3

BLOCK	*BLOCK SIZE*	*ADDRESS LINES*	*ADDRESS RANGE*	
B1	128 KB	17	0x0_0000	0x1_FFFF
B2	128 KB	17	0x0_0000	0x1_FFFF
B3	128 KB	17	0x0_0000	0x1_FFFF
B4	128 KB	17	0x0_0000	0x1_FFFF

STEP 4

TYPE	*BLOCK*	*MEMORY MAP*
DRAM	B3	0x0_0000
		0x1_FFFF
	B4	0x2_0000
		0x3_FFFF
EEPROM	B1	0x4_0000
		0x5_FFFF
	B2	0x6_0000
		0x7_FFFF

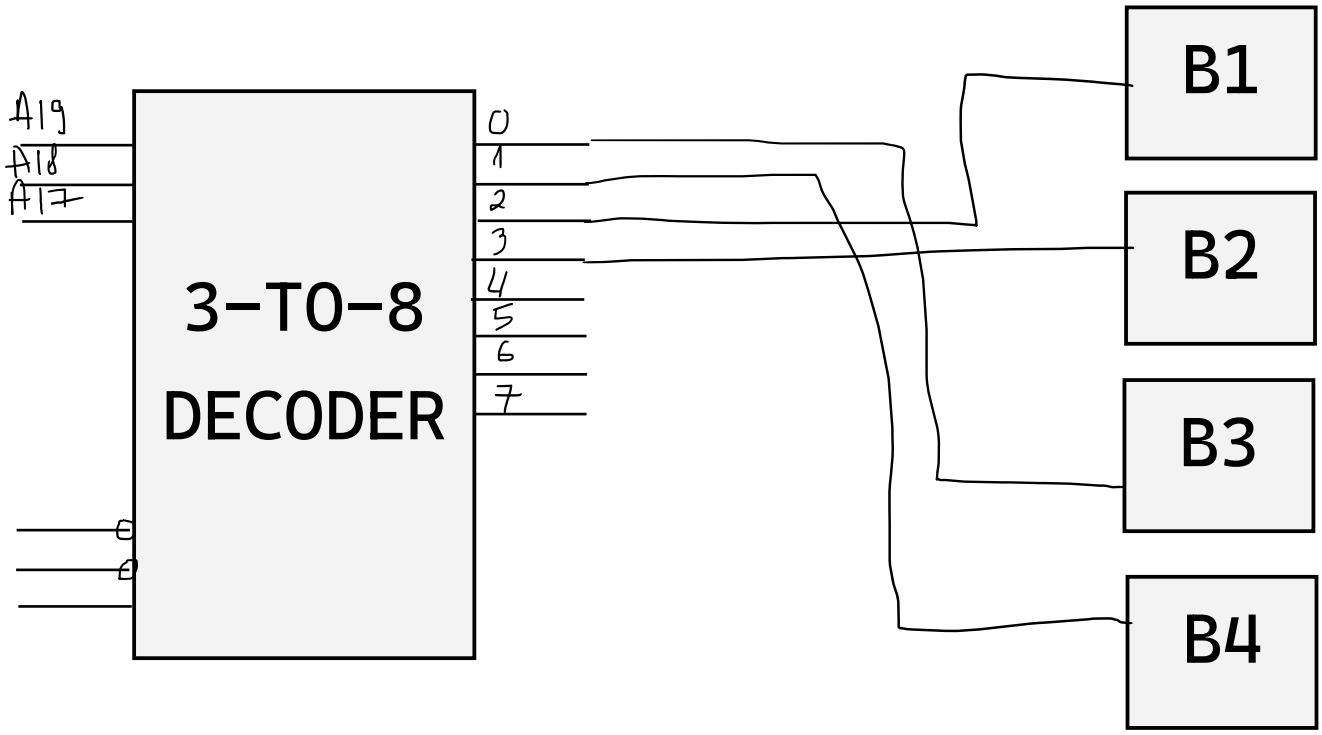
STEP 5

A19	*A18*	*A17*	*A16*	*A15*	*A14*	...	*A1*	*A0*	
0	0	0	0	0	0		0	0	*B3*
0	0	0	1	1	1		1	1	
0	0	1	0	0	0		0	0	*B4*
0	0	1	1	1	1		1	1	
0	1	0	0	0	0	...	0	0	*B1*
0	1	0	1	1	1		1	1	
0	1	1	0	0	0		0	0	*B2*
0	1	1	1	1	1		1	1	

STEP 6

$$\overline{C_{S1}} = \overline{\overline{A_{19}} \cdot A_{18} \cdot \overline{A_{17}}}$$
$$\overline{C_{S2}} = \overline{A_{19} \cdot \overline{A_{18}} \cdot \overline{A_{17}}}$$
$$\overline{C_{S3}} = \overline{\overline{A_{19}} \cdot \overline{A_{18}} \cdot \overline{A_{17}}}$$
$$\overline{C_{S4}} = \overline{\overline{A_{19}} \cdot \overline{A_{18}} \cdot A_{17}}$$

STEP 7



Design the memory map and memory decoder for a 16 bits microprocessor system using the following memory requirements:

- **128KB EEPROM, using 64K x 8 bits memories**
- **512KB DRAM, using 64K x 8 bits memories**

STEP 1

$$EEPROM\ \#\ circuits\ = \frac{128\ KB}{64\ K\ *\ 8\ bits} = 2$$

$$DRAM\ \#\ circuits\ = \frac{512\ KB}{64\ K\ *\ 8\ bits} = 8$$

STEP 2

$$EEPROM\ \#\frac{circuits}{block} = \frac{16}{8} = 2$$

$$EEPROM\ \#\ blocks = \frac{2}{2} = 1 \rightarrow B1$$

$$DRAM\ \#\frac{circuits}{block} = \frac{16}{8} = 2$$

$$DRAM\ \#\ blocks = \frac{8}{2} = 4 \rightarrow B2, B3, B4, B5$$

STEP 3

BLOCK	*BLOCK SIZE*	*ADDRESS LINES*	*ADDRESS RANGE*	
B1	128 KB	17	0x0_0000	0x1_FFFF
B2	128 KB	17	0x0_0000	0x1_FFFF
B3	128 KB	17	0x0_0000	0x1_FFFF
B3	128 KB	17	0x0_0000	0x1_FFFF
B3	128 KB	17	0x0_0000	0x1_FFFF

STEP 4

TYPE	*BLOCK*	*MEMORY MAP*
EEPROM	B1	0x0_0000
		0x1_FFFF
DRAM	B2	0x2_0000
		0x3_FFFF
	B3	0x4_0000
		0x5_FFFF
	B4	0X6_0000
		0x7_FFFF
	B5	0x8_0000
		0x9_FFFF

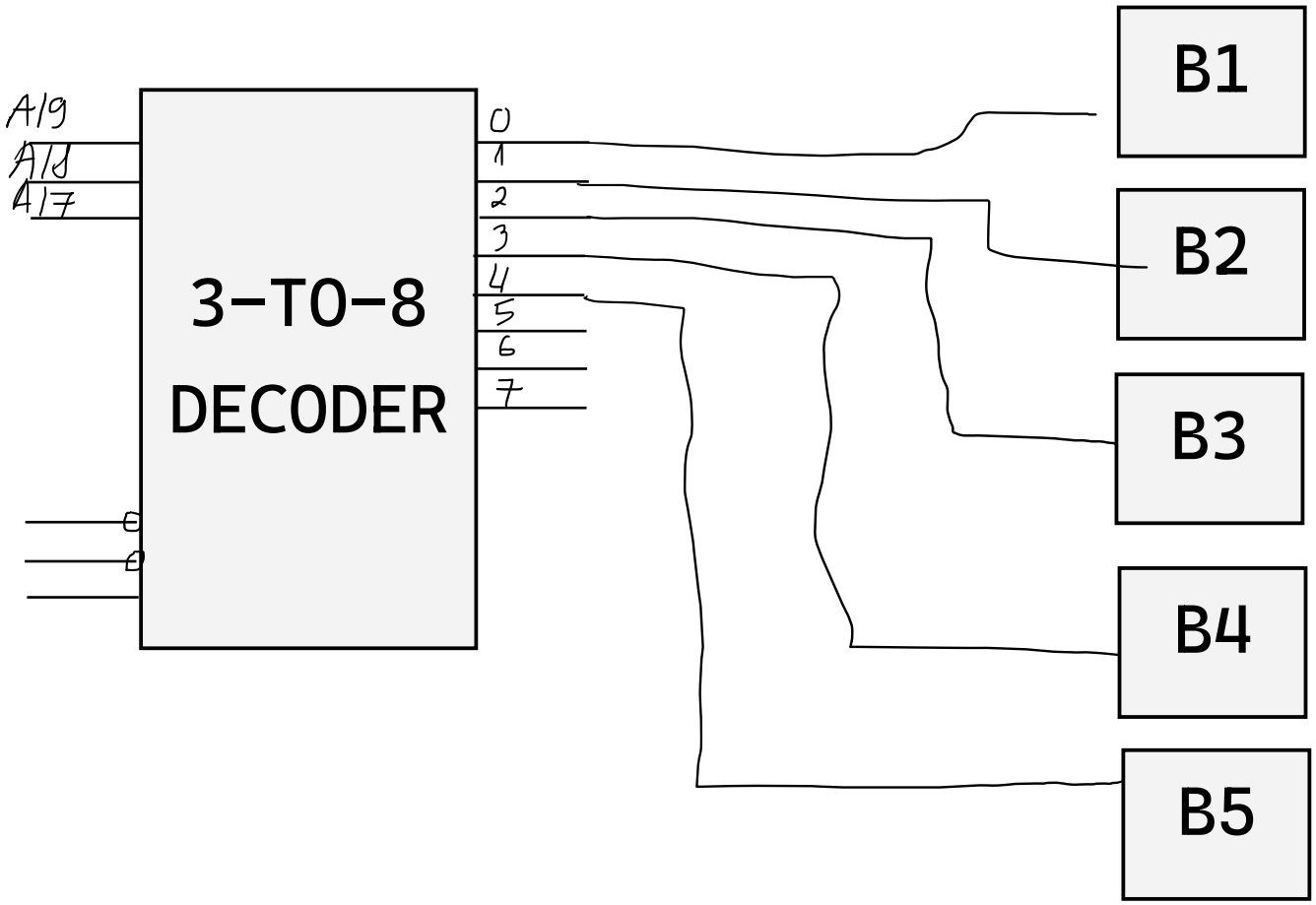
STEP 5

A19	A18	A17	A16	A15	A14	...	A1	A0	
0	0	0	0	0	0		0	0	B1
0	0	0	1	1	1		1	1	
0	0	1	0	0	0		0	0	B2
0	0	1	1	1	1		1	1	
0	1	0	0	0	0		0	0	B3
0	1	0	1	1	1	...	1	1	
0	1	1	0	0	0		0	0	B4
0	1	1	1	1	1		1	1	
1	0	0	0	0	0		0	0	B5
1	0	0	1	1	1		1	1	

STEP 6

$$\overline{C_{S1}} = \overline{\overline{A_{19}} \cdot \overline{A_{18}} \cdot \overline{A_{17}}}$$
$$\overline{C_{S2}} = \overline{\overline{A_{19}} \cdot \overline{A_{18}} \cdot A_{17}}$$
$$\overline{C_{S3}} = \overline{\overline{A_{19}} \cdot A_{18} \cdot \overline{A_{17}}}$$
$$\overline{C_{S4}} = \overline{\overline{A_{19}} \cdot A_{18} \cdot A_{17}}$$
$$\overline{C_{S5}} = \overline{A_{19} \cdot \overline{A_{18}} \cdot \overline{A_{17}}}$$

STEP 7



Design the memory map and memory decoder for a 16 bits microprocessor system using the following memory requirements:

- **64KB EEPROM ending at FFFFFH, using 16K x 16 bits memories**
- **64KB DRAM, starting at 00000h, using 32K x 8 bits memories**

STEP 1

$$EEPROM\ \#\ circuits\ =\ \frac{64\ KB}{16\ K\ *\ 16\ bits} = 2$$

$$DRAM\ \#\ circuits\ =\ \frac{64\ KB}{32\ K\ *\ 8\ bits} = 2$$

STEP 2

$$EEPROM\ \#\frac{circuits}{block} = \frac{16}{16} = 1$$

$$EEPROM\ \#\ blocks = \frac{2}{1} = 2 \rightarrow B1, B2$$

$$DRAM\ \#\frac{circuits}{block} = \frac{16}{8} = 2$$

$$DRAM\ \#\ blocks = \frac{2}{2} = 1 \rightarrow B3$$

STEP 3

BLOCK	*BLOCK SIZE*	*ADDRESS LINES*	*ADDRESS RANGE*	
B1	32 KB	15	0x0000	0x7FFF
B2	32 KB	15	0x0000	0x7FFF
B3	64 KB	16	0x0000	0xFFFF

STEP 4

TYPE	*BLOCK*	*MEMORY MAP*
DRAM	B3	0x0_0000
		0x0_FFFF
. . .		
EEPROM	B1	0xF_0000
		0xF_7FFF
	B2	0xF_8000
		0xF_FFFF

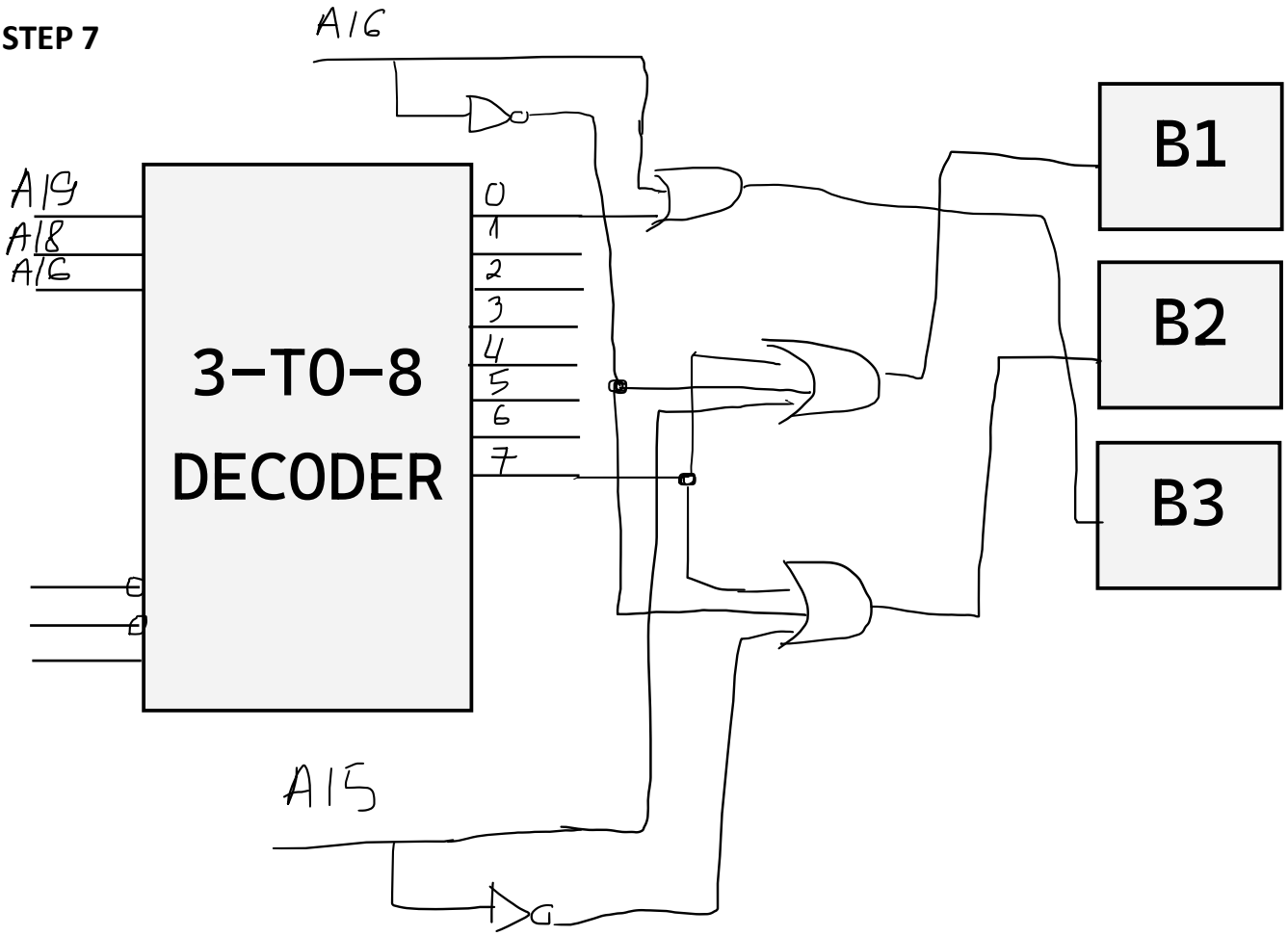
STEP 5

A19	A18	A17	A16	A15	A14	A13	A12	...	A1	A0	
1	1	1	1	0	0	0	0		0	0	B1
1	1	1	1	0	1	1	1		1	1	
1	1	1	1	1	0	0	0		0	0	B2
1	1	1	1	1	1	1	1	...	1	1	
0	0	0	0	0	0	0	0		0	0	B3
0	0	0	0	1	1	1	1		1	1	

STEP 6

$$\overline{C_{S1}} = \overline{A_{19} \cdot A_{18} \cdot A_{17} \cdot A_{16} \cdot \overline{A_{15}}}$$
$$\overline{C_{S2}} = \overline{A_{19} \cdot A_{18} \cdot A_{17} \cdot A_{16} \cdot A_{15}}$$
$$\overline{C_{S3}} = \overline{\overline{A_{19}} \cdot \overline{A_{18}} \cdot \overline{A_{17}} \cdot \overline{A_{16}}}$$

STEP 7



Design the memory map and memory decoder for a 16 bits microprocessor system using the following memory requirements:

- **256KB EEPROM ending at 7ffffH, using 32K x 16 bits memories**
- **256KB DRAM, using 64K x 8 bits memories**

STEP 1

$$EEPROM\ \#\ circuits\ =\ \frac{256\ KB}{32\ K\ *\ 16\ bits} = 4$$

$$DRAM\ \#\ circuits\ =\ \frac{256\ KB}{64\ K\ *\ 8\ bits} = 4$$

STEP 2

$$EEPROM\ \#\frac{circuits}{block} = \frac{16}{16} = 1$$

$$EEPROM\ \#\ blocks = \frac{4}{1} = 4 \rightarrow B1, B2, B3, B4$$

$$DRAM\ \#\frac{circuits}{block} = \frac{16}{8} = 2$$

$$DRAM\ \#\ blocks = \frac{4}{2} = 2 \rightarrow B5, B6$$

STEP 3

BLOCK	*BLOCK SIZE*	*ADDRESS LINES*	*ADDRESS RANGE*	
B1	64 KB	16	0x0000	0xFFFF
B2	64 KB	16	0x0000	0xFFFF
B3	64 KB	16	0x0000	0xFFFF
B4	64 KB	16	0x0000	0xFFFF
B5	128 KB	17	0x0_0000	0x1_FFFF
B6	128 KB	17	0x0_0000	0x1_FFFF

STEP 4

TYPE	*BLOCK*	*MEMORY MAP*
DRAM	B5	0x0_0000
		0x1_FFFF
	B6	0x2_0000
		0x3_FFFF
EEPROM	B1	0x4_0000
		0x4_FFFF
	B2	0x5_0000
		0x5_FFFF
	B3	0x6_0000
		0x6_FFFF
	B4	0x7_0000
		0x7_FFFF

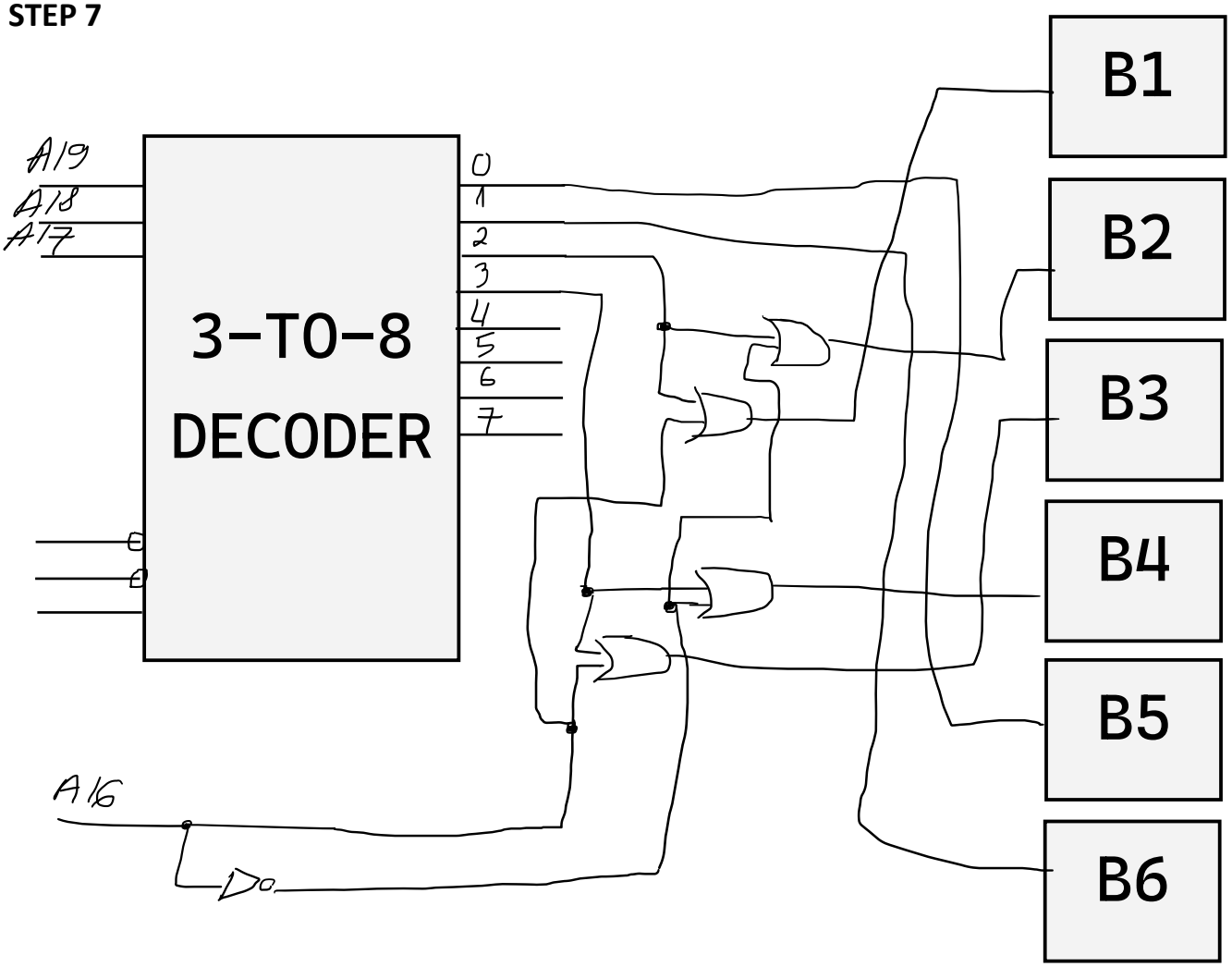
STEP 5

A19	A18	A17	A16	A15	A14	...	A1	A0	
0	0	0	0	0	0		0	0	B5
0	0	0	1	1	1		1	1	
0	0	1	0	0	0		0	0	B6
0	0	1	1	1	1		1	1	
0	1	0	0	0	0		0	0	B1
0	1	0	0	1	1		1	1	
0	1	0	1	0	0	...	0	0	B2
0	1	0	1	1	1		1	1	
0	1	1	0	0	0		0	0	B3
0	1	1	0	1	1		1	1	
0	1	1	1	0	0		0	0	B4
0	1	1	1	1	1		1	1	

STEP 6

$$\overline{C_{S1}} = \overline{\overline{A_{19}} \cdot A_{18} \cdot \overline{A_{17}} \cdot \overline{A_{16}}}$$
$$\overline{C_{S2}} = \overline{\overline{A_{19}} \cdot A_{18} \cdot \overline{A_{17}} \cdot A_{16}}$$
$$\overline{C_{S3}} = \overline{\overline{A_{19}} \cdot A_{18} \cdot A_{17} \cdot \overline{A_{16}}}$$
$$\overline{C_{S4}} = \overline{\overline{A_{19}} \cdot A_{18} \cdot A_{17} \cdot A_{16}}$$
$$\overline{C_{S5}} = \overline{\overline{A_{19}} \cdot \overline{A_{18}} \cdot \overline{A_{17}}}$$
$$\overline{C_{S6}} = \overline{\overline{A_{19}} \cdot \overline{A_{18}} \cdot A_{17}}$$

STEP 7



Design the memory map and memory decoder for a 16 bits microprocessor system using the following memory requirements:

- **192KB EEPROM, using 32K x 16 bits memories**
- **128KB DRAM, using 32K x 8 bits memories**

STEP 1

$$EEPROM\ \#\ circuits\ = \frac{192\ KB}{32\ K\ *\ 16\ bits} = 3$$

$$DRAM\ \#\ circuits\ = \frac{128\ KB}{32\ K\ *\ 8\ bits} = 4$$

STEP 2

$$EEPROM\ \#\frac{circuits}{block} = \frac{16}{16} = 1$$

$$EEPROM\ \#\ blocks = \frac{3}{1} = 3 \rightarrow B1, B2, B3$$

$$DRAM\ \#\frac{circuits}{block} = \frac{16}{8} = 2$$

$$DRAM\ \#\ blocks = \frac{4}{2} = 2 \rightarrow B4, B5$$

STEP 3

BLOCK	*BLOCK SIZE*	*ADDRESS LINES*	*ADDRESS RANGE*	
B1	64 KB	16	0x0000	0xFFFF
B2	64 KB	16	0x0000	0xFFFF
B3	64 kb	16	0x0000	0xFFFF
B4	64 KB	16	0x0000	0xFFFF
B5	64 KB	16	0x0000	0xFFFF

STEP 4

TYPE	*BLOCK*	*MEMORY MAP*
EEPROM	B1	0x0_0000
		0x0_FFFF
	B2	0x1_0000
		0x1_FFFF
DRAM	B3	0x2_0000
		0X2_FFFF
	B4	0x3_0000
		0x3_FFFF
	B3	0x4_0000
		0X4_FFFF

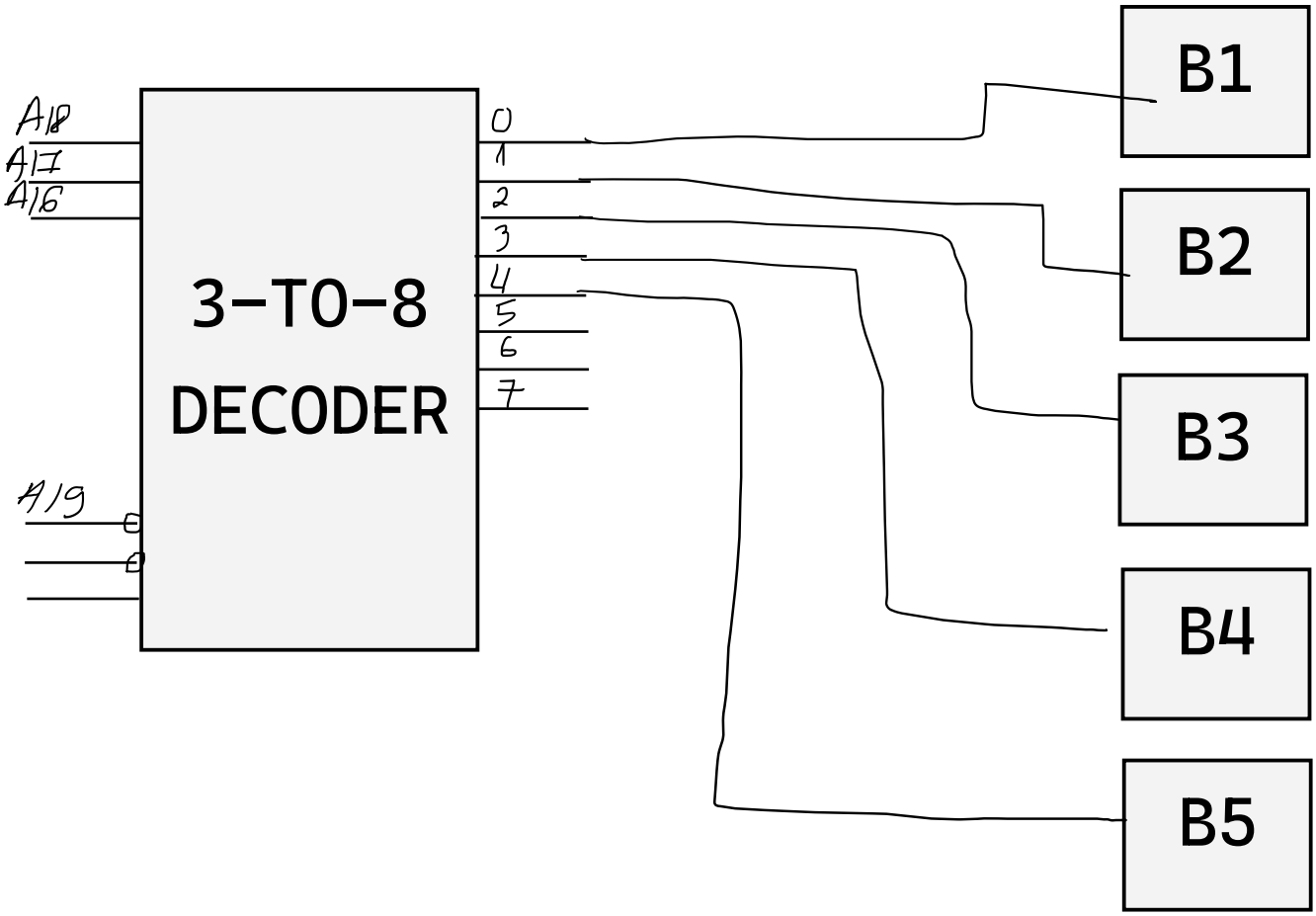
STEP 5

A19	A18	A17	A16	A15	A14	...	A1	A0	
0	0	0	0	0	0		0	0	B1
0	0	0	0	1	1		1	1	
0	0	0	1	0	0		0	0	B2
0	0	0	1	1	1		1	1	
0	0	1	0	0	0		0	0	B3
0	0	1	0	1	1	...	1	1	
0	0	1	1	0	0		0	0	B4
0	0	1	1	1	1		1	1	
0	1	0	0	0	0		0	0	B5
0	1	0	0	1	1		1	1	

STEP 6

$$\overline{C_{S1}} = \overline{\overline{A_{19}} \cdot \overline{A_{18}} \cdot \overline{A_{17}} \cdot \overline{A_{16}}}$$
$$\overline{C_{S2}} = \overline{\overline{A_{19}} \cdot \overline{A_{18}} \cdot \overline{A_{17}} \cdot A_{16}}$$
$$\overline{C_{S3}} = \overline{\overline{A_{19}} \cdot \overline{A_{18}} \cdot A_{17} \cdot \overline{A_{16}}}$$
$$\overline{C_{S4}} = \overline{\overline{A_{19}} \cdot \overline{A_{18}} \cdot A_{17} \cdot A_{16}}$$
$$\overline{C_{S5}} = \overline{\overline{A_{19}} \cdot A_{18} \cdot \overline{A_{17}} \cdot \overline{A_{16}}}$$

STEP 7



Design the memory map and memory decoder for a 16 bits microprocessor system using the following memory requirements:

- **96KB EEPROM ending at FFFFFH, using 16K x 16 bits memories**
- **128KB DRAM, using 64K x 2 bits memories**

STEP 1

$$EEPROM\ \#\ circuits\ =\ \frac{96\ KB}{16\ K\ *\ 16\ bits} = 3$$

$$DRAM\ \#\ circuits\ =\ \frac{128\ KB}{64\ K\ *\ 2\ bits} = 8$$

STEP 2

$$EEPROM\ \#\frac{circuits}{block} = \frac{16}{16} = 1$$

$$EEPROM\ \#\ blocks = \frac{3}{1} = 3 \rightarrow B1, B2, B3$$

$$DRAM\ \#\frac{circuits}{block} = \frac{16}{2} = 8$$

$$DRAM\ \#\ blocks = \frac{8}{8} = 1 \rightarrow B4$$

STEP 3

BLOCK	*BLOCK SIZE*	*ADDRESS LINES*	*ADDRESS RANGE*	
B1	32 KB	15	0x0000	0x7FFF
B2	32 KB	15	0x0000	0x7FFF
B3	32 KB	15	0x0000	0x7FFF
B4	128 KB	17	0x0_0000	0x1_FFFF

STEP 4

TYPE	*BLOCK*	*MEMORY MAP*
DRAM	B4	0x0_0000
		0x1_FFFF
. . .		
EEPROM	B1	0xE_8000
		0xE_FFFF
	B2	0xF_0000
		0xF_7FFF
	B3	0xF_8000
		0xF_FFFF

STEP 5

A19	A18	A17	A16	A15	A14	A13	A12	...	A1	A0	
0	0	0	0	0	0	0	0		0	0	B4
0	0	0	1	1	1	1	1		1	1	
1	1	1	0	1	0	0	0		0	0	B1
1	1	1	0	1	1	1	1		1	1	
1	1	1	1	0	0	0	0	...	0	0	B2
1	1	1	1	0	1	1	1		1	1	
1	1	1	1	1	0	0	0		0	0	B3
1	1	1	1	1	1	1	1		1	1	

STEP 6

$$\overline{C_{S1}} = \overline{A_{19} \cdot A_{18} \cdot A_{17} \cdot \overline{A_{16}} \cdot A_{15}}$$
$$\overline{C_{S2}} = \overline{A_{19} \cdot A_{18} \cdot A_{17} \cdot A_{16} \cdot \overline{A_{15}}}$$
$$\overline{C_{S3}} = \overline{A_{19} \cdot A_{18} \cdot A_{17} \cdot A_{16} \cdot A_{15}}$$
$$\overline{C_{S4}} = \overline{\overline{A_{19}} \cdot \overline{A_{18}} \cdot \overline{A_{17}} \cdot}$$

STEP 7