Problem 1

Region	Address	Variable
.stack	F800h	a
	F7FCh	b
	F7FAh	c
	F7F8h	s[3]
	F7F4h	s[2]
	F7E0h	s[1]
	F7ECh	s[0]

Variable	Size / Mem Size (bytes)	Address	Alignment	Content
a	4 / 4	F800h	Yes	00 00 00 17
b	2 / 2	F7FCh	Yes	00 17
c	1 / 2	F7FAh	Yes	??
s[3]	4 / 4	F7F8h	Yes	00
s[2]	4 / 4	F7F4h	Yes	00 00 00 03
s[1]	4 / 4	F7E0h	Yes	00 00 00 02
s[0]	4 / 4	F7ECh	Yes	00 00 00 01

Problem 2

Region	Address	Variable
.bss	1_0014h	i
.data	1_0010h	s[2]
	1_000Ch	s[1]
	1_0008h	s[0]
	1_0004h	c
	1_0000h	f

Variable	Size / Mem Size (bytes)	Address	Alignment	Content
f	4 / 4	1_0000h	Yes	00 00 20 40
c	2 / 4	1_0004h	Yes	41 00
s[0]	4 / 4	1_0008h	Yes	01 00 00 00
s[1]	4 / 4	1_000Ch	Yes	00 00 00 00
s[2]	4 / 4	1_0010h	Yes	01 00 00 00
i	4 / 4	1_0014h	Yes	00 00 00 00