Design the memory map and memory decoder for a 16 bits microprocessor (20 address lines) system using the following memory requirements:

- 128KB ROM, using 64K x 16 bits memories, at the end
- 256KB SRAM, using 64K x 16 bits memories
- 512KB DRAM, using 256K x 16 bits memories

$Processor\ Address\ Space: 2^{20} = 1\ MB = 10\_0000h$

- Nr of circuits

$$ROM\ nr\ of\ circuits = \frac{128\ KB}{64K * 16b} = \frac{128\ KB}{128\ KB} = 1$$
$$SRAM\ nr\ of\ circuits = \frac{256\ KB}{64K * 16b} = \frac{256\ KB}{128\ KB} = 2$$
$$DRAM\ nr\ of\ circuits = \frac{512\ KB}{256K * 16b} = \frac{512\ KB}{512\ KB} = 1$$

- Circuit size

$ROM\ circuit\ size = 64K *\ 16b = 128KB = 2^{17} = 2\_0000h$
$SRAM\ circuit\ size = 64K *\ 16b = 128KB = 2^{17} = 2\_0000h$
$DRAM\ circuit\ size = 256K *\ 16b = 512KB = 2^{19} = 8\_0000h$

- Memory Map
  1. Step 1 – above
  2. Step 2 – Blocks

$$ROM\ \frac{circuits}{block} = \frac{16}{16} = 1\ cpb$$
$$SRAM\ \frac{circuits}{block} = \frac{16}{16} = 1\ cpb$$
$$DRAM\ \frac{circuits}{block} = \frac{16}{16} = 1\ cpb$$

$$ROM\ blocks = \frac{1\ circuit}{1\ cpb} = 1\ block\ (B1)$$
$$SRAM\ blocks = \frac{2\ circuits}{1\ cpb} = 2\ blocks\ (B2, B3)$$
$$DRAM\ blocks = \frac{1\ circuit}{1\ cpb} = 1\ block\ (B4)$$

  3. Step 3 – Block Sizes

$ROM\ block\ size\ (B1) = 128\ KB = 2^{17} = 2\_0000h\ \ (0\_0000h\ \rightarrow 1\_FFFFh)$
$SRAM\ block\ size\ (B2, B3) = 128\ KB = 2^{17} = 2\_0000h\ \ (0\_0000h\ \rightarrow 1\_FFFFh)$
$DRAM\ block\ size\ (B4) = 512\ KB = 2^{17} = 8\_0000h\ (0\_0000h\ \rightarrow 7\_FFFFh)$

4. Step 4 – Memory Map

$B2$: $0\_0000h - 1\_FFFFh$
$B3$: $2\_0000h - 3\_FFFFh$
$B4$: $4\_0000h - B\_FFFFh$
…
$B1$: $E\_0000h - F\_FFFFh$