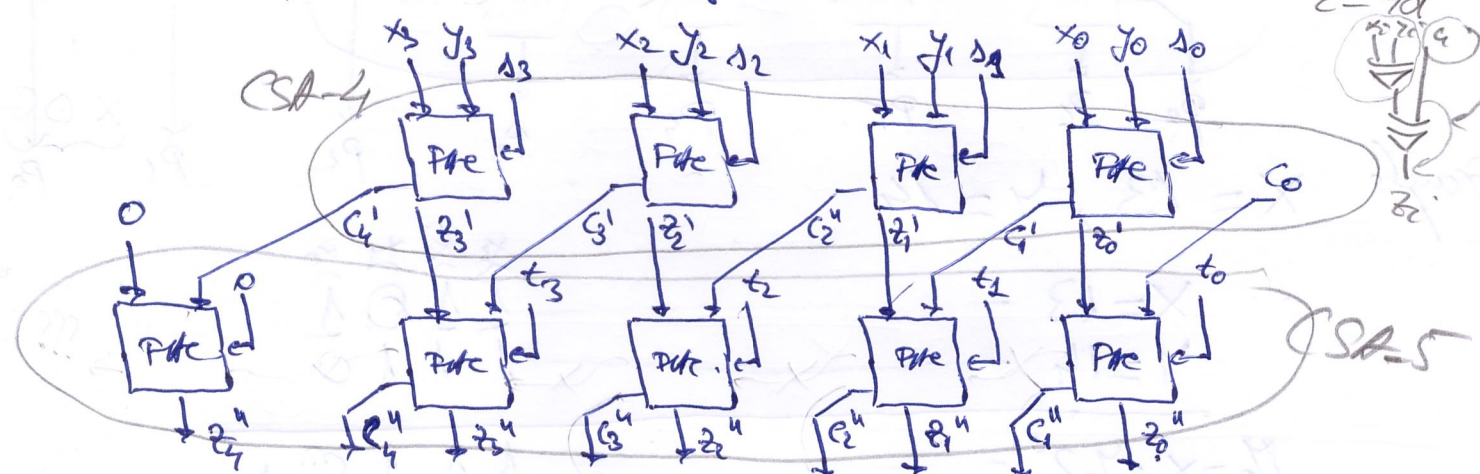


Carry Save Adder

- results in redundant format \rightarrow num vector
- carry vector is 1-bit more significant than the num vector
- used for multi-operand additions.
- multiplication.

Let X, Y, S, T 4-bit operands
 $X + Y + S + T = ?$

$2/cut$
 $D_{CSA} = 2d$
 $z = 4d$



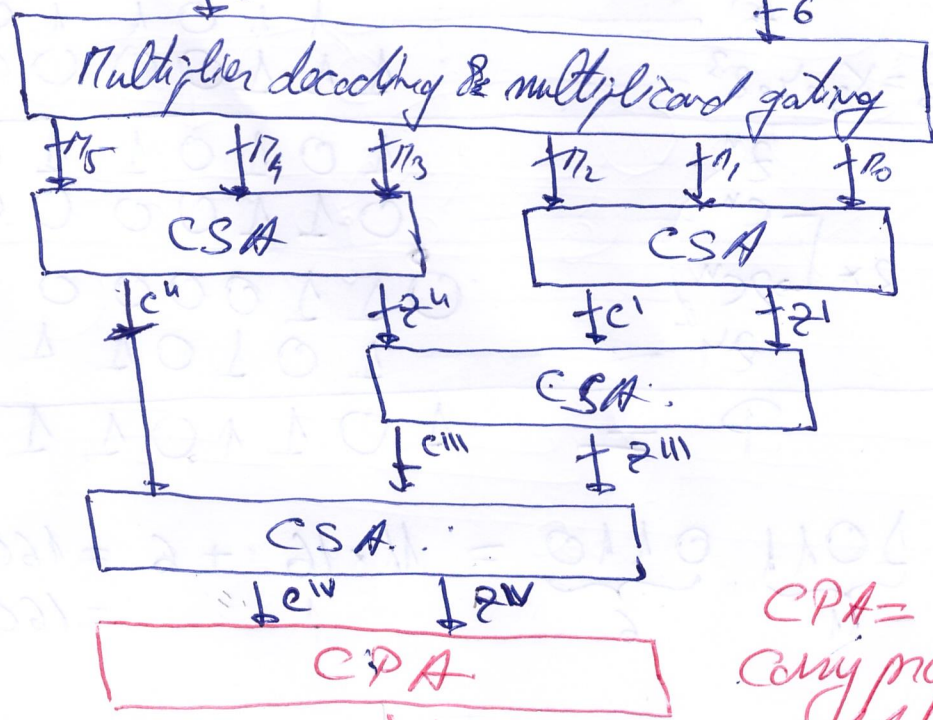
CSA - used for combinational multiplication.

Let X, Y - 6 bits, unsigned.

$$P = X \cdot Y = \sum_{i=0}^5 m_i$$

$X \pm 6$ $Y \pm 6$

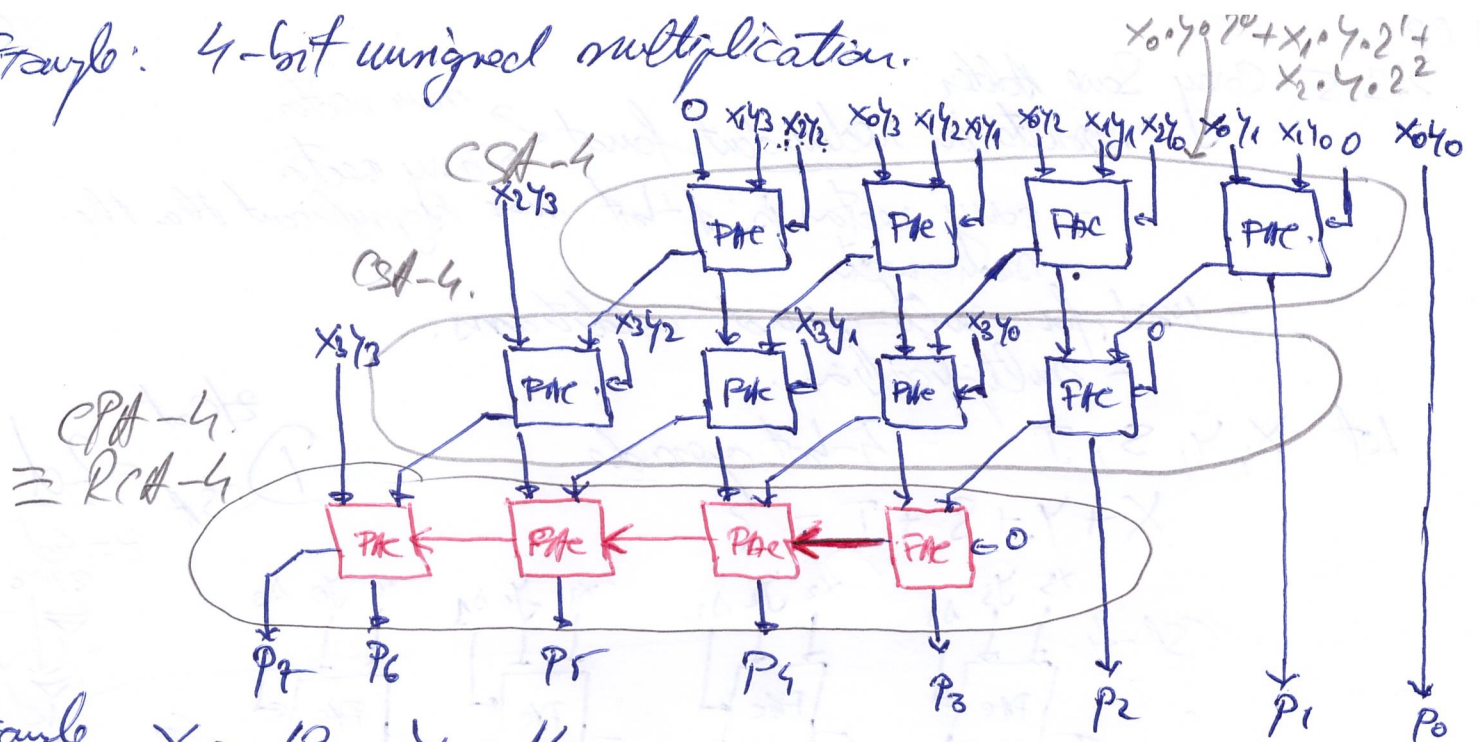
m_i - 1-bit product
 $m_i = x_i \cdot y_i \cdot 2^i$



CPA =
 carry propagate
 adder
 DAA, CLA, PL-CLA, SRA,
 CSOA, CSA

P

Example: 4-bit unsigned multiplication.



Example: $X = 13$, $Y = 14$

$$\begin{array}{r} X = 13 \quad \underline{} \\ Y = 14 \quad \underline{} \end{array} \quad \begin{array}{cccc} x_3 & x_2 & x_1 & x_0 \\ 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 0 \end{array}$$

$$\begin{array}{r} P_0 = x_0 \cdot y_0 \cdot 2^0 \quad \underline{} \quad 1 \ 1 \ 1 \ 0 \\ P_1 = x_1 \cdot y_0 \cdot 2^1 \quad \underline{} \quad 0 \ 0 \ 0 \ 0 \ 0 \\ P_2 = x_2 \cdot y_0 \cdot 2^2 \quad \underline{} \quad 1 \ 1 \ 1 \ 0 \ 0 \ 0 \end{array} \quad \left| \begin{array}{l} \\ + \text{CSA} \end{array} \right.$$

$$\begin{array}{r} 2^1 \\ C^1 \end{array} \quad \begin{array}{r} \underline{} \quad 1 \ 1 \ 0 \ 1 \ 1 \ 0 \\ \underline{} \quad 0 \ 0 \ 1 \ 0 \ 0 \ 0 \end{array}$$

$$\begin{array}{r} 2 \times \left[\begin{array}{l} 2^1 \\ C^1 \end{array} \right] \rightarrow 2^{c^1} \\ 2^1 \end{array} \quad \begin{array}{r} \underline{} \quad 0 \ 0 \ 1 \ 0 \ 0 \ 0 \\ \underline{} \quad 1 \ 1 \ 0 \ 1 \ 1 \ 0 \end{array} \quad \left| \begin{array}{l} \\ + \text{CSA} \end{array} \right.$$

$$\begin{array}{r} 2^4 \\ C^4 \end{array} \quad \begin{array}{r} \underline{} \quad 1 \ 0 \ 1 \ 0 \ 1 \ 1 \ 0 \\ \underline{} \quad 0 \ 1 \ 1 \ 0 \ 0 \ 0 \end{array}$$

$$\begin{array}{r} 2 \times \left[\begin{array}{l} 2^4 \\ C^4 \end{array} \right] \rightarrow 2^{c^4} \\ 2^4 \end{array} \quad \begin{array}{r} \underline{} \quad 0 \ 1 \ 1 \ 0 \ 0 \ 0 \\ \underline{} \quad 1 \ 0 \ 1 \ 0 \ 1 \ 1 \ 0 \end{array} \quad \left| \begin{array}{l} \\ + \text{CFA} \end{array} \right.$$

$$P = 1 \ 0 \ 1 \ 1 \ 0 \ 1 \ 1 \ 0$$

$$P = \underbrace{1011}_{11} \underbrace{0110}_6 = 11 \times 16 + 6 = 160 + 16 + 6 = 182$$

$$\begin{array}{r} 14 \\ 13 \\ \hline 42 \\ 14 \\ \hline 182 \end{array}$$

2.4. Reliable computing

(2)

- performance
- power consumption
- reliability !!!

Attributes of a reliable computing

- availability: readiness of system service
- reliability: continuity of system service
- maintainability: ability to undergo system repairs or modifications.

2.4.1 Binary adders with parity control.

ATT

fault $\xrightarrow{\text{actuals}}$ error $\xrightarrow{\text{negative}}$ failure $\xrightarrow{\text{causality}}$ fault

→ increase reliability by using parity control.
- attach an even parity bit to all operands

X, Y, C_{in}

$X + Y + C_0 \rightarrow Z$
Cont.

$$X_p = X_{n-1} \oplus X_{n-2} \oplus \dots \oplus X_1 \oplus X_0$$

$$Y_p = Y_{n-1} \oplus Y_{n-2} \oplus \dots \oplus Y_1 \oplus Y_0$$

$$Z_p = Z_{n-1} \oplus Z_{n-2} \oplus \dots \oplus Z_1 \oplus Z_0$$

→ verify parity of Z, all carrys without constant

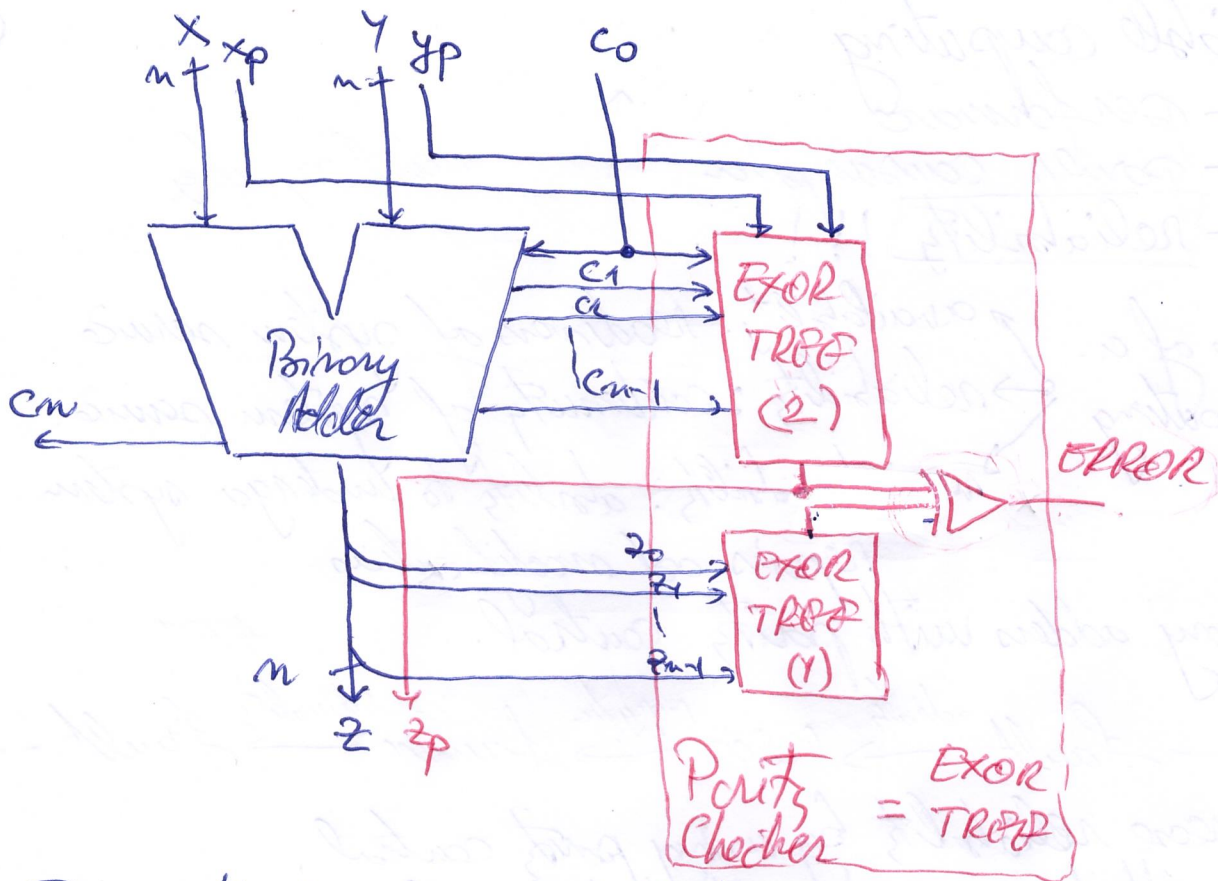
$$Z_i = X_i \oplus Y_i \oplus C_i \rightarrow (1) \quad \text{Let } C_p = C_{n-1} \oplus C_{n-2} \oplus \dots \oplus C_0$$

$$\Rightarrow Z_p = X_{n-1} \oplus Y_{n-1} \oplus C_{n-1} \oplus X_{n-2} \oplus Y_{n-2} \oplus C_{n-2} \oplus \dots \oplus X_0 \oplus Y_0 \oplus C_0$$

$$Z_p = X_p \oplus Y_p \oplus \underbrace{C_{n-1} \oplus C_{n-2} \oplus \dots \oplus C_0}_{C_p}$$

$$(2) Z_p = X_p \oplus Y_p \oplus C_p$$

⇒ predict value of Z_p (1)

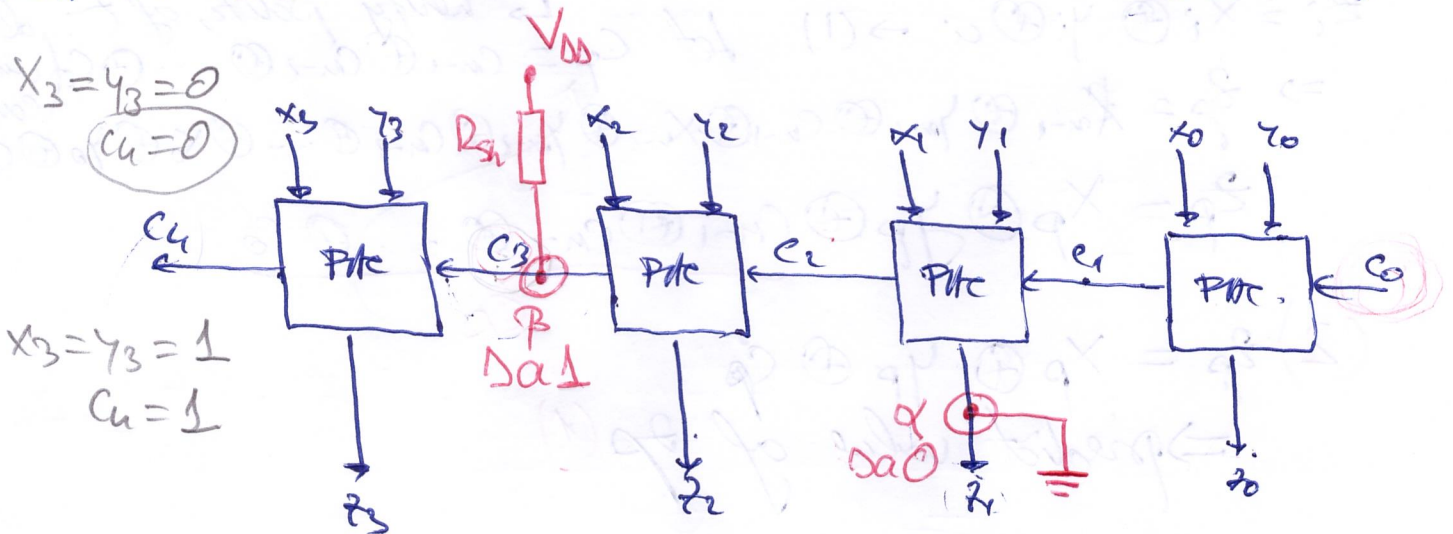


Errors that can affect the binary adder.

- multiple faults
- single faults \rightarrow harder to detect
- logic manifestation

Single Stuck-at Fault (SSaF)

RCA on 4 bits.



α : $z_1 \text{ Da } 0 \rightarrow$ only z_1 is affected.

$\rightarrow c_2$ is not affected

\Rightarrow odd no of bits affected.

P : $c_3 \text{ Da } 1 \rightarrow c_3$ is affected $\Rightarrow z_3$ is affected.

$\Rightarrow c_4$ can be affected $\Rightarrow z_4$ can be affected

\Rightarrow even no of bits are affected.

Can parity control detect both α & β SSAF

(3)

fault-free case

input bits

$$\begin{array}{rcl}
 X & = & 0011 \\
 Y & = & 0011 \\
 \hline
 C & = & 00110 \\
 Z & = & 0110
 \end{array}
 \left\{
 \begin{array}{l}
 x_p = 0 \oplus 0 \oplus 1 \oplus 1 = 0 \\
 y_p = 0 \\
 c_p = 0 \\
 \rightarrow z_p(2) = 0 \oplus 0 \oplus 0 \oplus 0 = 0 \\
 \rightarrow z_p(1) = 0 \oplus 1 \oplus 1 \oplus 0 = 0
 \end{array}
 \right.$$

no error!!

Fault α

$$\begin{array}{rcl}
 X & = & 0011 \\
 Y & = & 0011 \\
 \hline
 C & = & 00110 \\
 Z & = & 0100
 \end{array}
 \left\{
 \begin{array}{l}
 x_p = 0 \\
 y_p = 0 \\
 c_p = 0 \\
 \rightarrow z_p(2) = 0 \\
 \rightarrow z_p(1) = 1
 \end{array}
 \right.$$

difference !!!

Fault β

$$\begin{array}{rcl}
 X & = & 0011 \\
 Y & = & 0011 \\
 \hline
 C & = & 01110 \\
 Z & = & 1110
 \end{array}
 \left\{
 \begin{array}{l}
 x_p = 0 \\
 y_p = 0 \\
 c_p = 1 \\
 \rightarrow z_p(2) = 1 \\
 \rightarrow z_p(1) = 1
 \end{array}
 \right.$$

NO difference !!!

no Error ? ! ?

Single parity bits cannot detect all possible SSAF.
- cannot detect errors on the carry chain

$$\begin{array}{rcl}
 X & = & 0001 \\
 Y & = & 0001 \\
 \hline
 C & = & 00010 \\
 Z & = & 0010
 \end{array}$$

$$\left\{
 \begin{array}{l}
 x_p = 1 \\
 y_p = 1 \\
 c_p = 1 \\
 \rightarrow z_p(1) = 1
 \end{array}
 \right.$$