**Design the memory map and memory decoder for a 16 bits microprocessor (20 address lines) system using the following memory requirements:**

- **128KB ROM, using 64K x 16 bits memories**
- **256KB SRAM, using 128K x 16 bits memories, at the beginning**
- **512KB DRAM, using 128K x 16 bits memories**

$$\boldsymbol{Address\ Space}: \mathbf{2^{20} = 1MB = 10\ 0000h}$$
$$\boldsymbol{Address\ Range}: \mathbf{0\ 0000h - F\ FFFFh}$$

**STEP 1**

$$\#\boldsymbol{circuits} = \frac{\boldsymbol{total\ memory\ req}}{\boldsymbol{circuit\ memory}}$$

$$ROM\ \#\ circuits\ = \frac{128\ KB}{64\ K * 16b} = \frac{128\ KB}{128\ KB} = 1\ circuit$$

$$SRAM\ \#\ circuits\ = \frac{256\ KB}{128\ K * 16b} = \frac{256\ KB}{256\ KB} = 1\ circuit$$

$$DRAM\ \#\ circuits = \frac{512\ KB}{128\ K * 16b} = \frac{512\ KB}{256\ KB} = 2\ circuits$$

$$ROM\ circuit\ size = 128KB = 2^{17} = 2\_0000h$$
$$SRAM\ circuit\ size = 256KB = 2^{18} = 4\_0000h$$
$$ROM\ circuit\ size = 256KB = 2^{18} = 4\_0000h$$

**STEP 2**

$$\#\frac{\boldsymbol{circuits}}{\boldsymbol{block}} = \frac{\boldsymbol{processor\ bits}}{\boldsymbol{circiut\ bits}}$$

$$\#\ \boldsymbol{blocks} = \frac{\#\ \boldsymbol{circuits}}{\#\ \boldsymbol{circuits\ per\ block}}$$

$$\boldsymbol{block\ size} = \frac{\boldsymbol{total\ memory\ req}}{\#\ \boldsymbol{blocks}}$$

$$ROM\ \#\frac{circuits}{block} = \frac{16}{16} = 1\ cpb$$

$$ROM\ \#\ blocks = \frac{1}{1} = 1 \rightarrow B1$$

$$ROM\ block\ size = \frac{128KB}{1} = 128KB$$

$$SRAM\ \#\frac{circuits}{block} = \frac{16}{16} = 1$$

$$SRAM\ \#\ blocks = \frac{1}{1} = 1 \rightarrow B2$$

$$SRAM\ block\ size = \frac{256KB}{1} = 256KB$$

$$DRAM\ \#\frac{circuits}{block} = \frac{16}{16} = 1$$

$$DRAM\ \#\ blocks = \frac{2}{1} = 2 \rightarrow B3, B4$$

$$DRAM\ block\ size = \frac{512KB}{2} = 256KB$$

**STEP 3**

| *BLOCK* | *BLOCK SIZE* | *ADDRESS LINES* | *ADDRESS RANGE* | | *BLOCK SIZE (hexa)* |
|---|---|---|---|---|---|
| B1 | 128 KB | 17 | 0x0_0000 | 0x1_FFFF | 0x2_0000 |
| B2 | 256 KB | 18 | 0x0_0000 | 0x3_FFFF | 0x4_0000 |
| B3 | 256 KB | 18 | 0x0_0000 | 0x3_FFFF | 0x4_0000 |
| B4 | 256 KB | 18 | 0x0000 | 0x3_FFFF | 0x4_0000 |

**STEP 4**

| *TYPE* | *BLOCK* | *MEMORY MAP* |
|---|---|---|
| SRAM | B2 | 0x0_0000 |
| | | 0x3_FFFF |
| ROM | B1 | 0x4_0000 |
| | | 0x5_FFFF |
| DRAM | B3 | 0x6_0000 |
| | | 0x9_FFFF |
| | B4 | 0xA_0000 |
| | | 0xD_FFFF |