Digital microsystems design

Lab 4

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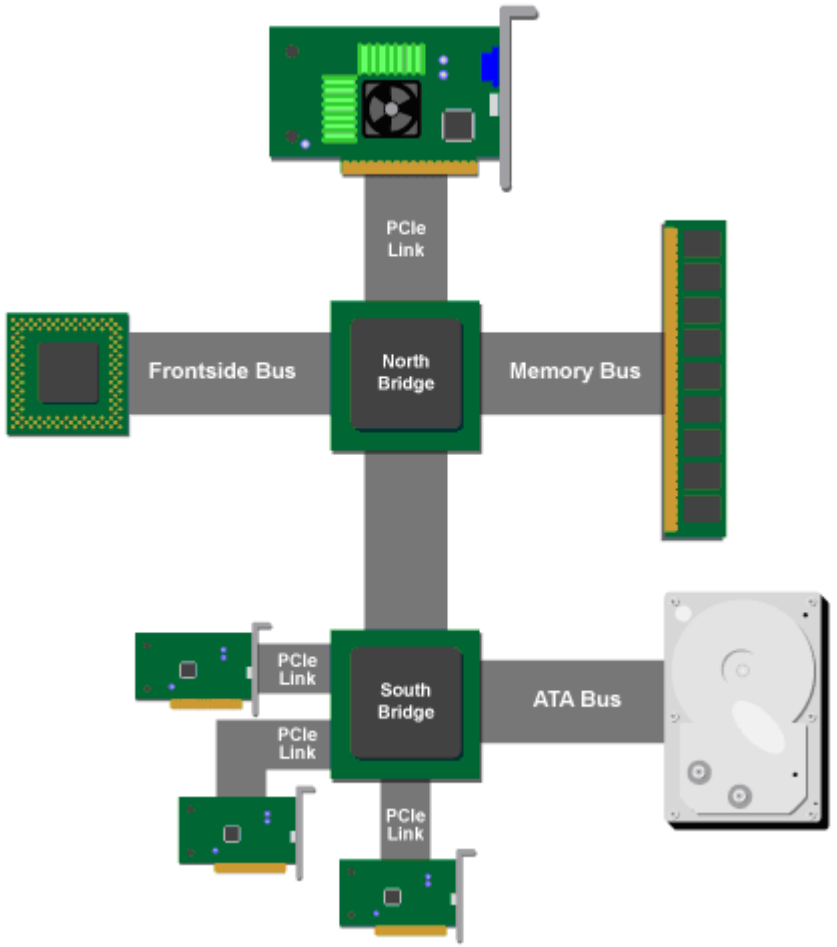
2018-2019

System architecture

- PCI express

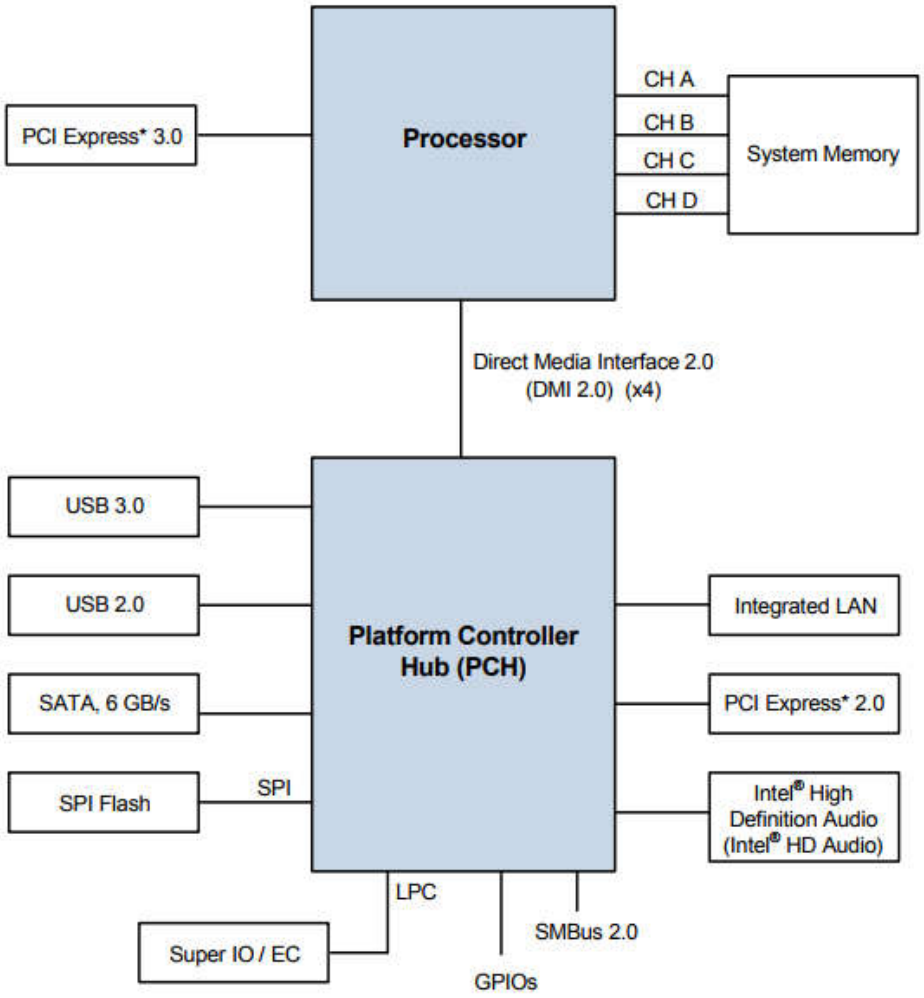


System architecture

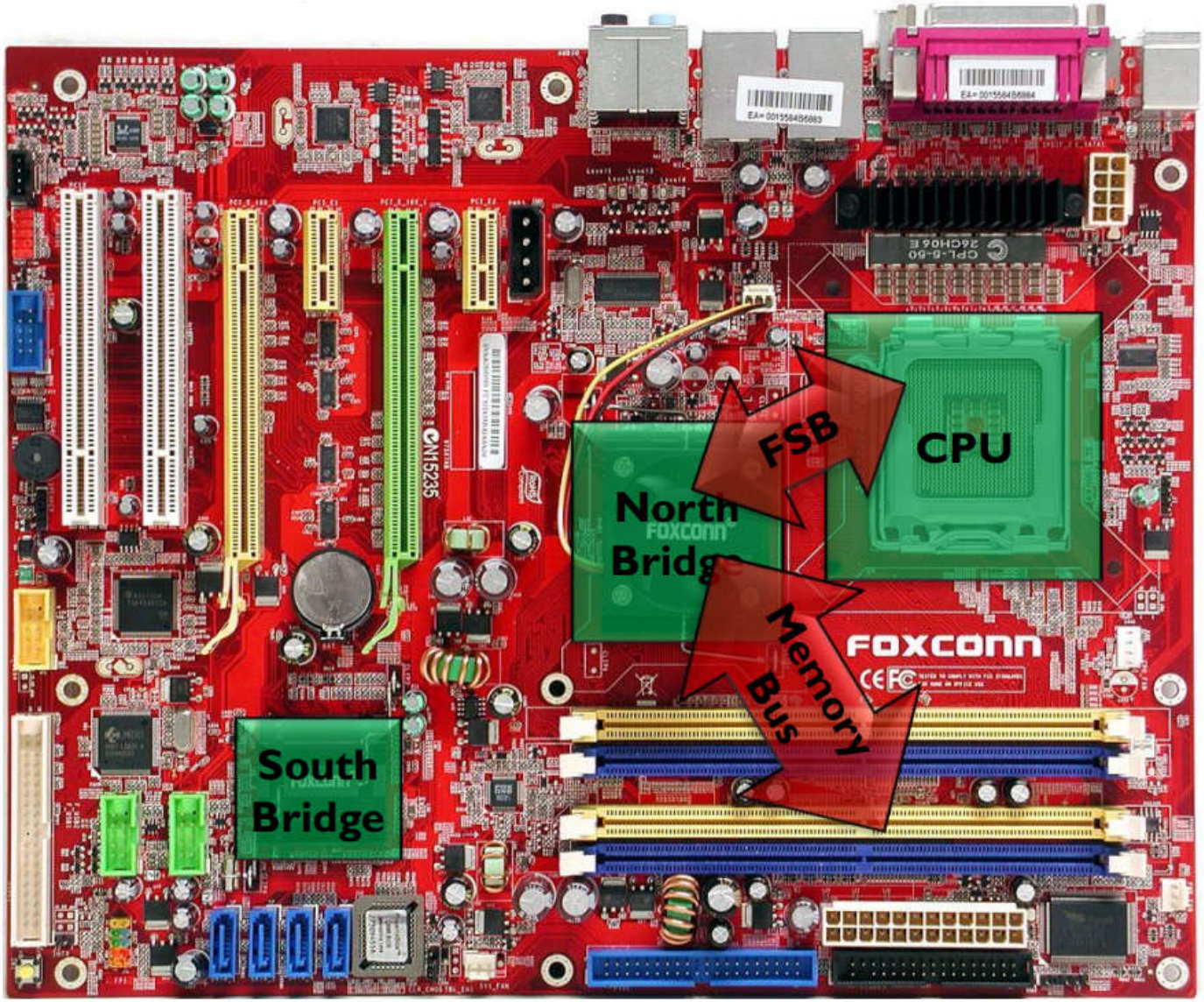
- Chipsets
  - Designed for use with a specific family of processors
  - Northbridge: connects the CPU to high-speed components like RAM, video card
  - Southbridge: connects to slower peripheral devices like PCI slots, USB, IDE, ...

System architecture

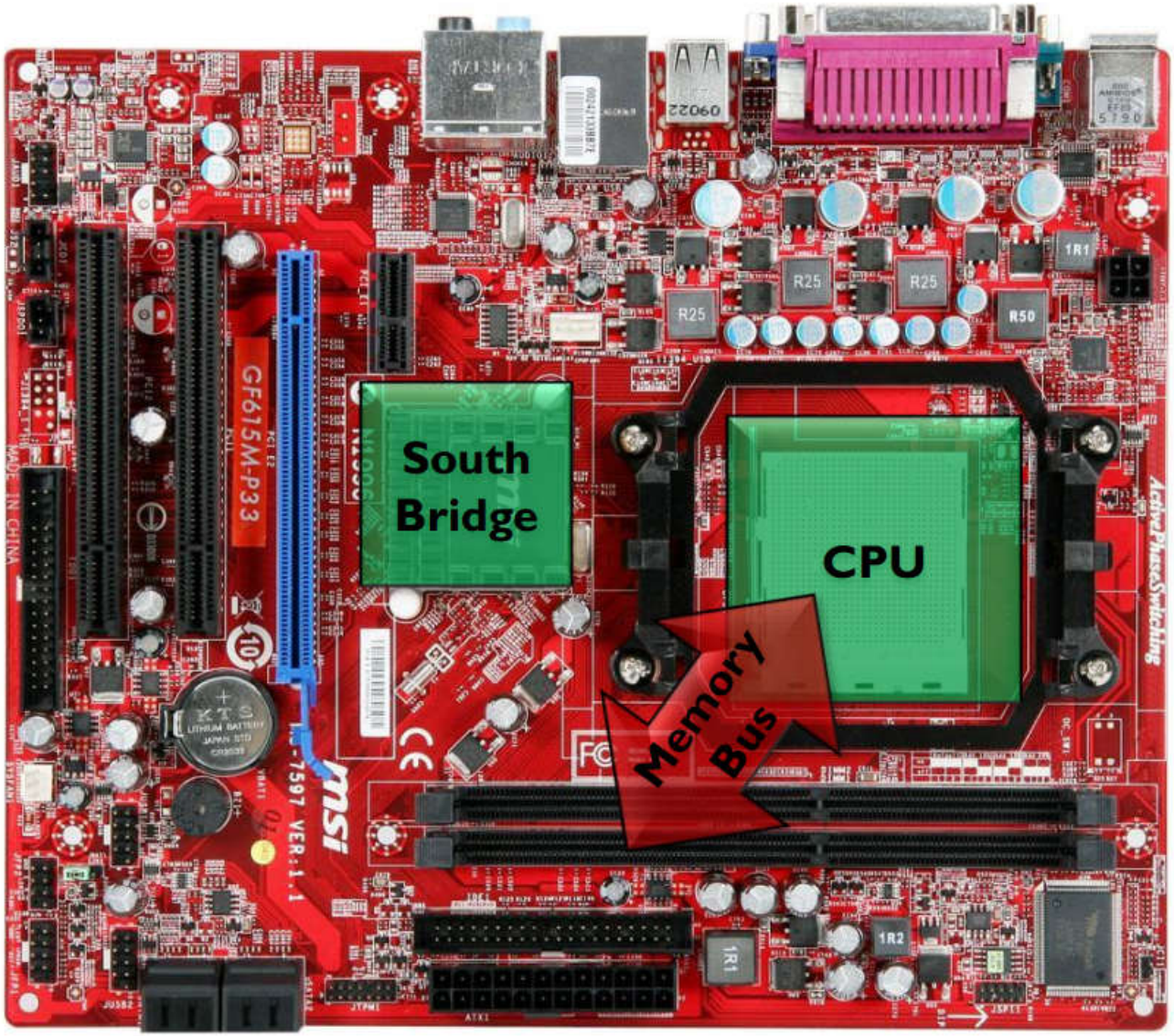
- iCore7



Mainboard

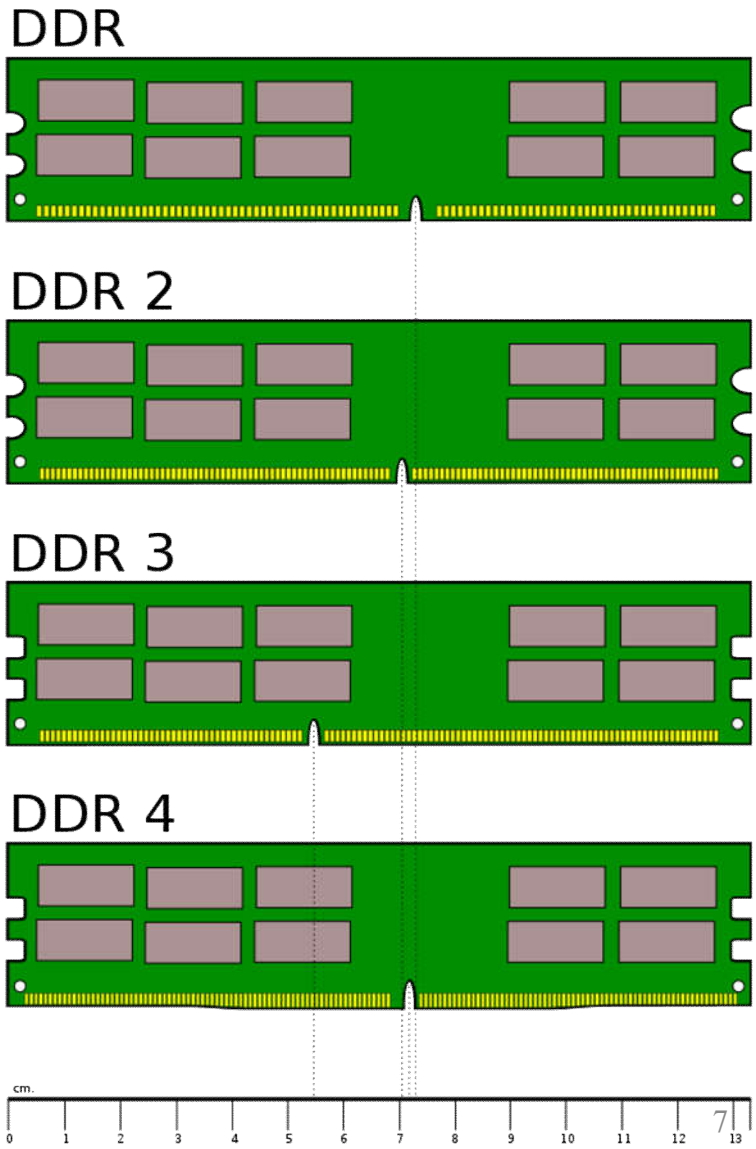


Mainboard



Main memory

- Main memory interface types
  - DIMM – Dual Inline Memory Module

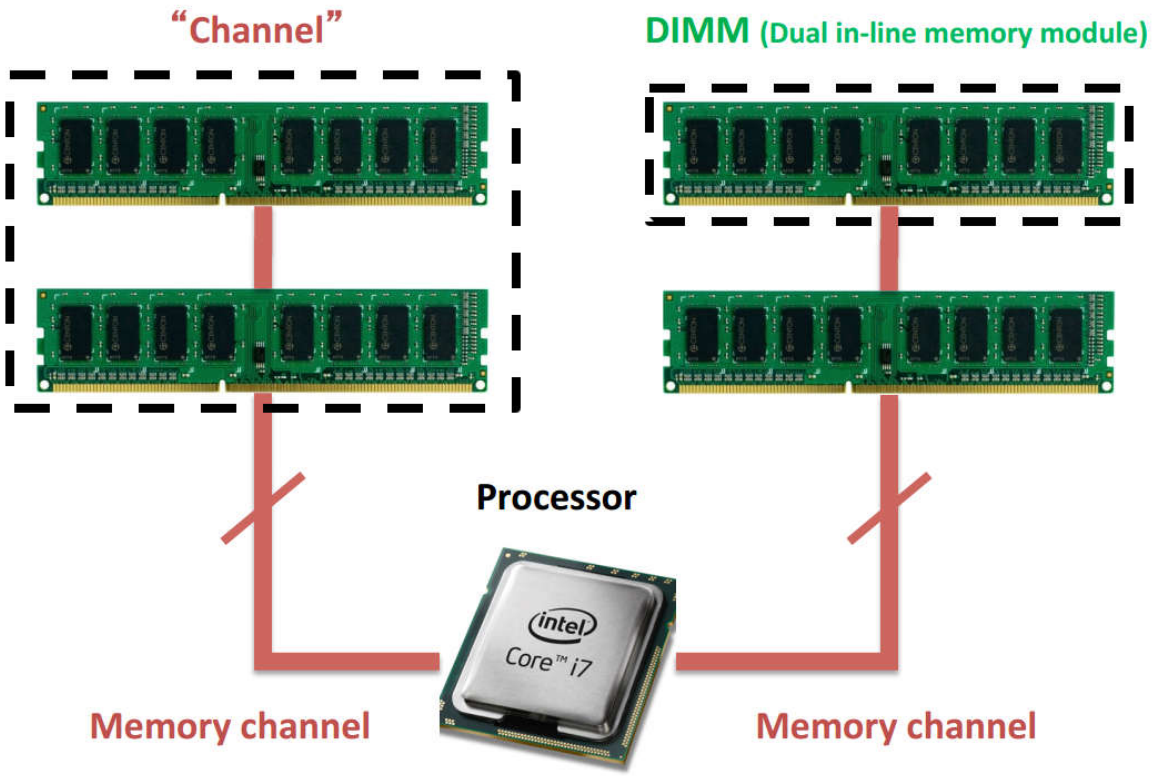


DRAM organization

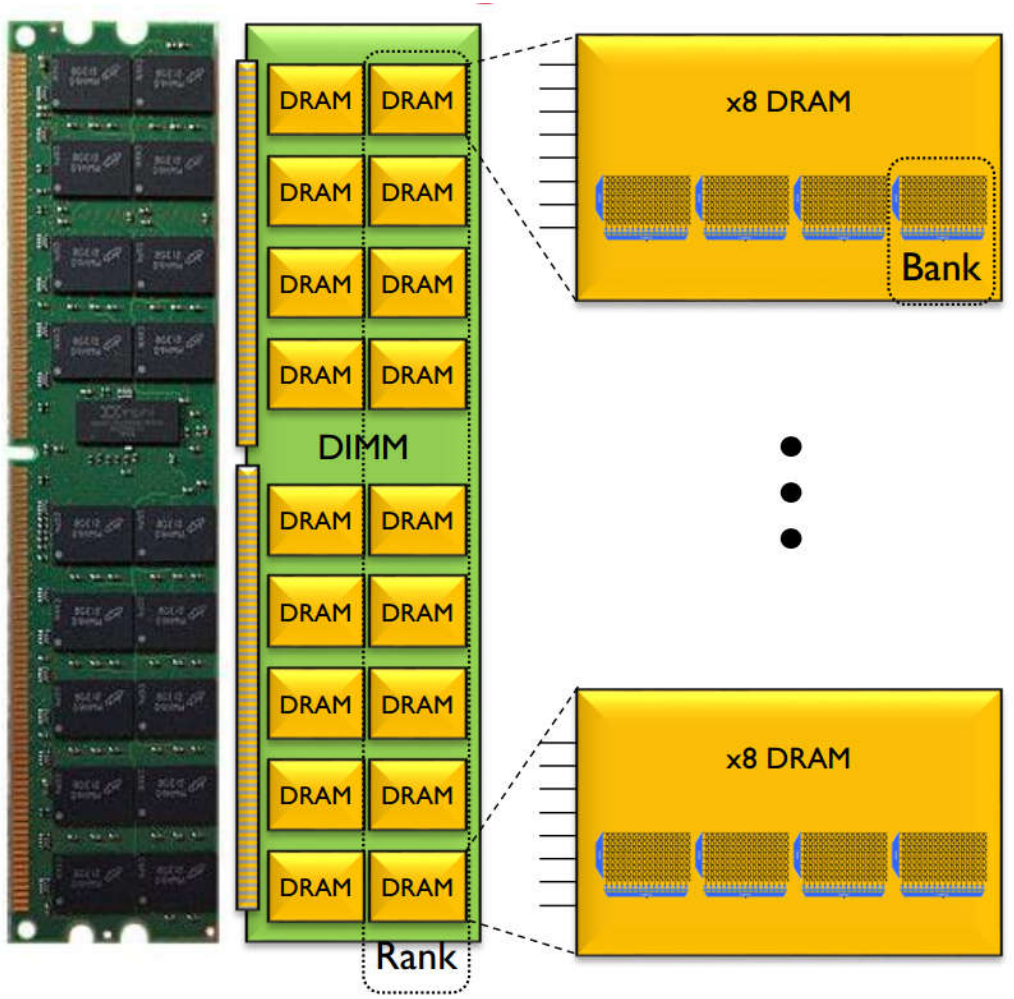
- Structures
  - DDR Channels
    - Single-channel, dual-channel, quad-channels
  - DDR Ranks
    - 1, 2, 4
  - DRAM Chips
    - 16, 8, 9
  - DRAM Banks
    - 1, 2, 4, 8
  - DRAM Rows
  - DRAM Columns
  - DRAM data bits

DRAM organization

- DRAM channels
  - Separate paths/channels to independent memories
  - Symultaneous access from the controller

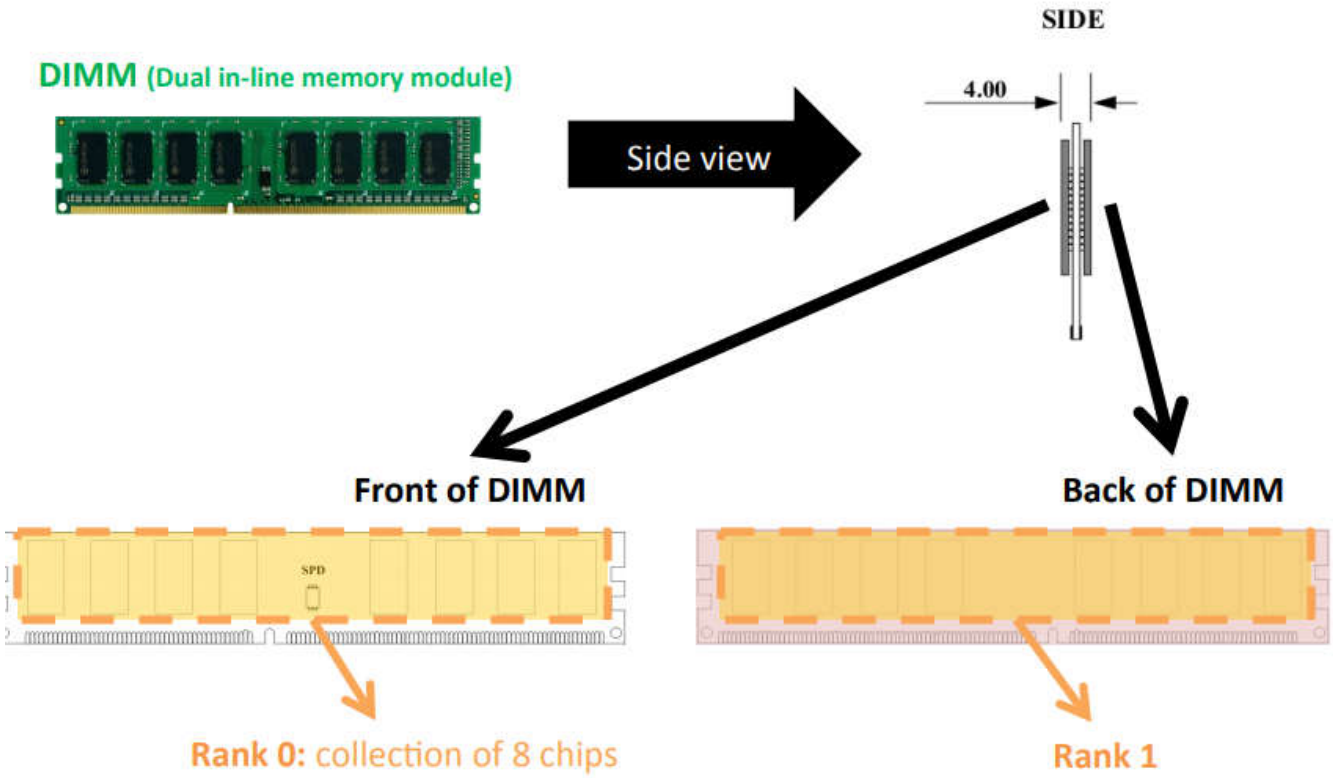


DRAM organization



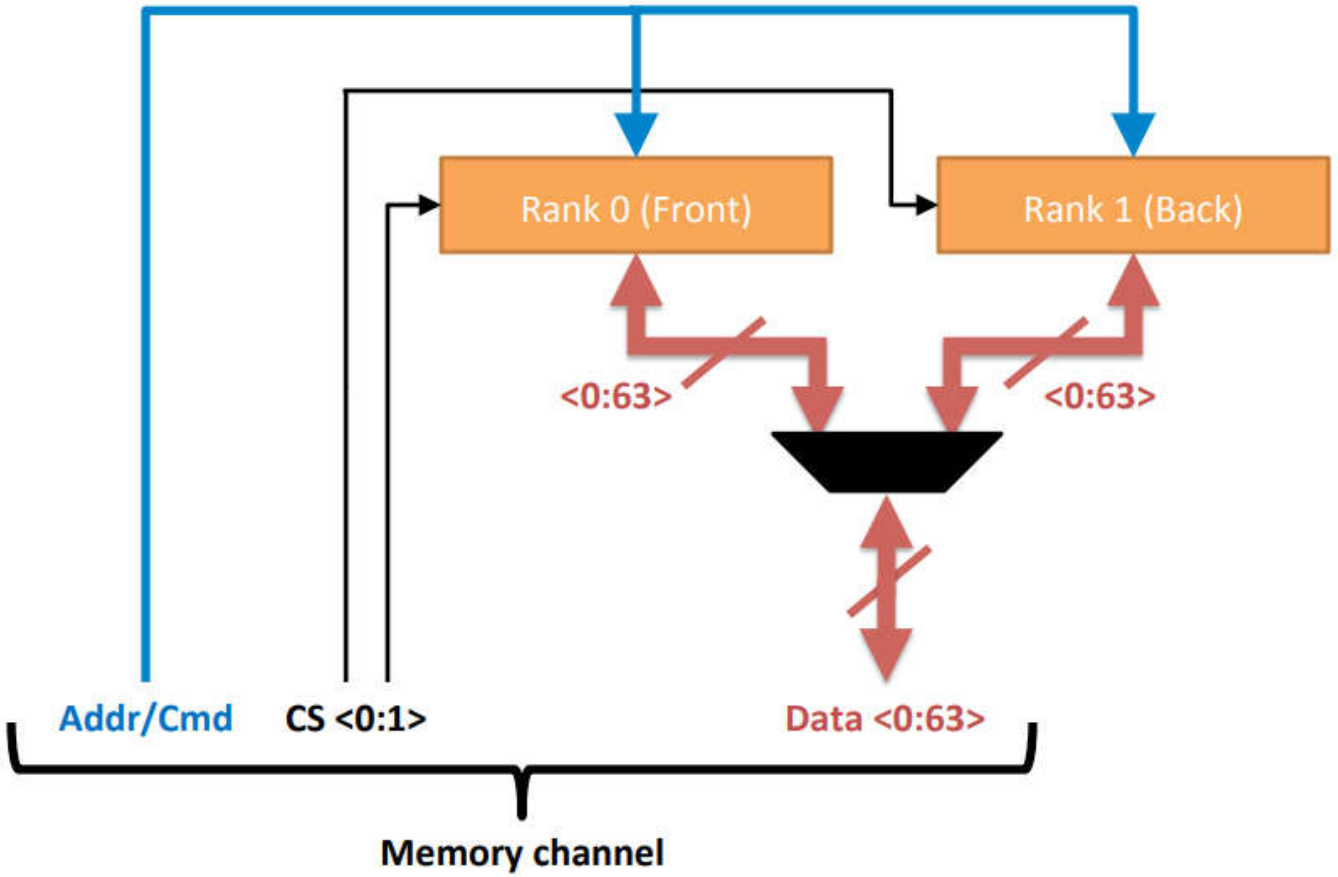
DRAM organization

- Memory ranks
  - Each rank has dedicated CS signal (a rank is a mem block)
  - 1, 2, 4 ranks / DIMM



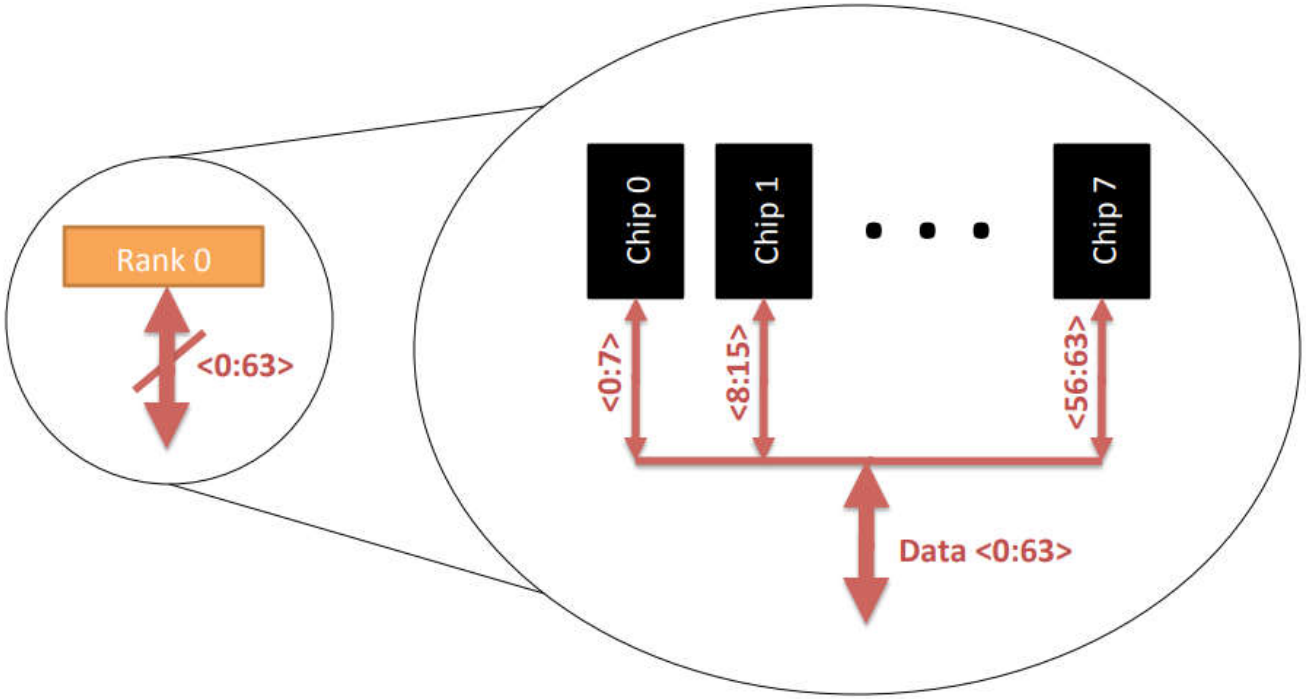
DRAM organization

- Memory ranks



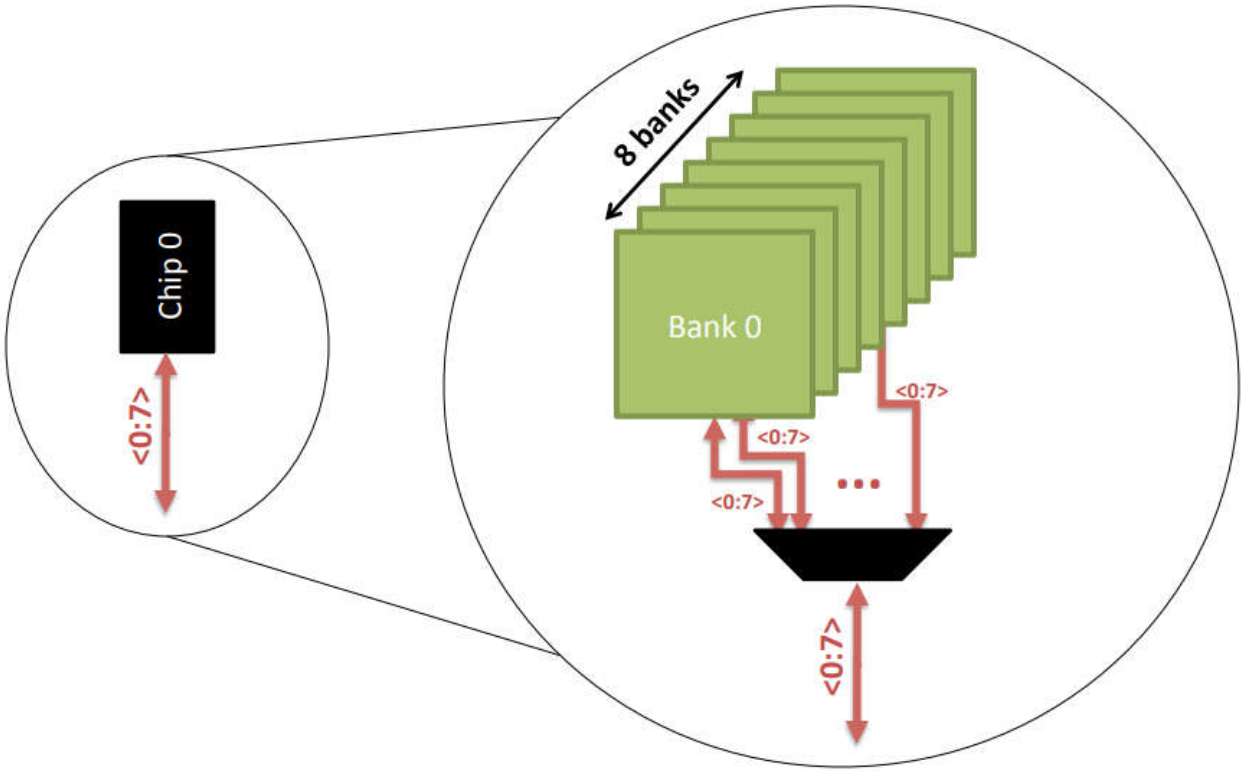
DRAM organization

- Memory chips per rank
  - A rank has 64 bits data bus width
  - Number of circuits per rank



DRAM organization

- Memory banks per chip
  - Support for interleaving



DRAM organization

- Memory banks

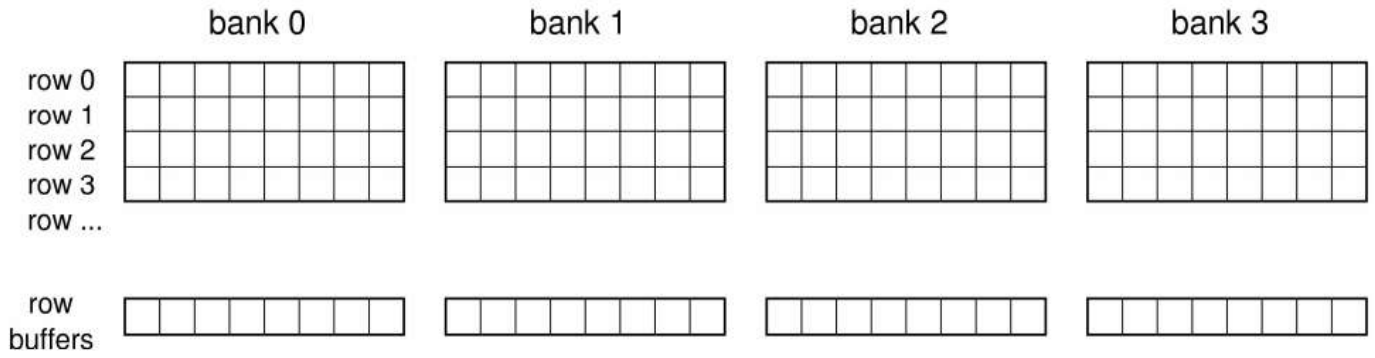
Typical figures:

4 – 8 banks

16K rows / bank

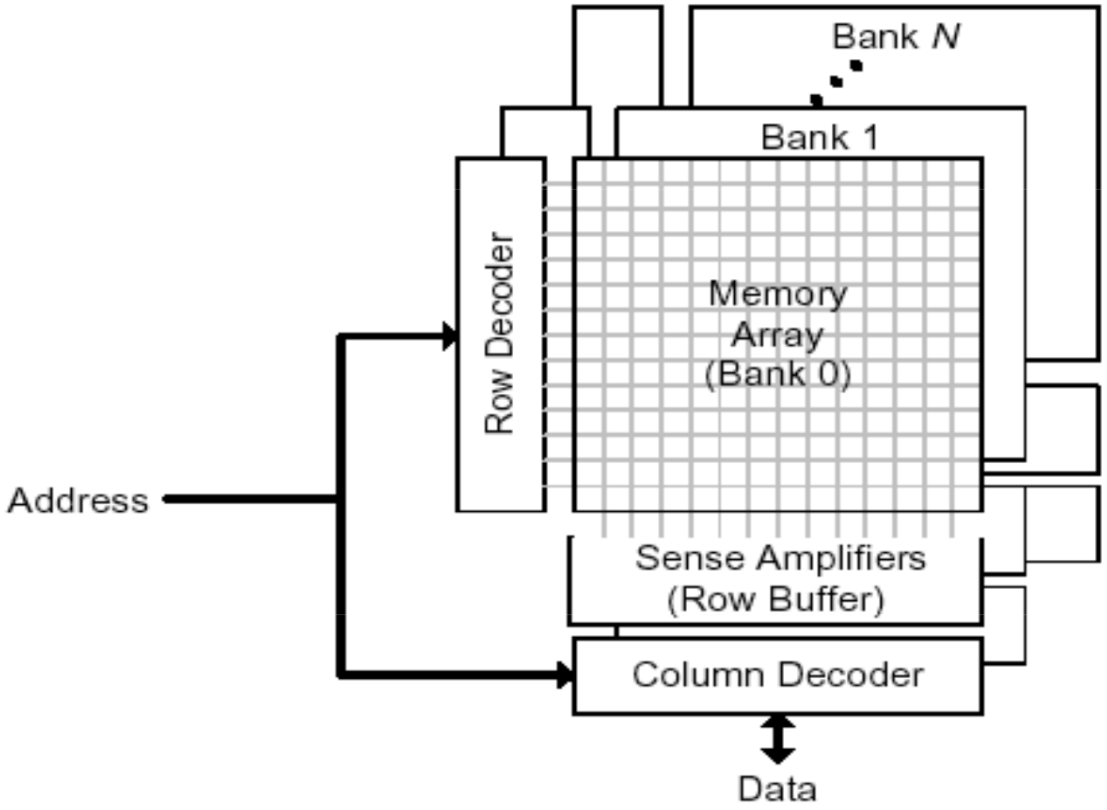
1024 columns / row

4 – 16 bits / column



DRAM memories

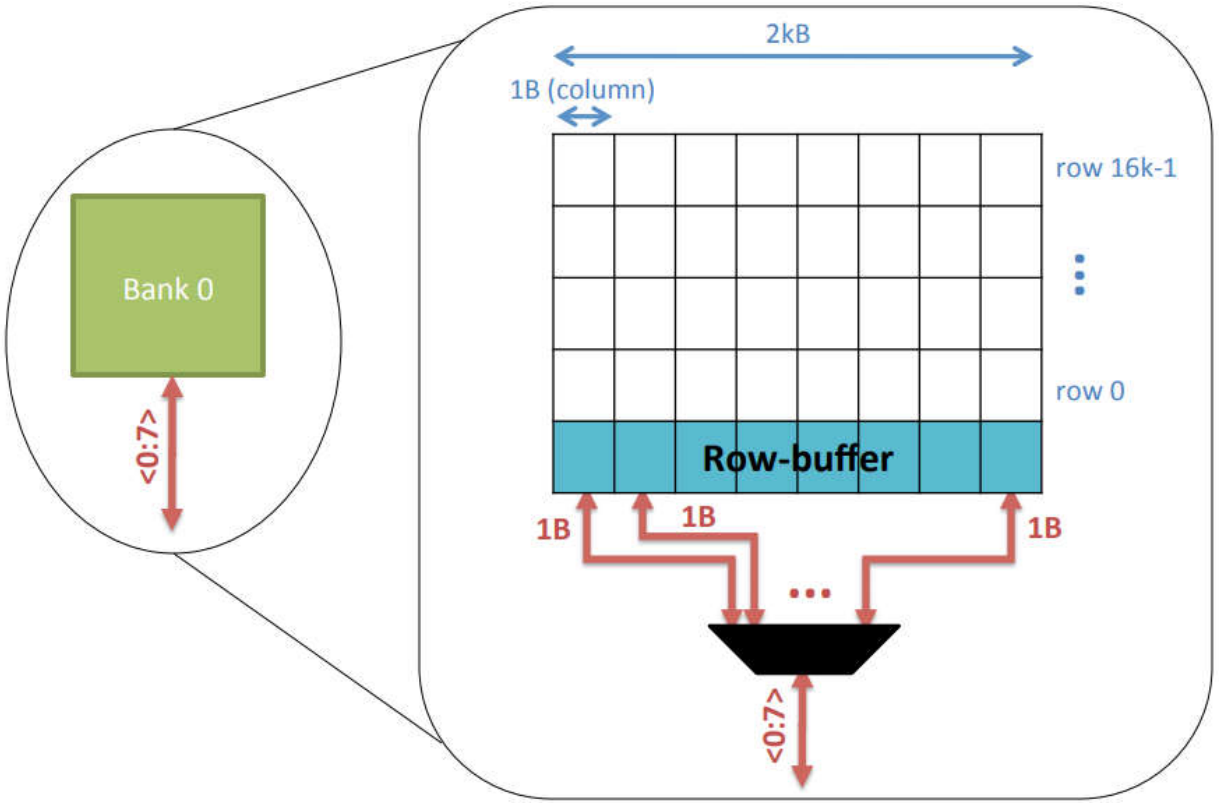
- 3-D DRAM



S. Rixner et al. Memory Access Scheduling. ISCA 2000.

DRAM organization

- Memory arrays per bank



Main memory

- DDR3
  - 2GB 2Rx8 PC3-8500U
  - 2GB 1Rx4 PC3-10600R

Standard name	Memory clock (MHz)	Cycle time (ns)	I/O bus clock (MHz)	Data rate (MT/s)	Module name	Peak transfer rate (MB/s)	Timings (CL-tRCD-tRP)	CAS latency (ns)
DDR3-800D DDR3-800E	100	10	400	800	PC3-6400	6400	5-5-5 6-6-6	12½ 15
DDR3-1066E DDR3-1066F DDR3-1066G	133⅓	7½	533⅓	1066⅔	PC3-8500	8533⅓	6-6-6 7-7-7 8-8-8	11¼ 13⅛ 15
DDR3-1333F* DDR3-1333G DDR3-1333H DDR3-1333J*	166⅔	6	666⅔	1333⅓	PC3-10600	10666⅔	7-7-7 8-8-8 9-9-9 10-10-10	10½ 12 13½ 15
DDR3-1600G* DDR3-1600H DDR3-1600J DDR3-1600K	200	5	800	1600	PC3-12800	12800	8-8-8 9-9-9 10-10-10 11-11-11	10 11¼ 12½ 13¾
DDR3-1866J* DDR3-1866K DDR3-1866L DDR3-1866M*	233⅓	4²⁄₇	933⅓	1866⅔	PC3-14900	14933⅓	10-10-10 11-11-11 12-12-12 13-13-13	10⁵⁄₇ 11¹¹⁄₁₄ 12⁶⁄₇ 13¹³⁄₁₄
DDR3-2133K* DDR3-2133L DDR3-2133M DDR3-2133N*	266⅔	3¾	1066⅔	2133⅓	PC3-17000	17066⅔	11-11-11 12-12-12 13-13-13 14-14-14	10⁵⁄₁₆ 11¼ 12³⁄₁₆ 13⅛

* optional

CL - Clock cycles between sending a column address to the memory and the beginning of the data in response

tRCD - Clock cycles between row activate and reads/writes

tRP - Clock cycles between row precharge and activate

https://en.wikipedia.org/wiki/DDR3_SDRAM

Main memory

- DDR4

Standard name	Memory clock (MHz)	I/O bus clock (MHz)	Data rate (MT/s)	Module name	Peak transfer rate (MB/s)	Timings CL-tRCD-tRP	CAS latency (ns)
DDR4-1600J* DDR4-1600K DDR4-1600L	200	800	1600	PC4-12800	12800	10-10-10 11-11-11 12-12-12	12.5 13.75 15
DDR4-1866L* DDR4-1866M DDR4-1866N	233.33	933.33	1866.67	PC4-14900	14933.33	12-12-12 13-13-13 14-14-14	12.857 13.929 15
DDR4-2133N* DDR4-2133P DDR4-2133R	266.67	1066.67	2133.33	PC4-17000	17066.67	14-14-14 15-15-15 16-16-16	13.125 14.063 15
DDR4-2400P* DDR4-2400R DDR4-2400T DDR4-2400U	300	1200	2400	PC4-19200	19200	15-15-15 16-16-16 17-17-17 18-18-18	12.5 13.32 14.16 15
DDR4-2666T DDR4-2666U DDR4-2666V DDR4-2666W	325	1333	2666	PC4-21333	21333	17-17-17 18-18-18 19-19-19 20-20-20	12.75 13.50 14.25 15
DDR4-2933V DDR4-2933W DDR4-2933Y DDR4-2933AA	366.6	1466.5	2933	PC4-23466	23466	19-19-19 20-20-20 21-21-21 22-22-22	12.96 13.64 14.32 15
DDR4-3200W DDR4-3200AA DDR4-3200AC	400	1600	3200	PC4-25600	25600	20-20-20 22-22-22 24-24-24	12.50 13.75 15

https://en.wikipedia.org/wiki/DDR4_SDRAM

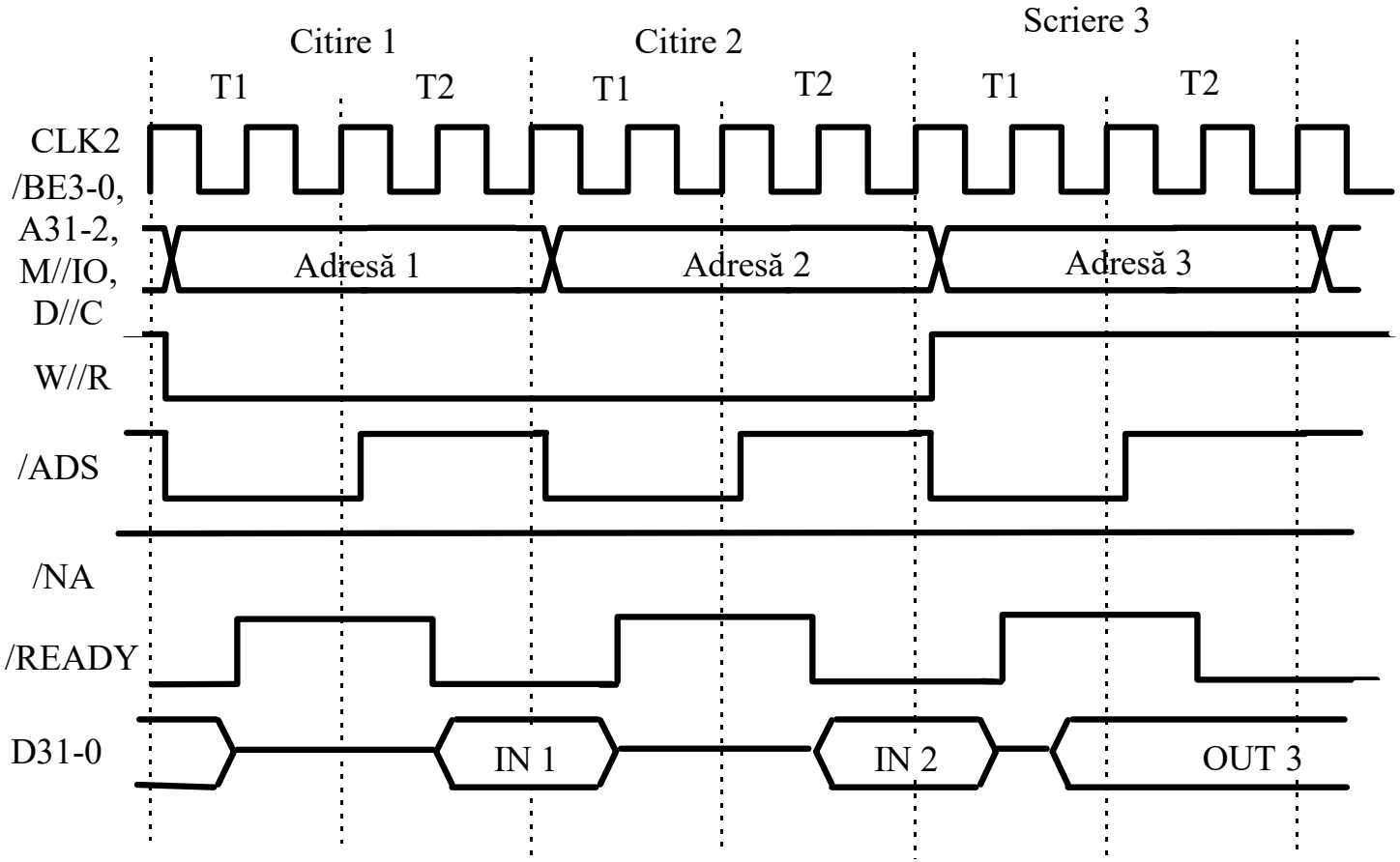
Main memory

- Chip size = 2^14*2^10*8banks*8bits = 2^4*2^20*8*8bits = 128 MB
- Rank size = 128 MB * 8 chips/rank = 1024 MB = 1GB
- DDR size = 2 ranks * 1GB = 2GB

Raw Card Version	DIMM Capacity	DIMM Organization	SDRAM Density	SDRAM Organization	Number of SDRAMs	Number of Physical Ranks	Number of Banks in SDRAM	Number of Address Bits Row/Column
A	512MB	64 Meg x 64	512 Megabit	64 Meg x 8	8	1	8	13/10
	1GB	128 Meg x 64	1 Gigabit	128 Meg x 8	8	1	8	14/10
	2GB	256 Meg x 64	2 Gigabit	256 Meg x 8	8	1	8	15/10
	4GB	512 Meg x 64	4 Gigabit	512 Meg x 8	8	1	8	16/10
	8GB	1 Gig x 64	8 Gigabit	1 Gig x 8	8	1	8	16/11
B	1GB	128 Meg x 64	512 Megabit	64 Meg x 8	16	2	8	13/10
	2GB	256 Meg x 64	1 Gigabit	128 Meg x 8	16	2	8	14/10
	4GB	512 Meg x 64	2 Gigabit	256 Meg x 8	16	2	8	15/10
	8GB	1 Gig x 64	4 Gigabit	512 Meg x 8	16	2	8	16/10
	16GB	2 Gig x 64	8 Gigabit	1 Gig x 8	16	2	8	16/11
C[1]	256MB	32 Meg x 64	512 Megabit	32 Meg x 16	4	1	8	12/10
	512MB	64 Meg x 64	1 Gigabit	64 Meg x 16	4	1	8	13/10
	1GB	128 Meg x 64	2 Gigabit	128 Meg x 16	4	1	8	14/10
	2GB	256 Meg x 64	4 Gigabit	256 Meg x 16	4	1	8	15/10

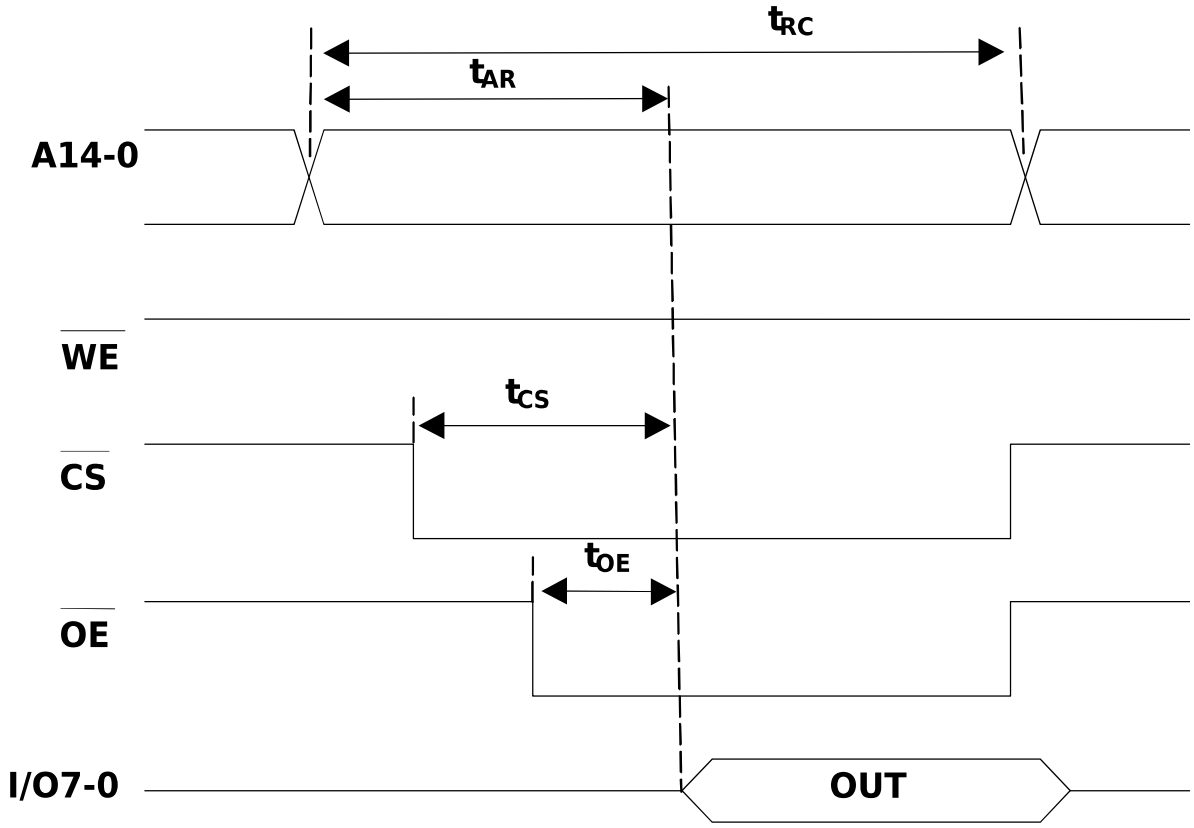
Machine cycles

- Normal cycles



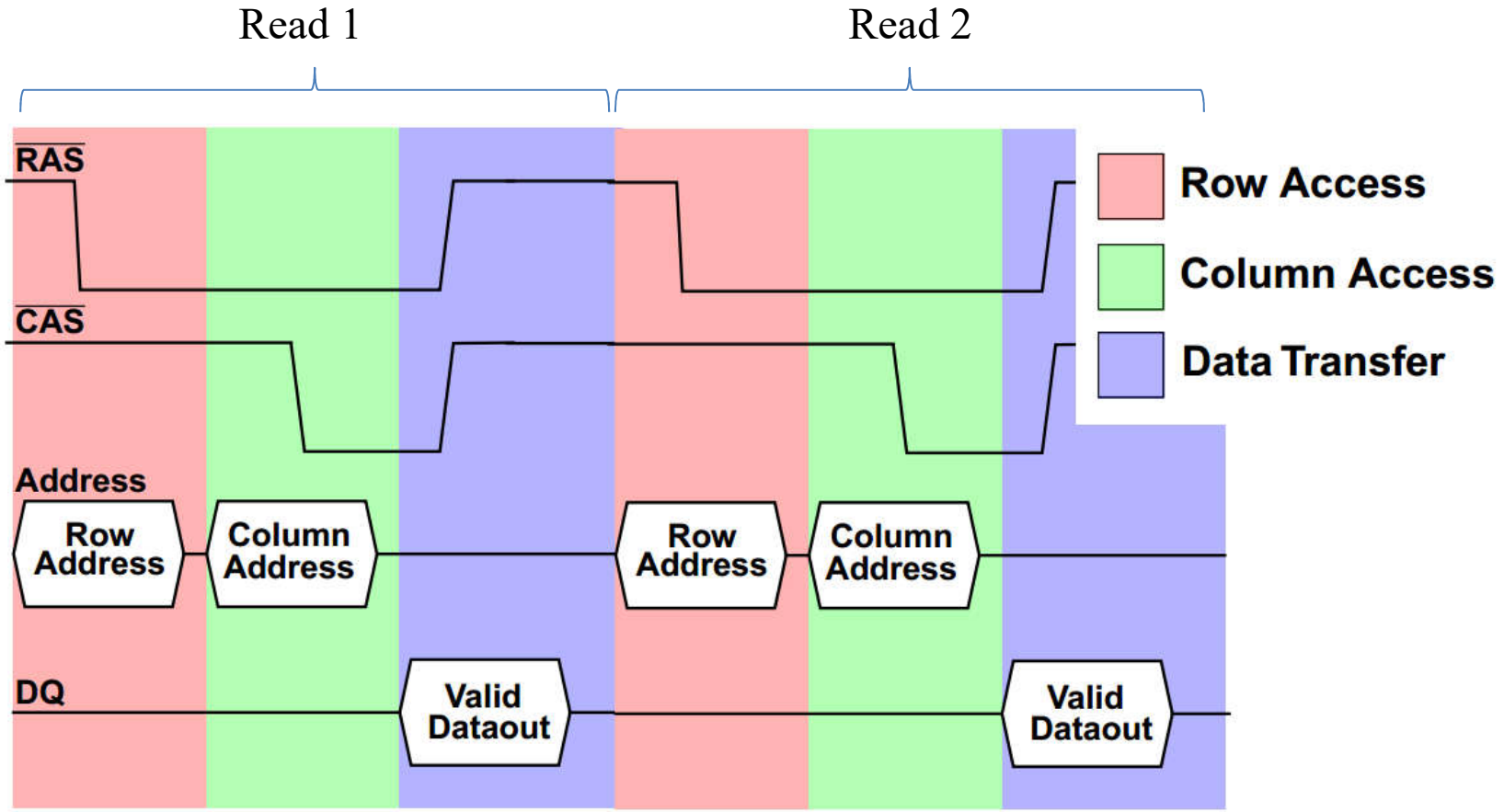
SRAM memories

- SRAM read access cycle



DRAM operation

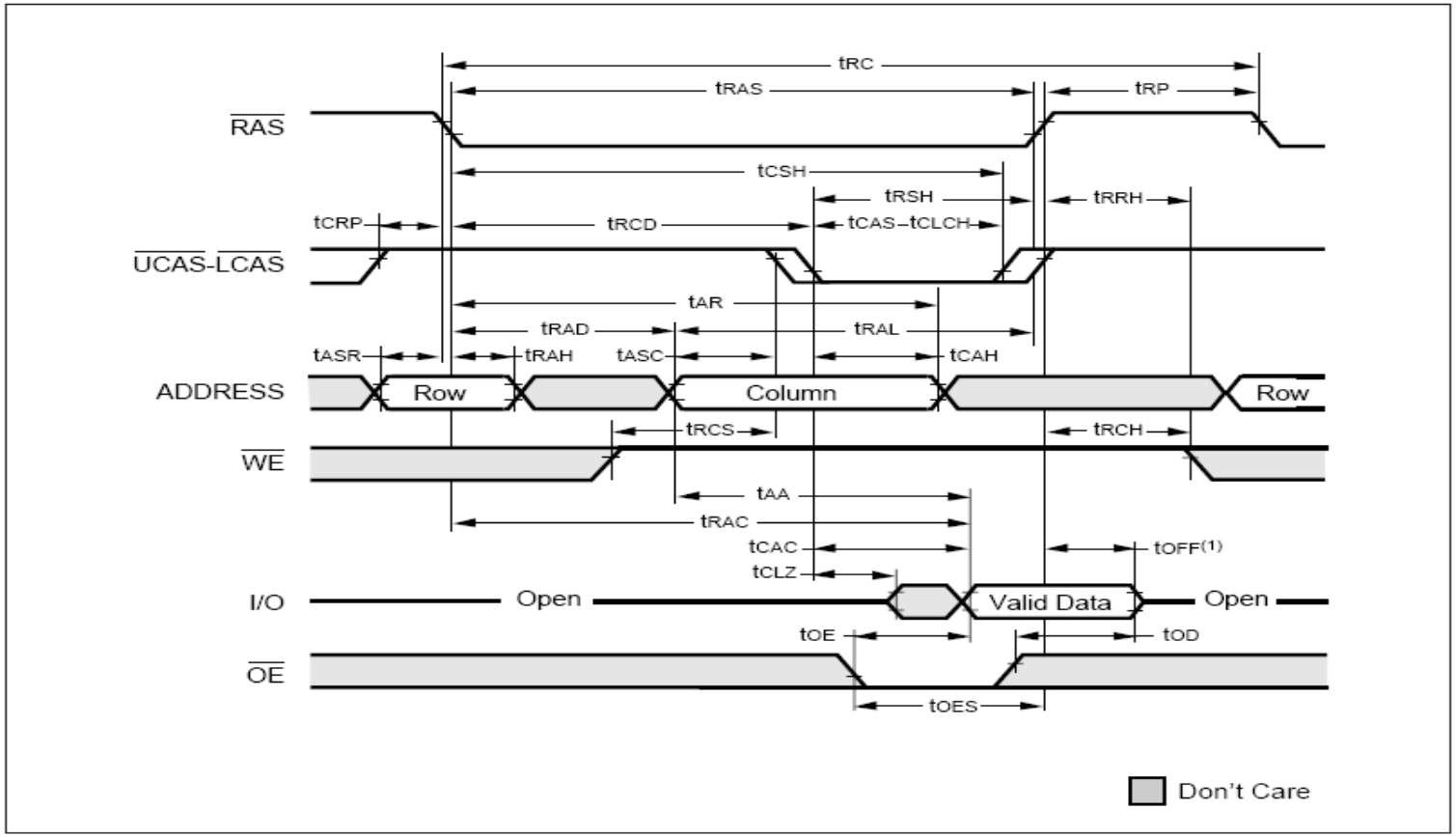
- Read cycles for conventional DRAM



DRAM operation

- Read cycle

READ CYCLE



Note:
1. t_{OFF} is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.