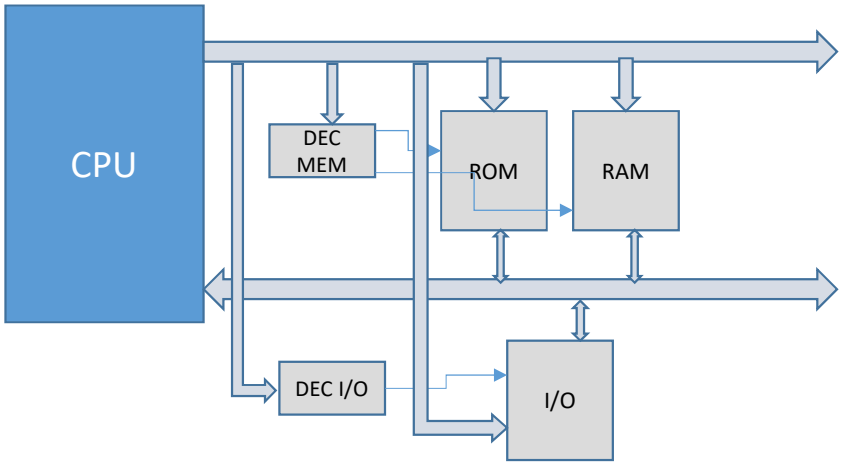
# Digital microsystems design

Lab 3

# Overview

- External connectivity of a microprocessor
  - Memory / I/O connectivity



# Exercise

- Design the memory map and the memory decoder for a 32bits uP system using the following memory requirements:
  - 256MB EPROM ending at FFFFFFFFH, using 64M x 16bits memories
  - 512MB SRAM, using 64M x 8 bits memories
  - 1GB DRAM, using 128M x 4 bits memories, placed as a contiguous memory address space

# Solution

- Determine the size of the whole address space of the processor
- Determine the number of memory circuits required by the design
- Determine the number of 32bits blocks and their sizes (in MB and hexa)
- Determine the number of selection lines
- Design the memory map
- Design the memory decoder using a 3-to-8 decoder

# Solution

- Determine the size of the whole address space of the processor
  - Max amount of memory = 2 ^ address bus width of the processor
  - 2^32 = 2^2 x 2^30 = 4 GB
  - Address space of the processor:
    - 0000_0000h – FFFF_FFFFh

# Solution

- Determine the number of memory circuits required by the design
  - No of circuits = size of the required memory / size of the available memory circuits
  - No of EEPROM circuits = 256MB / (64M x 16 bits)
    = 256MB / 128MB = 2
  - No of SRAM circuits = 512MB / 64MB = 8
  - No of DRAM circuits = 1GB / (128M x 4)
    = 1GB / (128M x 1/2B) = 1024MB / 64MB = 16

# Solution

- Determine the number of 32bits blocks
  - Circuits have to be grouped into blocks in order to match the data bus width of the processor
    - No of circuits per block = processor data bus width / memory data bus width
    - No of blocks = no of circuits / no of circuits per block
  - EEPROM
    - No of EEPROM circuits per block = 32 / 16 = 2
    - No of EEPROM blocks = 2 / 2 = 1
  - SRAM
    - No of SRAM circuits per block = 32 / 8 = 4
    - No of SRAM blocks = 8 / 4 = 2
  - DRAM
    - No of SRAM circuits per block = 32 / 4 = 8
    - No of DRAM blocks = 16 / 8 = 2

# Solution

- Determine the size of each block (in MB and hexa)
  - EEPROM
    - Block B1: 2 * 128 MB = 256 MB = 2^8*2^20 = 2^28 = 1000_0000h
  - SRAM
    - B2: 4 * 64 MB = 256 MB = 2^28 = 1000_0000h
    - B3: 4 * 64 MB = 256 MB = 2^28 = 1000_0000h
  - DRAM
    - B4: 8 * 128 M x 4bits = 512 MB = 2^29 = 2000_0000h
    - B5: 8 * 128 M x 4bits = 512 MB = 2^29 = 2000_0000h

# Solution

- Visualize the system (block diagram)

# Solution

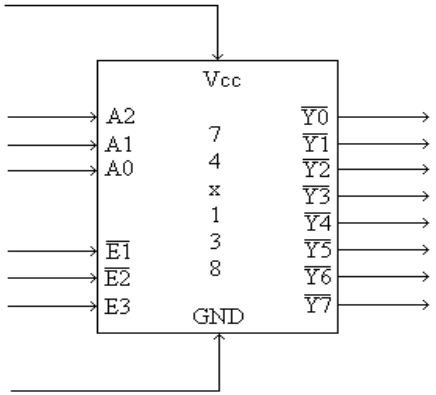
- Memory map
  - B1
  - B2
  - B3
  - B4
  - B5

# Solution

- Decoding
  - Decoding circuits
    - 74x138: decoder 3 → 8,
    - 74x139: decoder 2 x 2 → 4,
    - 74x42: decoder 4 → 10,
    - 74x154: decoder 4 → 16.

# Solution

- 74x138 decoder




| E3 | /E2 | /E1 | A2 | A1 | A0 | /Y7 | /Y6 | /Y5 | /Y4 | /Y3 | /Y2 | /Y1 | /Y0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | X | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| X | 1 | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| X | X | 1 | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

# Solution

- Memory decoder
  - Component of a digital system that generates selection signal for the slave module addressed by in the current bus transaction
  - Inputs: most significant bits of the address bus
  - Outputs: selection signals for each memory module
  - Design steps
    - Memory requirements and constraints
    - Memory setup
    - Memory map
    - Logic design
    - Optimization (speed, space, complexity)

# Solution

- Decoding table

| A 31 | A 30 | A 29 | A 28 | A 27 | A 26 | A 25 | A 24 | | | | | | | A4 | A3 | A2 | A1 | A0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | | | | B1 |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | B2 |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | B3 |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | B4 |
| | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | B5 |
| | | | | | | | | | | | | | | | | | | | |

# Solution

- Selection functions

# Solution

- Memory decoder