$X = -6 = 1110_{sn}$

$Y = +7 = 0111_{sn}$

$P = X * Y = -42.$

A	Q	M	COUNT
0000		0111	00
	1110		
0000	0111		01
+111			
0111			
0011	1011		10
+111			
1010			
0101	0101		11 *COUNT3==1
1010	1010		

012.

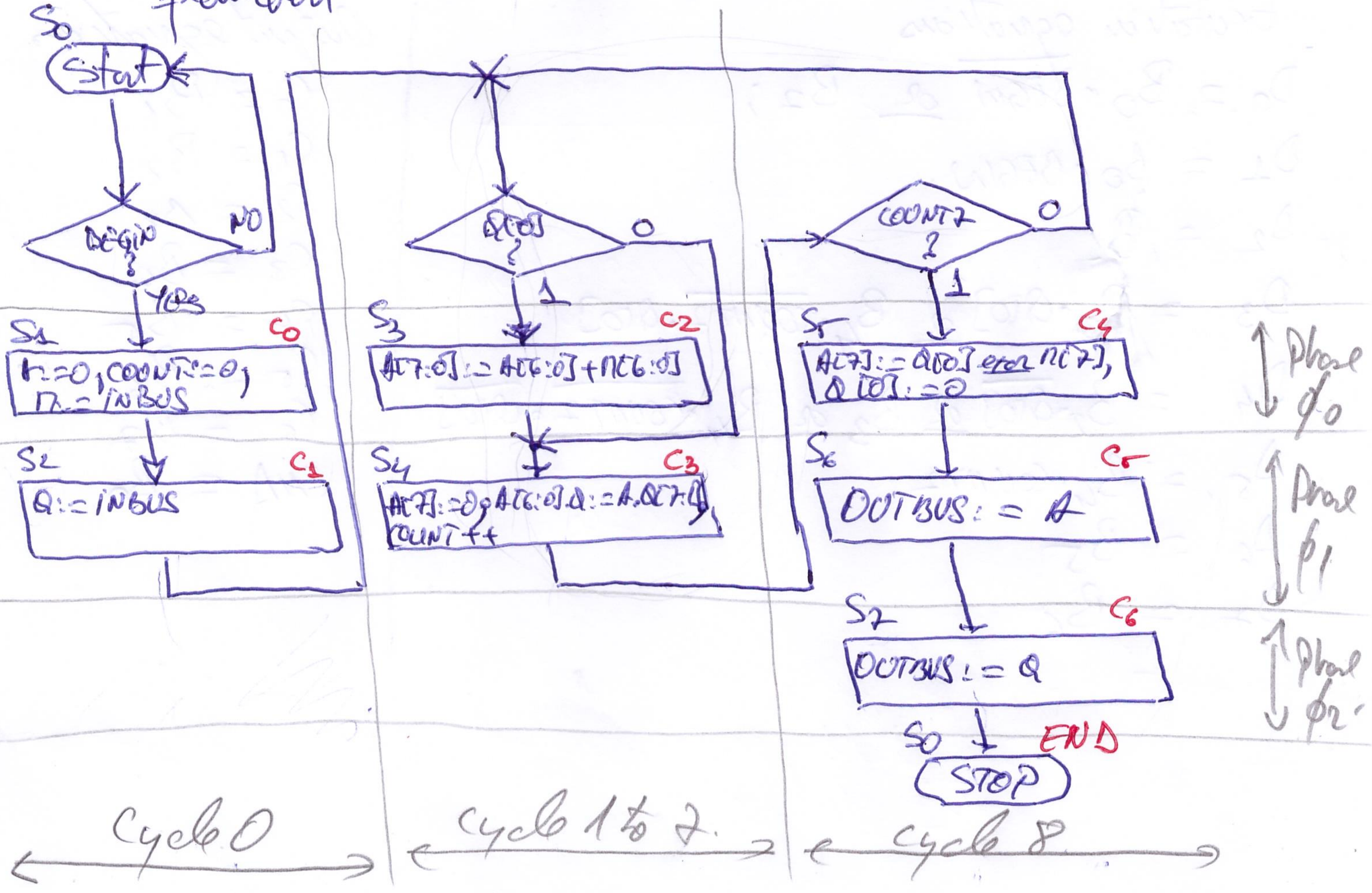
0012.

$P = 10101010 =$

$= -\underbrace{1}_{2^5}\,0\,\underbrace{1010}_{10} = -(32+10) = -42$

4.3. Elements of Control Unit synthesis.

- flowchart

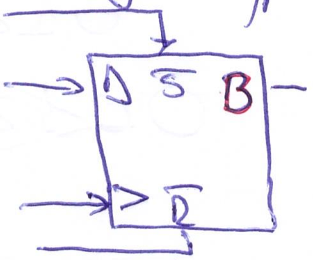


(A) State table method (serial adder)

(B) One Hot method.

- uses one storage element per state.
  - → at any given moment one and only one storage element is set (output is active) ⇒ the "hot" storage element.

Consider using D type flip-flop



$B(t+1) = D$

State variable: $B_0, B_1, \text{——}, B_7$

State encoding:-

State	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
S_0	0	0	0	0	0	0	0	1
S_1	0	0	0	0	0	0	1	0
S_2	0	0	0	0	0	1	0	0
S_3	0	0	0	0	1	0	0	0
S_4	0	0	0	1	0	0	0	0
S_5	0	0	1	0	0	0	0	0
S_6	0	1	0	0	0	0	0	0
S_7	1	0	0	0	0	0	0	0

Excitation equations

$D_0 = B_0 \cdot \overline{BEGIN}$ or B_7;

$D_1 = B_0 \cdot BEGIN$.

$D_2 = B_1$

$D_3 = B_2 \cdot Q[0]$ or $B_4 \cdot \overline{COUNT7} \cdot Q[0]$

$D_4 = B_2 \cdot \overline{Q[0]}$ or B_3 or $B_4 \cdot \overline{COUNT7} \cdot \overline{Q[0]}$

$D_5 = B_4 \cdot COUNT7$

$D_6 = B_5$

$D_7 = B_6$

Output equations

$C_0 = B_1$

$C_1 = B_2$

$C_2 = B_3$

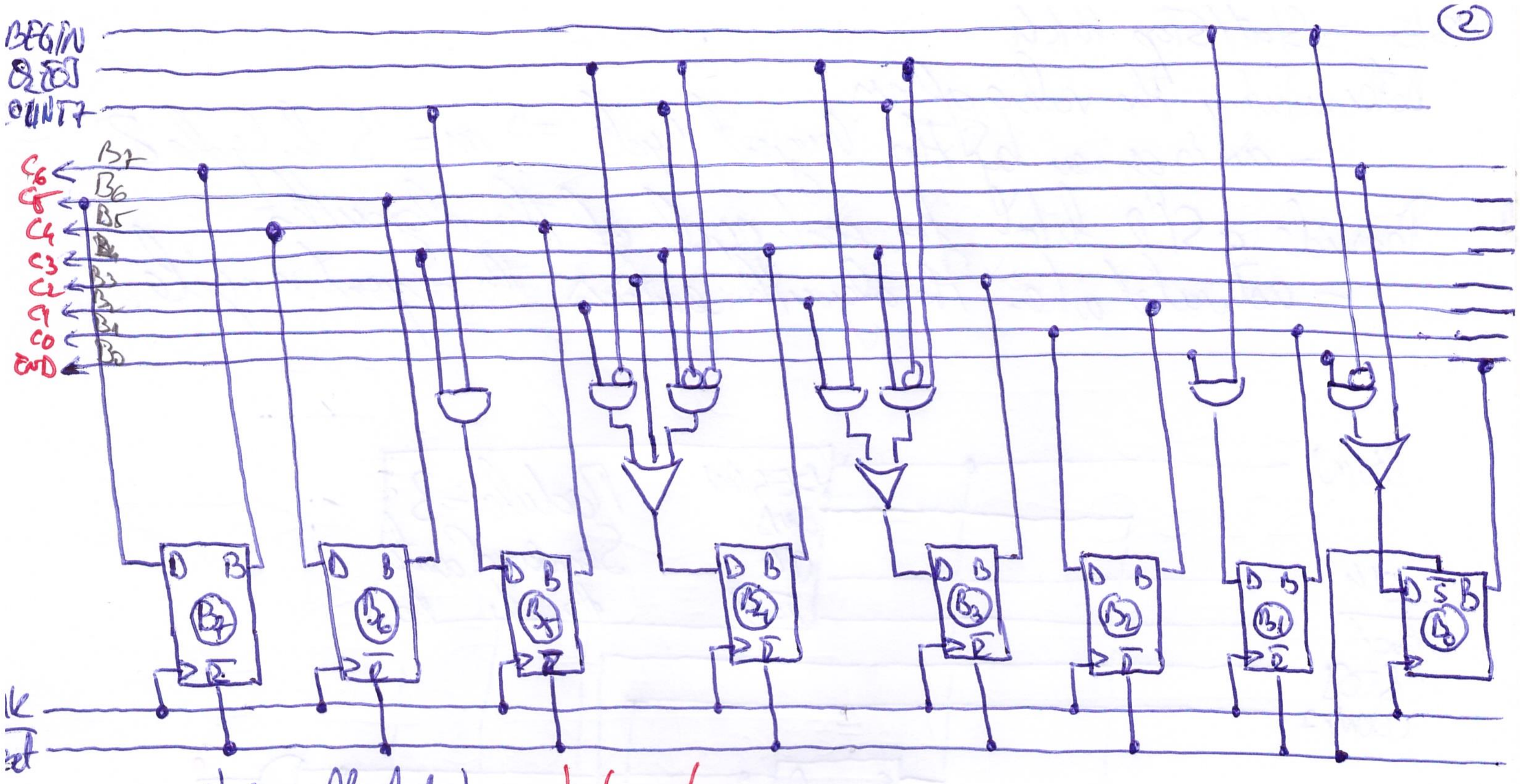
$C_3 = B_4$

$C_4 = B_5$

$C_5 = B_6$

$C_6 = B_7$

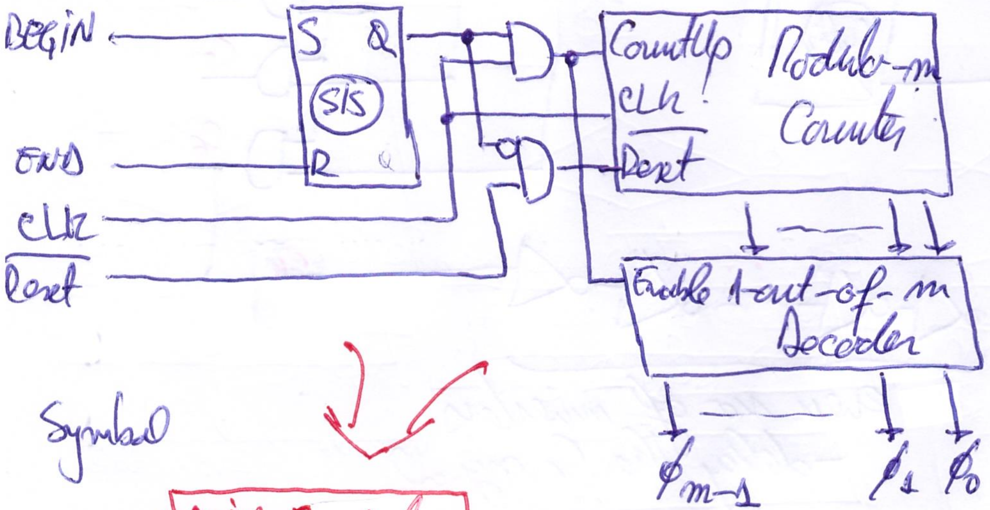
$END = B_0$

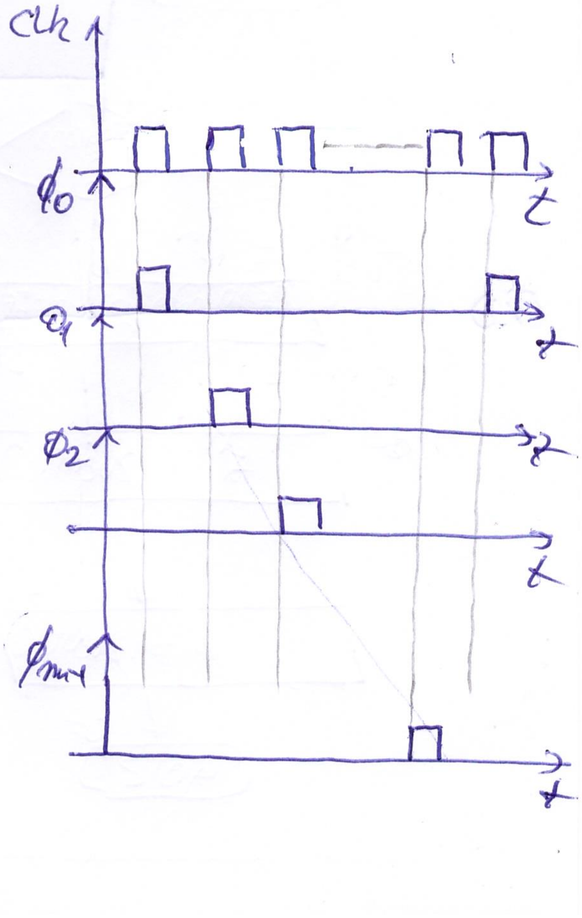


- it is affected by clock skew
  - the clock signal does not reach simultaneously all f.f.

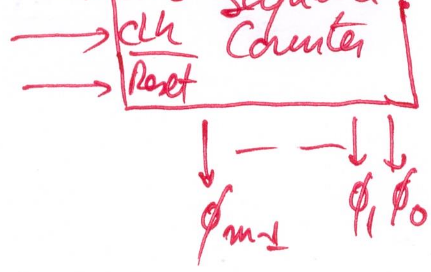
c) Sequence Counter

- constructed around a Sequence Counter device.
  Sequence Counter: generates non-overlapping, synchronous phase pulses





Symbol



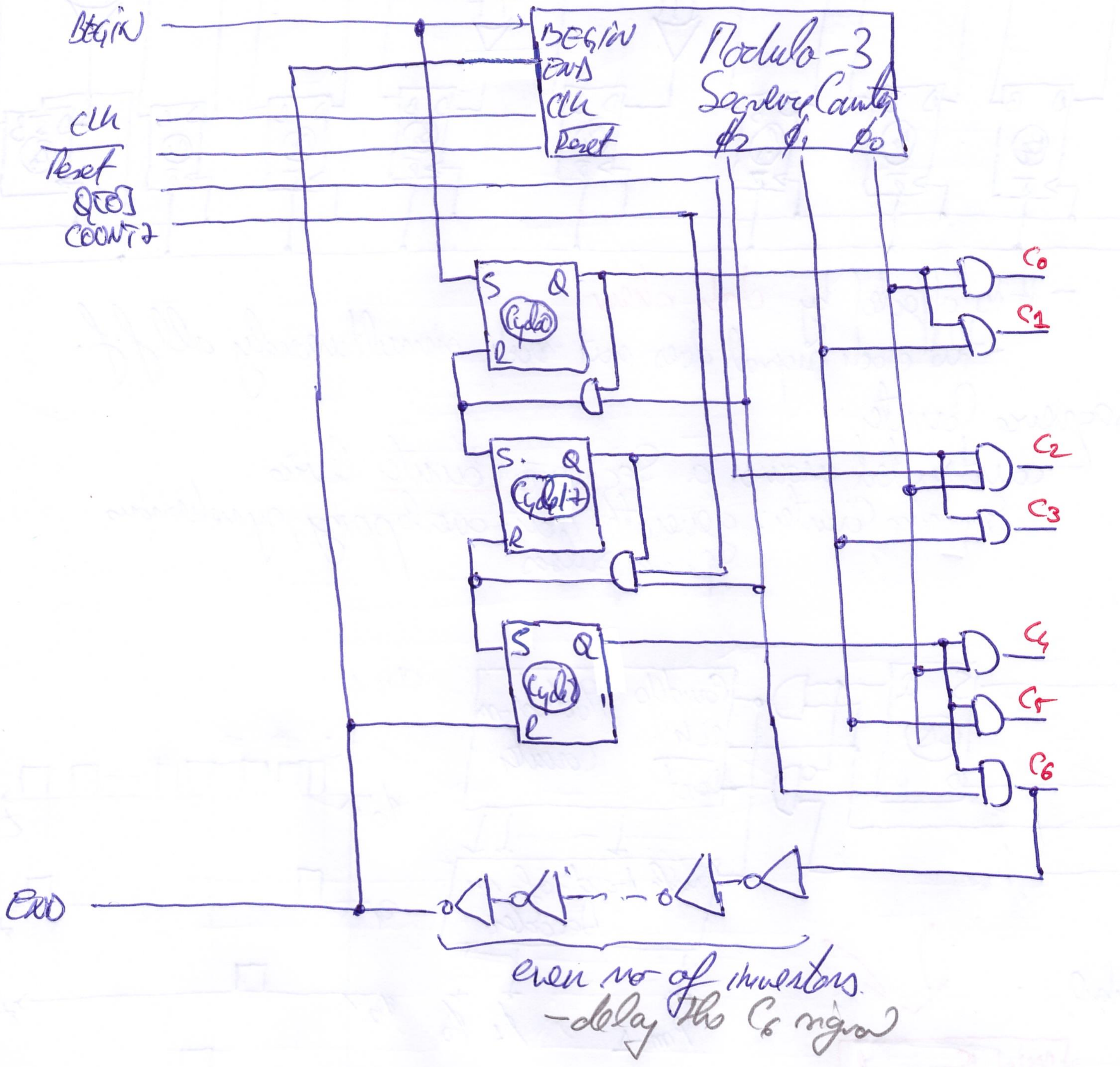
S/S – Start/Stop latch

Determining the value of m

– m is given by the largest cycle => m = 3 for cycle 8

Provide a S/R latch for each cycle of the algorithm

– activated when the algorithm enters the respective cycle.



4.4. Two's Complement Multiplication Based on Robertson's Procedure (3)

- multiply 2 no. in C2
  - use conversions
    - 1. convert X, Y C2 → SM *
    - 2. multiply in SM: X * Y = P
    - 3. convert P SM → C2 *

* delay

Robertson's interpretation:

Let $X_{C2} = \overset{\text{sign}}{x_{n-1}}\ \overbrace{x_{n-2} --- x_1 x_0}^{\text{magnitude}}$

value of X, as integer $X = -x_{n-1} \cdot 2^{n-1} + \overbrace{0x_{n-2}x_{n-3} -- x_1x_0}^{\text{positive in C2, SM}}.$

value of X, as fractional $X = -x_{n-1} \cdot 2^{0} + \underbrace{0.x_{n-2}x_{n-3} --- x_1x_0}_{\text{positive in C2, SM}}$

A positive in C2 ≡ the same positive in SM.

A negative in C2 = a positive in SM + correction.

Let X, Y - fractionals

$$P = X_{C2} * Y = (-x_{n-1} \cdot 2^0 + \underbrace{0x_{n-2}x_{n-3} — x_1x_0}_{X^*\text{, positive in SM.}}) * Y$$

$$= \overbrace{X^*_{SM} * Y}^{\text{bulk of } *\text{, SM-multiplication}} — \underbrace{x_{n-1} * Y * 2^0}_{\text{final correction}}$$

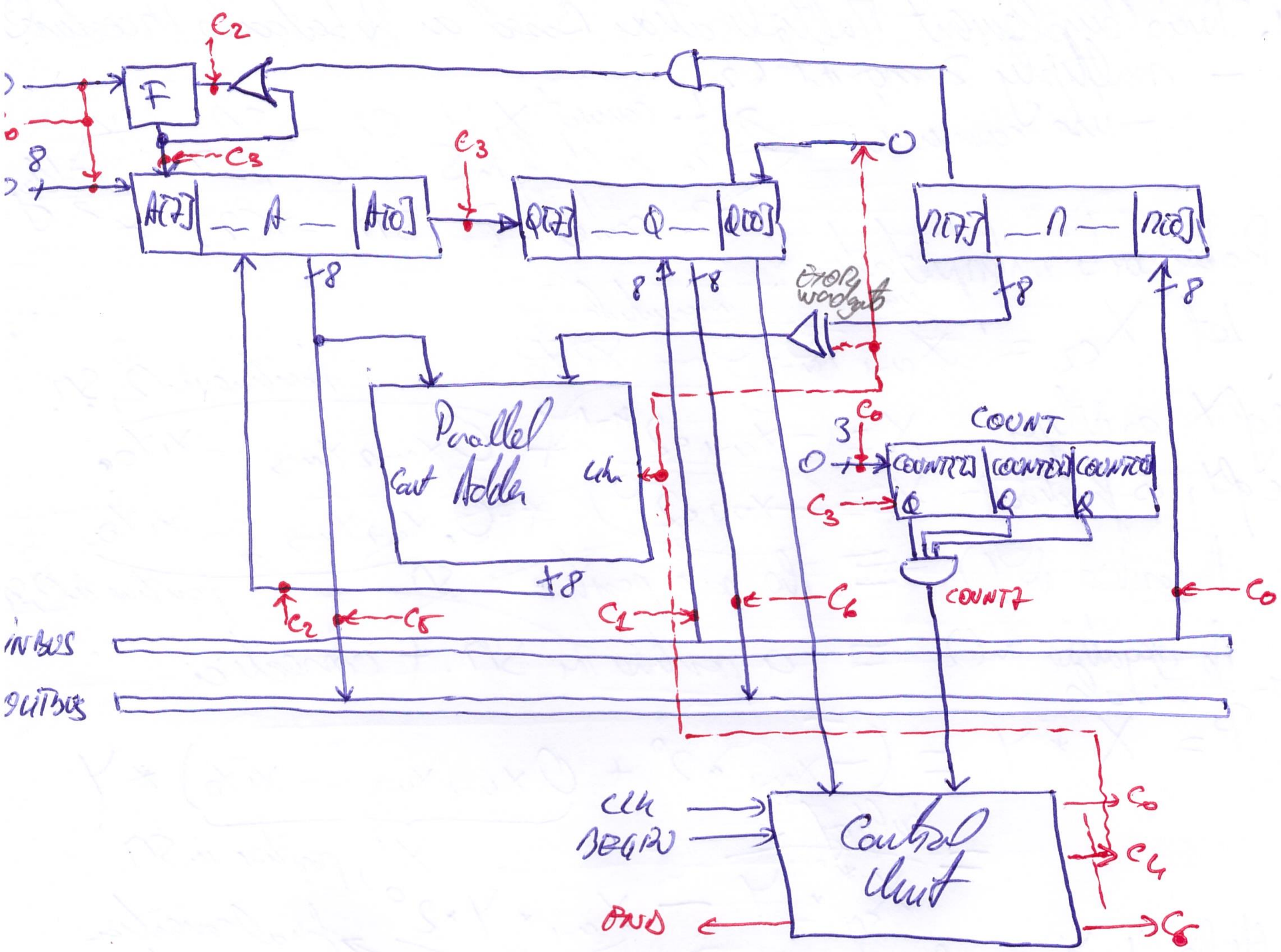
Multiplicand Y can also be negative ⇒ all the partial products are negative ⇒ the partial products need to have the sign of Y *

<u>multiplier 3</u>

<u>define registers</u> A[7:0], Q[7:0], M[7:0], COUNT[2:0], F;

<u>declare bus</u> INBUS[7:0], OUTBUS[7:0];

```
BEGIN:      A:=0, COUNT:=0, F:=0,                    {c0}
INPUT:      M:=INBUS;
            Q:=INBUS;                                {c1}
TEST1:      if Q[0]=0 then go to RShift,
ADD:        A:=A+M, F:=F or (Q[0] and M[7]);         {c2}
RShift:     A[7]:=F, A[6:0].Q:=A.Q[7:1],             {c3}
INCREMENT:  COUNT:=COUNT+1;
TEST2:      if COUNT7 ≠ 1 then go to TEST1,
TEST3:      if Q[0]=0 then go to OUTPUT,
CORRECTION: A:=A-M, Q[0]:=0;                         {c2, c4}
OUTPUT:     OUTBUS:=A;                               {c5}
            OUTBUS:=Q;                               {c6}
END:        ------------------------------------     {END}
```


F
C2
C3
8
A[7]
A
A[0]
Q[7]
Q
Q[0]
M[7]
M
M[0]
Parallel Adder
Cout
Cin
COUNT
COUNT[2]
COUNT[1]
COUNT[0]
COUNT7
C0
C1
C4
C5
C6
INBUS
OUTBUS
CLK
BEGIN
END
Control Unit