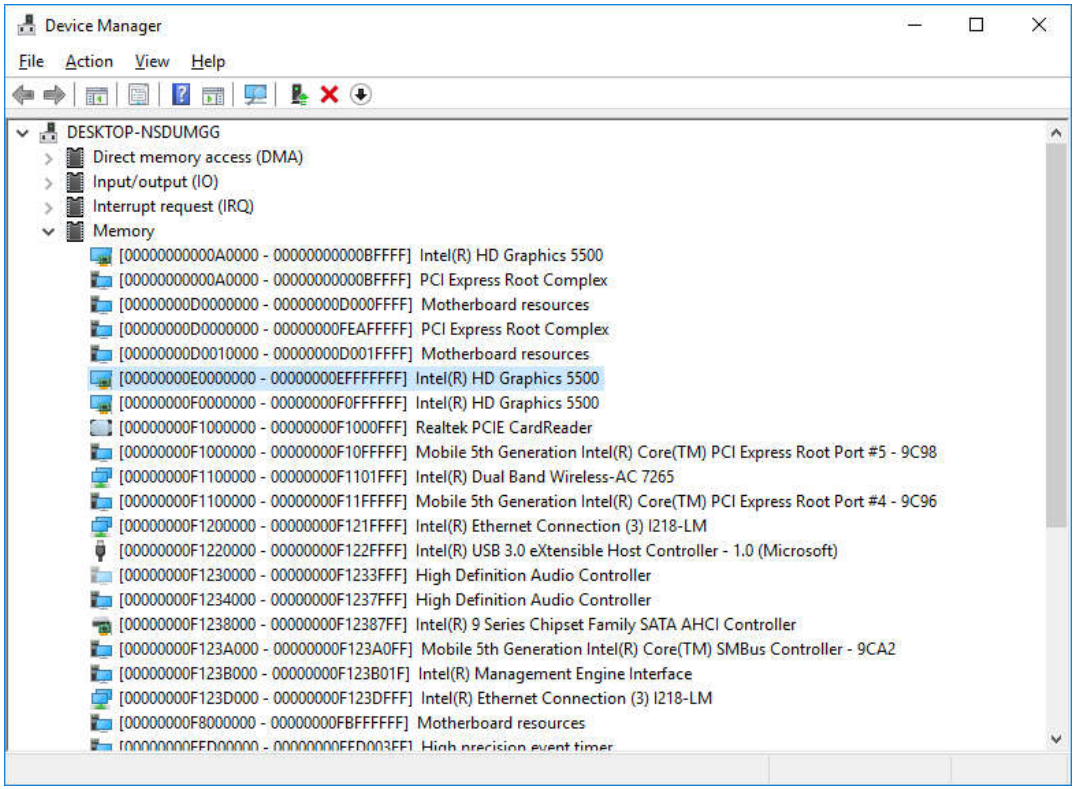
Digital microsystems design

Lab 3

Memory map

- x86/x64

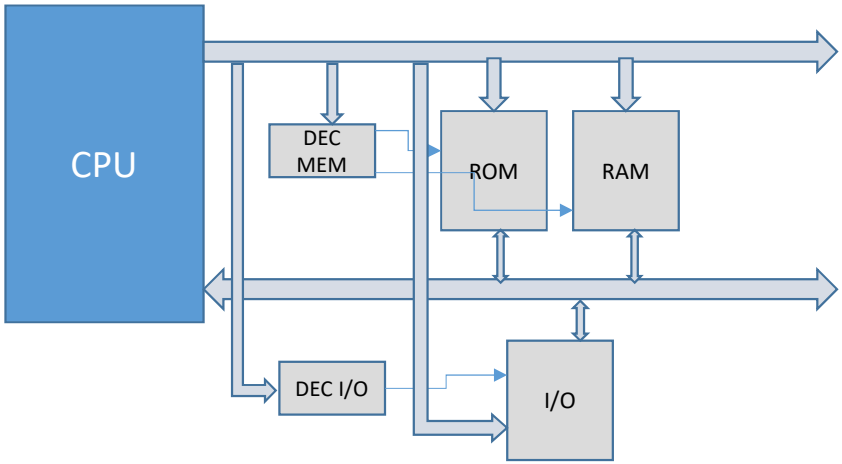


Exercise

- Design the memory map for a 32 bits microprocessor system with 32 address lines using the following memory requirements:
  - 512 MB EEPROM, using 128 M x 16 bits memories
  - 1 GB SRAM, using 64 M x 32 bits memories
  - 2 GB DRAM, using 256 M x 8 bits memories

Overview

- External connectivity of a microprocessor
  - Memory / I/O connectivity



Step 0

- How much memory the processor can access?
  - Max amount of memory = 2 ^ address bus width of the processor
  - 2^32 = 2^2 x 2^30 = 4 GB
  - Address space of the processor:
    - 0000_0000h – FFFF_FFFFh

Step 1

- How many circuits are needed?
  - No of circuits = size of the required memory / size of the available memory circuits
  - No of EEPROM circuits = 512 MB / (128 M x 16 bits) =
    = 512 MB / 256 MB = 2
  - No of SRAM circuits = …
  - No of DRAM circuits = …

Step 2

- How many memory blocks are required?
  - Circuits have to be grouped into blocks in order to match the data bus width of the processor

  - No of circuits per bloc = processor data bus width / memory data bus width
  - No of blocks = no of circuits / no of circuits per block

  - No of EEPROM circuits per block = 32 / 16 = 2
  - No of EEPROM blocks = 2 / 2 = 1

  - No of SRAM blocks …

  - No of DRAM blocks …

Step 3

- Visualize the systems (block diagram)

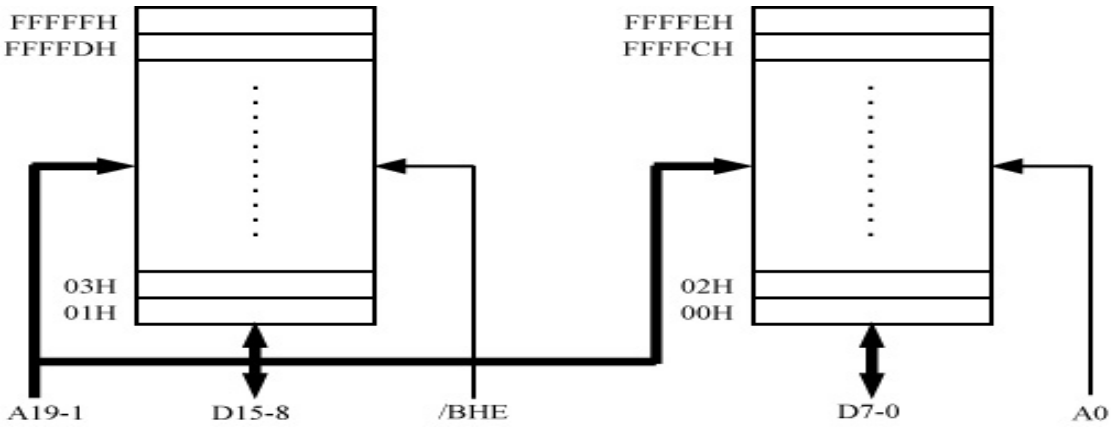
Data transfers

- 16 bits processors have to implement both:
  - 16 bits transfers
  - 8 bits transfers
- 8086: /BHE and A0

$\overline{BHE}$	A_0	Characteristics
0	0	Whole word
0	1	Upper byte from/to odd address
1	0	Lower byte from/to even address
1	1	None

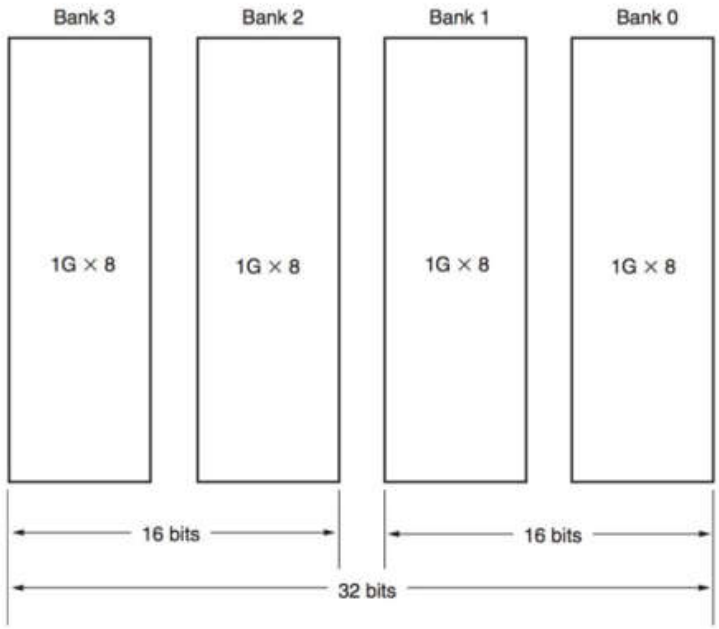
Data transfers

- 16 bits transfers – even address (A0 = 0 , /BHE = 0)
- 8 bits transfers
  - Odd address (A0 = 1, /BHE = 0)
  - Even address (A0 = 0, /BHE = 1)



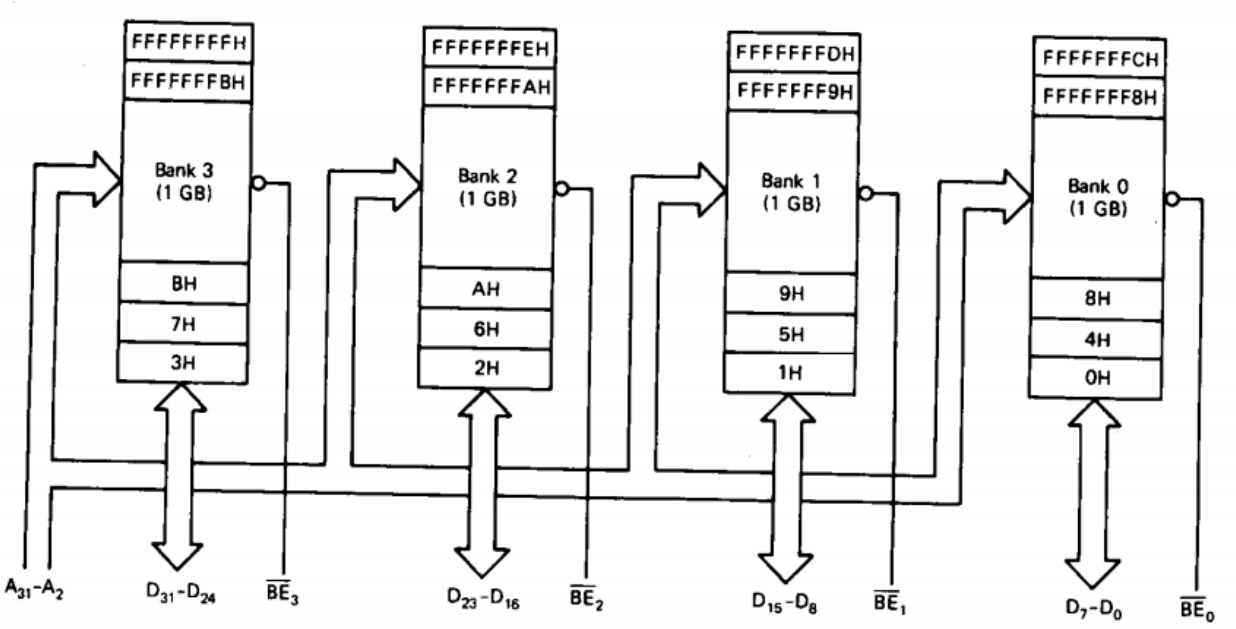
Data transfer

- 32 bits data bus
  - 32 bits transfers
  - 16 bits transfers
  - 8 bits transfers



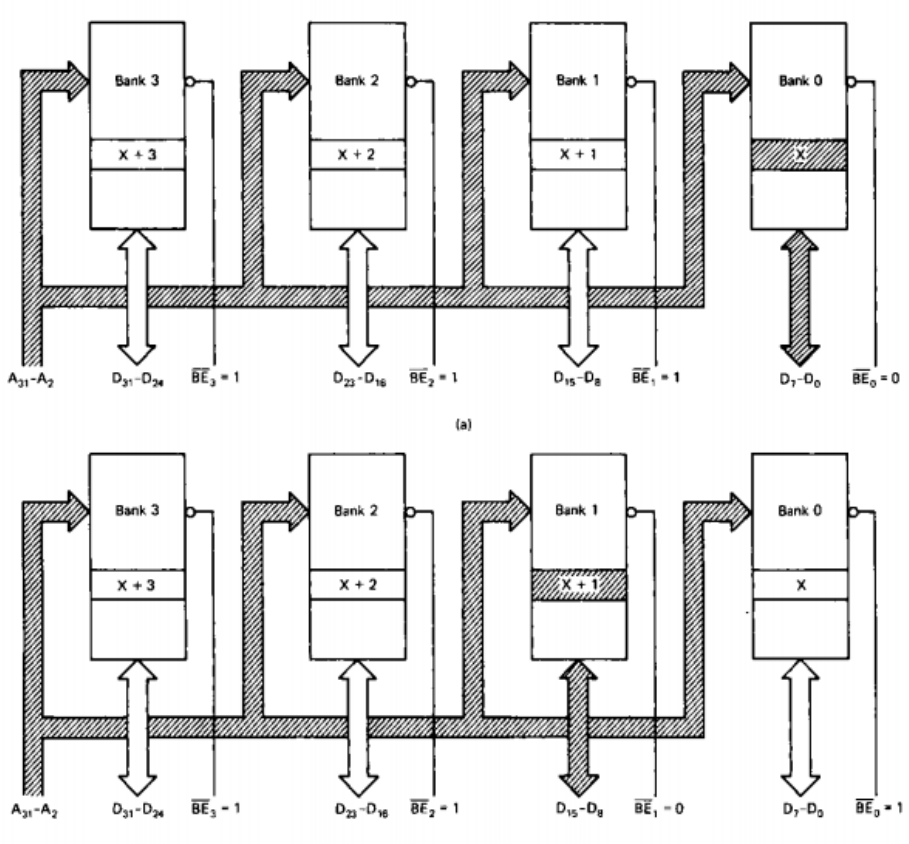
Data transfer

- Hardware organization of physical address space (32 bits)
  - 32 bits memory block



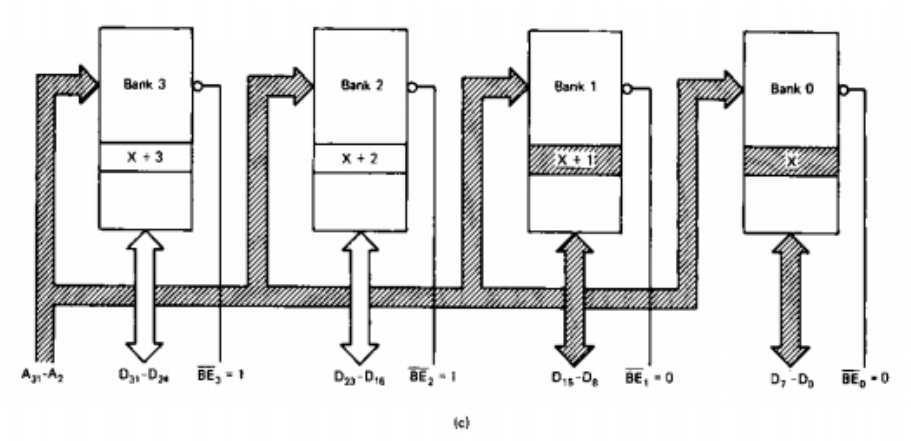
Data transfer

- 1 byte
  - Address 4xk
  - Address 4xk+1



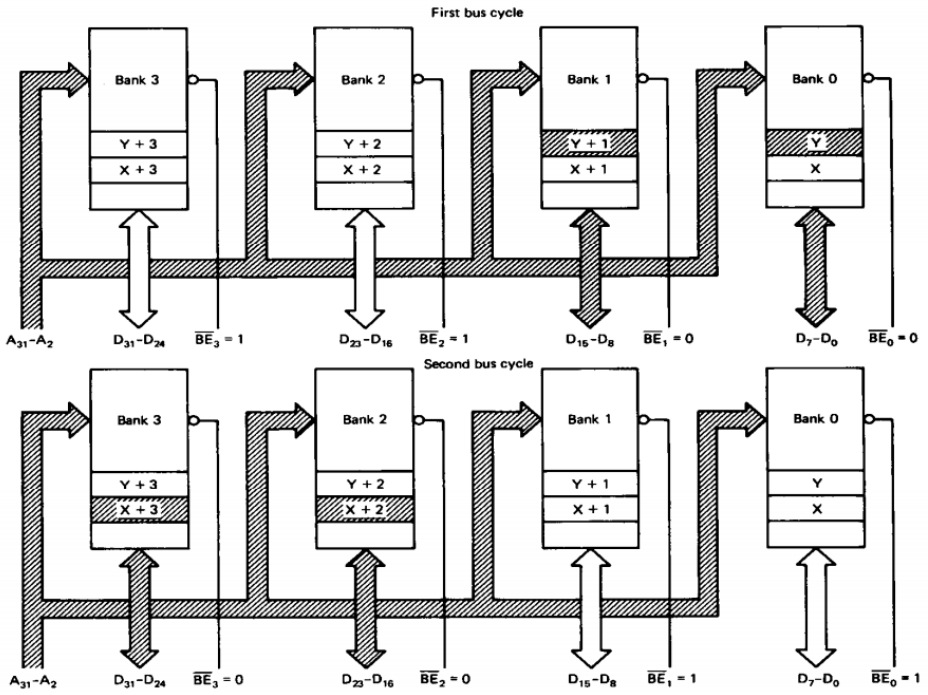
Data transfer

- 1 word
  - Address 4xk
- 1 double word
  - Address 4xk



Data transfer

- Misaligned double-word data transfer
  - Address 4xk+2 – the processor will perform 2 bus cycles



Step 4

- Characterize each block
  - Selection is made at block level, not at the circuit level
  - Size, number of address lines, range of addresses

  - EEPROM block: 512 MB = 2^9 x 2^20 = 2^29
    - 29 address lines
    - Size of the block: 2^29 = 1 000…00 = 20000000 H

      29 of 0

    - Address range: 0000_0000H – 1FFF_FFFFH

Step 4

- Characterize each block
  - SRAM

Step 4

- Characterize each block
  - DRAM

Step 5

- Memory map

Solution

```
EPROM
no of blocks = 1
B1

512 MB = 2000_0000h

SRAM = 4 circuits
no of circuit per block = 32 /32 = 1
no of SRAM blocks = 4 / 1 = 4
B2, B3, B4, B5

256 MB = 2^8 * 2^20 = 2^28 = 1000_0000h



DRAM = 8 circuits
no of circuits per block = 32 / 8 = 4
no of DRAM blocks = 8 / 4 = 2
B6, B7

4 * 256 MB = 1 GB = 2^30 = 4000_0000h


Memory map
    Start address - Ending address
B1  0000_0000h    - 1FFF_FFFFh
B2  2000_0000h    - 2FFF_FFFFh
B3  3000_0000h    - 3FFF_FFFFh
B4  4000_0000h    - 4FFF_FFFFh
B5  5000_0000h    - 5FFF_FFFFh
B6  8000_0000h    - BFFF_FFFFh
B7  C000_0000h    - FFFF_FFFFh
```

Next

- Decoding table
- Memory decoder