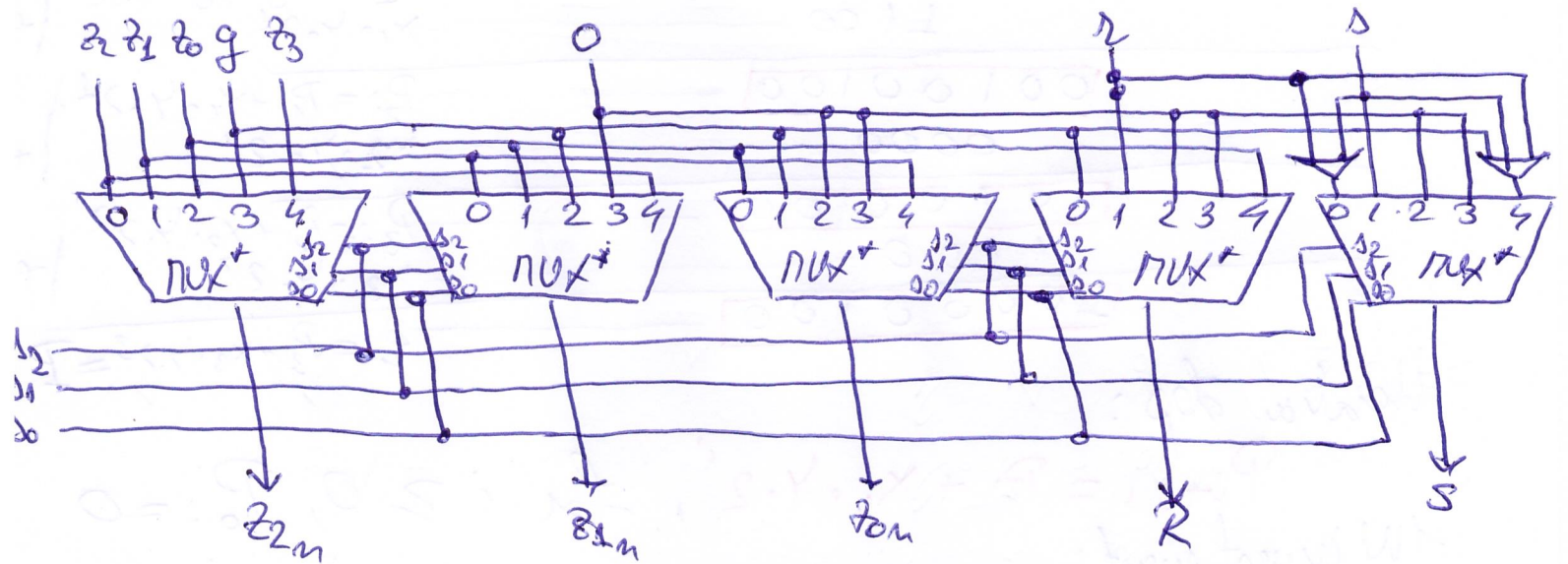


#C12 3.5.

(4)

Only 4 of the 5 binary variables can be active for a given f.p. operand pair X and Y
 \Rightarrow encode the 5 variables using only 3 signals: s_2, s_1, s_0

Inputs					Outputs		
z_1	z_3	z_0	z_1	z_{10}	s_2	s_1	s_0
0	0	0	0	1	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	1	0	0	0	0	1	1
1	0	0	0	0	1	0	0



$MUX^+ \equiv$ degenerate MUX.

Chapter V Functional analysis & synthesis of Binary Multiplier Devices.

4.1. Multiplication methods.

a) paper and pencil.

$X = \text{multiplier}$ $Y = \text{multiplicand}$

consider $X = 11$ $Y = 12$, unsigned.

$$\begin{array}{r} 1100 \\ 1011 = x_3x_2x_1x_0 \end{array}$$

$$\begin{array}{l} 1100 \sim x_0 \cdot 4 \cdot 2^0 \\ 1100 \sim x_1 \cdot 4 \cdot 2^1 \\ 0000 \sim x_2 \cdot 4 \cdot 2^2 \\ 1100 \sim x_3 \cdot 4 \cdot 2^3 \end{array}$$

$$10000100 - P = \sum_{i=0}^3 x_i \cdot 4 \cdot 2^i = 4 + 128 = 132$$

$$\begin{array}{r} 12 \\ 11 \\ \hline 12 \\ 12 \\ \hline 132 \end{array}$$

HW investment

- 2 4-bit registers for X, Y
- multi-operand adder (CSA)
- multiplexed gating

b) keep the partial products fixed.

1100	Y
1011 = $x_3x_2x_1x_0$	X
00000000	$P_0 := 0$
1100	$x_0 \cdot 4 \cdot 2^0$ +
00001100	$P_1 := P_0 + x_0 \cdot 4 \cdot 2^0$ +
1100	$x_1 \cdot 4 \cdot 2^1$
00100100	$P_2 := P_1 + x_1 \cdot 4 \cdot 2^1$ +
0000	$x_2 \cdot 4 \cdot 2^2$
00100100	$P_3 := P_2 + x_2 \cdot 4 \cdot 2^2$ +
1100	$x_3 \cdot 4 \cdot 2^3$
10000100	$P_4 := P_3 + x_3 \cdot 4 \cdot 2^3 = P$

Iteration stop:

$$P_{i+1} := P_i + X_i \cdot 4 \cdot 2^i, \text{ for } i \geq 0, P_0 := 0$$

HW investment:

- 2 4-bit registers for X, Y
- 8-bit register for partial products
- 8-bit adder
- 4 Shifters for the 4-bit products.

c) keep the 1-bit products fixed.

1100	Y
1011 = $x_3x_2x_1x_0$	X
00000000	$P_0 := 0$
1100	$x_0 \cdot Y$ +
00001100	$P_1 := P_0 + x_0 \cdot Y$
000001100	$P_1 := P_0 \cdot 2^{-1}$ +
1100	$x_1 \cdot Y$
00100100	$P_2 := P_1 + x_1 \cdot Y$
00100100	$P_2 := P_1 \cdot 2^{-1}$ +
0000	$x_2 \cdot Y$
00100100	$P_3 := P_2 + x_2 \cdot Y$
00100100	$P_3 := P_2 \cdot 2^{-1}$

$$\begin{array}{r}
 00100100 \text{ --- } P_3 = P_2 \times 2^{-1} \quad (2) \\
 \boxed{1100} \text{ --- } \times 0.4 \quad] + \\
 \hline
 10000100 \text{ --- } P_3 = P_3 + X_3 \cdot Y \\
 10000100 \text{ --- } P_4 = P_3 \times 2^{-1} = P
 \end{array}$$

Iteration step: $\begin{cases} P_i = P_i + X_i \cdot Y \\ P_{i+1} = P_i \times 2^{-1} \end{cases}$ for $i \geq 0, P_0 = 0.$

Hardware Investment

- 2 4-bit registers for $X, Y.$
- 8-bit register for the p-product; RShift register 4-bit
- 4-bit adder.

4.2 Sequential Binary Multiplication for Sign-Magnitude numbers

Let $X = X_7 \cdot X_6 \cdot X_5 \cdot X_4 \cdot X_3 \cdot X_2 \cdot X_1 \cdot X_0$

$Y = Y_7 \cdot Y_6 \cdot Y_5 \cdot Y_4 \cdot Y_3 \cdot Y_2 \cdot Y_1 \cdot Y_0$

$\underbrace{\quad \quad \quad \quad \quad \quad \quad \quad}_{\text{sign}} \quad \underbrace{2^{-1} \quad 2^{-2} \quad 2^{-3} \quad 2^{-4} \quad 2^{-5} \quad 2^{-6} \quad 2^{-7}}_{\text{weight}}$

X, Y - SN, 8 bit.
- fractional
fractional < 1

$P = X \cdot Y = P_{15} \cdot P_{14} \cdot P_{13} \text{ --- } P_2 \cdot P_1 \cdot P_0$

multiply 2 unsigned on 7 bits, for the magnitude part

\Rightarrow result on 14 bits (unsigned)

\Rightarrow add the sign. $P_{15} = X_7 \oplus Y_7$

- in computers we work with values on 16 bits

\Rightarrow add. $P_0 = 0$ fractional extension

multiplication of 2 unsigned nos on 8 bits.
 \Rightarrow 2p bit result
e.g. $\begin{array}{r} 15 \\ + 15 \\ \hline 25 \end{array}$
4-bit 4-bit 8-bit
unsigned, unsigned

multiplier 2

$0.12 \rightarrow 0.120$

declare registers

$A[7:0], Q[7:0], N[7:0], \text{COUNT}[2:0];$

declare bus

$\text{INBUS}[7:0], \text{OUTBUS}[7:0];$

BEGIN:

INPUT:

$A := 0, \text{COUNT} := 0, \}$

$N := \text{INBUS};$

$Q := \text{INBUS};$

TEST1:

if $Q[0] = 0$ then go to RShift

ADD:

$A[7:0] := A[6:0] + N[6:0];$

RShift:

$A[7] := 0, A[6:0], Q := A, Q[7:1];$

INCREMENT:

$\text{COUNT} := \text{COUNT} + 1;$

TEST2:

if $\text{COUNT} \neq 1$ then go to TEST1

SIGN:

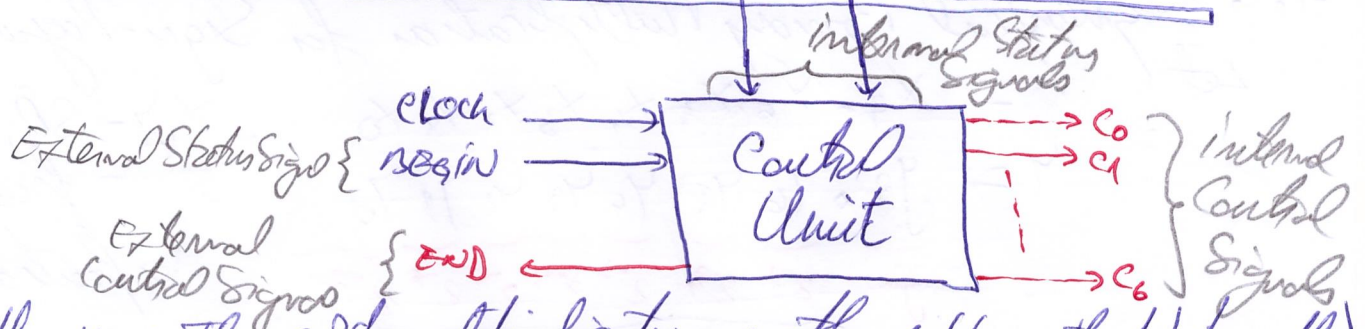
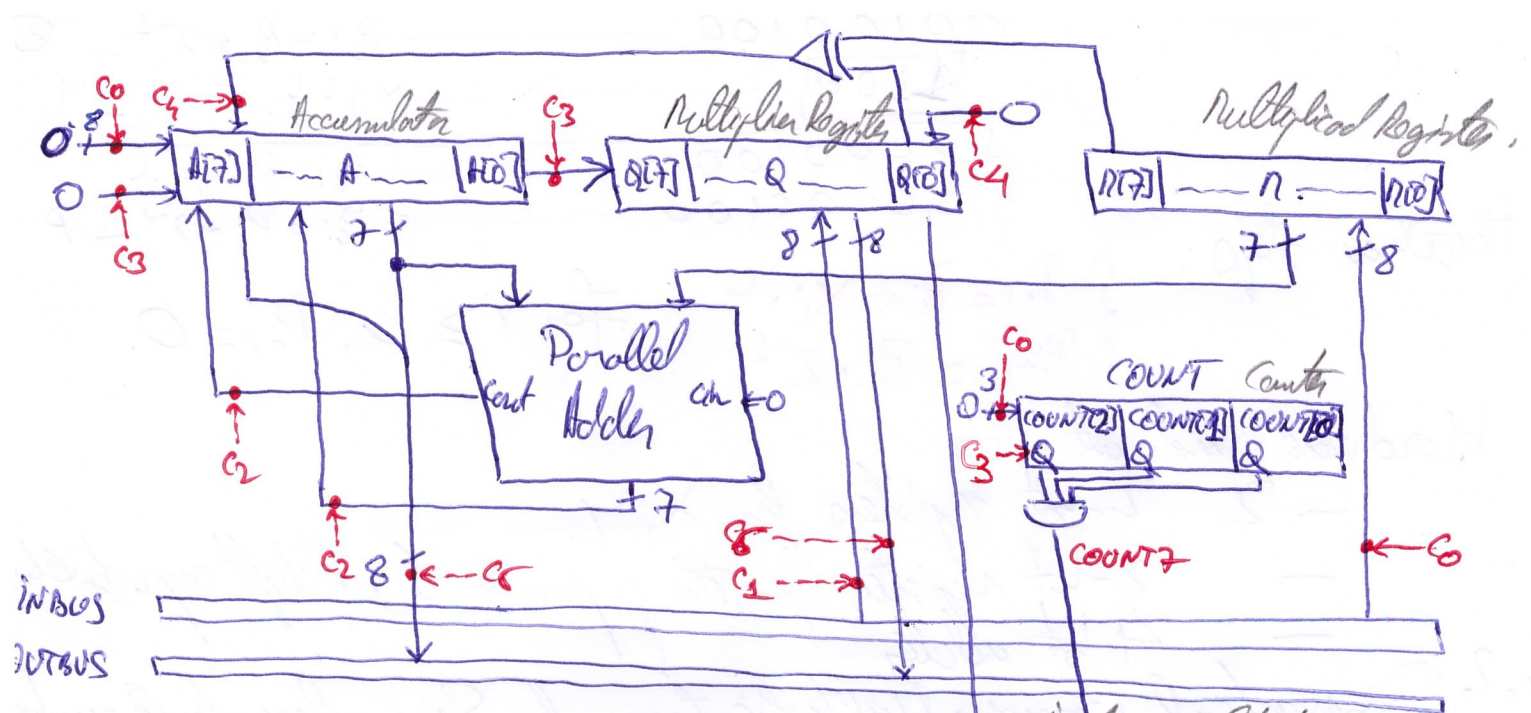
$A[7] := Q[0] \text{ xor } N[7], Q[0] := 0;$

OUTPUT:

$\text{OUTBUS} := A;$

END.

END.



Algorithm uses the 3rd multiplication method (keep the 1-bit product)
 iteration stop $\left\{ \begin{array}{l} P_i := P_i + X_i \cdot Y \rightarrow \text{label TEST \& add} \\ P_{i+1} := P_i \times 2^{-1} \rightarrow \text{label RShift} \end{array} \right.$

TEST: if X_i is 0: avoid adding 0 to P_i and jump to $P_{i+1} := P_i \times 2^{-1}$

! - at any given time X_i is the current bit of X is stored in Q[10]

Partial products:

- at the beginning of the algorithm is in A. ($P_0 := 0$)
- with each iteration, P_{i+1} advances into register Q one bit at a time, during RShift
- $\Rightarrow X$ is right shifted by losing the least significant bits, one at a time, at RShift.

Parallel Adder:

- updates the partial product
- on 7 bits: because P_i and Y are in 5-17, at addition of 5-17 nos just ignore the signs.
- addition's carry out is stored into A[7].
- \Rightarrow avoid overflow

COUNTER: - counts the 7 iterations (7 magnitude bits in Y) (3)
 - incremented at each RShift

COUNT 7 - activated when COUNT's state becomes 111 (value of 7)

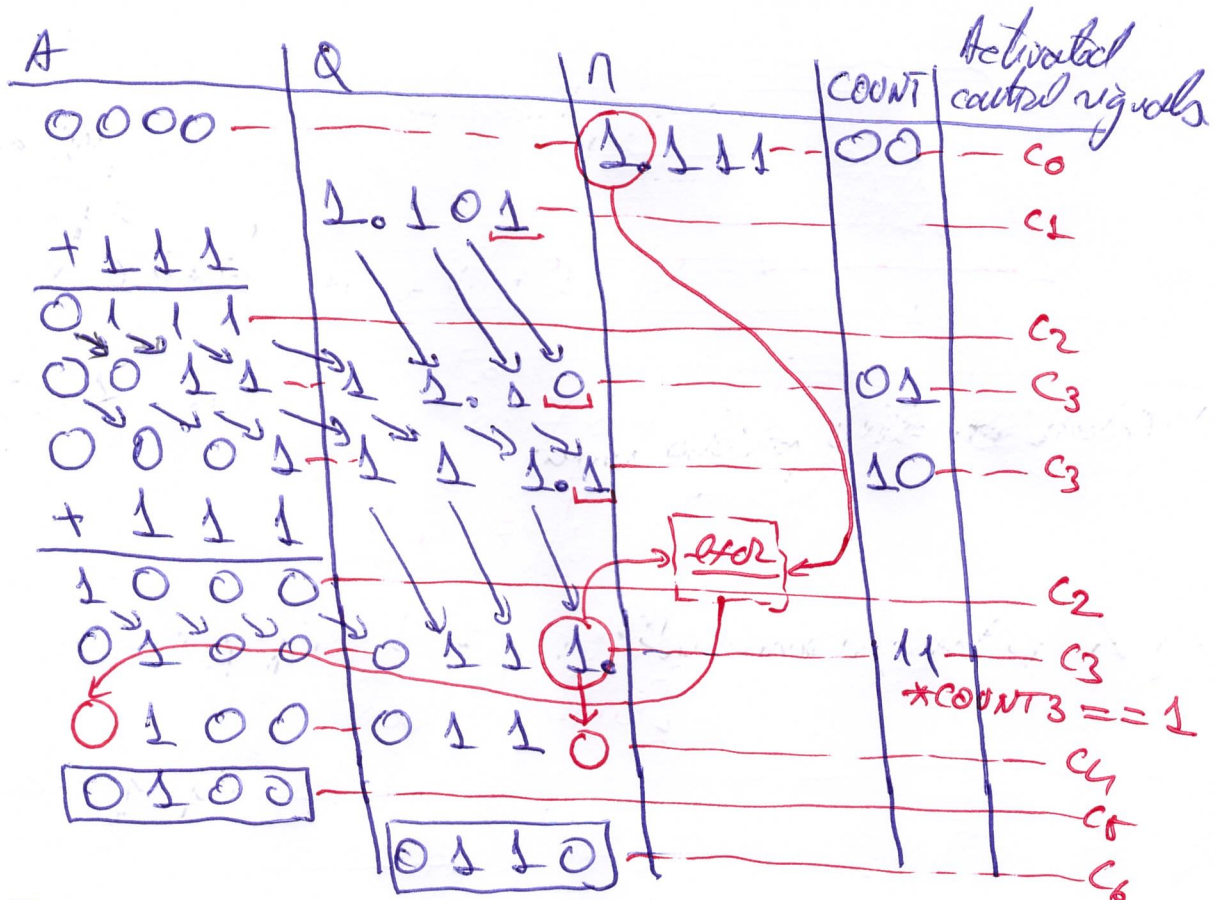
CONTROL UNIT: sequences the operations by activating the control signals

- each clock cycle one control signal is active.
- control signals are represented with $\text{---}\rightarrow\bullet$
- data lines are solid.
- control signals affect \rightarrow data lines, or storage elements.

Example:

$$X = -0.625 = -5 \times 2^{-3} = \underset{\text{sign}}{1} \cdot \underset{5}{101} \text{sn}$$

$$Y = -0.875 = -7 \times 2^{-3} = \underset{\text{sign}}{1} \cdot 111 \text{sn}$$



$$P = 0.1000110 = 100011 \times 2^{-6} = 35 \times 2^{-6}$$

$$X = -5 \times 2^{-3} \quad Y = -7 \times 2^{-3} \quad P = X \times Y = 35 \times 2^{-6}$$