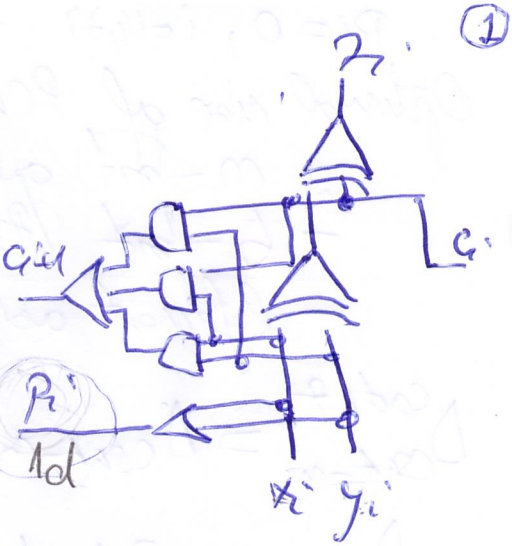
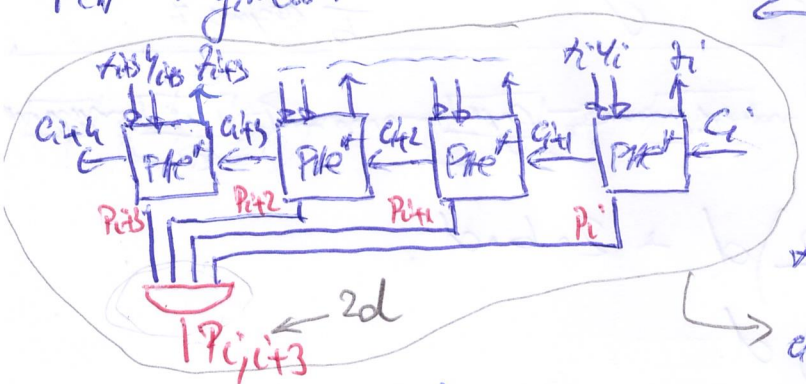
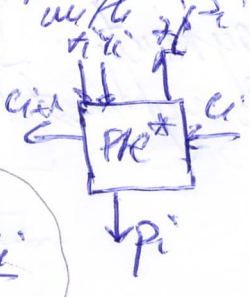
2.3.2 Carry Skip Adder (CSkA)

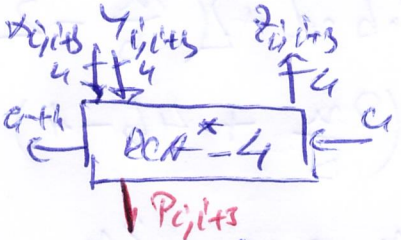
$G_{i,j}$; $P_{i,j}$ $P_{8,11}$ – simpler to obtain.
→ extend the PAE with P_i'



RCA segments.

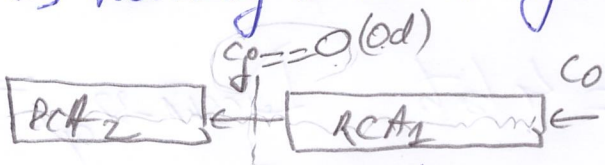




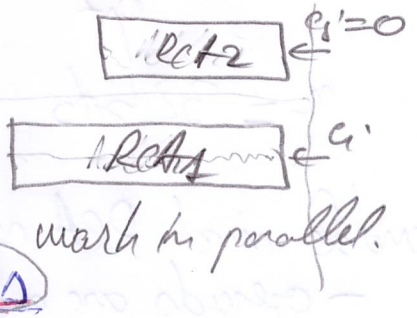


CMOS pre-discharge
- design technique: nodes cleared to 0 before operation

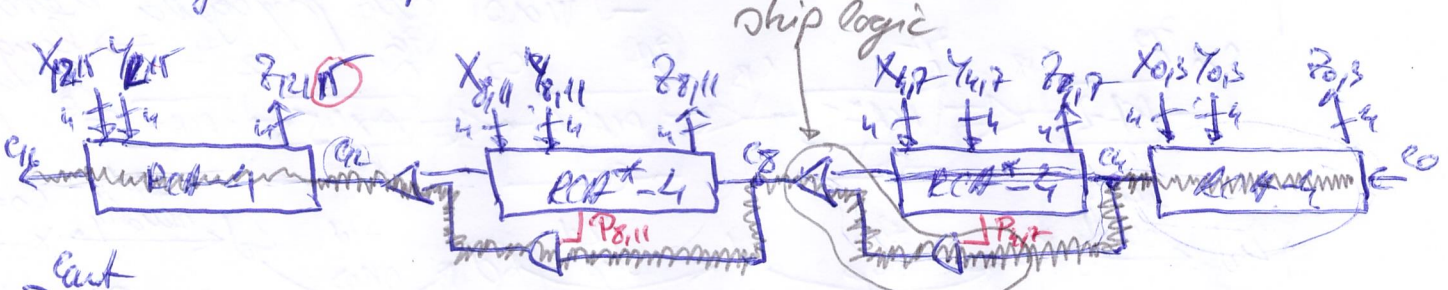
! - all carries are pre-discharged.
→ if the final value of a carry is 0
⇒ flat carry is correct from 0d.



⇒



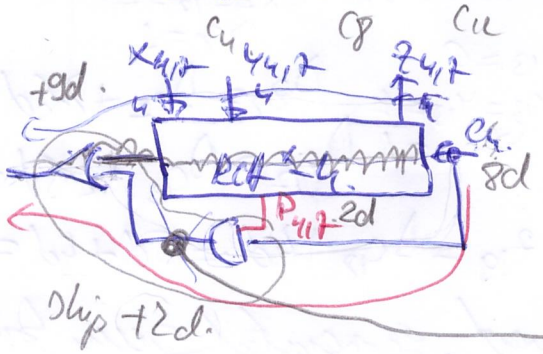
! a carry of 0 reduces the critical path
→ largest critical path (all carries need to be 1)

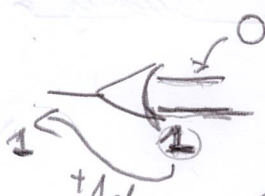


Last

$D_{CSkA-16} = \underbrace{2 \cdot 4d}_{c_4} + \underbrace{2d}_{c_8} + \underbrace{2d}_{c_{12}} + \underbrace{2 \cdot 4d}_{c_{16}} = 20d$

$D_{CSkA-16} = \underbrace{2 \cdot 4d}_{c_4} + \underbrace{2d}_{c_8} + \underbrace{2d}_{c_{12}} + \underbrace{2 \cdot 3d}_{c_{15}} + \underbrace{2d}_{s_{15}=XOR} = 20d$





$P_{4,7} \cdot c_4 = 0$ → $P_{4,7} = 0$

$P_4 \cdot P_5 \cdot P_6 \cdot P_7 = ?$

⇒ [?] $P_i = 0$, $i \in [4,7]$

$p_i = 0,\ i \in [4,7] \rightarrow x_i + y_i = 0 \Rightarrow x_i = y_i = 0 \Rightarrow c_{i+1} = 0$

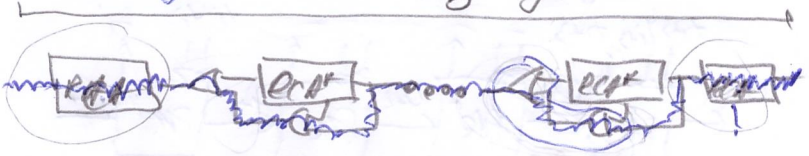
Optimal use of RCA segment.

- n-bit operands x, y.
- b-bit RCA segments.

$n = b * k,\ k \in \mathbb{N}$

- leftmost and the rightmost RCA segments have no chip logic

$\frac{n}{b}$ segments.



$D_{CSkA-n}^{cout} = D_{CSkA-n}$

$D_{CSkA-n} = 2b \cdot d + 2\left(\frac{n}{b} - 2\right)d + 2 \cdot b \cdot d.$

$= \left(\frac{2n}{b} + 4b - 4\right) d.$

$\frac{d\, D_{CSkA-n}}{d\, b} = 0 \Rightarrow -\frac{2n}{b^2} + 4 = 0 \quad b_{opt} = \frac{\sqrt{2n}}{2}$

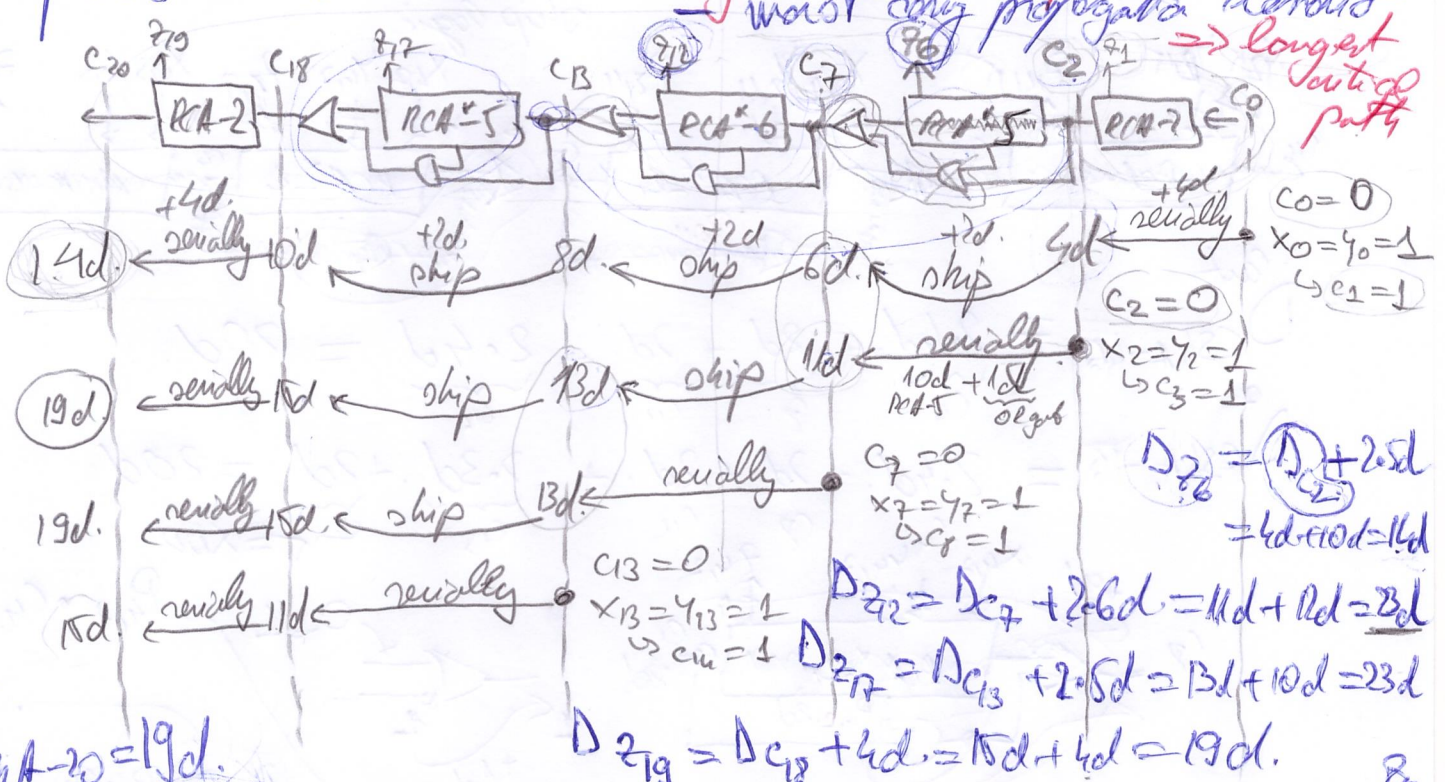
$D_{CSkA-n} = 4(\sqrt{2n} - 1)d.$

$n = 32$ bits $\quad b_{opt} = 4$ bits $\quad D_{CSkA-32_{opt}} = 28d$

$D_{RCA-32} = 2 \cdot 32d = 64d$

Variable-sized RCA segments.

- operands are on 20 bits
- analyse the critical path - worst carry propagation scenario => longest critical path



$D_{z_6} = D_{c_2} + 2 \cdot 5d = 4d + 10d = 14d$

$D_{z_{12}} = D_{c_7} + 2 \cdot 6d = 11d + 8d = 19d$

$D_{z_{17}} = D_{c_{13}} + 2 \cdot 5d = 13d + 10d = 23d$

$D_{z_{19}} = D_{c_{18}} + 4d = 15d + 4d = 19d.$

$D_{CSkA-20}^{cout} = 19d.$

$D_{CSkA-20}^{z} = 23d$ what do the slowest generated sum bits? $z_6, z_{12}, z_{17}, z_{19}$

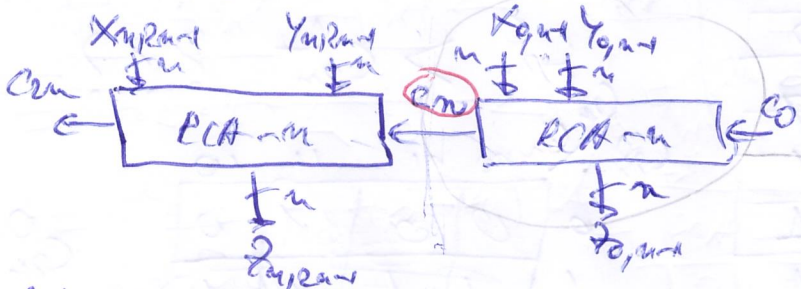
Multilevel CSkA architecture

2.3.3 Carry Select Adder (CSeA)

principle of sum conditioned by carry

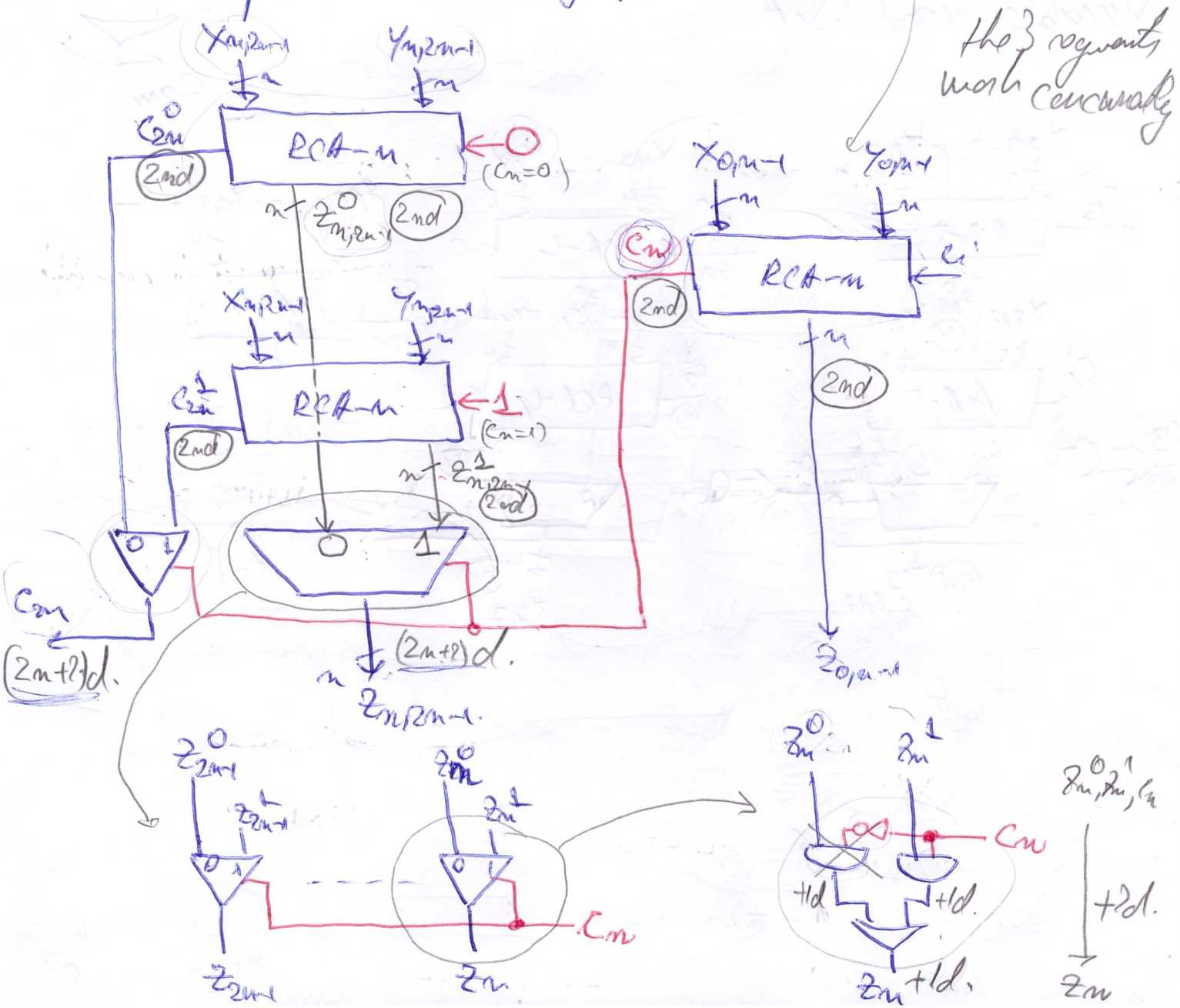
- as long as c_i is not yet calculated. → $c_i=0$: $(z_i^0; c_{i+1}^0)$ a
  → $c_i=1$: $(z_i^1; c_{i+1}^1)$
- select the exact pair (z_i^0, c_{i+1}^0) / (z_i^1, c_{i+1}^1) after c_i is known.

Consider a 2n bit RCA



$\Delta_{RCA-2n} = 4n\,d$

- split the adder in half
- duplicate the most significant half.



$D^{Carry}_{CSeA-2n} = (2n+2)d$

if n is long enough

$D_{CSeA-2n} \simeq \frac{1}{2} \cdot D_{RCA-2n}$

Generation of C_{2n}:

Inputs			Output
C^0_{2n}	C^1_{2n}	C_n	C_{2n}
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	d
1	0	1	d
1	1	0	1
1	1	1	1

can never occur.

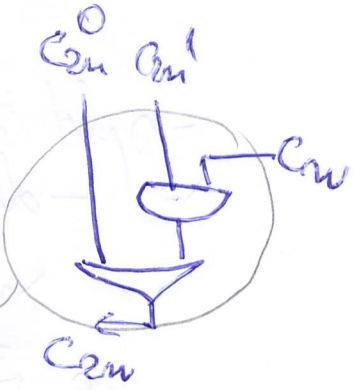
$\{C^0_{2n}, z^0_{n,2n-1}\} = X_{n,2n-1} + Y_{n,2n-1} + 0$

$\{C^1_{2n}, z^1_{n,2n-1}\} = X_{n,2n-1} + Y_{n,2n-1} + 1$

$C^0_{2n} > C^1_{2n}$???

C^0_{2n} \ $C^1_{2n}C_n$	00	01	11	10
0	0	0	1	0
1	d	d	1	1

$C_{2n} = C^0_{2n} + C^1_{2n} \cdot C_n$



Variable-sized CSeA